The 2024 IEEE 74th Electronic Components and Technology Conference

May 28 – 31, 2024

2024 Advance Program

Gaylord Rockies Resort & Convention Center

Denver, Colorado, USA

Sponsored by

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

For more information visit www.ECTC.net

INTRODUCTION FROM THE IEEE 74TH ECTC PROGRAM CHAIR MICHAEL MAYER

The 2024 IEEE 74th Electronic Components and Technology Conference (ECTC) at the Gaylord Rockies Resort & Convention Center, Denver Colorado • May 28 - 31, 2024

On behalf of the Program Committee and Executive Committee, it is my pleasure to invite you to IEEE's 74th Electronic Components and Technology Conference (ECTC), which will be held at the Gaylord Rockies Resort & Convention Center, Denver, Colorado, from May 28 to 31, 2024. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses, semiconductor foundry and assembly/testing service providers, substrate makers, equipment manufacturers, material suppliers, research institutions, universities, and investors, all under one roof. More than 1600 people attended the fully in-person ECTC 2023, and this year we plan for a solely in-person conference again.

At the 74th ECTC, 375+ technical papers will be presented across 36 oral sessions and 5 interactive presentation sessions. Key topics include advancements in packaging technologies, heterogeneous integration, systems design (Sessions 1, 7), and next-generation substrate manufacturing (Session 13). Reliability aspects will cover advanced substrates, high-density packages, and harsh environment reliability (Sessions 4, 16, 29, 35). Topics in assembly and manufacturing technology include 3D integration, bonding, and die bond/board-level reliability (Sessions 10, 23, 27). Topics about RF, high-speed components and systems include antenna-in-package design, signal integrity, and chiplet interconnect validation (Sessions 18, 22, 26). Emerging technologies topics include digital healthcare, AI, quantum computing, and additive manufacturing for printed electronics (Sessions 5, 11, 17). Interconnection technology sessions cover topics like die-to-wafer hybrid bonding, ultra-fine pitch technologies, and copper hybrid bonding (Sessions 2, 8, 14, 32). Materials and processing topics include advanced processes for chip stacking, hybrid bonding materials, polymer packaging innovations, and fine-pitch materials/processes (Sessions 9, 15, 21, 33). Thermal/mechanical simulation and characterization topics include reliability simulations, AI in modeling, advances in flex and redistribution layer technologies, process/hybrid bonding modeling, and thermal management solutions (Sessions 6, 12, 24, 30, 36). Photonics topics include co-packaged optics, optical interconnections, and photonics integration, materials, and processes (Sessions 3, 28, 34). Interactive presentations (Sessions 37-41) include innovations in bonding, power delivery systems, optimization algorithms, packaging for specific semiconductor devices, and reliability assessments. The 74th ECTC offers a platform for exploring cutting-edge microelectronic packaging advancements, fostering innovation, and addressing critical challenges.

The ECTC this year presents seven special sessions with industry experts, including five on Tuesday, each lasting 90 minutes. One session, chaired by Przemyslaw Gromala (Robert Bosch GmbH) and Erik Jung (Fraunhofer IZM), delves into Industry-Government Co-Investments for the Advanced Electronics Sector globally. Another, chaired by Ran Tao (NIST) and Benson Chan (Binghamton University), focuses on advancing metrology for next-generation microelectronics. An afternoon session on Thermal Management for AI, chaired by Zhi Yang (Groq) and Sevket Yuruker (Tesla), explores innovative solutions for power-hungry AI/ML applications. Following that, an RF Packaging session above 100 GHz, chaired by Maciej Wojnowski (Infineon Technologies AG) and Ivan Ndip (Fraunhofer IZM/Brandenburg University of Technology), is scheduled. Additionally, a Young Professionals Networking Event on May 28, 2024, from 7:00 p.m. to 7:45 p.m., chaired by Aakrati Jain (IBM), and an IEEE EPS Seminar on Substrates for Chiplets on the same day from 7:45 p.m. to 9:15 p.m., chaired by Takashi Hisada and Yasumitsu Orii (Rapidus Corporation), are scheduled for Tuesday.

On the morning of Wednesday, May 29, 2024, ECTC's keynote presentation on Petascale photonic chip connectivity for energy-efficient AI computing is scheduled, presented by Prof. Keren Bergman (Columbia University) and invited by Karlheinz Bock (TU Dresden), the conference's General Chair. Additionally, a Diversity and Career Growth Panel and Reception on May 29, 2024, from 6:30 p.m. to 7:30 p.m., chaired by Cristina Amon (University of Toronto) for ITherm and Vidya Jarayam (Intel) for ECTC. A Plenary Session on the Future of Semiconductor Industry is planned for Thursday, May 30, 2024, from 8:00 a.m. to 9:15 a.m., chaired by Rozalia Beica (Averatek) and Farhang Yazdani (BroadPak). A panel session on Workforce Challenges in Education and Workforce Development in the New Chips Economy, organized by the IEEE EPS President, includes chairs Patrick Thompson (Texas Instruments), Mark Poliks (Binghamton University), Jeff Suhling (Auburn University), and Kitty Pearsall (Boss Precision Inc.).

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and ECTC Exhibits. Co-located with the IEEE ITherm Conference, the 74th ECTC will offer 16 CEU-approved PDCs, organized by Kitty Pearsall and Jeffrey Suhling. The PDCs take place on Tuesday, May 28th and are taught by distinguished experts in their respective fields.

The Exhibits at ECTC run from Wednesday May 29th to Thursday May 30th and showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred exhibiting companies will be present Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 74th ECTC and to be a part of all the exciting technical and professional opportunities.

I want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 74th ECTC a success. I look forward to meeting you at the Gaylord Rockies Resort & Convention Center, Denver, Colorado, from May 28 to 31, 2024.

Michael Mayer
74th ECTC Program Chair
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74th ECTC ADVANCE REGISTRATION

Advance Registration

Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions, see page 32.

Register early … save US $150 or more! All registrations received after May 3, 2024, will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk in the Square Area, near the Cocoa Bean coffee shop.

On-Site Registration Schedule

Registration will be held in the Rockies Square Area on the lobby level.

Monday, May 27, 2024	3:00 p.m. – 6:00 p.m.
Tuesday, May 28, 2024	6:45 a.m. – 7:45 p.m.*

**6:45 a.m. – 8:00 a.m.: Morning PDCs & morning ECTC Special Session only*

Wednesday, May 29, 2024	6:45 a.m. – 4:00 p.m.
Thursday, May 30, 2024	7:30 a.m. – 4:00 p.m.
Friday, May 31, 2024	7:30 a.m. – 12:00 Noon

The above schedule for Tuesday will be rigorously enforced to prevent students from being late for their courses.

General Information

Conference organizers reserve the right to cancel or change the program without prior notice. The Gaylord Rockies Resort & Convention Center, as well as the ECTC, are both smoke free environments.

ITherm 2024

ITherm is co-located with ECTC! All ITherm sessions and exhibits take place in the Gaylord Rockies Resort & Convention Center. For more information about ITherm 2024 please visit www.ieee-itherm.net.

Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual's belongings is the individual's responsibility.

ECTC Sponsors

With over seven decades of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 1,500 individuals and organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Program, and several other sponsorship options that can be customized to your company's interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under "Sponsors".

To sign-up for sponsorship or to get more details, please contact Alan Huffman at **alan.huffman@ieee.org** or **+1-336-380-5124**.

Hotel Accommodations

Rooms for ECTC attendees have been reserved at the Gaylord Rockies Resort & Convention Center. The special conference rate for a single/double occupancy room is:

US $229.00 per night

This price includes single or double occupancy in one room.

Please note these rooms are on a first come, first serve basis. If the conference rate is no longer available, attendees will be offered the next best price available.

Room reservations must be made directly with the hotel by May 3, 2024, and before rooms run out, to ensure our preferred conference rate. All reservations made after the cutoff date of May 3, 2024 at 5 p.m. Mountain Time are accepted on a space and rate availability basis. **If you need to cancel a reservation, please do so by 5 p.m. Mountain Time, AT LEAST 5 days prior to arrival for a full refund.** Check-in time: 4 p.m. Check-out time: 11 a.m.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2024 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2024 from 3rd party companies. These emails and sites are not to be trusted. There are scam artists out there and if it's too good to be true it likely is. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC emailings to subscribers or ECTC emails from our Executive Committee. **ECTC's only authorized site** for reserving a room is through our website (www.ectc.net). However, you may use other trusted sites to book travel. Should you have any questions about booking a hotel room please contact ECTC staff at lrenzi@renziandco.com.

Transportation Services

There is no complimentary transportation to and from the hotel and airport. All attendees must make their own transportation arrangements.

74th ECTC CONFERENCE OVERVIEW

2024 ECTC Special Session on Industry-Government Co-Investments

Exploring the Impact of Industry-Government Co-Investments for the Advanced Electronics Sector in North America, Asia and Europe

Tuesday, May 28, 2024, 8:30 a.m. – 10:00 a.m.

Chairs: Przemyslaw Gromala, Robert Bosch GmbH and Erik Jung, Fraunhofer IZM


Essential to the global economy and innovation landscape, the semiconductor and microelectronics packaging industries are seeing government led investment programs. The introduction of the CHIPS and Science Act (Creating Helpful Incentives to Produce Semiconductors for America) in the United States has been inspiring similar programs, e.g. in Europe the European Chips Act.

Speakers in this special session discuss programs and co-investments for the United States, Europe, India and East Asia, including job creation, supply chain resilience, and enhanced technological innovation. We will examine the prospects of global collaborations and partnerships between national semiconductor and microelectronic packaging centers and industry leaders. The session will also discuss mechanisms for knowledge exchange, joint research initiatives, and mutually beneficial outcomes.

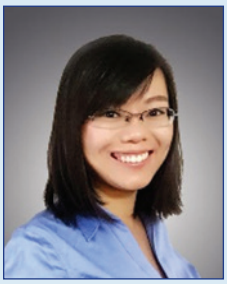
Elisabeth Steimetz, EPoSS, Europe; Rao Tummala, Advisor to the Government of India; Subramanian S. Iyer, National Advanced Packaging Manufacturing Program, USA; Gordon Harling, CMC Microsystems, Canada; Kwang-Seong Choi, Electronics and Telecommunications Research Institute, Korea

2024 ECTC Special Session on Metrology

Challenges and Opportunities in Advancing Metrology for Next-Generation Microelectronics

Tuesday, May 28, 2024, 10:30 a.m. – 12:00 p.m.

Chairs: Ran Tao, NIST and Benson Chan, Binghamton University




Metrology plays a pivotal role in semiconductor research and manufacturing and is critical to the success of this industry. Advancements in measurement science, material characterization, instrumentation, testing, and manufacturing capabilities are critically needed to drive product innovation and ensure quality, yield, and manufacturing efficiency. During the panel discussion, experts will share their insights on the metrology challenges and opportunities that today's semiconductor industry is facing across every segment of the supply chain, with a focus on advanced semiconductor packaging for next-generation microelectronics (e.g., heterogeneous integration, wafer level packaging, hybrid bonding, etc.).

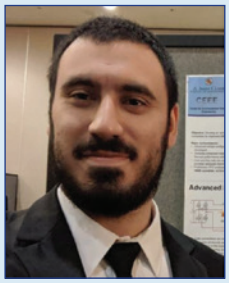
Marla Dowell, NIST; Gaurang Choksi, Intel Corporation; Zhihua Zou, TSMC; Chet Lenox, KLA Corporation

2024 ECTC Special Session on Thermal Management for AI

Efficient and Innovative Thermal Management for Power Hungry AI/ML Applications: Challenges and Opportunities

Tuesday, May 28, 2025, 1:30 p.m. – 3:00 p.m.

Chairs: Zhi Yang, Groq and Sevket Yuruker, Tesla

The rapid advancement of artificial intelligence (AI) and machine learning (ML) technologies has led to the proliferation of high-power AI/ML applications in various domains, such as autonomous vehicles, high performance computing and natural language processing. However, this growth is accompanied by escalating thermal challenges that can critically impact the performance, reliability, and lifespan of entire systems. The non-uniform distribution of heat sources on AI/ML hardware further complicates cooling strategies. Moreover, the reliance on traditional thermal management techniques may prove inadequate in addressing emergent challenges.

To address these challenges, several industry and academia experts are discussing the current status and opportunities for innovative thermal management developments/ methodologies in this special session.

PKi Wook Jung, Samsung; Igor Arsovski, Groq; Mudasir Ahmad, Google; Tiwei Wei, Purdue University; Christopher Ortiz, Ansys

2024 ECTC Special Session RF Packaging for Above 100 GHz

RF Packaging for Communication and Sensing Applications above 100 GHz – Technologies, Design Challenges and Emerging Solutions

Tuesday, May 28, 2024, 3:30 p.m. – 5:00 p.m.

Maciej Wojnowski, Infineon Technologies AG and Ivan Ndip, Fraunhofer IZM/Brandenburg University of Technology


In this session, experts from industry and academia will present the latest developments in RF packaging for communication and radar sensing applications above 100 GHz. The panel will begin with a presentation of emerging applications, resulting challenges and opportunities for RF packaging. The experts will share the latest developments in RF packaging materials and technologies. Emerging RF system integration platforms will be presented, stressing the importance of material characterization and modeling as well as co-design and co-simulation techniques. The panel will conclude with examples of recent R&D results for novel D-band waveguide interfaces in packages for 6G data links over plastic microwave fiber (PMF), antennas-in-package (AiP) and phased array front-end AiP modules.

Swaminathan Sankaran, Texas Instruments; Martin Letz, Schott AG; Alberto Valdes-Garcia, IBM Research; Madhavan Swaminathan, Penn State University; Uwe Maass, Fraunhofer IZM

2024 ECTC Heterogeneous Integration Roadmap (HIR) Workshop

Four Technical Sessions, spanning morning and afternoon of Tuesday, May 28, 2024

Chairs: Ravi Mahajan, Intel Corporation and William Chen, ASE

- *Engineering Chiplets for the AI Era*
- *Challenges and Innovations in Thermal Engineering from Fan-out to 2.5D and 3D Stacking*
- *Packaging Challenges and Innovation for Future Communication Systems*
- *CHIPS Act Roundtable Chat*

2024 ECTC Young Professionals Networking Event

Tuesday, May 28, 2024, 7:00 p.m. – 7:45 p.m.

Chair: Aakrati Jain, IBM

Join us for an invaluable opportunity to connect with industry leaders and fellow emerging talents! Tailored specifically for young professionals, including current graduate students, this event is crafted with your needs in mind. Engage in dynamic interactions with senior EPS members and professionals through a series of active and engaging activities. Seize the chance to delve deeper into packaging-related topics, pose career questions, and connect with industry professionals for a valuable learning experience.

2024 IEEE EPS Seminar on Substrates for Chiplets

Substrate-Scaling Challenges in Chiplet Integration

Tuesday, May 28, 2024, 7:45 p.m. – 9:15 p.m.

Chairs: Takashi Hisada, Rapidus Corporation and Yasumitsu Orii, Rapidus Corporation

Chiplet is driving performance scaling and cost efficiency of advanced semiconductor systems. There are difficult challenges for the substrates in chiplet integration such as very large size of the substrates, fine line and space ground rule with multiple layers, mechanical stress, reliability, and complexity of design.

The EPS Seminar organized by TC6 (High-Density Substrate and Board) will discuss technical and business challenges of chiplet on large substrates. We will have 7 panelists, and each panelist will give a short talk presenting insights on technology trends, technical challenges, application requirements, recent technical updates and more covering package form factors, design tools, materials, manufacturing tools, and assembly processes for advanced chiplet integration, followed by a panel discussion.

Gang Duan, Intel; Kinya Ichikawa, TSMC; Kenneth Larsen, Synopsys; Masahisa Ose, Resonac; Jeff Turner, AMAT; Yu-Po Wang, SPIL; Rozalia Beica, Averatek

2024 Keynote Speaker

Petascale Photonic Chip Connectivity for Energy Efficient AI Computing

Wednesday, May 29, 2024, 8:00 a.m. – 9:15 a.m.

Prof. Keren Bergman, Columbia University

High-performance data centers are increasingly bottlenecked by the energy and communications costs of interconnecting numerous compute and memory resources. Current systems face a gap of nearly two orders of magnitude between on-chip, intra-socket, communication capacities, and the capacities of links transporting data over longer distances. The per bit energy cost of data movement dominates that of data processing, as does density, throughput, and latency. Integrated silicon photonics offer the opportunity of optical connectivity that delivers high off-chip communication bandwidth densities with low power consumption. To realize these benefits deeply embedded packaging of photonics with the compute and memory is critical. This talk will cover these multi-chip packaging challenges as well as approaches for leveraging dense wavelength-division multiplexing photonic IO that can scale to realize Petabit/s chip escape bandwidths with sub-picojoule/bit energy consumption.

2024 ECTC/ITherm Diversity and Career Growth Panel and Reception Wednesday

Effective Practices to Attract, Promote and Retain a Diverse Workforce

Wednesday, May 29, 2024, 6:30 p.m. – 7:30 p.m.

Chairs: Cristina Amon, University of Toronto / ITherm and Vidya Jarayam, Intel / ECTC

Semiconductor, electronic packaging and energy-related companies are planning to grow their workforces to meet the current and expected demands due to policy incentives and domestic investments, including the CHIPS Act. To achieve business and economic success, we will need to attract a broader group of students to the relevant fields and expand beyond the traditional pool of candidates to include women and underrepresented minorities from rural candidates to veterans and mid-career retrainees. This panel will focus on how best practices in Diversity, Equity and Inclusion have been implemented and can be used to attract students and hire, develop, promote and retain employees within organizations to meet their goals.

The panelists will introduce some of the challenges faced by women, minorities , and underrepresented groups, as well as share their organization's strategies for professional development, promotion, retention, and success. This will be followed by an interactive Q&A with the audience.

After the panel session, a social and networking reception will be held. All ECTC and ITherm attendees are invited to join in on this engaging discussion and the reception afterwards.

Kylie Patterson, NIST-CHIPS Program Office; Allyson Stewart, Marvell Inc.; Al Ortega, Villanova University; Arron Gregory, NREL

These sessions are open to all conference attendees.

2024 ECTC Plenary Session on Future of Semiconductor Industry

The Future of Semiconductor Industry. Emerging Start-ups and Material Innovations in Advanced Packaging

Thursday, May 30, 2024, 8:00 a.m. – 9:15 a.m.

Chairs: Rozalia Beica, Averatek and Farhang Yazdani, BroadPak

Styled as a start-up competition, this session looks at next generation materials and companies.

It features presentations from start-up companies and reviewed by a panel of judges from the industry and investment community. Topics include Materials & Processes for MicroLED and System-In-Package, Thermal Management, Dielectrics & Metallization for High End IC Substrates

Victor Chiriac, Global Cooling Technology Solutions; Wayne Rickard, Terecircuits; Stefan Prastine, Thintronics; Mohsen Asad, Hyperloom

2024 IEEE EPS President's Panel Session on Workforce

Challenges in Education and Workforce Development in the New Chips Economy

Friday, May 31, 2024, 8:00 a.m. – 9:15 a.m.

Chairs: Patrick Thompson, Texas Instruments, Mark Poliks, Binghamton University, Jeff Suhling, Auburn University and Kitty Pearsall, Boss Precision Inc.

The semiconductor and packaging industries are currently experiencing unparalleled growth, driven by demand in areas such as AI, transportation electrification, digital manufacturing, data centers, mobile devices, hybrid flexible electronics, virtual reality, and photonics and MEMS. This expansion has prompted substantial global investments in new fabs and packaging infrastructure, supported by government spending in North America, Europe, and Asia.

However, the parallel surge in demand for skilled labor poses a considerable challenge, with estimates indicating a threefold increase in headcount required over the next five years. The industry is seeking individuals with multidisciplinary education, ranging from technician degrees to Ph.D. degrees. The panel will explore workforce needs, industry perspectives on student preparation, global approaches to electronics packaging education, and innovative strategies to attract students to the semiconductor packaging field.

John Oakley, Semiconductor Research Corporation; Toni Mattila, Business Finland; Robert Geer, SUNY Polytechnic University: Wenhui Zhu, Central South University: Jim Wieser, Texas Instruments

Luncheons

ECTC will be offering a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. Lunch tickets, found in your registration badge holder, must be presented for entrance into the lunch room. Lost lunch tickets will cost $100 to replace. Please come and enjoy time with other attendees and colleagues in the industry! Lunch times will vary, see below for specific details for each day.

Tuesday:	**12:00 Noon – 1:15 p.m.**
Wednesday:	**12:45 p.m. – 2:00 p.m.**
Thursday:	**12:45 p.m. – 2:00 p.m. – Sponsored by: The IEEE Electronics Packaging Society (EPS)**
Friday:	**12:45 p.m. – 2:00 p.m. – Don't miss out on this lunch! We will be raffling off a number of prizes including a hotel stay, free conference registrations, and many industry gadgets!**

General Chair's Speakers Reception

Tuesday, May 28, 2024 • 6:00 p.m. – 7:00 p.m.

(by invitation only)

ECTC Student Reception

Tuesday, May 28, 2024 • 5:00 p.m. – 6:00 p.m.

Hosted by Texas Instruments, Inc.

Students, have you ever wondered what career opportunities exist in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them be successful in their first job search and reach their current positions. You will have the chance to enjoy good food and network with industry leaders and achievers. Don't miss the opportunity to interact with people that you might not have the chance to meet otherwise!

Exhibitor Reception

Wednesday, May 29, 2024 • 5:30 p.m. – 6:30 p.m.

Open to all conference attendees.

74th ECTC Gala Reception

Thursday, May 30, 2024 • 6:30 p.m.

Hosted by Koh Young Technology

All badged attendees and their guests are invited to attend a reception hosted by Gala Reception sponsors.

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PROFESSIONAL DEVELOPMENT COURSES

Tuesday, May 28, 2024

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MORNING COURSES
8:00 a.m. – 12:00 Noon

1. HIGH RELIABILITY SOLDERING IN SEMICONDUCTOR PACKAGING

Course Leader: Ning-Cheng Lee – ShinePure Hi-Tech

Course Description

Semiconductor soldering is much more delicate and is very critical for reliability of devices. This course covers the critical parameters governing the reliability for soldering in semiconductor packaging. The reliability discussed includes parameters affecting the intermetallic compounds (IMC), voiding, electromigration, low temperature soldering, high temperature soldering, and electrochemical migration under a variety of material combinations. The failure modes are discussed in detail, with preferred choices of materials and designs recommended.

Course Outline

1. IMC -Effect of Cu Pad Grain Size on IMC
2. IMC - Interaction of Cu and Ni
3. IMC - Effect of Base Metal Co-P on IMC
4. Voiding - Effect of Solder Form
5. Voiding - Effect of Joint Height, Temperature, Electrical, and Mechanical
6. Voiding - Effect of Cu Structure on Kirkendall Voids
7. Electrochemical Migration (ECM)
8. Electromigration
9. LTS - Bi-Rich Whisker Growth
10. LTS - TCT Reliability of LTS
11. LTS - Collapse of LTS
12. LTS - Deposition, Hot Tear, Bi Stratification of LTS
13. LTS - Hot Tear of Homogeneous LTS BiSn - Effect of Profile
14. LTS - Drop Test of LTS
15. HTS - TLPB (Transient Liquid Phase Bonding)

IMPORTANT NOTICE

Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

Who Should Attend

Anyone who cares about achieving high reliability solder joints for semiconductor packaging and wants to know how to achieve it should take this course

2. PHOTONIC TECHNOLOGIES FOR COMMUNICATION, SENSING, AND DISPLAYS

Course Leader: Torsten Wipiejewski – Huawei Technologies

Course Description

This course will provide an overview of the various photonic technologies that enable optical communication, optical sensing, and modern display applications. These applications are key for the information and communication technology of today and pave a way to the future. High speed optical communication from board level in data centers to long haul transmission requires photonic components with high speed and high reliability. We will discuss the main components such as laser diodes of several types, high speed optical modulators and photodetectors as well as integration schemes such as photonic integrated circuits (PICs) and packaging aspects. Photonic technologies are also widely used as sensors for various applications including health monitoring. One key advantage is the potential for non-invasive measurements that facilitate the usage by end-users without specific medical knowledge. Packaging should provide a high accuracy solution at low cost. Displays are the main media nowadays for bringing information to people. They range in size from smart watches to smart phones, laptops, and tablets all the way to large screen TVs and video walls. We review current technologies and new developments such as quantum dots and micro-LEDs as well as some features of 3D displays. Micro-LEDs for large size displays require novel assembly technologies to mount chips of just several micrometers in size with extremely high yield at very low cost. The mass transfer of thousands of chips simultaneously is an option to achieve this challenging target.

Course Outline

1. Fundamental Properties of Photonic Components
2. Light Sources (LEDs, Laser Diodes, Others)
3. Transmitter and Receiver Components in Optical Communication (Lasers, Modulators, Photodetectors, Passive Optical Components, Photonic Integrated Circuits, Silicon Photonics, Optical Modules, Monolithic and Hybrid Integration, Packaging
4. Optical Sensing Elements and Applications (Spectrometers, Light Sources, Photoacoustic Sensors, Frequency Combs)
5. Display Technologies Liquid Crystal Displays (LCD), Organic Light Emitting Diode Displays (OLED), Quantum Dot Emissive Layers, Micro-LED Arrays and Large Size Displays using Chiplet Mass Transfer and Bonding, 3D Displays
6. Summary and Outlook

Who Should Attend

The course addresses engineers, scientists and students who would like to get a general overview of various photonics technologies used in today's products and future developments. The aim is to describe which photonic technologies can be used in various applications and what current limitations are and which new technologies are being developed for further improvements or aiming at technology breakthroughs.

3. FROM WAFER TO PANEL LEVEL PACKAGING

Course Leaders: Tanja Braun and Piotr Mackowiak – Fraunhofer IZM

Course Description

Wafer and Panel Level Packaging are two of the dominating trends in microelectronics packaging. Both approaches with different flavors as RDL last face-up or face-down have reached maturity and are introduced in high volume manufacturing. Main driver for moving from wafer to panel level packaging is of course lowering the packaging cost. More packages can be processed in parallel and panel formats have a much better area utilization (ratio between panel/wafer size and package size) than round wafer shapes. Additionally, PLP has the opportunity to adapt processes, materials and equipment from other technology areas. Printed Circuit Boards (PCB), Liquid Crystal Displays (LCD) or photo-voltaic cells (PV) are manufactured on panel sizes and adapted technologies can offer new approaches also for Fan-out Panel Level Packaging.

The PDC will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging. This will include material and process discussion, technologies, equipment, applications and market trends as well as cost and environmental aspects.

Course Outline

1. Introduction Advanced Packaging
2. Trends in Wafer Level Packaging
3. Fan-In and Fan-Out Wafer Level
4. Introduction and Definition Panel Level Packaging (PLP)
5. Fan-Out Panel Level Packaging: Technologies, Challenges & Opportunities, Cost and Environmental

Who Should Attend

Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level

Packaging and the transition to Panel Level Packaging. Engineers and managers are welcome as detailed technology descriptions as well as market trends, applications and cost modeling are presented.

4. ELIMINATING FAILURE MECHANISMS IN ADVANCED PACKAGES

Course Leader: Darvin Edwards – Edwards Enterprises

Course Description

Primary reliability failure mechanisms that plague semiconductor packages will be summarized along with solutions to enable faster qualification. The reliability of new package technologies such as heterogeneous package integration and chiplet technologies will be emphasized, as well as an overview of reliability issues in more traditional packages. Topics studied include reliability of Direct Cu Bonding (DCB), micro bump mechanical reliability, high density interconnect (HDI) reliability, TSV-chip interactions, electromigration performance, stress induced interlevel dielectric (ILD) damage under bumps and Cu pillars, saw induced ILD damage, solder joint reliability, the impact of aging on reliability performance and many more.

Primary failure analysis techniques will be described. For each failure mode, the resultant failure mechanisms and failure analysis techniques required to verify the mechanisms will be summarized. This solutions-focused course concentrates on key process parameters, design techniques and material selections that can eliminate failures and improve reliability, ensuring participants can design-in reliability and design-out failures for quicker time to market. The emphasis is on giving the student an intuitive understanding of the interaction between the various trade-offs, and providing the knowledge about the methodologies and tools needed to drive early evaluation of these reliability risks. Primary reliability failure mechanisms that plague semiconductor packages will be summarized along with solutions to enable faster qualification.

Course Outline

1. Introduction to Package Reliability
2. Failure Modes vs. Failure Mechanisms
3. Failure Analysis Techniques
4. FC-BGA Package Failure Mechanisms
5. WLCSP Package Failure Mechanisms
6. Embedded Die & Fan-Out WLP/PLP Failure Mechanisms
7. TSV Failure Mechanisms
8. High Density Interconnection Reliability
9. Direct Bond Interconnect Reliability and Testing
10. Chiplet Challenges
11. Materials, Modeling, Design Rules and Reliability
12. Summary

Who Should Attend

This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions.

5. NAVIGATING THERMAL AND RELIABILITY CHALLENGES IN CHIP COMPONENTS FOR AUTOMOTIVE HIGH-PERFORMANCE COMPUTE SYSTEMS

Course Leader: Fen Chen – Automotive Reliability/Validation Consultation Services

Course Description

The landscape of driving is rapidly shifting towards fully autonomous vehicles (AV). In the absence of human drivers, the functionality and performance of a Compute system becomes paramount requiring it to consistently outpace human response for driving safety. AV Compute systems typically consist of multiple larger-size PCBs housing redundant CPUs, AI processors, and crucial IC components to ensure higher performance, safety, and reliability of AV driving.

Throughout the rigorous AV Compute reliability qualification process, these systems undergo various thermal and mechanical stresses. Preventing chip thermal failure under these demanding environmental conditions is a critical concern. In this short course, we will delve into several key areas. In the initial segment, we will review fundamental chip thermal design, cooling solutions, and chip-level reliability considerations. A spotlight will be cast on comparing lidded and lidless package thermal and reliability performances, along with exploring the latest trends in chip thermal management.

In the subsequent part, we will present the thermal mission profile and diverse stress test requirements for AV hardware validation, adhering to automotive industry standards. We'll shine a light on the thermal reliability challenges associated with qualifying vehicle Compute. Moving ahead, we'll delve into the most recent advancements in vehicle thermal management technologies.

Course Outline

1. High Performance Compute for Vehicle Applications
2. Chip Power + Temperature Trending and Reliability
3. Chip Heat Transfer Basics and Survey
4. Lidded and Lidless Package Thermal and Rel Performance Comparison
5. Chip Thermal Management Hot Trends
6. Vehicle Thermal Mission Profile Introduction
7. Vehicle-level Reliability Requirements
8. Reliability Challenges
9. Vehicle System Level Thermal Management Technologies Overview
10. Liquid Cooling Cold Plate Performance and Reliability
11. TIM Performance and Reliability
12. Board Strain and Chip Reliability
13. Heat Pipe Performance and Reliability
14. Thermal Mitigation at Chip Level, Board Level and System Level
15. Closing Remarks

Who Should Attend

Engineers and tech managers already involved in the chip thermal design for automotive applications, and those who need a fundamental understanding or a broad overview of the chip thermal and reliability management for automotive applications.

6. POLYMERS FOR ADVANCED PACKAGING

Course Leader: Jeffrey Gotro – InnoCentrix, LLC

Course Description

The course has been completely updated to include a detailed discussion of the polymers and polymer-related processing for Fan-Out Wafer Level (FOWLP) packaging as well as Fan-Out Panel Level packaging (FOPLP). The course will provide an overview of the important structure-property-process-performance relationships for polymers used in wafer level packaging. The main learning objectives will be:

1-Gain insights on how polymers are used in Fan Out Packaging, specifically mold compounds and polymer redistribution layers (RDL).

2-Understand the key polymer and process challenges in Fan-Out Wafer-Level Packaging.

3-Learn about polymers and processes used in Fan Out Panel Level Packaging including new materials for mold compounds and a detailed description of the polymers used for RDL in FOPLP.

Course Outline

1. Overview of Polymers used in Fan-Out Wafer-Level Packaging (FOWLP)
2. Wafer-level Process Flows (Chip-First Versus Chip-Last (RDL first))
3. Epoxy Mold Compounds for Fan-Out packages
4. Photosensitive Polyimides and Polybenzoxazoles for RDL
5. Polymer Reliability Challenges in Fan-Out Wafer-Level Packaging
6. Processes and Materials for Fan-out Panel-level Packaging (FOPLP)

7. Wafer Versus Panel Processing; Polymer Challenges and Solutions
8. Pre-Applied Underfills and Wafer-Level Underfills, Chemistry and Process

Who Should Attend

Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used in electronic packaging will also find this course valuable.

7. FLIP CHIP TECHNOLOGIES

Course Leader: Shengmin Wen – HaiSemi, Inc.

Course Description

This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various types of wafer bumping technologies, substrate design and selection, underfill selection, Co-design and modeling, and reliability evaluation.

Course Outline

1. Introduction to Flip Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Substrate Technologies, Underfill, Package Warpage Control, and Yield
5. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
6. Flip Chip Si Package Co-Design and Chip-Package Interaction
7. Flip Chip New Trends: Wafer Level CSP; Wafer Level Fan-Out; and Panel-Level Packaging
8. Bumping Ground Rules
9. Flip Chip Under-bump Metal and Intermetallic
10. Flip Chip Solder Deposition Processes
11. Cu Pillar Technology
12. Flip Chip Solder Selection and Characterization
13. Flip Chip Electromigration
14. Non-Solder Interconnects
15. Review and Package Selection Exercise

Who Should Attend

The goal of this course is to provide the students with a list of options to apply to their flip chip assembly applications so that a reliable, innovative, better time to market, and more cost-effective solution can be achieved. Students are encouraged to bring topics and technical issues from their past, present, and future job function for group discussions. A group exercise at the end of the class is planned to serve as a capstone project, making sure that the students can walk away with an in-depth understanding of the technology, and are ready to apply and meet their real-world packaging needs.

8. RELIABLE INTEGRATED THERMAL PACKAGING FOR POWER ELECTRONICS

Course Leader: Patrick McCluskey – University of Maryland

Course Description

Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation has resulted in significant improvements in efficiency over previous technologies, but it also has made it essential that the reliability of power electronics be characterized and enhanced. Recently, increased power levels, made possible by new compound semiconductor materials, combined with increased packaging density have led to higher heat densities in power electronic systems, especially inside the switching module, making thermal management more critical to performance and reliability of power electronics. This course will emphasize approaches to integrated thermal packaging that address performance limits and reliability concerns associated with increased power levels and power density. Following a quick review of active heat transfer techniques, along with prognostic health management, this short course will present the latest developments in the materials (e.g. organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS, and systems and in the techniques for their reliability assessment.

Course Outline

1. Motivation for Integrated Thermal Packaging for Power Electronics and Heterogeneous Integration
2. Simulation and Assessment of Active Thermal Management Techniques
3. Application of Thermal Management to Commercial Power Systems
4. Durability and Reliability Assessment
5. Thermal Packaging and Reliability of Active Devices
6. Thermal Packaging and Reliability of Modules
7. Reliability and Packaging at the Board and System Level
8. Flexible Materials, Packaging, and Thermal Management
9. Reliability of Additive Manufactured Systems and Materials
10. AI/ML for Prognostics of Power Electronics

Who Should Attend

Engineers and Managers who want to learn more about the thermal limitations and reliability concerns involved in the heterogeneous integration and packaging of power electronic devices and systems.

AFTERNOON COURSES
1:30 p.m. – 5:30 p.m.

9. ADDITIVE FLEXIBLE HYBRID ELECTRONICS – MANUFACTURING AND RELIABILITY

Course Leader: Pradeep Lall – Auburn University

Course Description

Technology progression in the field of electronics has been marked with "Dennard Scaling," which defined that smaller transistors offered less power consumption, higher frequencies and higher density. Given that current gate lengths have approached 3nm, it is widely realized that future performance needs to be realized through packaging innovations and heterogeneous integration. Heterogeneous integrated modules may require a unique mix of components and custom design specific to a particular application. This course covers additive manufacturing methods for the realization of circuits and packaging for high-mix low-volume heterogeneous integration. This course will cover manufacturing, design, assembly, and accelerated testing of additively printed electronics for applications in some emerging areas.

Manufacturing processes for additive fabrication of rigid and flexible electronics will be discussed. The manufacture of thin additively packaged electronic architectures requires the integration of thin chips, flexible encapsulation, compliant interconnects, and nano-particle inks for metallization traces. Several additive-printed electronics processes for fabricating and assembling electronics have become tractable. Pick-and-place of thin-silicon and compliant interposers through interconnection processes such as reflow requires an understanding of the deformation and warpage processes. Several product areas for applying additive electronics are tractable, including Internet-of-Things (IoT), medical wearable electronics, communications, and automotive electronics.

Course Outline

1. Heterogeneous Integration
2. Need for High-Mix Low-Volume
3. Additive Technologies - Aerosol-Jet Printing, Ink-Jet Printing, Screen-Printing and Gravure Printing
4. Structure Integrated Packaging - Laser-

Direct Sintering, In-Mold Labeling
5. Ultra-Thin Chips
6. Die-Attach Materials for Additive Semiconductor Packaging
7. Flexible Encapsulation Materials
8. Dielectric Materials for Large-Area Electronics
9. Substrates for Flexible and Rigid Additive Applications
10. Power Sources Integration and Reliability
11. Accelerated Testing Protocols for Complex Integrated Systems
12. Additive Complex Integrated Package Assembly

Who Should Attend

The targeted audience includes scientists, engineers, and managers considering the use of heterogeneous integration, as well as reliability, product, or applications engineers who need a deeper understanding of additively-print processes to enable high-mix low-volume applications and understand the advantages, limitations; and, failure mechanisms

10. FUNDAMENTALS OF RF DESIGN AND FABRICATION PROCESSES OF FAN-OUT WAFER/LEVEL AND ADVANCED RF PACKAGES

Course Leaders: Ivan Ndip – Fraunhofer IZM/Brandenburg University of Technology and Markus Wöhrmann – Fraunhofer IZM

Course Description

Due to their myriad of advantages in system-integration, fan-out wafer/panel-level packages (FO WLPs/PLPs) and other advanced RF packages (e.g., glass interposers and chip-embedding packages) will play a key role in the development of emerging electronic systems. The fabrication processes and RF performance of these packages will contribute significantly to the cost and performance of the entire system. The objective of this course is to provide and illustrate the fundamentals of the fabrication processes and RF design of these advanced packages for emerging RF/wireless applications.

An overview of distinct types of wafer-level packages, fan-out technologies, glass interposers and chip-embedding packages will first be given. This will be followed by a presentation of new fan-out-packaging and interposer-based concepts for emerging and future applications (e.g., 5G mmWave, mmWave radar sensors, 6G) as well as a thorough discussion of the materials and fabrication processes of FO-WLPs/PLPs, multilayered RDLs, glass interposers and chip embedding packages. The basics of efficient RF design and measurement of the fundamental building blocks of these advanced packages will be given for frequencies up to the millimeter-wave range. Finally, examples of these advanced packages designed and fabricated at Fraunhofer IZM will be discussed.

Course Outline

1. Overview: Different Types of Wafer-Level Packages, Fan-Out Technologies, and Advanced RF Packages
2. Requirements of 5G Packaging and New Fan-Out Packaging Concepts for 5G mmWave Applications
3. Materials and Fabrication Processes: FO-WLPs/PLPs, Multi-Layered RDLs, Glass Interposers and Chip Embedding Packages
4. Fundamentals of RF Design and Measurement: FO-WLPs/PLPs, Glass Interposers and Chip-Embedding Packages
5. Examples of Advanced Packages Designed and Fabricated at Fraunhofer IZM

Who Should Attend

Engineers, scientists, researchers, designers, managers, and graduate students interested in the fundamentals of electronic packaging as well as those involved in the process of electrical design, layout, processing, fabrication and/or system-integration of electronic packages for emerging applications (e.g., 5G, 6G, mmwave radar sensors) should attend.

11. FAN-OUT PACKAGING AND CHIPLET HETEROGENEOUS INTEGRATION

Course Leader: John Lau – Unimicron

Course Description

Fan-out wafer/panel-level packaging has been getting lots of traction since TSMC used their integrated fan-out to package the application processor chipset for the iPhone 7. In this lecture, the following topics will be presented and discussed. Emphasis is placed on the fundamentals and latest developments of these areas in the past few years. Their future trends will also be explored. Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with varied sizes and functions, and from different fabless design houses, foundries, wafer sizes, and feature sizes into a system or subsystem on a common package substrate. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented.

Course Outline

1. Formation of FOWLP: (a) Chip-First (Face-Down), (b) Chip-First (Face-up), and (c) Chip-Last Fabrication of Redistribution Layers (RDLs) Formation of FOPLP: (a) Chip-First (Face-Down), (b) Chip-First (Face-Up), and (c) Chip-Last
2. TSMC InFO: (a) InFO-PoP, and (b) InFO-AiP Driven by 5G mmWave
3. Samsung PLP: (a) PoP for SmartWatches and (b) SiP SbS for Smartphones
4. Warpages: (a) Warpage Types and (b) Allowable Warpages
5. Reliability of FOWLP and FOPLP: (a) Thermal-Cycling and (b) Drop Course - Many Examples of FOWLP and FOPLP
6. Chiplet Design and Heterogeneous Integration (HI) Packaging vs. System-On-Chip (SoC) Advantages and Disadvantages of Chiplet Design and HI Packaging - Many Examples of Chiplet Design and HI Packaging
7. Chiplets Lateral Interconnects (Bridges) - Many Examples
8. Chiplet Design and HI Packaging on Organic Substrates (SiP) - Many Examples
9. Chiplet Design and HI Packaging on Silicon Substrates (TSV-Interposers) - Many Examples
10. Chiplet Design and HI Packaging on Fan-Out RDL Substrate - Many Examples
11. Assembly Technologies for Chiplet Design and HI Packaging

Who Should Attend

If you are involved with any aspect of the electronics industry, you should attend this course. The lectures are based on the publications by many distinguished authors and the books (by the lecturer) such as Fan-Out Wafer-Level Packaging (Springer, 2018) and Chiplet Design and Heterogeneous Integration Packaging (Springer, 2023).

12. ANALYSIS OF FRACTURE AND DELAMINATION IN MICROELECTRONIC PACKAGES

Course Leader: Andrew Tay – National University of Singapore

Course Description

The main objective of this course is to provide a fundamental understanding as well as techniques of applying the fracture mechanics methodology to predicting fracture and delamination in microelectronic packages. The mechanism of delamination failure due to thermal stress and moisture will be described and analyzed. Simulation of transient heat transfer and moisture diffusion processes occurring during package qualification will be described. An introduction to the fundamentals of interfacial fracture mechanics will be given together with descriptions of some numerical methods of calculating fracture mechanics parameters. Experiments which verify the methodology for predicting delamination in

packages will then be described followed by some interesting case studies.

Course Outline

1. Development of Hygrothermal Stresses in Microelectronics Packages
2. Finite Element Analysis and Stress Singularities in Microelectronic Packages.
3. Inadequacy of Maximum Stress Failure Criterion
4. Fundamentals of Fracture Mechanics Methodology
5. Computation of Fracture Mechanics Parameters
6. Measurement of Fracture Toughness
7. Experimental Verification of the Methodology
8. Case Studies on Delamination of Pad-Encapsulant Interfaces, Die-Attach Layers, and On-Chip Interconnect Structures (BEOL)
9. Cohesive Zone Modeling of Delamination and Case Study

Who Should Attend

This course is designed for packaging design engineers who perform reliability analysis of microelectronics and photonics packages.

13. ADVANCED PACKAGING FOR MEMS AND SENSORS

Course Leader: Horst Theuss – Infineon Technologies AG

Course Description

Sensors are everywhere! They create data and provide the "food" for the Internet of Things. Which specific requirements distinguish MEMS and sensor packaging from standard assembly? How are these challenges being tackled? Do we need advanced packaging technologies for MEMS? These are just a few questions which are addressed in the course. From a general introduction into package platforms, MEMS-specific challenges will be derived – e. g. the need for low package induced stress and its impact to MEMS performance, the necessity to create cavities or the implementation of MEMS-specific package materials and processes. The course reviews the state of the art, but also explores some topics in more detail. These topics refer to case studies comprising pressure and impact sensors, microphones, mirrors, magnetic sensors, and Radar devices. A further section elaborates on robustness requirements and approaches for risk mitigation in harsh environments.

A discussion on advanced packaging contains developmental studies on integrating MEMS-microphones or RF-antennas into Fan-Out-Wafer-Level-Packages. The concluding chapter deals with systems and heterogeneous integration. Where is the overlap of the processor-driven world of advanced packaging and the MEMS/Sensor world? Where are differences, how can we overcome them and where will the future lead us?

Course Outline

1. Packaging - What is different for MEMS and Sensors?
2. Cavity Packaging
3. Low Stress Packaging and Materials
4. Chemical Robustness
5. Case Studies
6. Heterogeneous Integration and Advanced Packaging

Who Should Attend

The course is intended for engineers and technical managers working in the field of MEMS or sensors. It gives an overview on the MEMS packaging landscape but also elaborates more fundamentally into selected topics. It will as well welcome students and newcomers, who are interested in broadening their MEMS-specific knowledge.

14. NANO MATERIALS AND POLYMER COMPOSITES FOR ELECTRONIC PACKAGING

Course Leaders: C.P. Wong – Georgia Tech and Daniel Lu – Henkel Corporation

Course Description

Nano materials and polymer composites are widely used in electronic and photonic packaging as adhesives, encapsulants, thermal interface materials, insulators, dielectrics, molding compounds and conducting elements for interconnects. These materials also play a critical role in the recent advances of high performance encapsulants for ball grid array (BGA), chip scale package, system in package (SIP), package-on-package, and heterogeneous integration packaging, electrically conductive adhesives (both ICA and ACA), embedded passives (high K polymer composites), and nanoparticles and nano functional materials such as CNTs (some with graphenes). It is imperative that both materials suppliers and customers have a thorough understanding of polymeric materials, the latest advances on nano materials, and their impact to advance electronic packaging and integration technologies.

Course Outline

1. Introduction to Nanotechnology
2. Nanosolder
3. Carbon Nanotube (CNT)
4. Nanomaterials for Wafer Level Packaging
5. Super Hydrophobic Surface
6. Surface Functionalization
7. Functionalized Graphene for Energy Storage and Electrocatalysis
8. Electrically Conductive Adhesives
9. Conductive Nano Composites
10. Conductive Nano-Ink
11. Transparent Nanocomposite

IMPORTANT NOTICE

Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

Who Should Attend

Students, researchers, engineers, scientists and managers who are involved in research and development, designing, processing and manufacturing of microelectronic and optoelectronic components and packages, and suppliers and developers of materials for semiconductor and electronic packaging.

15. DESIGN-ON-SIMULATION FOR ADVANCED PACKAGING RELIABILITY AND LIFE PREDICTION

Course Leaders: Kuo-Ning Chiang – National Tsing Hua University

Course Description

The electronic packaging community has widely used Design-on-Simulation (DoS) methodology for designing new packaging structures. However, it has encountered many challenges in ensuring a trustable simulation result. Artificial intelligence (AI)/machine learning approaches can be combined with DoS to solve this uncertainty. This course aims to illustrate the solution methodology and procedure, including the fundamentals of physics associated with different failure mechanisms in electronic packaging, finite element analysis (FEA) and simulation, large database generation, and AI training performance of different machine learning algorithms. This course will also describe how to combine AI and finite element simulation to estimate the reliability life and obtain the best structure combination of each packaging component using wafer-level packages as demonstrations. The course will cover the following topics: 1) Introduction to advanced packaging; 2). Physics of failures due to thermal, mechanical, moisture/humidity and electromigration. 3). Finite element simulation, 4) Material constitutive equations, 5) AI-Assisted DoS, and 6) Solder joint reliability life cycle prediction empirical equations.

Course Outline

1. Introduction to Advanced Packaging
2. Finite Element Analysis and Simulation
3. Material Properties and Constitutive Equations
4. AI-Assisted Design-On-Simulation Methodology
5. AI Solvers
6. Case Study: Solder Joint Reliability Life Cycle Prediction Empirical Equations

Who Should Attend

This course is intended for technical managers and staff members, reliability engineers, scientific researchers, and graduate students who are involved in thermal/mechanical modeling, package design, material selection, qualification, and reliability assessment of chip-package interaction, package, and package/board interaction.

16. THERMAL SPREADING AND CONTACT RESISTANCE

Course Leaders: Yuri Muzychka – Memorial University of Newfoundland and Marc Hodes – Tufts University

Course Description

This course will mainly focus on fundamentals and applications of thermal spreading and contact resistance for thermal management in electronics packaging. The course will be based in part on the new text Thermal Spreading and Contact Resistance, by Y. Muzychka and M. Yovanovich, Wiley, 2023. The last part of the course will discuss analytical techniques relevant to the modeling of thermoelectric modules, micro-devices, thermal interface materials (TIMs), heat sinks and heat pipes, to complement the core material on spreading and contact resistance, providing a holistic view of the power of analysis in thermal design.

Course Outline

1. Introduction
2. Thermal Spreading (Constriction) Resistances
3. Semi-Infinite, Finite Domains, and Multi-Component Systems
4. Thermal Spreaders With Isotropic, Compound, and Orthotropic Materials
5. Single and Multi-Source Systems
6. Non-Uniform Conductance in Heat Sinks
7. Interface Materials
8. Thermal Contact Resistance of Rough Conforming and/or Non-Conforming Surfaces
9. Simple Models
10. Spreading Resistance in Domains With Surface Roughness
11. Role of Spreading Resistance in Flows Over Superhydrophobic Surfaces
12. Practical Examples and Case Studies
13. Analysis Relevant to Thermoelectric Modules, Heat Sinks and Heat Pipes

Who Should Attend

Mechanical and electrical engineers working in thermal management of electronics packaging at device level, package level, or system level. Both experienced applications engineers and newcomers to the field will benefit from participation in the proposed short course, as will academics doing research in the field.

IMPORTANT NOTICE

Morning PD Courses 1 through 8 or afternoon PD Courses 9 through 16 run concurrently.
Make sure you indicate which course you plan to attend in the morning and/or in the afternoon. As sessions run concurrently, attendance is only allowed at one session in the morning and one session in the afternoon.
See page 32 for registration information

AREA ATTRACTIONS

Overlooking the city of Denver skyline, framed by the Rocky Mountains, the Gaylord Rockies Resort & Convention Center is the first true tourism product in Aurora, Colorado - a rapidly growing community directly east of Denver.

Located just 10 minutes from Denver International Airport, this resort is the fifth Gaylord Hotels® property and one of the largest resorts in the world to debut under the Marriott International brand. The Denver area has seen unprecedented growth in the past decade, but the Gaylord Rockies Resort & Convention Center is the definition of a game changer for the region, delivering 1,501 sleeping rooms, 485,000 square feet of convention center space and an extensive indoor/outdoor water park on a sprawling 85-acre site. The resort also offers eight dining options, a luxurious spa and salon, indoor and outdoor pools, a 75-foot TV in the Mountain Pass Sports Bar, and picture-perfect views of the mountains. Book your stay today!

Program Sessions: Wednesday, May 29, 9:30 a.m. - 12:35 p.m.

Session 1: Advances in Fan-Out, Wafer-Level, and Panel-Level Packaging Technologies Enabling New Applications	Session 2: Advanced Die-to-Wafer Hybrid Bonding for Heterogeneous Integration	Session 3: Co-Packaged Optics
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Photonics**
Session Co-Chairs: **Beth Keser** **ZeroASIC** **Email: bethk@kesers.com** **Steffen Kroehnert** **ESPAT Consulting** **Email: steffen.kroehnert@espat-consulting.com**	**Session Co-Chairs:** **Katsuyuki Sakuma** **IBM Research** **Email: ksakuma@us.ibm.com** **Tiwei Wei** **Purdue University** **Email: tiwei@purdue.edu**	**Session Co-Chairs:** **Richard Pitwon** **Resolute Photonics** **Email: richard.pitwon@resolutephotonics.com** **Nicolas Boyer** **Ciena** **Email: nboyer@ciena.com**
1. 9:30 AM - How to Manipulate Warpage in Fan-Out Wafer and Panel Level Packaging Tanja Braun, Ole Hölck, Marius Adler, Mattis Obst, Steve Voges, Karl-Friedrich Becker, Rolf Aschenbrenner - Fraunhofer IZM; Marcus Voitel, Marc Dreissigacker, Martin Schneider-Ramelow - Technical University Berlin	***1. 9:30 AM - Direct Die-to-Wafer Hybrid Bonding Using Plasma Diced Dies and Bond Pad Pitch Scaling Down to 2 µm*** Ye Lin, Pieter Bex, Koen Kennes, Jaber Derakhshandeh, Prathamesh Dhakras, Samuel Suhard, Carine Gerets, Sven Dewilde, Violeta Georgieva, Anne Jourdain, Gerald Beyer, Eric Beyne - imec	***1. 9:30 AM - High Density Integration of Silicon Photonic Chiplets for 51.2T Co-Packaged Optics*** Sukeshwar Kannan, Ray Chang, Hari Potluri, Sheng Zhang - Broadcom, Inc.; Jay Li, Bruce Xu, Hsi-Chang Hsu - Siliconware Precision Industries Co., Ltd.
2. 9:50 AM - Advanced FO-PLP With Multi-Chip Using 3 nm AP for Wearable Application Jooyoung Choi, Hyungmin Kim, Jaehoon Choi, Eun Seok Choi, Hwanpil Park, Gyunghwan Oh, Seungsoo Ha, Wonkyung Choi - Samsung Electronics Co., Ltd.; Dong Wook Kim - Samsung	***2. 9:50 AM - Multi-Functional Self-Assembled Monolayer (SAM) for Chip-to-Chip and Chip-to-Wafer Hybrid Bonding Yield Enhancement*** Murugesan Mariappan, H Hashimoto, T Fukushima - Tohoku University; K Mori - T-Micro; A Kurachi, T Imori - JX Metals Corporation	***2. 9:50 AM - Ultra Low-Loss Ion-Exchange Waveguides in Optimized Alkali Glass for Co-Packaged Optics*** Lars Brusberg, Matthew J. Dejneka, Chukwudi A. Okoro, David J. McEnroe, Aramais R. Zakharian, Chad C. Terwilliger - Corning Research and Development Corp.
3. 10:10 AM - Transcending the Reticle Limit in On-Wafer Die Integration and Advanced Packaging: Full-Wafer Patterning With High-Productivity Electron Beam Lithography Andrew Ceballos, Kenneth MacWilliams, Ted Prescop, Tsenguun Byambadorj, David Lam - Multibeam Corporation; Timothy Michalka - TLM Technologies, LLC; Craig Bishop, Cliff Sandstrom, Tim Olson - Deca Technologies, Inc.	***3. 10:10 AM - 3D Heterogeneous Integration With Sub-3 µm Bond Pitch Chip-to-Wafer Hybrid Bonding*** Yi Shi, Haris Niazi, Michael Baker, Yuan Meng, Ashish Dhall, Xavier Brun - Intel Corporation	***3. 10:10 AM - A Surface-Mount Photonic Package With a Photonic-Wire-Bonded Glass Interposer as a Hybrid Integration Platform for Co-Packaged Optics*** Hiroshi Uemura, Taichi Misawa, Yasutaka Mizuno, Hajime Arao, Tetsuya Nakanishi, Keiji Tanaka, Tomomi Sano, Katsumi Uesaka - Sumitomo Electric Industries, Ltd.; Mami Miyairi, Yoshikatsu Ishizuki, Taiji Sakai - FICT LIMITED; Yoichiro Kurita - Tokyo Institute of Technology
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - 600 mm x 600 mm Fan-Out Panel Level Package (FOPLP) as an Alternative to Lead-Frame-Free Quad Flat No Lead (QFN) Package Jacinta Aman Lim, Yoon Muk Park, Brett Dunlap, Jane Lee - nepes Corporation; Robin Davis - DECA	***4. 11:15 AM - Novel Three-Layer Stacking Process With Face-To-Back CoW 6 µm-Pitch Hybrid Bonding*** Akihiro Urata, Takahiro Kamei, Akihisa Sakamoto, Hirotaka Yoshioka, Kan Shimizu, Yoshihisa Kagawa, Hayato Iwamoto - Sony Semiconductor Solutions Corporation	***4. 11:15 AM - Development of All-Photonics-Function Embedded Package Substrate Using 2.3D RDL Interposer for Co-Packaged Optics*** Akihiro Noriki, Fumi Nakamura, Satoshi Suda, Takayuki Kurosu, Takeru Amano - National Institute of Advanced Industrial Science and Technology; Hirotaka Uemura, Haruhiko Kuwatsuka, Naoki Matsui, Reona Motoji, Dan Maeda, Tomoya Sugita - Kyocera Corporation
5. 11:35 AM - Challenges and Analysis for Pitch 25 µm - 100 µm Mixed Micro Bumps and Interconnection in Fan-Out Embedded Bridge Die With TSV Package (FO-EB-T) Kuei Hsiao Kuo, Jia Han Li, Chia Shing Wu, Feng Lung Chien - Siliconware Precision Industries Co., Ltd.	***5. 11:35 AM - Dielectric Stack Optimization for Die-Level Warpage Reduction for Chip-to-Wafer Hybrid Bonding*** Chandra Rao Bhesetti, Dileep Kumar Mishra, Nagendra Sekhar Vasarla, Sasi Kumar Tippabhotla, Ismael Cereno Daniel, Ser Choong Chong, King Jien Chui, Srinivasa Rao Vempati - Institute of Microelectronics A*STAR	***5. 11:35 AM - Advanced 3D Packaging of 3.2Tbs Optical Engine for Co-packaged Optics (CPO) in Hyperscale Data Center Networks*** Aparna Prasad, Sandeep Razdan, Paul Ton, Cristiana Muzio - Cisco Systems, Inc.
6. 11:55 AM - High Precision and Productivity Bridge-Die-Last Bonding Process and Its Reliability for Pillar-Suspended Bridge (PSB) Architecture Ichiro Kono, Yoshihiro Kometani, Atsushi Kuroha - AOI Electronics; Ken Ukawa - Sumitomo Bakelite Co., Ltd.; Yoichiro Kurita - Tokyo Institute of Technology	***6. 11:55 AM - Low Temperature Wafer Level Hybrid Bonding Enabled by Advanced SiCN and Surface Activation*** Fumihiro Inoue, Junya Fuse, Sodai Ebiko, Ryosuke Sato - Yokohama National University; Atsushi Nagata, Yoshihiro Kondo - Tokyo Electron Kyushu, Ltd.; Kenichi Saito, Takuo Kawauchi - Tokyo Electron, Ltd.; Junghwan Park, Chiwoo Ahn, Myeonghyeon Kim, Jiho Kang - SK Hynix, Inc.	***6. 11:55 AM - 3D-Printed Beam Expanding Lens for Chip to Fiber Vertical Coupling*** Yasutaka Mizuno, Hiroshi Uemura, Tomoya Saeki, Keiji Tanaka, Katsumi Uesaka - Sumitomo Electric Industries, Ltd.
7. 12:15 PM - Vertical Fan-Out WLP technology With Enhanced Form Factor and Performance for Mobile Applications Ichiro Kono, Yoshihiro Kometani, Atsushi Kuroha - AOI Electronics; Yoichiro Kurita - Tokyo Institute of Technology	***7. 12:15 PM - A Study on D2W Hybrid Cu Bonding Technology for HBM Multi-Die Stacking*** Hyeonmin Lee, Jihoon Kim, Hyungchul Shin, Wonil Lee, Aeni Jang, Hyuekjae Lee, Byungchan Kim, Ilhwan Kim, Dongjoon Oh, Jumyong Park, Un-Byoung Kang, Dae-Woo Kim - Samsung Electronics Co., Ltd.	***7. 12:15 PM - Characterization of QSFP and OSFP CPO ELS Modules Employing an 8-channel CWDM TOSA in Practical Air-Cooling Conditions*** Kohei Umeta, Taketsugu Sawamura, Kyoko Nagai, Yuki Shiroishi, Hideyuki Nasu - Furukawa Electric Co., Ltd.

Program Sessions: Wednesday, May 29, 9:30 a.m. - 12:35 p.m.

Session 4: Reliability of Advanced Substrates and Interconnects	Session 5: Digital Health Care: Wearable Sensors, and Flexible Electronics	Session 6: Thermal-Mechanical Reliability Simulations
Committee: Applied Reliability	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Rabindra N. Das** **MIT Lincoln Labs** **Email: rabindra.das@ll.mit.edu** **Hee Seok Kim** **Washington State University** **Email: heeskim@uw.edu**	**Session Co-Chairs:** **Rabindra N. Das** **MIT Lincoln Labs** **Email: rabindra.das@ll.mit.edu** **Hee Seok Kim** **Washington State University** **Email: heeskim@uw.edu**	**Session Co-Chairs:** **Wei Wang** **Clemson University** **Email: wwang@g.clemson.edu** **Karsten Meier** **TU Dresden** **Email: karsten.meier@tu-dresden.de**
1. 9:30 AM - Reliability Assessment of Stacked-Vias With Different Configurations Through a Unit Cell-based Substrate Design Krishna Tunga, Joseph Ross, Shidong Li, Sushumna Iruvanti, Bakul Parikh - IBM Corporation	***1. 9:30 AM - Three-Dimensional Integration of a Flexible Battery and a Flexible Wireless Charger for Powering Wearables*** Guangqi Ouyang, Subramanian Iyer - University of California, Los Angeles	***1. 9:30 AM - Modeling and Optimization of Thermal Cycling Performance to Reduce Ratcheting-Induced Passivation Cracking in High-Voltage Power Modules*** Bill Chen, Yong Liu - ON Semiconductor
2. 9:50 AM - Enhanced Biased HAST Reliability of Polyimide for High-Density Redistribution Layers Takumi Onuma, Daisaku Matsukawa, Takahiro Tanabe - HD MicroSystems LLC	***2. 9:50 AM - Ferrite-Based NFC Antenna and Sensor Package Module Development for Implantable Continuous Glucose Monitor*** Gaurav Mehrotra, Young Kim, Marko Mailand - Renesas Electronics Corporation; James Masciotti - Senseonics, Inc.; Ginger Huang, Jackson Chen, Ryan Lai - Advanced Semiconductor Engineering, Taiwan	***2. 9:50 AM - Interfacial Reliability and Predictive Models for Potted Board Assemblies in Inclined 25000 g Mechanical Shock*** Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Jeff Suhling - Auburn University; Ken Blecker - US Army
3. 10:10 AM - Effect of Lamination Process-Induced Residual Stress on the CTE of Advanced Prepregs Before and After Solder Reflow Process Byoung-Phil Kang - Chungbuk National University/ SIMMTECH; Jong-Yun Lee - Chungbuk National University; Jaesung Kim, Jongwoo Park, Kyu-Jin Lee - SIMMTECH; Yongrae Jang, Bongtae Han - University of Maryland	***3. 10:10 AM - Design and Development of Sustainable Low-Cost Single-Use Electrode Leads for Wearable Medical Devices*** Babatunde Falola, Riadh Al-Haidari, Udara Somarathna, Bryan Cabrera, Mohammed Alhendi, Mark D Poliks - Binghamton University; Nancy Stoffel - General Electric Global Research; Gurvinder Khinda, Tzu-Jen Felix Kao - General Electric Healthcare; Rafael Tudela - Tapecon, Inc.	***3. 10:10 AM - Peridynamic Simulation of Failure Due to Electromigration*** Yanan Zhang, Sundaram Vinod Kumar Anicode, Erdogan Madenci - University of Arizona; Xuejun Fan - Lamar University; Yile Hu - Shanghai Jiao Tong University
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Fan-Out PoP Solder Joint Reliability Investigation by System Power Cycling Chi Ko Yu, Techi Wong, Hank Hsieh, P. H. Tsao, M.Z. Lin, Liham Chu - MediaTek, Inc.	***4. 11:15 AM - Conformal Patch for Dehydration Monitoring in Dementia Patients*** Musafargani Sikkandhar, Ramona B. Damalerio, Wei Da Toh, Ming-Yuan Cheng - Institute of Microelectronics A*STAR	***4. 11:15 AM - A Robust Mesh Size Control Technology Suitable for Various Empirical Equations for Predicting Solder Joint Reliability*** Kuo-Ning Chiang, C. E Lee - National Tsing Hua University; Cadmus Yuan - Feng Jia University
5. 11:35 AM - Fatigue-Fracture Propensity Measurement and Competing Risk Model for FCBGA Interfaces Under Sustained Humidity and Temperature Exposure Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Madhu Kasturi, Jeff Suhling - Auburn University	***5. 11:35 AM - Silicon-Based Membrane Pressure Sensor for Inline Monitoring of Pressure and Hermeticity of Small-Volume Bonded Packages*** Jannik Koch, Levin Brinkmann, Alexander Kassner, Folke Dencker, Marc Wurz - Institute of Micro Production Technology	***5. 11:35 AM - Multi-Material Corner Singularity in Electronic Packaging: Avoiding Mesh Dependence in Analyzing Stress*** Yaxiong Chen, Torsten Hauck - NXP Semiconductor, Inc.; Ganesh Subbarayan - Purdue University
6. 11:55 AM - Evaluation of Vapor Pressure Induced Debonding Failure in Fan-Out Package Under Reflow Condition Bo-Shuo Chen, Tz-Cheng Chiu - National Cheng Kung University; Wei-Jie Yin, Chin-Li Kao - Advanced Semiconductor Engineering, Taiwan	***6. 11:55 AM - A Noninvasive Flexible Bio Optical Sensor for Hemoglobin Detection*** Yu-Chih Lee, Kai-Lun Yu, Shu-An Tsai, Pai-Sheng Shih, Guo-Sin Huang, Tien-Chia Liu, Chih-Lung (Steven) Lin, Jen-Chun Chen, Jen-Kuang Fang, Harrison Chang - Advanced Semiconductor Engineering, Inc.; Tzyy-Wei Fu, Sheng-Hao Tseng - National Cheng Kung University	***6. 11:55 AM - Bayesian Optimization of Large, Glass BGA Package Design for System-Level Reliability in Chiplet-Based High-Performance Computing and AI Architectures*** Emanuel Torres Surillo, Christian Molina-Mangual, Pratik Nimbalkar, Hyunggyu Park, Ramon Sosa, Vanessa Smet - Georgia Institute of Technology
7. 12:15 PM - Characterization and Sensitivity Analysis of Piezoresistive Stress Sensor for Thermal and Mechanical Loads and Implementation for In-Situ Health Monitoring of Solder Bumps Adwait Inamdar, Willem van Driel, GuoQi Zhang - Delft University of Technology; Varun Thukral, Letian Zhang, Jeroen Zaal, Michiel van Soestbergen, Hanz Tuinhout - NXP Semiconductor, Inc.	***7. 12:15 PM - A Multi-Channel, Embedded, and Geometrically Optimized Filter Bank Utilizing Advanced Packaging Topologies for Miniaturized RF Modules in IoT and Wearable Systems*** Hani Al-Jamal, Marvin Joshi, Manos M. Tentzeris - Georgia Institute of Technology; Nick Kingsley - Teradyne	***7. 12:15 PM - Prediction of Moisture Absorption Characteristics Under Normal/ Accelerated Preconditioning Condition in Multi-Chip Packages*** Hyunggyun Noh, Jinsoo Bae, Keunho Rhew, Soojin Yoo, Jiyoung Lim, Yuchul Hwang, Sangwoo Pae - Samsung Electronics Co., Ltd.

Program Sessions: Wednesday, May 29, 2:00 p.m. - 5:05 p.m.

Session 7: Heterogeneous Integration: Systems Design, Signal & Power Delivery, and Process Optimization

Committee:
Packaging Technologies

Session Co-Chairs:
Lihong Cao
ASE
Email: lihong.cao@aseus.com

Subhash L. Shinde
Notre Dame University
Email: sshinde@nd.edu

1. 2:00 PM - Next Generation Large Size High Interconnect Density CoWoS-R Package
Chien-Hsun Lee, C.L. Lai, M. Liu, J. Hu, S.L. Tsai, H.Y. Chen, J. Lin, C.C. Hsieh, C.K. Hsu, Kathy Yan, Shin-Puu Jeng, Jun He - Taiwan Semiconductor Manufacturing Company, Ltd.

2. 2:20 PM - World's First UCIe Interoperability Silicon Enabling Open Standards Heterogeneous Integration
Xavier Brun, Stephen Wong - Intel Corporation; Manuel Mota - Synopsys, Inc.

3. 2:40 PM - Scalable Advanced DBHi Chiplet Package Using Silicon Bridge With 30 µm-pitch Solder Joints
Akihiro Horibe, Takahito Watanabe, Chinami Marushima, Sayuri Kohara, Hiroyuki Mori - IBM Research, Tokyo; Divya Taneja, Thomas Wassick, Isabel de Sousa - IBM Infrastructure; Qianwen Chen, Eric Perfecto, Aakrati Jain, Joseph Ross - IBM Research

4. 3:45 PM - Performance Evaluation of UCIe-based Die-to-Die Interface on Low-Cost 2D Packaging Technology
Srujan Penta - Marvell Technology, Inc. / Georgia Institute of Technology; Ting Zheng, Aatreya Chakravarti, Wolfgang Sauter, Eric Tremble, Anthony Sigler, Carl Benes - Marvell Technology, Inc.; Muhannad Bakir - Georgia Institute of Technology

5. 4:05 PM - Signal & Power Integrity Optimization Utilizing Silicon Core Substrate (SCS)
Seann Ayers, Steven Verhaverbeke, Han-Wen Chen, Liu Jiang, El Mehdi Bazizi - Applied Materials, Inc.

6. 4:25 PM - Package Power Delivery Architecture for High Performance Computing Systems With a 1 kW IVR Operated in CCM-DCM Boundary Mode With High Efficiency
Ramin Rahimzadeh Khorasani, Madhavan Swaminathan - Pennsylvania State University; Rohit Sharma - Indian Institute of Technology Ropar

7. 4:45 PM - Study for Realization of the Next Generation High Density RDL Packaging for 2.5D Large Silicon Interposer
Masaki Mizutani, Yusuke Tokuyama, Noriyuki Shiozawa, Mizuma Murakami, Hiromi Suda, Ken-Ichiro Shinoda, Ken-Ichiro Mori - Canon, Inc.; Douglas Shelton - Canon USA, Inc.

Session 8: Sub-Micron Scaling in Wafer-to-Wafer Hybrid Bonding

Committee:
Interconnections

Session Co-Chairs:
Jean-Charles Souriau
CEA Leti
Email: jcsouriau@cea.fr

Matthew Yao
GE Aerospace
Email: matthew.yao@ge.com

1. 2:00 PM - Study of Ultra Fine 0.4 µm Pitch Wafer-to-Wafer Hybrid Bonding and Impact of Bonding Misalignment
Yukako Ikegami, Takumi Onodera, Masanori Chiyozono, Akihisa Sakamoto, Kan Shimizu, Yoshihisa Kagawa, Hayato Iwamoto - Sony Semiconductor Solutions Corporation

2. 2:20 PM - 3-Layer Fine Pitch Cu-Cu Hybrid Bonding Demonstrator With High Density TSV for Advanced CMOS Image Sensor Applications
Stephane Nicolas, Jerzy-Javier Suarez-Berru, Nicolas Bresson, Carole Socquet-Clerc, Myriam Assous, Stephan Borel - Grenoble Alps University/CEA-LETI

3. 2:40 PM - Scaling Cu/SiCN Wafer-to-Wafer Hybrid Bonding Down to 400 nm Interconnect Pitch
Boyao Zhang, Soon-Aik Chew, Michele Stucchi, Sven Dewilde, Serena Iacovo, Liesbeth Witters, Tomas Webers, Koen Van Server, Joeri De Vos, Andy Miller, Gerald Beyer, Eric Beyne - imec

4. 3:45 PM - Fine Pitch and Low Temperature Nanocrystalline-Nanotwinned Cu and SiCN-to-SiO2 Wafer-to-Wafer Hybrid Bonding
Wei-Lan Chiu, Ou-Hsiang Lee, Chia-Wen Chiang, Hsiang-Hung Chang, Chin-Hung Wang, Wei-Chung Lo - Industrial Technology Research Institute; James Yi-Jen Lo, Chiang-Lin Shih, Hsih-Yang Chiu - Nanya Technology Corporation

5. 4:05 PM - Single-Grain Cu µ-Joint Formation Directed by Selective Under-Seed-Metallurgy (USM) for Hybrid Bonding
Murugesan Mariappan, H Hashimoto, T Fukushima - Tohoku University; K Mori - T-Micro; M Sawa, J Nampo - JCU Corporation

6. 4:25 PM - 0.5 µm Pitch Wafer-to-Wafer Hybrid Bonding at Low Temperatures With SiCN Bond Layer
Kai Ma, Nikos Bekiaris, Sesh Ramaswami - Applied Materials, Inc.; Taotao Ding, Gernot Probst, Tobias Wernicke, Thomas Uhrmann, Markus Wimplinger - EV Group, Inc.

7. 4:45 PM - Development of Double Cantilever Beam Technique for Wafer-to-Wafer Bond Energy Measurement
Guohua Wei, Matthew Gerber, Derik Rudd, Robert Sibley, Pengfei Nie, Logan Battrell, Andrew Bayless, Sam Ireland, Mark Fischer, Dan Markowitz, David Palsulich - Micron Technology, Inc.

Session 9: Advanced Processes for Chip Stacking Committee: Materials & Processing

Committee:
Materials & Processing

Session Co-Chairs:
Qianwen Chen
IBM Research
Email: chenq@us.ibm.com

Vidya Jayaram
Intel
Email: vidya.jayaram@intel.com

1. 2:00 PM - IR Laser Release for 3D Stacked Devices: Effect of the Release Stack Structure on the Debonding Mechanism
François Chancerel, John Slabbekoorn, Steven Brems, Alain Phommahaxay, Erik Beyne - imec; Peter Urban, Julian Bravin, Thomas Uhrmann, Markus Wimplinger - EV Group, Inc.

2. 2:20 PM - High Performance 3D Package Technology for Mobile Application Processor (AP)
Sun Jae Kim, Cheol Kim, Huiyeong Jang, Jongpa Hong, Seongyo Kim, Yongwon Choi, Chajea Jo, Sun-Kyung Seo, Dong Kwan Kim, Dae-Woo Kim - Samsung Electronics Co., Ltd.

3. 2:40 PM - Advancements in Photonic Debonding: Processing Silicon-Based Power Devices
Vahid Akhavan, Vikram Turkani, Harry Chou, Rudy Ghosh, Boone Munson - PulseForge, Inc.; Rajesh Rao, Vishal Trivedi, Leo Mathew - Applied Novel Devices; Andy Jones, Nathan Parker, Seth Molenhour, Luke Prenger - Brewer Science, Inc.

5. 4:05 PM - IR Laser Debond from Silicon Carrier Wafers With Inorganic Thin Films for High-Density 2.5D and 3D Integration
Thomas Sounart, Tushar Talukdar, Henning Braunisch, Paul Nordeen, Kimin Jun, Aleksandar Aleksov, Adel Elsherbini, Shawna Liff, Johanna Swan - Intel Corporation

6. 4:25 PM - Backside Thinning Process Development for High-Density TSV in a 3-Layers Integration
Renan Bouis, Lionel Vignoud, Jerome Dechamp, Damien Hebras, Paul Valentin, Jeremy Marchand, Stephan Borel - Grenoble Alps University/CEA-LETI; Myriam Assous - CEA-LETI

7. 4:45 PM - Process Development and Characterization of Ru-Based UBM for In Bumps Interconnects Integration for Quantum Assemblies
Harold Le Tulzo, Diane Bijou, Thérese Souza, Anthony Gallegos, Jérôme Daviot - Technic France; Candice Thomas, Edouard Deschaseaux, Céline Feautrier, Jean Charbonnier, Alain Gueugnot - CEA-LETI; Jaber Derakhshandeh, Tassawar Hussain - imec

Refreshment Break: 3:00 p.m. - 3:45 p.m.

Program Sessions: Wednesday, May 29, 2:00 p.m. - 5:05 p.m.

Session 10: Novel 3D Integration and Hybrid Bonding Solutions	Session 11: Next-Generation Artificial Intelligence, Quantum Computing, and Secure Packaging	Session 12: Artificial Intelligence and Advanced Modeling Approaches
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Zia Karim** **Yield Engineering Systems** **Email: zkarim@yieldengineering.com** **Wenhao (Eric) Li** **Intel** **Email: wenhao.li@intel.com**	**Session Co-Chairs:** **Rohit Sharma** **IIT Ropar** **Email: rohit@iitrpr.ac.in** **Santosh Kudtarkar** **Analog Devices** **Email: santosh.kudtarkar@analog.com**	**Session Co-Chairs:** **Yong Liu** **OnSemi** **Email: Yong.Liu@onsemi.com** **KN Chiang** **National Tsinghua University** **Email: knchiang@pme.nthu.edu.tw**
1. 2:00 PM - Investigation of Distortion in Wafer-to-Wafer Bonding With Highly Bowed Wafers Shuo Kang, Serena Iacovo, Koen D'havé, Stefaan Van Huylenbroeck, Joeri De Vos, Gerald Beyer, Eric Beyne - imec; Thomas Plach, Gernot Probst, Taotao Ding, Markus Wimplinger, Thomas Uhrmann - EV Group, Inc.	***1. 2:00 PM - Reworkable Superconducting Qubit Package for Quantum Computing*** Rabindra Das, John Cummings, Thomas Hazard, Danna Rosenberg, David Conway, Shireen Warnock, Michael Gingras, Cyrus Hirjibehedin, Bethany Huffman, Steven Weber, Jonilyn Yoder, Mollie Schwartz - MIT Lincoln Laboratory	***1. 2:00 PM - Machine-Learning Guided Strain-Relief Patterns for Maximizing Stretchability of Printed Conductors*** Rui Chen - Eastern Michigan University; Suresh Sitaraman - Georgia Institute of Technology
2. 2:20 PM - Development of 0.5 µm Pixel 3-Wafers Stacked CMOS Image Sensor With Through Silicon Deep Contact and In-Pixel Cu-to-Cu Bonding Process Do Yeon Kim - Samsung Electronics Co., Ltd.	***2. 2:20 PM - AR-Enabled Soft Wearable Electronics for Human-Machine Interfaces*** Hodam Kim, Woon-Hong Yeo - Georgia Institute of Technology	***2. 2:20 PM - Development of Real-Time Thermal Monitoring of GaN-based Power Inverter Modules Using Digital Twin*** Bin He, Gongyue Tang - Institute of Microelectronics A*STAR; Jaydeep Saha, Rahul Sadanand Bhujade, Sanjib Kumar Panda - National University of Singapore
3. 2:40 PM - Non-TCB Process Cu/SiO2 Hybrid Bonding Using Plasma-Free Hydrophilicity Enhancement With NaOH for Chip-to-Wafer Bonding Yu-An Chen, Jia-Juen Ong, Wei-You Hsu, Shih-Chi Yang, Chih Chen - National Yang Ming Chiao Tung University; Wei-Lan Chiu, Hsiang-Hung Chang - Industrial Technology Research Institute	***3. 2:40 PM - Fine Pitch Nb-Nb Direct Bonding for Quantum Applications*** Pablo Renaud, Christophe Dubarry, Nicolas Bresson, Edouard Deschaseaux, Frank Fournel, Christophe Morales, Anne-Marie Papon, Candice Thomas - Grenoble Alps University/CEA-LETI; Jean Charbonnier - CEA-LETI	***3. 2:40 PM - Creep Parameters for Solder Interconnects by Nanoindentation Inverse-FEA Method*** Shidong Li, Christine Taylor, Charles Arvin - IBM Corporation
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - A Novel Approach to Low Temperature Bonding Using Single Wafer Thermal Processing System Masha Gorchichko, Shashank Sharma, Ben Ng, Tyler Sherwood, Yoocharn Jeon, Kun Li, Sarabjot Singh, Evan Iler, Raghav Sreenivasan, Sid Krishnan - Applied Materials, Inc.	***4. 3:45 PM - Si Interposer With Cu TSVs on Cu Substrate Thermally and Electrically Anchoring Qubit Chips in Millikelvin Assembly*** Misato Taguchi, Takaaki Okidono, Takuji Miki, Makoto Nagata - Kobe University	***4. 3:45 PM - Deep Convolution Neural Networks for Automatic Detection of Defects Which Impact Hybrid Bonding Yield*** Oliver Zhao, Dominik Suwito, Bongsub Lee, Thomas Workman, Laura Mirkarimi - Adeia
5. 4:05 PM - Moving Towards Microchannel-Based Chip Cooling Paul Semenza, Gity Samadi - SEMI; Dave Thomas - SPTS Technologies, Ltd.; Garrett Oakes, Dave Kirsch - EV Group, Inc.; Yin Hang - Meta Platforms, Inc.; Kuo-Chung Yee - Taiwan Semiconductor Manufacturing Company, Ltd.; Michael Cumbie, Paul Benning - HP Inc.; Madhusudan Iyengar - Google; Lihong Cao, William Chen - Advanced Semiconductor Engineering, Inc. (US)	***5. 4:05 PM - Novel Approach for 3D Defect Detection and Metrology of HBMs Using Minimum Labeled Data*** Ziyuan Zhao, Jie Wang, Richard Chang, Xulei Yang, Ramanpreet Pahwa - Institute for Infocomm Research A*STAR; Ser Choong Chong - Institute of Microelectronics A*STAR	***5. 4:05 PM - Experimentally Validated Thermal Modeling Prediction for BEOL and BSPDN Stacks*** Xinyue Chang - imec/KU Leuven; Herman Oprins, Bjorn Vermeersch, Vladimir Cherman, Melina Lofrano, Seongho Park, Zsolt Tokei, Ingrid De Wolf - imec
6. 4:25 PM - Novel Inorganic Layer Based IR Release Process for High Temperature W2W and D2W Integration Thomas Uhrmann, Peter Urban, Boris Považay, Michael Josef Gruber, Bernd Thallner, Markus Wimplinger - EV Group, Inc.	***6. 4:25 PM - Design and Fabrication of a 2.5D Cryogenic Interposer With Integrated Superconducting TSVs and Resonators*** King Jien Chui, Hongyu Li - Institute of Microelectronics A*STAR	***6. 4:25 PM - Analysis of Mechanical Behavior of Hybrid SAC-LTS Joints Under Temperature Cycling With a Modified Garofalo Creep Model*** Souvik Chakraborty, Jeff Suhling - Auburn University; Yaxiong Chen, Gaurav Sharma, Abdullah Fahim, Torsten Hauck - NXP Semiconductor, Inc.; Ronit Das, Atif Mahmood, Peter Borgesen - Binghamton University
7. 4:45 PM - D2W Hybrid Bonding System Achieving Both High-Accuracy and High Throughput With Minimal Configuration Kentaro Mihara, Takashi Hare, Hirofumi Sakai, Shimpei Aoki, Toyoharu Terada - Toray Engineering Co., Ltd.; Mariappan Murugesan, Hiroyuki Hashimoto, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima - Tohoku University; Fumihiro Inoue - Yokohama National University; Akira Uedono - University of Tsukuba	***7. 4:45 PM - PQC-HI: PQC-enabled Chiplet Authentication and Key Exchange in Heterogeneous Integration*** Md Sami Ul Islam Sami, Kimia Zamiri Azar, Hadi Mardani Kamali, Farimah Farahmandi, Mark Tehranipoor - University of Florida	***7. 4:45 PM - ILD Crack Mechanical Reliability Mitigation*** Yutaka Suzuki, Williamson Jaimal, Rajen Murugan - Texas Instruments, Inc.

Program Sessions: Thursday, May 30, 9:30 a.m. - 12:35 p.m.

Session 13: Next-Generation Substrate Manufacturing Technologies	Session 14: Breakthrough Ultra-Fine Pitch Redistribution Layer and Solder Bumping Technologies	Session 15: Novel Materials and Process for Hybrid Bonding
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs: **Markus Leitgeb** **AT&S** **Email: m.leitgeb@ats.net** **Kuldip Johal** **MKS Instruments- MSD** **Email: kuldip.johal@atotech.com**	**Session Co-Chairs:** **Seung Yeop Kook** **GLOBALFOUNDRIES** **Email: seung-yeop.kook@globalfoundries.com** **Wei Zhou** **Micron** **Email: zhouwei@micron.com**	**Session Co-Chairs:** **Ivan Shubin** **Raytheon Technologies** **Email: ishubin@gmail.com** **Dwayne Shirley** **Marvel Semiconductor** **Email: shirley@ieee.org**
1. 9:30 AM - Development of Next Generation Chemical Mechanical Planarization Processes for Panel-Level Heterogeneous Integration Francoise Angoua, Aaditya Candadai, Daniel Rosales-Yeomans, Yosef Kornbluth, Dilan Seneviratne, Rahul Manepalli - Intel Corporation	***1. 9:30 AM - A Study on Improvement and Extension of Fine-Pitch Micro-Bump Interconnects Technology: New Metallurgy & Flux-Less Oxide-removal Laser Assembly (FLOLA)*** Seok-Geun Ahn, Ju-Hyeon Oh, Gwang-Jae Jeon, Dae-Ho Lee, Seok-Hyun Lee - Samsung Electronics Co., Ltd.	***1. 9:30 AM - Towards Standardization of Hybrid Bonding Interface: In-Depth Study of Dielectrics on Direct Bonding*** Yi Yang, Xavier F. Brun - Intel Corporation; Marco Flores - Arizona State University; Marc Weber - Washington State University
2. 9:50 AM - Dry Processes to Form Fine Via/Trench and Seed Layer on Advanced Substrate Wen Xiao, Qin Zhong, Cindy Mora, Anindarupa Chunder, Nicholas Loo, Sik Hin Chi, Cheng Sun, Weihua Qing, Harish V Penmethsa, Craig Rosslee, Jeff Turner - Applied Materials, Inc.	***2. 9:50 AM - A Novel Copper Microporous-Assisted Bonding Method for Fine-Pitch Cu/Sn Microbump 3D Interconnects*** Keyu Wang, Shuhang Lyu, Tiwei Wei - Purdue University	***2. 9:50 AM - Demonstration of Low Temperature Cu-Cu Hybrid Bonding Using a Novel Thin Polymer*** Yasuhisa Kayaba, Takuo Shikama, Wataru Okada, Kahori Tamura, Yuzo Nakamura, Yutaka Hisamune, Rikia Furusho - Mitsui Chemicals, Inc.
3. 10:10 AM - Direct Laser Patterning Using Excimer Laser on Polyimide Compositions With Low Dielectric Properties and Good Flexibility for Re-Distribution Layer Kanta Wataji, Akira Suwa, Junichi Fujimoto, Yasuhumi Kawasuji - Gigaphoton Inc; Takashi Yamaguchi, Taiyo Nakamura, Takashi Tazaki - Arakawa Chemical Industries, Ltd.; Masaru Sasago - ba2.so-net.ne.jp	***3. 10:10 AM - Challenges and Innovations in Dual Damascene Polymer RDL With 2 µm Pitch and Beyond*** Benjamin Briggs, Roger Quon, Chris Bencher, Ryan Ley, C.C. Chuang, Peng Suo, Andy Chang Bum Yong, Luisa Bozano, Jorge Fernandez, Prayundi Lianto, Niranjan Khasgiwale, Siddarth Krishnan - Applied Materials, Inc.	***3. 10:10 AM - Process Challenges in Thin Wafers Fabrication With Double Side Hybrid Bond Pads for Chip Stacking*** Dileep Kumar Mishra, Nagendra Sekhar Vasarla, Chandra Rao Bhesetti, Ser Choong Chong, Srinivasa Rao Vempati - Institute of Microelectronics A*STAR
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - New Power Delivery Network (PDN) Approach for Extremely Large FC-BGA With Organic Substrate Based on Over 1 mm-Thick Core Kyojin Hwang, Woobin Jung, Junghwa Kim, Heeseok Lee, Jisoo Hwang, Heejung Choi - Samsung Electronics Co., Ltd.	***4. 11:15 AM - Void Migration Kinetics in Fine Line Cu RDL Under Electric Current Stressing and the Improvement of Electromigration Reliability by Polyimide Passivation*** Yen-Cheng Huang, Kwang-Lung Lin - National Cheng Kung University; Min-Yan Tsai, Ting-Chun Lin, Yung-Sheng Lin - Advanced Semiconductor Engineering, Inc. (US)	***4. 11:15 AM - Development of Low Temperature Processable Polyimides for Organic Hybrid Bonding Applications*** Kota Nomura, Masaya Jukei, Hitoshi Araki, Tomoyuki Honda, Yu Shoji - Toray Industries, Inc.; Takenori Fujiwara - Toray Singapore Research Center
5. 11:35 AM - X-Ray Photoelectron Spectroscopy (XPS) Investigations to Monitor the Surface Chemistry During Palladium-Free Colloidal Copper Activation Ibbi Ahmet, André Beyer, Laurence J. Gregoriades, Julia Lehmann, Yvonne Welz - Atotech (MKS Instruments)	***5. 11:35 AM - Reliable Chiplet Integration on High Density Laminate (2.X D) for AI Hardware*** Divya Taneja, Jonathan Pouliot-Grenier, Isabel de Sousa - IBM Canada, Ltd.; Joseph Ross, Sathya Raghavan, Griselda Bonilla - IBM Research; Horiyuki Mori - IBM Research, Tokyo; Brian Quinlan Quinlian, Thomas Wassick - IBM Systems	***5. 11:35 AM - Effect of (111) Surface Ratio on the Bonding Quality of Cu-Cu Joints*** Huang Jian-Yuan, Chen Chih - National Yang Ming Chiao Tung University
6. 11:55 AM - Development of Glass Core Substrate With the Stress Analysis, Transmission Characteristics and Reliability Koji Fujimoto, Yashuhiro Okawa, Takahiro Tai, Satoru Kuramochi - DNP Co., Ltd.	***6. 11:55 AM - Zero-Misalignment Technology Achieves 333 IO/mm/Layer on Mold*** Veronica Strong, Trianggono Widodo, Holly Sawyer, Carolyn Aubertine, Aleksandar Aleksov, Johanna Swan - Intel Corporation	***6. 11:55 AM - Copper Microstructure Optimization for Fine Pitch Low Temperature Cu/SiO2 Hybrid Bonding*** Marie Maubert, Mathilde Gottardi, Pierre-Emile Philip, Emilie Fragnaud, Gilles Romero, Arnaud Cornelis, Hadi Hijazi - Grenoble Alps University/CEA-LETI; Frank Fournel, Maria-Luisa Calvo-Munoz - CEA-LETII
7. 12:15 PM - High Aspect Ratio (AR) Through Glass Via (TGV) Etch Performance on Glass Core Substrates for High Density 3D Advanced Packaging Applications Venugopal Govindarajulu, Coby Tao, Zia Karim, Aneelman Brar - Yield Engineering Systems; Sung Jin Kim - Absolics	***7. 12:15 PM - Charting a Path for the Chiplet Era and Beyond With Deep Submicron RDLs*** Craig Bishop - Deca Technologies, Inc.; Andrew Ceballos, Kenneth MacWilliams - Multibeam Corporation; Timothy Michalka - TLM Technologies, LLC	***7. 12:15 PM - Multi-Tier Die Stacking Through Collective Die-to-Wafer Hybrid Bonding*** Koen Kennes, Ye Lin, Samuel Suhard, Pieter Bex, Dieter H. Cuypers, Alain Phommahaxay, Gerald Beyer, Eric Beyne - imec; Alice Guerrero - Brewer Science, Inc.; Dennis Bumueller - SUSS MicroTec GmbH

Program Sessions: Thursday, May 30, 9:30 a.m. - 12:35 p.m.

Session 16: Reliability of High-Density and High-Power Packages	Session 17: Advanced Additive Manufacturing for Printed Electronics and Integrated Systems	Session 18: Radio Frequency Antenna-in-Package and Component Design
Committee: **Applied Reliability**	**Committee:** **Emerging Technologies**	**Committee:** **RF, High-Speed Components & Systems**
Session Co-Chairs: **Scott Savage** **Medtronic Microelectronics** **Email: scott.savage@medtronic.com** **Nokibul Islam** **JCET Group** **Email: Nokibul.ISLAM@jcetglobal.com**	**Session Co-Chairs:** **Xinpei Cao** **Henkel Corporation** **Email: xinpei.cao@henkel.com** **Tengfei Jiang** **University of Central Florida** **Email: Tengfei.jiang@ucf.edu**	**Session Co-Chairs:** **Amit P. Agrawal** **AMD** **Email: ap_agrawal@yahoo.com** **Sungwook Moon** **Samsung** **Email: sw2013.moon@samsung.com**
1. 9:30 AM - Structural Characterization of 2.5D System in Package Combined With High Bandwidth Memory for Enhanced Quality and Reliability Byoungdo Lee, Jinwoo Choi, Sangyong Lee, Jinwoo Park, Gyujei Lee, Kangwook Lee - SK Hynix, Inc.	***1. 9:30 AM - Embedded RF Packaging Via Ceramic 3D Printing and Printed Electronics Additive Manufacturing*** Abdullah Obeidat, Mohammed Abdelatty, Ashraf Umar, Zhi Dou, Firas Alshatnawi, Riadh Al-Haidari, Waleed Al-Shaibani, Mohammed Alhendi, Mark Poliks - Binghamton University; Cathleen Hoel, Jason Case, Joseph Iannotti - General Electric Company	***1. 9:30 AM - Design and Simulation Study of 300-GHz Molded Patch Antenna in Packaging Substrate*** Harshpreet Singh Phull Bakshi, Rajen Murugan, Sylvester Ankamah-Kusi - Texas Instruments, Inc.
2. 9:50 AM - Reliability Investigations of Advanced Photosensitive Polymer based RDL Processes Protected by Inorganic Capping Layers Emmanuel Chery, Nelson Pinho, Eric Beyne - imec; Ritwik Bhatia, Ganesh Sundaram - Veeco	***2. 9:50 AM - A CMOS Nanosensing Platform for Continuous Brain Multianalyte Monitoring*** Yue Gu, Jesus Maldonado Vazquez, De-Shaine Murray, Hitten Zaveri, Dennis Spencer - Yale University	***2. 9:50 AM - Wideband Antennas on Thin-Film Packaging Substrates for 140 GHz 6G Applications*** Thi Huyen Le, Michael Phillip Kaiser, Julia-Marie Köszegi, Kavin Senthil Murugesan, Lutz Gerhold, Ivan Ndip, Martin Schneider-Ramelow - Fraunhofer IZM; Habib Hichri - Ajinomoto Fine-Techno USA Corporation; Ryohei Oishi, Reki Nakano - Ajinomoto Co., Inc.
3. 10:10 AM - Indium Thermal Interface Material (TIM) Degradation: Bake Experiments, Models, and Reliability Implications Amir Behnam, Chris Dmuchowski, Kaushik Mysore - Advanced Micro Devices, Inc.	***3. 10:10 AM - Novel Sub-THz Antenna SoP Modules Enabled by Micrometer-Scale Metal 3D Printing for B5G/6G Applications*** Genaro Soto Valle Angulo, Kexin Hu, Manos M. Tentzeris - Georgia Institute of Technology	***3. 10:10 AM - Miniaturized High-Efficiency Substrate Integrated Waveguide (SIW) Cavity Slot Antenna at 28 GHz Based on Through Fused-Silica Via (TFS) Technology*** Hanna Jang, Payman Pahlavan, Yong-Kyu Yoon - University of Florida
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Methods for Non-Destructive Failure Analysis of Hybrid Bonded Components Matthew Bahr, Jeremy Walraven, William Mook, Amun Jarzembski, Wyatt Hodges, William Delmas, Zachary Piontkowski, Matthew Jordan - Sandia National Laboratories	***4. 11:15 AM - Direct-Write Printed RRAM Cells*** Jordan Howard-Jennings, Riadh Al-Haidari, Emuobosan Enakerakpo, Stephen Gonya, Mohammed Alhendi, Mark Poliks - Binghamton University; Kevin Bell, Tom Rovere - Lockheed Martin	***4. 11:15 AM - A Compact mmWave 1x4 Antenna Array Design With Shorted Parasitic Elements for 5G AiP Applications*** Sheng-Chi Hsieh, Cheng-Yu Ho - Advanced Semiconductor Engineering, Inc. (US)
5. 11:35 AM - Electromigration Failure Mechanisms of Cu-Cu Joints at Low Stressing Temperatures Shih-Chi Yang - Department of Materials and Science Engineering; Chih Chen - National Yang Ming Chiao Tung University	***5. 11:35 AM - Micro-3D Printing of Packaging Substrates with Embedded Through Holes for Organic Interposers*** Nahyeon Kwon, Haksoon Jung, Yongwoo Lee, Sungmin Eum, Yechan Han - Ulsan National Institute of Science & Technology; Hyunjin Park, Yunsik Park - Korea Research Institute of Chemical Technology (KRICT); Jimin Kwon - Ulsan National Institute of Science and Technology (UNIST)	***5. 11:35 AM - High-Performance Polymer Microwave Fiber Coupler in eWLB Package for Sub-THz Communication*** Vasileios Liakonis - Infineon Technologies AG/National Technical University of Athens; Yannis Papananos - National Technical University of Athens; Maciej Wojnowski, Walter Hartner - Infineon Technologies AG
6. 11:55 AM - A Data-Driven Machine Learning Model to for the Stress-Strain Behavior of Single Grain SAC305 Solder Joints Debabrata Mondal, Jeffrey Suhling, Elham Mirkoohi, Pradeep Lall - Auburn University	***6. 11:55 AM - A Novel Fully Additive Fabrication Approach for Creating Double-Stacked Copper Spiral Inductors*** Roghayeh Imani, Shailesh Chouhan, Jerker Delsing - Lulea University of Technology; Sarthak Acharya - University of Oulu	***6. 11:55 AM - RF Modelling and Characterization of TSV and Inductive Links of Hybrid Bonding*** Xiao Sun, Chin-Ya Su, Shih-Hung Chen, Soon Aik Chew, Boyao Zhang, Eric Beyne - imec
7. 12:15 PM - BGA Electromigration Performance and Why it Has Become the Bottleneck Riet Labie, Chinmay Nawghane, Dimitrios Tsiakos, Jan Mertens - imec; Wolfgang Sauter, Eric Tremble, Richard Graf - Marvell Technology, Inc.	***7. 12:15 PM - A Flexible Composite Heat Sink Embedded Ag Microchannels for Potential Flexible Electronic Applications*** Han Cai, Yongjin Wu, Yanxin Zhang, Yunna Sun, Zhuoqing Yang, Guifu Ding - Shanghai Jiao Tong University; Jiangbo Luo - Shanghai Aerospace Electronic and Communication Equipment Research Institute	***7. 12:15 PM - Terahertz Metasurfaces on Flex Using Aerosol Jet Printing and a Novel Parylene Liftoff Process*** Sambit Kumar Ghosh, Ethan Kepros, Yihang Chu, Bhargav Avireni, Brian Wright, Premjeet Chahal - Michigan State University

Program Sessions: Thursday, May 30, 2:00 p.m. - 5:05 p.m.

Session 19: 3D Integration Copper-Copper Hybrid Bonding	Session 20: Novel High-Density 3D & Thru-Via Structures and Processes	Session 21: Innovations in Polymer Packaging Materials Committee:
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs: **John Knickerbocker** **IBM Corporation** **Email: knickerj@us.ibm.com** **Peng Su** **Juniper Networks** **Email: pensu@juniper.net**	**Session Co-Chairs:** **David Danovitch** **University of Sherbrooke** **Email: David.Danovitch@USherbrooke.ca** **Yoshihsia Kagawa** **Sony** **Email: Yoshihisa.Kagawa@sony.com**	**Session Co-Chairs:** **Zhanhming Zhou** **Qualcomm** **Email: zhou.zhming@gmail.com** **Mark Poliks** **Binghamton University** **Email: mpoliks@binghamton.edu**
1. 2:00 PM - A Study of Low Temperature SoIC Targeting 200 nm Bond Pitch Wei-Ming Wang, C.W. Yeh, Han-Jong Chia, R.F. Tsui, Ji James Cui, Chih-Hang Tung, Kuo-Chung Yee, Douglas C.H. Yu - Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 2:00 PM - Integration of Planarized Nb-Based Vias to Form a Multi-Level Superconducting Back-End-of-Line*** Candice Thomas, Edouard Deschaseaux, Rémi Vélard, Giovanni Romano, Jean-Philippe Michel, Norman Vivien, Richard Souil, Cassandre Beluffi, Catherine Pellissier, Jean Charbonnier - Grenoble Alps University/CEA-LETI	***1. 2:00 PM - Novel Sheet Molding Compound Technology for Wafer Level Packaging to Overcome Wafer Warpage Issue*** Yuki Sugiura, Daisuke Mori, Yasuhito Fujii, Takashi Yagihashi, Eiichi Nomura - Nagase ChemteX Corporation; Kenta Imamura - Nagase America LLC; Ippei Yamai - Nagase & Co., Ltd.
2. 2:20 PM - Low Resistance and High Isolation HD TSV for 3-Layers CMOS Image Sensors Stéphan Borel, Myriam Assous, Rémi Velard, Jerzy-Javier Suarez-Berru, Stéphane Nicolas, Jérôme Dechamp, Renan Bouis, Lionel Vignoud, Paul Valentin, Jérémy Marchand, Antonio Roman, Messaoud Bedjaoui - Grenoble Alps University/CEA-LETI	***2. 2:20 PM - Observation of Thermal Expansion Behavior of Nanotwinned-Cu/SiO2 & Regular-Cu/SiO2 Hybrid Structure Via In-Situ Heating AFM*** Huai-En Lin, Chih Chen - National Yang Ming Chiao Tung University; Wei-Lan Chiu, Hsiang-Hung Chang - Industrial Technology Research Institute	***2. 2:20 PM - Development of UV-Curable Molding Materials With Minimum Die-Shift for FOWLP/FOPLP*** Markus Schindler, Severin Ringelstetter - DELO Industrial Adhesives; Mariana Pires, Mikhail Begel, Andrea Kneidinger, Markus Wimplinger, Thomas Uhrmann - EV Group, Inc.
3. 2:40 PM - Integrated Hybrid Bonding System for the Next Generation Advanced 3D Packaging Raymond Hung, Gilbert See, Ying Wang, Chang Bum Yong, Ke Zheng, Yauloong Chong, Avi Shantaram, Ruiping Wang, Arvind Sundarrajan - Applied Materials, Inc.; Nithyananda Hedge, Setfan Schmid, Manfred Glantschnig - Besi NL	***3. 2:40 PM - 3D Interconnects for Quantum Computing*** Jaber Derakhshandeh - imec	***3. 2:40 PM - Temperature-Dependent Dielectric Characterization of Low Loss Thin Film Polymers up to Sub-THz Bands*** Kavin Senthil Murugesan, Jens Schneider, Michael Kaiser, Julia-Marie Köszegi, Lutz Gerhold, Ivan Ndip, Martin Schneider-Ramelow - Fraunhofer IZM; Habib Hichri, Ryohei Oishi, Reki Nakano - Ajinomoto Fine-Techno USA Corporation
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Process Development and Performance Benefits of 0.64 µm - 0.36 µm Pitch Hybrid Bonding on Intel Process Tushar Talukdar, Adel Elsherbini, Kimin Jun, Brandon Rawlings, Richard Vreeland, William Brezinski, Haris Niazi, Siyan Dong, Yi Shi, Pilin Liu, Xavier Brun, Johanna Swan - Intel Corporation	***4. 3:45 PM - Laser Drilling of Around 3-Micron Via Into Ajinomoto Build-Up Film*** Toshio Otsu, Shuntaro Tani, Hiroharu Tamaru, Yohei Kobayashi - University of Tokyo; Shoko Nagayama, Ryo Miyamoto - Ajinomoto Fine-Techno Co., Inc.; George Okada - Spectronix Corp., Ltd.; Naoyuki Nakamura, Junichi Nishimae - Mitsubishi Electric Corporation	***4. 3:45 PM - Low-Temperature Polymer Hybrid Bonding With Nanopaticulated Cu and Photosensitive Acrylic Adhesive*** Hirokatsu Sakamoto, Tadashi Teranishi, Rumi Nagai, Ryo Itaya, Akihiko Happoya - Daicel Corporation; Hideaki Tamate - T-Micro; Takafumi Fukushima - Tohoku University
5. 4:05 PM - Methodologies for Characterization of W2W Bonding Strength Mario Gonzalez, Kris Vanstreels, Oguzhan Orkut Okudur, Serena Iacovo, Eric Beyne - imec	***5. 4:05 PM - Thermo-Mechanical Reliability Analysis and Raman Spectroscopy Characterization of Sub-micron Through Silicon Vias (TSVs) for Backside Power Delivery in 3D Interconnects*** Shuhang Lyu, Thomas Beechem, Tiwei Wei - Purdue University	***5. 4:05 PM - Development of New Concept Photo Imageable Dielectric Materials for Next Generation Advanced Packaging*** Kazuki Sato, Kazuaki Ebisawa, Makiko Irie, Yiyang Zhan, Atsushi Kubo - Tokyo Ohka Kogyo Co., Ltd.
6. 4:25 PM - Enhanced Biased HAST Reliability of Polyimide for High-Density Redistribution Layers Takumi Onuma, Daisaku Matsukawa, Takahiro Tanabe - HD MicroSystems LLC	***6. 4:25 PM - Organic Interposers Using Zero-Misalignment-Via Technology and Silicon Wafer Carriers for Large Area Wafer-Level Package Applications*** Alekdandar Aleksov, Tushar Talukdar, Veronica Strong, Holly Sawyer, Carolyn Aubertine, Johanna Swan, Thomas Sounart - Intel Corporation	***6. 4:25 PM - The Development of Thick Core Material for Cutting Edge Packaging*** Tomo Mugurma, Tom Shin - Panasonic Industrial Devices Sales Company of America; Masafumi Honma, Teppei Washio, Yuichi Ishikawa, Yutaka Tashiro, Hirosuke Saito, Jun Yasumoto, Genki Takahashi, Yoshiki Okushima - Panasonic Industry Co., Ltd.
7. 4:45 PM - Facile Wafer-to-Wafer Hybrid Bonding Integration at Sub 0.5 µm Pitch Hemanth Kumar Cheemalamarri, San Sandra, Arvind Sundaram, Anh Tran Van Nhat, Chen Gim Guan, Chandra Rao Bhesetti, Steven Lee Hou Jang, Raju Mani, Nandini Venkataraman, King Jien Chui, Srinivasa Rao Vempati, Singh Navab - Institute of Microelectronics A*STAR	***7. 4:45 PM - Bendability Enhancement and Miniaturization of Through-X Via (TXV) Based on Flexible Fan-Out Wafer-Level Packaging With Additive Tiny Cu Pillar Assembly*** Atsushi Shinoda, Chang Liu, Akihiro Tominaga, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima - Tohoku University	***7. 4:45 PM - Development of Magnetic Molding Compound for Low Pressure Molding Inductors With Both Good Magnetic Properties and High Reliability*** Hiroki Sonokawa, Yoshinori Endo, Mika Tanaka, Takashi Inagaki, Teruo Ito - Resonac Corporation

Program Sessions: Thursday, May 30, 2:00 p.m. - 5:05 p.m.

Session 22: Signal & Power Integrity for Advanced Packages and Systems	Session 23: Novel Bonding Technology for Advanced Assembly Substrates and Integration	Session 24: Advances on Flex and Redistribution Layer Technologies and Warpage
Committee: **RF, High-Speed Components & Systems**	**Committee:** **Assembly & Manufacturing Technology**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Hideki Sasaki** **Rapidus** **Email: hideki.sasaki@rapidus.co.jp** **Srikrishna Sitaraman** **Marvel** **Email: srikrishna. sitaraman@gmail.com**	**Session Co-Chairs:** **Valerie Oberson** **IBM** **Email: voberson@ca.ibm.com** **Pascale Gagnon** **IBM** **Email: pgagnon@ca.ibm.com**	**Session Co-Chairs:** **Ning Ye** **Western Digital** **Email: ning.ye@wdc.com** **Rui Chen** **Eastern Michigan University** **Email: rchen7@emich.edu**
1. 2:00 PM - High Bandwidth and Energy Efficient Electrical-Optical System Integration Using COUPE Technology Chih-Hsin Lu, Chia-Chia Lin, Tzu-Chun Tang, Chung-Yi Lin, Jay Chang, Chung-Hao Tsai, Harry Hsia, J.C. Twu, C.S. Liu, Gene Wu, Kuo-Chung Yee, Douglas Yu - Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 2:00 PM - Advanced Thermocompression Bonding Application on High Density Fan-Out Embedded Bridge Technology for HPC/AI/ML*** Wiwy Wudjud, Lihong Cao - Advanced Semiconductor Engineering, Inc. (US); ShuYu Lin, Yungshun Chang, Jean Yen, Reno Liao, Leo H.S. Cheng, YiHsien Wu, Simon Y.L. Huang, Ivan R.C. Chen, ChengYu Lee, Joey C.I. Huang - Advanced Semiconductor Engineering, Inc.	***1. 2:00 PM - Accurate Prediction of Solder Stresses/Strains in Multi-Layered Electronics Packages During Temperature Cycling*** Xuejun Fan, Mukunda Khanal, Jiang Zhou - Lamar University
2. 2:20 PM - High Frequency Assessment of Djordjevic-Sarkar Model for Low Loss Package Dielectrics Cemil Geyik, Michael Hill, Zhichao Zhang, Kemal Aygun - Intel Corporation	***2. 2:20 PM - Various Defect Mechanism Analysis for Optimization of Vacuum Fluxless Solder Reflow Performance Using 10 µm or Below Microbumps*** Lei Jing, Alvin Lin, Xinxuan Tan, Anderson Chen, Vladimir Kudriavtsev, Lucky Murugesh, Zia Karim - Yield Engineering Systems	***2. 2:20 PM - Comparison of Sustainable and Non-Sustainable Ink Process-Performance Interactions for Additively Printed Circuits*** Pradeep Lall, Ved Soni, Sabina Bimali, Daniel Karakitie - Auburn University; Scott Miller - NextFlex
3. 2:40 PM - System Level Analysis and Design Optimization of Back-Side Power Delivery Network for Advanced Nodes Kyunghwan Song - Samsung; Sungwook Moon - Samsung Electronics Co., Ltd.-Foundry Business; Duhyoung Ahn, Hyeonjin Kim, Minseok Kang - Foundry Business, Samsung Electronics	***3. 2:40 PM - Chip-on-Wafer (CoW) Technology Utilizing Laser-Assisted Bonding With Compression (LABC) for Bump Counts Exceeding 500,000 at a 20 µm Pitch*** Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Jungho Shin, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh, Ho-Gyeong Yun, Seok Hwan Moon, Ji Eun Jung, Gaeun Lee, Yong-Sung Eom - Electronics and Telecommunications Research Institute	***3. 2:40 PM - Simulation and Metrological Applications for RDL Patterning Development of Glass Substrate*** Chang-Chun Lee - National Tsing Hua University; Jui-Chang Chuang - National Tsing Hua University/Industrial Technology Research Institute; Chen-Tsai Yang, Chung-I Li - Industrial Technology Research Institute; Shih-Hsien Lee, Shih-Hao Kuo - Applied Materials, Inc.
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - PDN Impedance Optimization of AR/VR Systems: A Trade-Off in VRM Bandwidth and Board Decouplings Wendem Beyene, Ling Jiang, Koichi Yamaguchi, Xiaoping Liu, Ashkan Hashemi - Meta Platforms, Inc.	***4. 3:45 PM - Novel Molded FCBGA Package Platform for Highly Reliable Automotive Applications*** Inrack Kim, Nari Kim, Gayoung Shin - Amkor Technology Korea; Youngdo Kweon - Amkor Technology, Inc.	***4. 3:45 PM - An AI-Assisted Automated Computational Framework for Warpage Prediction of Advanced Electronic Packaging*** Yu-Jui Liang, Jui-Pu Hsia, Chin-Hung Lai, Cong-Sheng Su, Yu-Chi Huang, Jian-Ren Hou - National Cheng Kung University; Xian-Zheng Huang, Wei-Long Chen - Advanced Semiconductor Engineering, Inc. (US)
5. 4:05 PM - Physical-Based Package Verification Methodology for High-Speed Channel Crosstalk and Correlation With BER Measurements Po-Wei Chiu, Chao-Chin Lee, Guan-Yu Lin, Jinsung Youn, Youngsoo Lee, Hong Shi, Alan Fang, Santiago Asuncion - Advanced Micro Devices, Inc.	***5. 4:05 PM - Study of Fabrication and Reliability for 120 mm x 120 mm Extremely Large Advanced 2.5D Package*** Kazue Hirano, Dongchul Kang, Sadaaki Katoh, Masaki Takahashi - Resonac Corporation	***5. 4:05 PM - Investigation of Mechanical Reliability of Flexible/Stretchable Electronic Materials Using Multi-Axial Stretch Techniques*** Kaushik Godbole, Benjamin Stewart, Suresh Sitaraman - Georgia Institute of Technology; Nicholas Ginga - University of Alabama in Huntsville
6. 4:25 PM - An Energy Efficient DDR5 I/O Performance Boost in Clamshell Configuration by Charge Pumping From Non-Target Device Ryuichi Oikawa - Renesas Electronics Corporation	***6. 4:25 PM - Thin Substrate Bonding*** Partia Naghibi - HRL Laboratories, LLC	***6. 4:25 PM - Simulation Methodologies for Warpage Prediction and Localized Stress Hotspot Detection for SMT Risk Assessment*** Zhi Yang, Igor Arsovski, Clint Harames, Jim Miller - Groq; Krishna Mellachervu - ANSYS, Inc.
7. 4:45 PM - Signal Integrity Analysis and Design Optimization Using Neural Networks Juhitha Konduru, José Schutt-Ainé - University of Illinois; Oleg Mikulchenko, Loke Yip Foo - Intel Corporation	***7. 4:45 PM - High-Throughput Characterization of Nanoscale Topography for Hybrid Bonding by Optical Interferometry*** Bongsub Lee, Oliver Zhao, Arianna Avellán, Suhail Sadiq, Gill Fountain, Dominik Suwito, Guilian Gao, Laura Mirkarimi - Adeia	***7. 4:45 PM - Analyzing the Influence of RDL Stack-Up on Wafer Warpage in FOWLP Through Experimental and Numerical Investigations*** Saskia Huber, Philipp Scheibe, Sükrücan Mutlu, Olaf Wittler, Martin Schneider-Ramelow - Fraunhofer IZM

Program Sessions: Friday, May 31, 9:30 a.m. - 12:35 p.m.

Session 25: High-Performance Computing, Design Challenges, and Solutions	Session 26: Chiplet Interconnect Design and Validation	Session 27: Advanced Die Bond and Board Level Reliability
Committee: Packaging Technologies	**Committees: Interconnections and RF, High-Speed Components & Systems**	**Committees: Materials & Processing and Assembly & Manufacturing Technology**
Session Co-Chairs: **Eric Tremble** **Marvell** **Email: etremble@marvell.com** **Young-Gon Kim** **Renesas Electronics America** **Email: young.kim.jg@renesas.com**	**Session Co-Chairs:** **Gang Duan** **Intel** **Email: gang.duan@intel.com** **Jaemin Shin** **Qualcomm Technologies** **Email: jaemins@qti.qualcomm.com**	**Session Co-Chairs:** **Jason Rouse** **Taiyo America** **Email: jhrouse@taiyo-america.com** **Omkar Gupte** **AMD** **Email: Omkar.Gupte@amd.com**
1. 9:30 AM - An Energy-Efficient Si-Integrated Micro-Cooler for High Power and Power-Density Computing Applications Yu-Jen Lien, Cheng-Chieh Hsieh, Terry Ku, Li Wang, Po-Ju Chen, Kcyee Yee, C. H. Douglas Yu - Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM - Impact of Pitch Scaling on 3D Die-to-Die Interconnects*** Nicolas Pantano, Michele Stucchi, Geert Van Der Plas, Eric Beyne - imec	***1. 9:30 AM - Effect of Chip-Package Variables on the Reliability of High Thermal Die Attach Materials for RF, Power, and Automotive Applications*** A R Nazmus Sakib, Ruther Ricon - Renesas Electronics America; Jake Eom, Yoshitsugu Kawashima, Kosuke Azuma, Ganesh Tharumalingam, Young Kim - Renesas Electronics Corporation
2. 9:50 AM - High Power Thermal Test Vehicle With 2-Phase Cooling for AI Datacenters, 5G RAN, and EDGE Compute Nodes Yang Liu, Nagesh Basavanhally, Mark Earnshaw, Todd Salamon, Rick Papazian, Ting-Chen Hu, Mark Cappuzzo, Rose Kopf, David Apigo, Bob Farah - Nokia Bell Labs	***2. 9:50 AM - A 32GB/s Full Duplex Bi-Directional Transceiver With Crosstalk Cancellation for Chiplet Interconnections*** Jae-Woo Park - Sungkyunkwan University; Nicolas Pantano, Geert Van Der Plas, Eric Beyne - imec; Jung-Hoon Chun - Sungkyunkwan University	***2. 9:50 AM - The Challenges of High-Temperature Lead-Free Solder Paste for Power Discrete Applications*** Hongwen Zhang - Indium Corporation
3. 10:10 AM - Block Level and Package Level Thermal Assessment for Back Side Power Delivery Network Melina Lofrano, Herman Oprins, Vladimir Cherman, Liesbeth Witters, Anne Jourdain, Geert Van der Plas, Eric Beyne - imec	***3. 10:10 AM - Modeling and Analysis of Heterogeneously Integrated Chiplet-to-Chiplet Communication Link in 2.5D Advanced Packaging*** Haofeng Sun, Bobi Shi, Thong Nguyen, Jose Schutt-Aine - University of Illinois	***3. 10:10 AM - Reliability Analysis of Cu Sintered Die-Attach for SiC Power Devices: Mechanical, Electrical, and Thermal Evaluation*** Xu Liu, Shaogang Wang, Dong Hu, Paddy French, Guoqi Zhang - Delft University of Technology; Chenshan Gao, Qianming Huang, Huaiyu Ye - Southern University of Science and Technology
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - Coax MIL 2.0 – Next Generation Coaxial Magnetic Package Core Inductors for Higher Efficiency Integrated Voltage Regulators Beomseok Choi, Jaeil Baek, Brandon Marin, Shuren Qu, Siddharth Kulasekaran, Jose Chavarria, Leigh Wojewoda, Kaladhar Radhakrishnan - Intel Corporation	***4. 11:15 AM - Signal, Power and Thermal Co-Optimization Methodology for FPGA Advanced Package*** Wei Liu, Guang Chen, Brian Wang, Jenny Xiaohong Jiang, Ed Milligan - Intel Corporation	***4. 11:15 AM - Complex Board Via Structure Induced Uneven Stress/Strain Impact on Interconnect Stability: SAC305, Full and Hybrid LTS Comparison*** Tae-Kyu Lee, Yujin Park, Gnyaneshwar Ramakrishna - Cisco Systems, Inc.; Jonghyun Nam, Daljin Yoon, Heera Roh - SK Hynix, Inc.
5. 11:35 AM - Integrated Design Ecosystem for Chiplets Heterogeneous Integration and Chip-to-Chip Interconnects in Advanced Packaging Technology Lihong Cao - Advanced Semiconductor Engineering, Inc. (US); Chen-Chao Wang, Chih-Yi Huang, Hung-Chun Kuo - ASE Corporate R&D Center	***5. 11:35 AM - An Advanced Packaging Figure of Merit (AP-FoM) for Benchmarking of Heterogeneous Integration Technologies*** Chuei-Tang Wang, Shu-An Shang, Yu-Ming Hsiao, Mirng-Ji Lii, Kam Heng Lee, Jun He - Taiwan Semiconductor Manufacturing Company, Ltd.	***5. 11:35 AM - Mitigating Solder Beading in Non-Eutectic Low-Temperature Solder: Mechanism and Solution*** Lip Teng Saw, Mutharasu Devarajan - Western Digital Corporation
6. 11:55 AM - Thermal and Mechanical Simulations of 3D Packages With Custom High Bandwidth Memory (HBM) Kamalika Chatterjee, Yan Li, Pouya Asrar, WooPoung Kim - Samsung Semiconductor, Inc.	***6. 11:55 AM - Signal Integrity Designs at Organic Interposer CoWoS-R for HBM3-9.2 Gbps High Speed Interconnection of 2.5D-IC Chiplets Integration*** Sheng-Fan Yang, Wei-Chiao Wang, Yi-Tzeng Lin, Chih-Chiang Hung, Hao-Yu Tung, Justin Hsieh - Global Unichip Corporation	***6. 11:55 AM - Thermal Aging Reliability of Socketable BGA Packages With Bi-Au-Coated Sn Spheres*** Jaewon Lee, Vanessa Smet - Georgia Institute of Technology
7. 12:15 PM - A Novel DC-DC Converter Module Using the Integrated Package Solution (iPaS) Substrate for Next Generation High Performance Computing (HPC) Applications Shuhei Yamada, Nobuyoshi Adachi, Kazuki Itoyama, Tatsuya Kitamura, Koshi Himeda, Atsushi Yamamoto - Murata Manufacturing Co., Ltd.; Keito Yonemori - Murata Electronics North America, Inc.	***7. 12:15 PM - Effective Interface Simulation Approach Based on Peak Distortion Analysis for UCIe IPs*** Joonhyun Kim, Seungki Nam, Sungwook Moon, Taeyun Kim, Sangin You, Chanmin Jo, Yongho Lee - Samsung Electronics Co., Ltd.	***7. 12:15 PM - Develop New Solder Alloy for High Reliability Device*** Albert T. Wu, Wei Ting Lin - National Central University; Watson Tseng, Chang-Meng Wang - Shenmao Technology, Inc.

Program Sessions: Friday, May 31, 9:30 a.m. - 12:35 p.m.

Session 28: Optical Interconnections	Session 29: Reliability in Harsh Environments Including Automotive	Session 30: Process and Hybrid Bonding Modeling and Characterization
Committee: Photonics	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Ping Zhou** **LDX Optronics** **Email: pzhou@ldxoptronics.com** **Masao Tokunari** **IBM** **Email: tokunari@jp.ibm.com**	**Session Co-Chairs:** **Varughese Mathew** **NXP Semiconductors** **Email: varughese.mathew@nxp.com** **Tae-Kyu Lee** **Cisco Systems** **Email: taeklee@cisco.com**	**Session Co-Chairs:** **Pradeep Lall** **Auburn University** **Email: lall@auburn.edu** **Xuejun Fan** **Lamar University** **Email: xuejun.fan@lamar.edu**
1. 9:30 AM - Fiber Array Attach for Co-Packaged Optics: High-Volume Production Process Control and Performance Paul Gond-Charton, Sebastien Gouin, Steve Pellerin, Louis-Michel Collin, Michelle Sevigny, Patrick Jacques, Elaine Cyr - IBM Canada, Ltd.	***1. 9:30 AM - Transitioning from Warpage "Control" to Warpage "Design": A Paradigm Shift*** Sukrut Prashant Phansalkar, Bongtae Han - University of Maryland	***1. 9:30 AM - Modeling of Copper Hybrid Bonding Anneal*** Joshua Hooge, Chris Netzband - Tokyo Electron, Ltd.
2. 9:50 AM - Photonic Building Blocks for Board-Level Disaggregation in Hyperscale Systems Richard Pitwon - Resolute Photonics, Ltd.; Bernard Lee, Tiger Ninomiya, Michael O'Farrell - Senko Advance Components	***2. 9:50 AM - Under Bump Metallization and the Stability of Solder Interconnect Assembly under Thermal and Electrical Load: Refreshed Understanding*** Hariram Mohanram - University of Texas, Arlington; Choong Un Kim - United Test and Assembly Center, Ltd.; Patrick Thompson, Qiao Chen, Sylvester Kusi - Texas Instruments, Inc.	***2. 9:50 AM - Investigation of the Sintering Dynamics of 100 nm Ag Nanoparticles via In Situ SEM Observation and Phase Field Simulation*** Xiao Hu, Dong Hu, Willem Van Driel, Guoqi Zhang - Delft University of Technology; René Poelma - Nexperia; Jianlin Huang - Ampleon B.V.
3. 10:10 AM - Interfacing Silicon Photonics for CPO Geert Van Steenberge, Jef Van Asch, Viktor Geudens, Toon De Baere, Nele De Moerlooze, Jeroen Missinne - imec/Ghent University; Joris Van Campenhout - imec	***3. 10:10 AM - Additively Printed In-Mold Electronics Circuits and Sensors Process-Performance Interactions for Automotive Applications*** Pradeep Lall, Hyesoo Jang, Ved Soni, Fatahi Musa, Md Golam Sarwar - Auburn University; Scott Miller - NextFlex	***3. 10:10 AM - Elucidating the Mechanism of Four Corner Voids in Chip-on-Wafer Hybrid Bonding*** Takaaki Hirano, Tatsumasa Hiratsuka, Hirotaka Yoshioka, Naoki Ogawa, Suguru Saito, Shoji Kobayashi, Yoshiya Hagimoto, Hayato Iwamoto - Sony Semiconductor Solutions Corporation
Refreshment Break: 10:30 a.m. - 11:15 a.m.		
4. 11:15 AM - High Power Performance Assessment of Low-Loss Spot Size Converter based on Self-Aligned Passive Fiber Attach Process Arpan Dasgupta, Jae Kyu Cho, Yusheng Bian, Takako Hirokawa, Zahidur Chowdhury, Farid Barakat, John Garant, Yarong Lin, Thomas Houghton, Arman Najafi, Ryan Sporer, Michelle Zhang - GlobalFoundries, Inc.	***4. 11:15 AM - Enhancing Cu Wire-Bonding Reliability by a Cu-Selective Passivation Coating*** Dinesh Kumar Kumaravel, Logan Estridge, Kevin Antony Jesu Durai, Khanh Tran, Oliver Chyan - University of North Texas; John Alptekin - Texas Instruments, Inc.; Varughese Mathew - NXP Semiconductor, Inc.	***4. 11:15 AM - Fan-Out Embedded Bridge Structure for Co-Packaged Optics Characterization and Evaluation*** Vito Lin, Teny Shih, Andrew Kang, Yu-Po Wang - Siliconware Precision Industries Co., Ltd.
5. 11:35 AM - A Compact, High Performance Passive Optical Network Transceiver Integration Approach Mark Earnshaw, Cris Bolle, Robert Farah, Rose Kopf, Mark Cappuzzo, Tzu-Yung Huang, Cuong Tran, Tam Huynh - Nokia Bell Labs	***5. 11:35 AM - High Acceleration Dynamic Methodology for Board-Level Shock Solder Joint Reliability Approach*** Min-Cheng Yu, Nan-Yi Wu, Wu-Lung Wang, Hsin-Chih Shih, Wei-Hong Lai, Chin-Li Kao, Alexcc Wang - Advanced Semiconductor Engineering, Inc.; Cp Hung - Advanced Semiconductor Engineering, Inc. (US)	***5. 11:35 AM - Advanced Atomic-Scale Insights Into the Chemical Mechanical Polishing Process With Ceria Abrasives Using Molecular Dynamics and Neural Network Potential*** Yoshishige Okuno, Teruo Hirakawa, Fukiko Ota, Hiromu Kubo, Yuuto Kurata, Akihiro Orita, Satoyuki Nomura - Resonac Corporation
6. 11:55 AM - Structural Design of Waveguide for Low Loss Adiabatic Coupler With Si Photonics Chip Takaaki Ishigure, Fumimasa Kondo - Keio University; Yuji Furuta, Hisashi Kaneda, Tomoharu Fujii - Shinko Electric Industries Co., Ltd.	***6. 11:55 AM - Thermomechanical Degradation of Sintered Copper Under High-Temperature Thermal Cycling*** Paul Paret, Sreekant Narumanchi - National Renewable Energy Laboratory; Sri Krishna Bhogaraju - CuNex GmbH; Dirk Busse, Alexander Dahlbüdding - Budatec GmbH; Gordon Elger - Technical University of Applied Science Ingolstadt	***6. 11:55 AM - Finite Element Modeling for Wafer-to-Wafer Direct Bonding Behaviors and Alignment Prediction*** Kyungmin Baek, Min-soo Han, Il Young Han, Jung Shin Lee, Jaeuk Sim, Joongha Lee, Daeho Min, Kyeongbin Lim - Samsung Electronics Co., Ltd.; Minwoo Daniel Rhee - Samsung
7. 12:15 PM - Hybrid Integrated Chip-Scale Laser Systems Based on Automated Assembly Xiaolei Zhao, Taylor Levaur, Lance Sweatt, Md. Arefin Islam, Lin Zhu - Clemson University	***7. 12:15 PM - Solder Reaction With Lead-frame of Cu Alloy C7025 and Its Effect on Joint Reliability*** Kejun Zeng, Venu Chauhan, Lance Wright - Texas Instruments, Inc.	***7. 12:15 PM - Measurement of the Interfacial Properties of Thin Metal Film by Laser Spallation Method for Advanced Wafer Level Package*** Young-Min Ju, Jin-Young Kim, Hui-Jin Um, Se-Min Lee, Dukyong Kim, Woong-Kyoo Yoo, Seung Hwan Lee, Hak-Sung Kim - Hanyang University; Daewoong Lee, Yeontaek Hwang - SK Hynix, Inc.

Program Sessions: Friday, May 31, 2:00 p.m. - 5:05 p.m.

Session 31: Advances in Flip Chip and Chip Scale Packages	Session 32: Advancement in Copper Hybrid Bonding Technologies Common to Multiple Applications	Session 33: Fine-Pitch Materials and Processes Committee:
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **Materials & Processing**
Session Co-Chairs: **Luu Nguyen** **Psi Quantum** **Email: lnguyen@psiquantum.com** **Glenn Ning Ge** **TetraMem** **Email: greene.ge@gmail.com**	**Session Co-Chairs:** **Thom Gregorich** **Infinera** **Email: tmgregorich@gmail.com** **Vempati Srinivasa Rao** **IME A-star** **Email: vempati@ime.a-star.edu.sg**	**Session Co-Chairs:** **Praveen Pandojirao-S** **Johnson & Johnson** **Email: praveen@its.jnj.com** **Bo Song** **HP Inc.** **Email: bo.song@hp.com**
1. 2:00 PM - New Double Sided Molded Package Platform Development With Open Cavity Mold on One Side and Exposed Die Mold on the Other Side MiKyeong Choi, HoSeung Seo, SeMin Gim, GyeongCheol Lee, JungHoon Na, GaHyeong Hwang, WonBae Bang, KiDong Sim, WonChul Do, KyungRok Park - Amkor Technology Korea; Ted Adlam, Jeff Davis - Amkor Technology, Inc.	***1. 2:00 PM - A Microstructural Investigation of Sub-1 µm Copper Bonding Contact Structures in Die-to-Wafer Hybrid Bonding*** Sari Al Zerey, Junghyun Cho - State University of New York at Binghamton; Roy Yu, Katsuyuki Sakuma - IBM Research	***1. 2:00 PM - The Patterned Photosensitive Dielectric Organic Material/Cu Simultaneous Novel CMP Process for Fine Damascene RDL Based on Process Design Assisted by Deep Learning*** Toshiaki Tanaka, Masaaki Yasuda, Takeyasu Saito, Masaru Sasago, Yoshihiko Hirai - Osaka Metropolitan University; Hideaki Nishizawa - Doi Laboratory, Inc.; Toshiro Doi - Doi Laboratory Inc.; Mitsuru Ozono, Hiroaki Kimuro, Hisatoshi Hirai - Advanced Industrial Science and Technology, Kyushu Center; Seiji Takahashi, Yoichi Minami - Lithotech Japan Corp.
2. 2:20 PM - Package Miniaturization and Wiring Impedance Reduction for High-Bandwidth Memory Devices With Vertical Wire Bonding Keita Mochizuki, Hiroyuki Wakioka, Tsutomu Fujita, Masatoshi Shomura, Takeori Maeda, Toshihiko Ohda, Yoshitaka Muto, Eiji Takano, Masahiro Inohara - KIOXIA Corporation	***2. 2:20 PM - Low-Temperature Cu-Cu Bonding Using <111>-Oriented and Nanocrystalline Hybrid Surface Grains*** Chen-Ning Li, Jia-Juen Ong, Shih-Chi Yang, Chih Chen - National Yang Ming Chiao Tung University; Wei-Lan Chiu, Hsiang-Hung Chang - Industrial Technology Research Institute	***2. 2:20 PM - Novel Negative-Tone Dry Film Resist and Process for Fine Pitch Copper Wiring With L/S = 1.5/1.5 µm on Build-Up Substrate*** Kei Togasaki, Natsuki Toda, Kensuke Yoshihara, Yosuke Kaguchi, Kanako Funai, Hitoshi Onozeki, Kenichi Iwashita - Resonac Corporation
3. 2:40 PM - Ultra-Thin Double Side SiP Technology With Embedded Trace Substrate Chehan (Jerry) Li, Jesus Mennen Belonio, Jon Gutierrez, Humi (Shih-Wen) Tang, Jessie (Yu-Shan) Wei - Renesas Electronics Corporation	***3. 2:40 PM - Copper Microstructure Effect on Electromigration Investigated by In Situ SEM EBSD Technique*** Yaqian Zhang, Sten Vollebregt, Guoqi Zhang - Delft University of Technology	***3. 2:40 PM - 20 µm Pitch Cu-to-Cu Flip-Chip Bonding Through Cu Nanoparticles Sintering*** Xinrui Ji, Leiming Du, Henk van Zeijl, Guoqi Zhang - Delft University of Technology; Jaber Derakhshandeh, Eric Beyne - imec
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - High Accuracy Selective Patterning for EMI Shielding of 5G AiP Ming-Hung Chen, Huei-Pin Chien, Yi-Chun Chou, Yu-Shuan Tsai, Kuan-Lin Kuo, Jei-Chieh Kao - Advanced Semiconductor Engineering, Inc. (US)	***4. 3:45 PM - Achieving Sub-nm Copper Recess Controllability for Advanced 3D Integration: An Experimental and Atomic-Scale Simulation Study on Wet Atomic Layer Etching Process*** Seung Ho Hahn, Wooyoung Kim, Bumki Moon, Minwoo Rhee - Samsung Electronics Co., Ltd.-Mechatronics Research; Kyeongbin Lim - Samsung Electronics Co., Ltd.	***4. 3:45 PM - Ultra–High Density RDL Patterning of High–Resolution Dielectrics by Maskless Exposure Technology for High Performance Computing and Artificial Intelligence Devices*** Ksenija Varga, Thomas Uhrmann, Roman Holly, Tobias Zenger - EV Group, Inc.; Dimitri Janssen, Niels Van Herck, Mario Reybrouck, Marieke Vandevyvere, Stefan Vanclooster - Fujifilm Electronic Materials Europe; Sanjay Malik - Fujifilm Electronic Materials; Benedict San Jose, Cliff Sandstrom - Deca Technologies, Inc.
5. 4:05 PM - Analysis of Thin Flip Chip Chip-Scale Package Warpage Causes and Variations Chee S Foong, Nishant Lakhera, Trent Uehling - NXP Semiconductor, Inc.; Amirul Afripin - NXP Malaysia Sdn. Bhd.	***5. 4:05 PM - Quantifying the Electrical Impact of Bonding Misalignment for 0.5 µm Pitch Hybrid Bonding Structures*** Kevin Ryan, Christopher Netzband, Andrew Tuchman, Scott Lefevre, Ilseok Son, Hirokazu Aizawa, Kaoru Maekawa - TEL Technology Center, America, LLC; Nathan Ip - Tokyo Electron America, Inc.	***5. 4:05 PM - Novel Photo Imageable Film for RDL*** Meiten Koh, Kazuyoshi Yoneda, Kazutaka Nakada, Yuna Kawata, Yusuke Naka, Mitsuya Uchida - Taiyo Ink Mfg. Co., Ltd.
6. 4:25 PM - Large Package Body Size Scaling With Two Novel Technologies: Multi Ball BGA and Liquid Metal Interconnect Xiao Lu - Intel Corporation	***6. 4:25 PM - Liquid Surface Tension-Driven Chip Self-Assembly Technology With Cu-Cu Hybrid Bonding for High-Precision and High-Throughput 3D Stacking of DRAM*** Zehua Du, Tetsu Tanaka, Takafumi Fukushima - Tohoku University; Hiroshi Kikuchi, Hayato Hishinuma - Yamaha Robotics Holdings Co., Ltd..	***6. 4:25 PM - Cu Nanowire Fine-Pitch Joints for Next Gen Heterogeneous Chiplet Integration*** Steffen Bickel, Iuliana Panchenko, Manuela Junghaehnel - Fraunhofer IZM; Olav Birlem, Sebastian Quednau - Nanowired GmbH
7. 4:45 PM - A Study About Direct Laser Reflow for Forming Stable and Reliable C4 Bump Interfaces on Semiconductor Substrates for Flip Chip Applications Matthias Fettke, Anne Fisch, Alexander Frick, Georg Friedrich, Thorsten Teutsch - Pac Tech GmbH	***7. 4:45 PM - Wafer-On-Wafer-On-Wafer (WoWoW) Integration Having Large-Scale High Reliability Fine 1 µm Pitch Face-To-Back (F2B) Cu-Cu Connections and Fine 6 µm Pitch TSVs*** Masaki Haneda, Yukako Ikegami, Kengo Kotoo, Kan Shimizu, Yoshihisa Kagawa, Hayato Iwamoto - Sony Semiconductor Solutions Corporation	***7. 4:45 PM - High-Planarity, Ultra-Low-Temperature-Curable Photosensitive Polyimide for Heterogeneous Integration*** Atsutaro Yoshizawa, Akira Asada, Daisaku Matsukawa, Takahiro Tanabe - HD MicroSystems LLC

Program Sessions: Friday, May 31, 2:00 p.m. - 5:05 p.m.

Session 34: Photonics Integration, Materials, and Processes	Session 35: Reliability and Current Stressing of Solder Interconnections	Session 36: Thermal Management and Cooling Solutions
Committee: Photonics	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Takaaki Ishigure** **Keio University** **Email: ishigure@appi.keio.ac.jp** **Mark Earnshaw** **Nokia** **Email: mark.earnshaw@nokia-bell-labs.com**	**Session Co-Chairs:** **Paul Tiner** **Texas Instruments** **Email: p-tiner@ti.com** **Pei-Haw Tsao** **Mediatek** **Email: ph.tsao@mediatek.com**	**Session Co-Chairs:** **Patrick McCluskey** **University of Maryland** **Email: mcclupa@umd.edu** **Chris Bailey** **Arizona State University** **Email: christopher.j.bailey@asu.edu**
1. 2:00 PM - Packaged Tunable Single-Mode III-V Laser Integrated on a Silicon Photonic Integrated Chip Using Photonic Wire Bonding Venkatesh Deenadayalan, Eric Thornton, Mario Ciminelli, Stefan Preble - Rochester Institute of Technology; George T. Nelson, Peter McGarvey - AIM Photonics; Justin Bickford - US Army Research Lab; Matthew Mitchell, Lukas Chrostowski, Sudip Shekhar - Dream Photonics; Juned N. Kemal, Sebastian Tobias Skacel - Vanguard Automation	***1. 2:00 PM - Electromigration in Eutectic Tin-Bismuth Bottom Terminated Components Solder Joints*** Prabjit Singh, Larry Palmer, Mehdi Hamid, Thomas Wassiac - IBM Corporation; Raiyo Aspandiar, Brian Franco - Intel Corporation; Haley Fu - iNEMI; Richard Coyle - Nokia Corporation; Vasu Vasudvan - Dell, Inc.; Aileen Allen - HP Inc.; Keith Howell - Nihon Superior Co.; Kei Muryayama - Shinko Electric Industries Co., Ltd.	***1. 2:00 PM - Electrical-Thermal Analysis of TSV Embedded Microfluidic Pin-Fin Heatsink in 3D IC for High Heat Dissipation With High Bandwidth Density and Low Latency*** Euichul Chung, Geyu Yan, Erik W. Masselink, Muhannad S. Bakir - Georgia Institute of Technology
2. 2:20 PM - Collective Die-to-Wafer Assembly Process for Optically Interconnected System-on-Wafer Koen Kennes, Anton Dvoretskii, Arnita Podpod, Pengfei Xu, Junwen He, Guy Lepage, Negin Golshani, Rafal Magdziak, Yoojin Ban, Filippo Ferraro, Andy Miller, Joris Van Campenhout - imec	***2. 2:20 PM - Impact of Current Induced Joule Heat Variation on Long-term Low Melting Temperature Solder Joint Stability*** Tae-Kyu Lee, Yujin Park, Gnyaneshwar Ramakrishna - Cisco Systems, Inc.; Jimmy-Bao Le, Chuanhao Nie - University of Texas, Arlington; Young-Woo Lee, Hui-Joong Kim, Seul-Gi Lee - MK Electron Co., Ltd.; Choong-Un Kim - United Test and Assembly Center, Ltd.	***2. 2:20 PM - Thermal Mitigation Strategy for Backside Power Delivery Network*** Feifan Xie, Tiwei Wei - Purdue University; Rongmei Chen - Peking University
3. 2:40 PM - A Compact Wafer-Level Heterogeneously Integrated Scalable Optical Transceiver for Data Centers Sajay Bhuvanendran Nair Gourikutty, Jiaqi Wu, Teck Guan Lim, Lai Yee Chia, Ser Choong Chong, Surya Bhattacharya - Institute of Microelectronics A*STAR; Liang Ding, Ronson Tan, Nagarajan Radhakrishnan - Marvell Semiconductor, Inc.; Xiaoguang Tu, Wanjun Wang, Chee-Keong Tan - Marvell Asia Pte Ltd	***3. 2:40 PM - Reliability Concerns Due to Changes in the Microstructure and Electrical Resistance of Low Temperature, SnBi-Based Solder Joints During Current Stressing*** Eric Cotts, Sitaram Panta, Eric Cotts, Babak Arfaei, Faramarz Hadian - State University of New York at Binghamton	***3. 2:40 PM - Thermal Management of 6-in-1 SiC Power Module With Double-Sided Impingement Cooling*** Yong Han, Gongyue Tang - Institute of Microelectronics A*STAR
Refreshment Break: 3:00 p.m. - 3:45 p.m.		
4. 3:45 PM - Scalable Fabrication of 3D Optical Redistribution for Co-Packaged Optics Using an Originally-Developed Nanoimprint Stepper Fumi Nakamura, Kenta Suzuki, Akihiro Noriki, Satoshi Suda, Takayuki Kurosu, Takeru Amano - National Institute of Advanced Industrial Science and Technology	***4. 3:45 PM - The Effect of Extended Dwell Time on Thermal Cycling Performance of Hybrid Low Temperature Solder Joints*** Richard Coyle, Chloe Feng, Richard Popowich - Nokia Bell Labs; Martin Anselm - Rochester Institute of Technology	***4. 3:45 PM - Thermal Performance of an Indium-Silver Alloy Metal TIM for a Large Body Lidded FCBGA After EOL and Long-term Reliability Tests*** SangHyuk Kim, EunSook Sohn, KyungRok Park - Amkor Technology Korea; YoungDo Kweon - Amkor Technology, Inc.
5. 4:05 PM - Laser Attach Process Development and Material Selection Alexander Janta, Pascale Gagnon, Eric Turcotte, Elaine Cyr, Jason Zheng - IBM Corporation	***5. 4:05 PM - Correlation of Mechanical and Microstructural Evolutions in Lead Free Solders Subjected to Various Thermal Exposures*** Mohammad Al Ahsan, S M Kamrul Hasan, Souvik Chakraborty, Jeffrey Suhling, Pradeep Lall - Auburn University	***5. 4:05 PM - AI-Driven Cold Plate Design and Optimization*** Yue Wu, Eric Chu, Fiona Shiau, Nathan Ai, Albert Zeng, Hoa Pham - Cadence Design Systems
6. 4:25 PM - Ultra-Compact Computing at the Edge Involving Unobtrusively Small Heterogeneous Integration Packaging Frank Libsch, Steve Bedell, Cyril Cabral, Arun Paidimarri, Chitra Subramanian, Seiji Munetoh - IBM Research	***6. 4:25 PM - Pad Cratering and Pin Pull Strength for Large BGA and Connectors — How Are They Correlated?*** Dongji Xie, Joe Hai, Vivienne Zou, Zhongming Wu, Minghong Jian - Nvidia Corporation	***6. 4:25 PM - Heat Dissipation Measurement in Flip-Chip Package Using Microfabricated Temperature Sensors on Lid*** Arsene Guédon, Nizar Bouguerra, Étienne Paradis, Dominique Drouin - University of Sherbrooke; Éric Duchesne, Stéphanie Allard - IBM Canada, Ltd.; Hél`ene Frémont - University of Bordeaux
7. 4:45 PM - Sintering for High Power Optoelectronic Devices Gordon Elger, Nihesh Mohan, Alberto Siligardi, Hamza Bin Aqeel, Hannes Schwan, Rocky Kumar Saha, Fabian Steinberger - Technical University of Applied Science Ingolstadt; Sri Krishna Bhogaraju, Rohan Ghosh - CuNex GmbH; Holger Klassen, Klaus Müller - ams OSRAM Group	***7. 4:45 PM - Board Level Drop Reliability of Hybrid Solder Joints With Controlled Bismuth Mixing Rate for Carbon Neutrality*** Seahwan Kim, Jaejun Yoon, Taejoon Noh, Seung Boo Jung - Sungkyunkwan University; Kyung Deuk Min - Samsung Electronics Co., Ltd.	***7. 4:45 PM - Innovative Two-Phase Immersion Cooling Solutions for High-Power Advanced Packages*** Sumit Sharma, Aqbal Ahmad, Chi-Chuan Wang - National Yang Ming Chiao Tung University; ICheng Huang, Ying-Xu Lu, Hung-Hsien Huang, Chen-Chao Wang, Chih-Pin Hung - Advanced Semiconductor Engineering, Inc. (US)

Wednesday May 29th

Session 37: Thermo-Mechanical Stress and Reliability Analysis for Materials in Future Packaging

Time: 10:00 AM - 12:00 PM

Committee: Interactive Presentations

Session Co-Chairs:
Mark Poliks
Binghamton University
Email: mpoliks@binghamton.edu

Jeffrey Lee
Integrated Service Technology Inc.
Email: jeffrey_lee@istgroup.com

Joshua Dillon
Marvell
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Venkata Mokkapati
AT&S
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Alternative Techniques for Cross-Sectioning and Quality Analysis of Solder-TIM Joints with Soft Indium Alloys
Daniel VanHart, Ali Davoodabadi - Universal Instruments Corp.

Investigating the Adhesion Between Glass Core and Polymer Buildup Films
Preeya Kuray, Yoji Nakajima, Junko Konishi - AGC, Inc.

Long-Term Reliability Analysis of Crystal Oscillator Under Immersion Cooling With Various Coolants
Yangfan Zhong, Dan Liu, Fangzhi Wen, Honghao Cao - Alibaba Group; Tina Bao, Kai Wang - Intel Corporation

Fusing Current Characterization of Various Cu RDL Designs in Wafer Level Packages
JeongMin Ju, JiYeon Yoon, EunSook Sohn - Amkor Technology Korea/Amkor Technology, Inc.; Nathan Whitchurch - Amkor Technology, Inc.

Impact of Bi-Content on the High Strain Rate Properties of SnAgCu Solders Under Sustained High-Temperature Operation
Pradeep Lall, Vishal Mehta, Mrinmoy Saha, Jeff Suhling - Auburn University; David Locker - US Army

Bond-Line Thickness Prediction for Thermal Interface Material Under Usage Conditions
Yangyang Lai, Jlefeng Xu, Karthik Deo, Jonghwan Ha, Seungbae Park, Junbo Yang - Binghamton University

Glass to Silicon Fine Pith Hybrid Bonding
Hemanth Kumar Cheemalamarri, Arvind Sundaram, Anh Tran Van Nhat, Chen Gim Guan, Jae Ok Yoo, Vempati Srinivasa Rao, Navab Singh - Institute of Microelectronics A*STAR

Multiphysics Overlay Modeling of Monolithic 3D Fusion and Hybrid Bonding Processes
Christian Muehlstaetter, Lukas Koller, Markus Wimplinger, Viorel Dragoi - EV Group, Inc.

Mitigating Cracking from TGV and RDL Stress in Glass Substrates With Low-CTE Electrodeposited Copper-Graphene Composites
Christian Molina-Mangual, Emanuel Torres-Surillo, Nithin Nedumthakady, Vanessa Smet - Georgia Institute of Technology

A Predictive Methodology for BGA Solder Joint Formation and Assembly Defects
Matt Bond, Mudasir Ahmad, Jin Kim, Sue Teng, Nima Shahidi, Yingshi Tang - Google

High-Performance Thermal and Electrical Characteristics of Via-Last (BBCube) Process in the Multi-Layer 3D Integration
Norio Chujo - Hitachi, Ltd.; Hiroyuki Ryoson, Koji Sakui, Shinji Sugatani, Masao Taguchi, Takayuki Ohba - Tokyo Institute of Technology

Embedded Liquid Cooling of High-Power Microelectronics Using Liquid Metal
Huicheng Feng, Bin He, Gongyue Tang, Xiaowu Zhang, Boon Long Lau, Jason Au, Javier Ong, Ming Chinq Jong, King Jien Chui - Institute of Microelectronics A*STAR

A Development of Sensorized Ear Model for New Behind the Ear (BTE) Hearing Aid
Maria Ramona Ninfa Bautista Damalerio, Wei Da Toh, Ruiqi Lim, Ming-Yuuan Cheng - Institute of Microelectronics A*STAR

Electrical Characterization and Reliability Studies of Nano-TSV
Ya-Ching Tseng, Daniel Lau, Simon Chun Kiat Goh, King-Jien Chui - Institute of Microelectronics A*STAR

A Simulation-Led Board Level Reliability Assessment of High Speed Printed Circuit Boards for Advanced Networking Applications
Omar Ahmed, Leif Hutchinson, Peng Su, Bernard Glasauer - Juniper Networks; Vishnu Shukla, Andrea Molina, Tengfei Jiang - University of Central Florida

Thermal Resistance Prediction Model for IC Packaging Optimization and Design Cycle Reduction
Guan-Wei Chen, Chung-Hsiang Hsu, Hung-Kai Wang, Yan-Cheng Lin - National Cheng Kung University; Tang-Yuan Chen, Chen-Chao Wang - Advanced Semiconductor Engineering, Inc.

Study of Stress and Warpage Estimation on FOWLP under Hygro-Thermal Coupling Loading Conditions
Yu-Wei Huang - Industrial Technology Research Institute; Ruchi A. K. Yadav, Hong-Yu Lin, Jian-Han Li, Chang-Chun Lee - National Tsing Hua University

Single and Multi NPU Chiplet Heterogeneous Integration Packaging Based on Fan-Out RDL Interposer With Silicon Bridge Technology
Insoo Kang, Jacinta Aman Lim - nepes Corporation

Monitoring of Wafer Thinning Induced In-Die Mechanical Stress With Embedded Sensors for Heterogeneous Integration
Alberto Piadena, Michele Quarantelli, Sharad Saxena, Christopher Hess, Larg Weiland, Rakesh Vallishayee, Yuan Yu, Tomasz Brozek, Andrzej Strojwas - PDF Solutions

Thermal Transport Properties of Hybrid Bonding With Passivation
Hakjun Kim, Jae Young Hwang, Young-chang Joo, Hyejin Jang - Seoul National University; Sangwoo Park, Sarah Eunkyung Kim - Seoul National University of Science and Technology

Optimization of Core Material Properties for Large Flip-Chip Ball Grid Array Substrate to Manage Both Warpage and Board Level Reliability
Hirokazu Noma, Masaki Takahashi, Nene Hatakeyama, Yuichi Yanaka, Akito Fukui, Keita Johno, Hitoshi Onozeki - Resonac Corporation

Embedded Cooling Method With Monolithic Dual-Layer Micro-Channel Cold Plate for High-Power Chips
Jianyu Du, Hongxu Wu, Huaiqiang Yu, Chi Zhang, Wei Wang - Peking University

Method to Evaluate the Adhesion Distribution on Wafers
Tatsumasa Hiratsuka, Takaaki Hirano, Kengo Kotoo, Nobutoshi Fujii, Suguru Saito, Shoji Kobayashi, Yoshiya Hagimoto, Hayato Iwamoto - Sony Semiconductor Solutions Corporation

Experimental and Numerical Investigation of Cu-Cu Direct Bonding Quality for 3D Integration
Sung-Hyun Oh, Hyun-Dong Lee, Jae-Uk Lee, Hoo-Jeong Lee, Eun-Ho Lee - Sungkyunkwan University; Sung-Ho Park, Won-Seob Cho, Yong-Jin Park, Alexandra Haag, Soichi Watanabe, Marco Arnold - BASF

High Voltage Effects on the Electrochemical Migration Mechanism
Rajan Ambat, Anish Rao Lakkaraju, Jyothsna Murali Rao - Technical University of Denmark

Atomistic Simulation Investigation of Various Plasma Surface Activations in SiCN Dielectric Bonding
Hojin Kim, Andrew Tuchman, Yu-Hao Tsai, Toru Hisamatsu, Ilseok Son, Sitaram Arkalgud - TEL Technology Center, America, LLC

A Novel Approach to Assess Board Level Solder Joint Reliability for Flip Chip on Leadframe Package Using Finite Element Analysis
Guangxu Li, Siva Gurrum, Frank Mortan, Jiang Li, Carlos Arroyo - Texas Instruments, Inc.

Reliability of Differently Shaped Solder Joints in Chip Resistor Under Drop Impact
Jonghwan Ha, Karthik Deo, Junbo Yang, Yangyang Lai, Seungbae Park - Binghamton University

Study of Damage Development in Under-Bump Interconnects by Thermo-Mechanical Stress in Package Interconnects
Jorge Mendoza, Choong-Un Kim - University of Texas, Arlington; Hung-Yun Lin - Texas Instruments, Inc.

Aging Behaviour and Environmental Impact of Under Bump Metallurgies for Wafer Level Balling
Arnaud Garnier, Laetitia Castagne, Stephane Moreau, Alexandra Fraczkiewicz, Theo Monniez, Daniel Mermin, Suzanne Guillou, Laura Vauche, Damien Saint-Patrice, Perceval Coudrain - Grenoble Alps University/CEA-LETI

Development of Interfacial Wedge Testing Technique and Mechanical Characterization of Flexible Electronic Materials
Joshua Corbin, Nicholas Ginga - University of Alabama in Huntsville

Automated Solder Joint Failure Mode Analysis Based on Dry and Pry Image Processing
Yinan Lu, Andrew Huang, Chaolun Zheng, Sean Lau, Bo Yang - Western Digital Corporation

Wednesday May 29th

Session 38: Photonics, mm-Wave Applications & Emerging Technologies

Time: 2:30 PM - 4:30 PM

Committee: Interactive Presentations

Session Co-Chairs:
Frank Libsch
IBM
Email: libsch@us.ibm.com

Saikat Mondal
Intel
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Pavel Roy Paladhi
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Email: rpaladhi01@gmail.com

Yoichi Taira
Keio University
Email: taira@appi.keio.ac.jp

Conformal Flexible Dry Electrode for ECG Monitoring
Riadh Al-Haidari, Babatunde Falola, Mohammed Alhendi, Mark Schadt, Mark Poliks - Binghamton University; Dan Balder, Andrew Stemmermann, Matthew Foster - SunRay Scientific, Inc.; Tzu-Jen Kao, Nancy Stoffel - General Electric Global Research

Reliability of Flexible Electronics Undergoing Vibration
Sara Lieberman, El Mehdi Abbara, Nathaniel Gee, Kankanige Udara Sandakelum Somarathna, Abhishek Navkar, Abdullah Obeidat, Zhi Dou, Mohammed Alhendi, Peter Borgesen, Mark Poliks - Binghamton University

Quantifying Uncertainties in the Correlation of Simulations and Measurements using the IEEE EPS Packaging Benchmark Suite
Jonatan Aronsson - CEMWorks, Inc.; Kemal Aygun - Intel Corporation

Polymer Waveguides for Co-Packaged Optics
Yi Shen, Michael Gallagher, Ross Johnson, Jake Joo, Masaki Kondo, James Ryley, Rui Zhang, Zhebin Zhang - DuPont; Marika Immonen, Matthew Neely, Everett Sarauer, David Senk - TTM Technologies, Inc.

Energy-Efficient 10-Chiplet Hyperscale AI HPU on Advanced Large-Scale RDL Package
Jiwon Yoon, Hyunwoo Kim, Juhyeon Lee, Joungho Kim, Sungjin Kim - Korea Advanced Institute of Science and Technology; Youngsu Kwon, Yigyeong Kim, Minseok Choi - Electronics and Telecommunications Research Institute; Heejun Jang, Kyun Ahn, Jinhan Kim, Taekyeong Hwang - Amkor Technology, Inc.

Development of Robust and Cost-Effective Electrical & Optical Interconnect Solution for High Performance Silicon Photonic Applications
Jae Kyu Cho, Takako Hirokawa, Yusheng Bian, Scott Pozder, Koushik Ramachandran, Arpan Dasgupta, Jason Kim, Zahidur Chowdhury, Norman Robson, Thomas Houghton - GlobalFoundries, Inc.

Low-Loss Non-Contact Interconnects Based on 3D Heterogeneous Redistribution Layer for Millimeter Wave Phased Arrays
Lichang Huang, Yunfei Cao - South China University of Technology; Yuting Tong, Sha Xu - Guangdong University of Technology; Xiaobin Xu, Jinxing Chen - Glorysky Electronic Technology Co., Ltd.

Thermal Performance and Reliability of Liquid Metal Alloys as Thermal Interface Materials for Computing Electronics Devices
Guangyu Fan, Jacob Wells - Indium Corporation; Michael Beam - SUNY Polytechnic Institute

Multi-Wideband Antenna in Package With Dual Polarizations
Mei Sun - Institute of Microelectronics A*STAR

Deep Reinforcement Learning-Based Power Distribution Network Design Optimization for Multi-Chiplet System
Weiyang Miao, Zhen Xie, Chuan Seng Tan - Institute of Microelectronics A*STAR/Nanyang Technological University; Mihai Dragos Rotaru - Institute of Microelectronics A*STAR

Novel Low Loss Polymer With High Thermal Resistance for Advanced IC Packaging
Hikaru Mizuno - JSR Micro, Inc.; Eri Mishima, Shunsuke Iizuka, Yuuichi Yashiro, Naoyuki Kawashima - JSR Corporation

Power Supply Design and Power Management in Complex System Design: Co-Packaged Optics-FPGA 3D SIP Module
Jugal Kishore Bhandari, Sandhya Dharavath, Venkata Ramana Pamidighantam, Mohd. Ubed, Anusha Veerandi, Rohin Kumar Yeluripati - LightSpeed Photonics Pte Ltd

Additively Manufactured SoP Modules for Smart Agriculture and Insect Pheromone Sensing Applications
Genaro Soto Valle Angulo, Manos M. Tentzeris - Georgia Institute of Technology; Andrew Fang - Walton High School

All-Cu 3D Interconnects as an Alternative to Hybrid Bonding
Tadatomo Suga, Kanji Otsuka - Meisei University

Additive Manufacturing of an Electronically Steerable Microstrip Leaky Wave Antenna on Thin Alumina Substrate
Ethan Kepros, Yihang Chu, Bhargav Avireni, Sambit Ghosh, Brian Wright, Premjeet Chahal - Michigan State University

Conductive Fabric Based RFID Wearable Textile Antennas for Product Authentication and Quality Control
Bhargav Avireni, Yihang Chu, Ethan Kepros, Sambit Kumar Ghosh, Premjeet Chahal - Michigan State University

Tire-Integrated Antennas for Wireless Sensors in Automotive Applications
Yihang Chu, Sambit Kumar Ghosh, Bhargav Avireni, Ethan Kepros, Premjeet Chahal - Michigan State University

Additively Manufactured Dissolvable Packaging for Recycle and Reuse of Chips for Sustainable Reduction of E-Waste
Dhiya Belkadi, Carl P Hahn, Hannah Lynn Houston, Sunehra Saleha, Min Sung Kim, Muhammad Mustafa Hussain - Purdue University

Experimental Study of Transmission Signal Performance of Sub-2 micron Fine Wiring With Novel Structure
Masaya Tanaka, Nobuyoshi Moriwaki, Satoru Kuramochi - Dai Nippon Printing Co., Ltd.

Comprehensive Socket Characterization and Correlation for High-Speed Interface Testing System
Varin Sriboonlue, Yeseul Jeon, Gerardo R. Luevano, Chris Ferguson, Ennai Ochoa - Qualcomm Technologies, Inc.

A Novel Method for LPDDR5 DRAM Jitter Measurement Through De-Embedding
Manho Lee, Chulhee Cho, Hyeongi Lee, Sehoon Park, Wonseok Hong, ByungSuk Woo, Woo-Shin Choi, Young-Chul Cho, Young-Soo Sohn, Jung-Hwan Choi - Samsung Electronics Co., Ltd.

An Effective Surface Roughness Extraction Method Using Particle Swarm Optimization (PSO) Algorithm and 2D Based Equations for High Speed Systems
Youngjae Lee, Kwangho Kim, Chulhee Cho, Sungjin Yoon, Hyeongi Lee, Wonji Hwang, Wooshin Choi, Young-Chul Cho, Jung-Hwan Choi, Young-Soo Sohn - Samsung Electronics Co., Ltd.

Ultimate Wafer-Level Lens Integration and Optimization Using Microlenses and Metalenses for High-End Active Pixel Sensor Applications
Hoi-Jin Lee, Sihun Han, Chanyeol Park, Sunyong Park, Woonphil Yang, Yitae Kim - Samsung Electronics Co., Ltd.

Microprinting Process Development Enabling Cost Effective, High Density and Flexible Electro-Optical Integration
Krzysztof Nieweglowski, David Weyers, Akash Mistry, Karlhenz Bock - TU Dresden

High Bandwidth Active Flexible Connector for Signaling in Wafer-Scale Systems
Randall Irwin, Joanna Fang, Subramanian Iyer - University of California, Los Angeles

Additive Manufacturing of High-Density (2.5 µm L/S) Ag-Cu Stacked Interconnects on Organic Substrates.
Shrivani Pandiya, Serge Ecoffey, Yann Beilliard, Dominique Drouin - University of Sherbrooke; Christophe Sansregret - Centre de Collaboration MiQroInnovation (C2MI); Isabel De Sousa - IBM Canada, Ltd.

Thursday May 30th

Session 39: Bonding Process and Analysis in Next-generation Interconnects

Time: 10:00 AM - 12:00 PM

Committee: Interactive Presentations

Session Co-Chairs:
Rao Bonda
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Jin Yang
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Email: jin1.yang@ieee.org

A Novel Detection Applied on Micro Defect in Bump Interface for 2.5DIC Package
Yi-Sheng Lin, Yu-Hsiang Hsiao, Cheng-Hsin Liu, Fan-Ju Hsiao - Advanced Semiconductor Engineering, Inc.

Hybrid Bonding Technology Chemical Mechanical Planarization Process Optimization Using Comprehensive 3D Modeling
Liu Jiang, El Mehdi Bazizi, Gregory Costrini, Prayudi Lianto, Gilbert See, Sefa Dag - Applied Materials, Inc.; Dimitrios Tsamados, Yves Saad - Synopsys, Inc.

Influence of Stiffener Design on Co-Packaged Optics (CPO) 2.5D Heterogeneous Packages
Karthik Arun Deo, Yangyang Lai, Jong Hwan Ha, Junbo Yang, Seungbae Park - Binghamton University

Adhesion Layer Influence on Thermomechanical Reliability of Electroplated Copper Through-Glass Via (TGV)
Junbo Yang, Ke Pan, Pengcheng Yin, Yangyang Lai, Seungbae Park - Binghamton University; Chukwudi Okoro - Corning, Inc.; Dhananjay Joshi, Scott Pollard - Corning Research and Development Corp.

A Study on the Surface Activation of Plasma Treatment for Hybrid Bonding Joint Interface
Chih-Jing Hsu, Hsu-Nan Fang, Tzu-Yu Su, Zhao-Ze Jiang, Yi-Hua Chen, Chien-Ching Chen, Yu-Bin Tsai, Che-Ming Hsu, Yuan-Feng Chiang, Jen-Chieh Kao, Yung-I Yeh - ASE Corporate R&D Center

Influence of Heat Treatment on the Quality of Die-to-Wafer Hybrid Bond Interconnects
Laura Wenzel, Catharina Rudolph, Adil Shehzad, Iuliana Panchenko, Manuela Jungh hnel - Fraunhofer IZM; Partha Mukhopadhyay, H. Jim Fulford - Tokyo Electron America, Inc.

Inverse Hybrid Bonding With Aluminum Oxide as Infill Using Atomic Layer Deposition
Rohan Sahay, Ashita Victor, Muhannad Bakir - Georgia Institute of Technology; Shreyam Natani, Dipayan Pal, Victor Wang, Chenghsuan Jimmy Kuo, Andrew Kummel - University of California, San Diego

Intelligent Design and Demonstration of Reliable All-Cu Interconnections on High-Density Glass Substrates at 10 Micron Pitch
Ramon Sosa, Antonia Antoniou, Vanessa Smet - Georgia Institute of Technology

Electromigration Kinetics of SAC/SnBi Hybrid Solder
Minhua Lu, Evan Colgan - IBM Research

Simulation of Bulge-Out Mechanism Enabling Sub-0.5 µm Scaling of Hybrid Wafer-to-Wafer Bonding
Jo De Messemaeker, Koen Van Sever, Yan Wen Tsau, Boyao Zhang, Kristof Croes, Eric Beyne - imec

Wet Cu Passivation for High Throughput Fluxless Thermal Compression Bonding of Cu-Sn Bumps for Die-to-Wafer Stacking
Jens Rip, Jaber Derakhshandeh, Dieter H. Cuypers, Eric Beyne - imec; Ryo Negishi, Itsuro Tomatsu - MEC Co., Ltd

Low Temperature Nanocrystalline Cu/Polymer Hybrid Bonding With Tailored CMP Process
Lee Ou-Hsiang, Hsiang-Hung Chang, Wei-Lan Chiou, Chia-Wen Chiang, Shih-cheng Yu, Ting-Yu Ke, Yu-Min Lin - Industrial Technology Research Institute; Chia-Hsin Lee, Andrew Tan - Brewer Science, Inc.

A Novel FOPLP Structure With Chip First & RDL First Process for Automotive Chip Application
Terry Wang, Chih Wei Lu, Eric Feng, Yu-Jhen Yang, Cheng-Yueh Chang, Pei-Pei Cheng - Industrial Technology Research Institute; Fredrick Lie - Applied Materials, Inc.; Austin Cheng - FAVITE, Inc.; Hsin-Yi Huang - Everlight Chemical Industrial Corp.; Meiten Koh - Taiyo Ink Mfg. Co., Ltd.; Aneta Wiatrowska, Lukasz Witczak - XTPL SA

A Unified and Adaptive Continual Learning Method for Feature Segmentation of Buried Packages in 3D XRM Images
Richard Chang, Jie Wang, Namrata Thakur, Ramanpreet Pahwa, Yang Xulei - Institute for Infocomm Research A*STAR

Low Thermal Budget Fine-Pitch Cu/Dielectric Hybrid Bonding With Cu Microstructure Modifications
Hemanth Kumar Cheemalamarri, Anh Tran Van Nhat, Gim Guan Chen, Arvind Sundaram, Binni Varghese, Nandini Venkataraman, Vempati Srinivasa Rao, Navab Singh - Institute of Microelectronics A*STAR

Characterization of 224 Gbps/Lambda Interconnects in Co-Packaged Optics for Hyperscale Data Centers and AI/ML Clusters
Jiaqi Wu, Teck Guan Lim, Sajay Bhuvanendran Nair Gourikutty, Surya Bhattacharya - Institute of Microelectronics A*STAR; Xin Li, Jason Tsung-Yang Liow - Rain Tree Photonics Pte. Ltd.

Fundamental Study on Reflow Mechanisms of Sn and Sn Alloys for Fine Bump Pitch Scaling
Chongyang Cai, Anup Panindre, Liang He, Jung Kyu Han, Gang Duan, Rahul Manepalli - Intel Corporation

Advanced Photo-imageable Dielectric Film Enabling Low CTE and sub-5 m Patterning for Next Generation Build-up Layer
Taku Ogawa, Ryuichi Okuda, Fumie Hattori, Hirokazu Ito - JSR Corporation

Room Temperature Bonding of CVD Polycrystalline Diamond Wafer to Semiconductor and Piezo-electric Single Crystalline Wafers
Tadatomo Suga, Junsha Wang Suga - Meisei University; Kazuya Yamamura - Osaka University; Izumi Kataoka - IIPT Inc.

Glass Panel Process Integrated Low Stress Organic Dielectric RDL Structure
Chien Kang Hsiung, Sarah Wozny, Marvin L Bernt - Applied Materials, Inc.; Terry Wang - Industrial Technology Research Institute; Kuan-Nang Chen - National Yang Ming Chiao Tung University

A Warpage Investigation for a Large Panel-Sized Interposer with Embedded Dies
Katsuaki To, Daisuke Yamanaka, Masashi Minami, Shan Ho Tsai, Sadaaki Katoh - Resonac Corporation

Development of Two Different Molding Methods in

2.5D Package With 20 m or Less Fine Bump Pitch CoW Structure
Takeshi Saito, Sadaaki Katoh, Keiko Ueno, Ryosuke Kimura, Tsai Shanho, Takahiro Iseki, Kan Donchoru - Resonac Corporation

Low Temperature Cu/SiO2 Hybrid Bonding With Protruding Copper Pads
Junpeng Fang, Qian Wang, Jiexun Yu, Ziqing Wang, Jian Cai - Tsinghua University; Yikang Zhou, Kai Zheng - Semiconductor Technology Innovation Center (Beijing) Corporation

Analysis of Vacancies in Wafer-Bonding Interface Via Positron Annihilation Lifetime Spectroscopy
Sotetsu Saito, Nobutoshi Fujii, Shunsuke Furuse, Naoki Ogawa, Suguru Saito, Yoshiya Hagimoto, Hayato Iwamoto - Sony Semiconductor Solutions Corporation

Annealing Effects in Sub-8 µm Pitch Die-to-Wafer Hybrid Bonding
Partha Mukhopadhyay, Andrew Tuchman, Kevin Ryan, Adam Gildea, Sitaram Arkalgud, Anton deVilliers, Jim Fulford - TEL Technology Center, America, LLC; Laura Wenzel, Catharina Rudolph - Fraunhofer IZM; Chuck Woychik, Chris Nichols - SkyWater Technology; John Allgair - BRIDG

3D Interconnect Technology With Serpentine and Trapezoidal Corrugation Using a Flexible Photosensitive Dielectric to Strengthen the Bendability of FHE
Chang Liu, Jiayi Shen, Atsushi Shinoda, Han Zhang, Tetsu Tanaka, Takafumi Fukushima - Tohoku University

Through Dielectric Via Etching in Magnetic Neutral Loop Discharge Plasma for 3D Chiplets Interconnect
Yasuhiro Morikawa - ULVAC, Inc.

A Novel Plasma Etching Technology of RIE-Lag Free TSV and Dicing Processes for 3D Chiplets Interconnect
Taichi Suzuki, Kenta Doi, Yasuhiro Morikawa - ULVAC, Inc.

Aluminum-to-Aluminum and Aluminum-to-Copper Thermal Compression Bonding for Heterogeneous Integration of Legacy Dielets
Krutikesh Sahoo, Randall Irwin, Golam Sabbir, Vineeth Harish, Subramanian Iyer - University of California, Los Angeles

Directional Atmospheric Plasma De-oxidation for Ultra Small Passive Component Assembly
Khouloud Ben Harzallah, David Danovitch, Malak Kanso - University of Sherbrooke; Christian Bergeron, Marc-Olivier Pion - IBM Canada, Ltd.

Exploring Bonding Mechanisms of SiCN for Hybrid Bonding
Sodai Ebiko, Fumihiro Inoue - Yokohama National University; Serena Iacovo, Soon-Aik Chew, Boyao Zhang - imec; Akira Uedono - University of Tsukuba

Thursday May 30th

Session 40: Materials, Manufacturing and Assembly Techniques in Advanced Packaging Solutions

Time: 2:30 PM - 4:30 PM

Committee: Interactive Presentations

Session Co-Chairs:
Mark Eblen
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Characterization of Warpage of Ultra-Low-K Dielectric Materials and Correlation With Modulus and Coefficient of Thermal Expansion
Mohanalingam Kathaperumal, Pragna Bhaskar, Austin Toro, Pratik Nimbalkar, Lila Dahal, Muhannad Bakir - Georgia Institute of Technology

A Highly-Reliable and Cost-Effective Approach by Reducing Flux Cleaning in Chiplet Processes Through Underfill Curing in a Pneumatic Ambient
Huan-Ping Su, Ming-Hua Hsu, Auger Horng - Ableprint Technology Co., Ltd.

300 nm Pitch W2W HBI for CFET and 3D DRAM Through Module Co-Optimization
Tyler Sherwood, Raghav Sreenivasan, Masha Gorchichko, Amit Prakash, Raghuveer Patlolla, Sarabjot Singh, Yoocharn Jeon, Jason Appell, Ryan Ley, Kun Li - Applied Materials, Inc.; David Hafner - EV Group, Inc.

Mechanical Characterization and Modeling of iSAC Lead-Free Solder
Golam Rakib Mazumder, Souvik Chakraborty, Mahbub Alam Maruf, Mohammad Al Ahsan, Jeffrey Suhling, Pradeep Lall - Auburn University

High Temperature RF Measurements Using Novel SiO2 Cables With Edge Launch Connectors
Firas Alshatnawi, Ashraf Umar, Emuobosan Enakerakpo, Mohamed Abdelatty, W.T. Alshaibani, Mohammed Alhendi, David Shaddock, Peter Borgesen, Mark Poliks - Binghamton University

Modeling and 3D Additively Manufactured Inductors on Complex Shape for Extreme High Temperature Electronics
Waleed Alshaibani, Ashraf Umar, Firas Alshatnawi, Emuobosan Enakerakpo, Mohamed Abdelatty, Mohammed Alhendi, Mark D. Poliks - Binghamton University; David Shaddock - General Electric Company

Underfill Selection Guideline for Fan-Out Heterogeneous Integration Package
Wen-Yu Teng, Liang-Yih Hung, Jackson Lee, Debby Li, Carl Chen, Don-Son Jiang, Yu-Po Wang - Siliconware Precision Industries Co., Ltd.

Comparison of Organic and Inorganic Dielectric Hybrid Bonding With Highly <111>-Oriented Nanotwinned Cu
Pin-Syuan He, Chih Chen - National Yang Ming Chiao Tung University

Key Technologies and Design Aspects for Wafer Level Packaging of High Performance Computing Modules
Kai Zoschke, Hermann Oppermann, Michael Schiffer, Ivan Ndip, Karl-Friedrich Becker, Marius Adler, Alexander Gäbler, Uwe Maass - Fraunhofer IZM; Gianna Paulin - Swiss Federal Institute of Technology; Walter Kocon - GlobalFoundries, Inc.

One-Step Glycine Modified Boron Nitride for Epoxy Composites With Enhanced Thermal Conductivity
Zihao Lin, Jiaxiong Li, Zhijian Sun, Kyoung-Sik Moon, Ching-Ping Wong - Georgia Institute of Technology; Andrew Fang - Walton High School

Investigation on the Use of Al-Ge eutectic Bonding in the Structural Part of a Multilayer Stacked MEMS device
Jun Wang, Manuel Mannarino, Jakob Visker, Shuo Kang, Bivragh Majeed, Lan Peng, Gauri Karve, Luc Haspeslagh - imec; G nther Weidlinger, Tobias Wernicke, J rgen Burggraf, Markus Wimplinger - EV Group, Inc.

Limits for Dicing Speed Based on Crack Stop Constructions With Different Levels of Robustness
Maria Heidenblut, Michael Goroll, Stefan Kaiser, Andreas Bauer, Kristina Hopfauf - Infineon Technologies AG

Vertical Stacking of Heterogeneous Chiplets of Duplexer on LNA/SOI
Tai Chong Chai, Rotaru Dragos Mihai, Xiangyu Wang, Pei Siang Sharon Lim, Lin Ji, Rathin Mandal, Raju Mani, Ming Chinq Jong, Yong Liang Ye - Institute of Microelectronics A*STAR

Multi Chip Stacked Memory Module Development Using Chip to Wafer (C2W) Hybrid Bonding for Heterogeneous Integration Applications
Nagendra Sekhar Vasarla, Dileep Kumar Mishra, Sasi Kumar Tippabhotla, Chandra Rao Bhesetti, Ser Choong Chong, King-Jien Chui, Srinivasa Rao Vempati - Institute of Microelectronics A*STAR

Challenges and Error Estimation in Immersion Cooling Liquid Dk-Df Extraction using Different Methods
Saikat Mondal, Xenofon Konstantinou, Cemil Geyik, Zhichao Zhang, Kemal Aygun - Intel Corporation

Fluidic Self Alignment for Hybrid Bonding Using Intel Process
Feras Eid, Yi Shi, Golsa Naderi, Shashi Bhushan Sinha, Rob Jordan, Wenhao Li, Charles El Helou, Felipe Bedoya, Anandi Roy, Tayseer Mahdi, Sheena Benson, Johanna Swan - Intel Corporation

An Advanced Remote-Plasma Assisted Ozone-Ethylene-Radical (OER) Process for Cu-SiO2 Hybrid Bonding Yield Enhancement
Tatsunori Shino, Eitaro Toyama, Tetsuya Nishiguchi - MEIDEN NANOPROCESS INNOVATIONS, Inc.; Mariappan Murugesan, Kiyoharu Mori - NICHe; Bungo Tanaka, Takafumi Fukushima - Tohoku University

Influence of Temporary Rigid Carrier Structure on Warpage During Wafer/Panel Level Packaging
Yoshinori Matsuura, Joji Fujii, Vivek Dutta - Mitsui Mining & Smelting Co., Ltd.

Extremely Advanced Substrate as an Integrated Package Solution (iPaS) for Next Generation High Performance Computing (HPC) Applications
Tatsuya Kitamura, Takeshi Furukawa, Shuhei Yamada, Koshi Himeda, Atsushi Yamamoto - Murata Manufacturing Co., Ltd.

A CMP Process for Hybrid Bonding Application With Conventional / nt-Cu and SixNy / SixOy Dielectrics
Tri Widodo, Yi Shi, Xavier F Brun - Intel Corporation; Prayudi Lianto, Avery Tan, Joselyn Lie, Patrick Lim, Guan Huei See - Applied Materials, Inc.

Effect of Material Aging on the Reliability of An Automotive BGA Device Under TC Test Conditions
Abdullah Fahim, Ryan Zhang, Amar Mavinkurve, Sandeep Shantaram, Ali Rezaie Adli, Wiwat Tanwongwan, Torsten Hauck - NXP Semiconductor, Inc.

Overlay Challenges of Extremely Large Exposure Field, Fine Resolution Lithography Due to Alignment Solution Errors and a Solution Using Early Zone Corrections in Advanced IC Substrates
John Chang, Xin Song, Timothy Chang - Onto Innovation

World's Smallest, Membrane-Based Capacitive Differential Pressure Sensor- Package Structure, Material Selection, Assembly Challenges & Solutions
KM Rafidh Hassan, Gaurav Mehrotra, Hazel Caballero, Young Kim, Steven Lee - Renesas Electronics America; Karim Allidina, Tommy Tsang, Mohannad Elsayed, Hani Tawfik - MEMS Vision International, Inc.

Packaging Challenges and Solutions for Next Generation Low-Profile WLCSP
Humi (Shih-Wen) Tang, Jerry (Che-Han) Li, Jessie (Yu-Shan) Wei, Baltazar Canete, Leo (Hsin-Hung) Huang, Jesus Mennen Belonio - Renesas Electronics Corporation

A Study on Novel Low Temperature Soldering Process Using Vapor phase
Youngja Kim, Woojin Choi, Seungyeop Oh, Sinyeob Lee, Sunwon Kang - Samsung Electronics Co., Ltd.

Numerically Study on Hybrid Discontinuous Microchannel Heat Ink Combining Manifold With Pin Fins (DMC-MPF) for High Power Electronic Device
Jianyu Du, Lang Chen, Ran Hu, Chi Zhang, Wei Wang - Peking University; Huaiqiang Yu - 26th Research Institute of China Electronics Technology Group Corporation

Room-Temperature Hybrid Bonding of Via-Middle TSV Wafer Fabricated by Direct Si/Cu Grinding and Residual Metal Removal
Naoya Watanabe - National Institute of Advanced Industrial Science and Technology; Hiroshi Yamamoto, Takahiko Mitsui - Okamoto Machine Tool Works, Ltd.

Low Temperature Cu-Cu Direct Bonding Using Ruthenium Passivation Layer Deposited Various Methods
Sang Woo Park, Min Seong Jeong, Yeon Ju Kim, Ji Hoon Kim, Jong Kyung Park - Seoul National University of Science and Technology; Hee Han - National NanoFab Center

Optimizing Die-to-Wafer Hybrid Bonding Through Metal Passivation and CMP Process
Yeon Ju Kim, Sang Woo Park, Min Seong Jeong, Ji Hun Kim, Jong Kyung Park - Seoul National University of Science and Technology

Ultra Thin Fan-Out 3D WLCSP Heterogeneous Integration Packaging
Jay Li, Zen-Wei Zhang, Sam Lin, Vito Lin, Teny Shih, Nicholas Kao - Siliconware Precision Industries Co., Ltd.; Yu-Po Wang - SPIL

Panel Level Plasma Etching Characteristics for Advanced Packaging
Md Ishak Khan, Wei Wei, Haobo Chen, Xiyu Hu, Nicholas Haehn, Xiaoying Guo, Leonel Arana - Intel Corporation; Kensuke Akazawa - ULVAC, Inc.

Development of a Reusable Smart-Catheter System for Improved Urinary Health Monitoring
Zhi Dou, W.T. AlShaibani, Erika Solano Diaz, Mohammed Alhendi, Abdullah Obeidat, Riadh Al-Haidari, Mark Schadt, Mark Poliks - Binghamton University; Kara Allanach, Daniel Wollin, Souvik Paul - CathBuddy, Inc.

Focal Extension – A Novel Lithography Technique to Enable Fine-Pitch Patterning on Large-Area Warped Substrate
Golam Sabbir, Subramanian Iyer - University of California, Los Angeles

Friday May 31st

Session 41: Student Posters

Time: 10:00 AM - 12:00 PM

Committee: Interactive Presentations

Session Co-Chairs:
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Low Temperature Cu/SiO2 Hybrid Bonding Using Area-Selective Metal Passivation (Interface Metal) Technology for 3D IC and Advanced Packaging
Mu-Ping Hsu, Wen-Tsu Tsai, Chi-Yu Chen, Zhong-Jie Hong, Kuan-Neng Chen - National Yang Ming Chiao Tung University; Ou-Hsiang Lee, Tzu-Ying Kuo, Hsiang-Hung Chang - Industrial Technology Research Institute

Distributed Vertical Power Delivery for High Performance Computing Systems With Buck-Derived Regulators
Sriharini Krishnakumar, Inna Partin-Vaisband - University of Illinois; Ramin Rahimzadeh Khorasani, Madhavan Swaminathan - Pennsylvania State University; Rohit Sharma - Indian Institute of Technology Ropar

Multi-Objective Optimization of a 1200V Fan-Out Panel-Level SiC MOSFET Packaging With Improved Genetic and Particle Swarm Algorithms
Xuyang Yan, Wei Chen, Jing Jiang, Jiajie Fan - Fudan University; Xuejun Fan - Lamar University; Guoqi Zhang - Delft University of Technology

Packaging of Silicon Photonic Neural Network Accelerators
Russell Schwartz, Nicola Peserico, Hamed Dalir, Volker Sorger - University of Florida

Comparison of Different Copper Nitride Passivation Layers Fabrication Methodology and Optimal Growth Condition for Low Temperature Copper-to-Copper Bonding in Advanced Packaging
Chiao-Yen Wang, Tzu-Heng Hung, Kuan-Neng Chen - National Yang Ming Chiao Tung University; Ping-Jung Liu - Taiwan Semiconductor Manufacturing Company, Ltd.

Fabrication and Testing of In-Line Structures for Non-Destructive Study of Solder Electromigration: Applications to SnBi Low Temperature Solder
Chetan Jois, Pei-En Chou, Ganesh Subbarayan - Purdue University

Application of Elevated-Laser-Liquid-Phase-Epitaxy (ELLPE) Technique on Different Oriented Wafers for Monolithic 3DIC Integration
Bo-Jheng Shih, Yu-Ming Pan, Chiao-Yen Wang, Huan-Yu Chiu, Huang-Chung Cheng, Kuan-Neng Chen - National Yang Ming Chiao Tung University; Chih-Chao Yang, Chang-Hong Shen - Taiwan Semiconductor Research Institute

Manufacturing and Characterization of Planar Transformers as Molded Interconnect Device Technology Component for an Industrial Production
Tim Nils Bierwirth, Folke Dencker, Marc Christopher Wurz - Leibniz University Hannover; Sebastian Bengsch, Michael Werner, Christian Henne, Stefan Bur - Ensinger GmbH; Rico Wachs - Tridelta Weichferrite GmbH

Hybrid Wiring Layers for Fine Pitch Integration
Vineeth Harish, Krutikesh Sahoo, Subramanian Iyer - CHIPS UCLA; Kai Zheng, Gilbert Park, Han-Wen Chen, Steven Verhaverbeke - Applied Materials, Inc.

Novel Single and Co-Ion Implantation Induced Backside Etch Stop Structures for 3D Multilayer Stacked Package
Yen-Shuo Chen, Hua-Tai Fan, Yu-Chien Ko, Fu-Hsiang Ko, Ching-Chia Lin - National Yang Ming Chiao Tung University; Tzu-Wei Chiu - Seriphy technology corporation; Chu-Chi Chen - Taiwan Semiconductor Research Institute

New Method for Fluid Filling Through Silicon Vias With Silver Ink for Packaging Techniques
Zachary Nelson, Alice Mo, Luke Theogarajan - University of California, Santa Barbara

Electrospray Printed Silver Films for EMI Shielding of SiP Architectures
Emma Pawliczak, Paul Chiarot - Binghamton University

Latency Insertion Method for Accelerated Simulation of Memristor Crossbar Array in Neuromorphic Chip
Yi Zhou, Tahsin Shameem, Zohreh Salehi, Shaloo Rakheja, Jose Schutt-Aine - University of Illinois; Hanzhi Ma, Junwei Yu, Erping Li - Zhejian University

A Novel Packaging Approach to Reduce Shading Losses in Emerging Submillimeter Concentrated Photovoltaic (CPV) Technologies
Corentin Jouanneau, Thomas Bidaud, Artur Turala, David Danovitch, Gwenaelle Hamon, Maxime Darnon - University of Sherbrooke

Fabrication and Packaging of a Heterogeneously Integrated, Flexible Quantum Dot Enabled Micro-Display
Henry Sun, Harshal Sonagara, Subramanian Iyer - University of California, Los Angeles; Lisong Xu, Kai Ding, Mingwei Zhu - Applied Materials, Inc.

Intense Pulsed Light Soldering of SAC305 for Flip-Chip Package
Seong-Ung Ryu, Young-Min Ju, Jong-Whi Park, Seok-Hoon Jeong, Hak-Sung Kim - Hanyang University

Design Space Exploration for Power Delivery Network in Next Generation 3D Heterogeneous Integration Architectures
Madison Manley, Ankit Kaul, Muhannad Bakir - Georgia Institute of Technology

Hybrid Interconnect Infrastructure for Inter-Chiplet Communication in Wafer-Scale Systems
Yousef Safari, Rezvan Mohammadrezaee, Dima Al Saleh, Boris Vaisband - McGill University

Reliability of Indium Solder Joints using Laser-Assisted Bonding (LAB) Process at Room Temperature
Ji Eun Jung, Yoon Hwan Moon, Ga-Eun Lee, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ki-seok Jang, Jin-Hyuk Oh, Yong-Sung Eom, Jung-Ho Shin, Kwang-Seong Choi - Electronics and Telecommunications Research Institute; Seung-Yoon Lee - Hanbat National University

Tailored Multi-mode, High-Q Nb Superconducting Resonators: Unique Platform for Magnon-Photon Coupling
Muntasir Mahdi, Bhargav Yelamanchili, Archit Shah, Sherman Peek, Michael Hamilton - Auburn University; Yuzan Xiong, Wei Zhang - University of North Carolina; Dan-Chi Nguyen - Ewha Womans University/The University of North Carolina; Tae Hee Kim - Ewha Womans University

Magnetic Cores for High Conversion Ratio Package Embedded Inductors
Sai Saravanan Ambi Venkataramanan, Prahalad Murali, Mohan Kathaperumal, Mark Losego - Georgia Institute of Technology; Dustin Allen Gilbert - University of Tennessee

Unveiling Mechanical Stress in Lithium-Metal Batteries for Flexible Electronics: A Novel Approach With Optical Techniques and Artificial Interfaces
Mayukh Nandy, Siyang Liu, Hongbin Yu - Arizona State University

Creep Properties of SAC305 Solder Specimens that Mimic the Microstructures of a Micro Solder Ball: Measurement and BLR Prediction
You-Gwon Kim, Heon-Su Kim, Tae-Wan Kim, Seong-Ung Ryu, Hak-Sung Kim - Hanyang University; Yongrae Jang, Bongtae Han - University of Maryland; Jun-Hyeong Lee, Jin-Kyu Kim - DUKSAN Hi-Metal Co., Ltd.

Cu@Ag Core-Shell Nanoparticles for High-Power Density Electronic Packaging
Tongtong Wang, Liang Xu - Shenzhen Institutes of Advanced Technology

RF Energy Harvesting Hybrid RFID Based Sensors for Smart Agriculture Applications
Yihang Chu, Ethan Kepros, Bhargav Avireni, Sambit Kumar Ghosh, Premjeet Chahal - Michigan State University

Influence of Nickel and Bismuth Addition on the Mechanical Shear Strength of SAC+ Ni, Bi Solders Under Isothermal Aging and Multiple Reflows
Jyothsna Bandayagari, Dr. Darshil Patel, Dr. Yingge Zhou - Binghamton University; Dr. Santosh Kudtarkar, Dr. Arun Raj, Dr. Shafi Saiyed - Analog Devices, Inc.

Process Development of Manifold Microchannels Cooling for Embedded Silicon Fan-Out (MMC- eSiFO) Package
Zhou Yang, Yuchi Yang, Peijue Lyu, Jianyu Du, Lang Chen, Chi Zhang, Wei Wang - Peking University

Demystifying Edge Cases in Advanced IC Packaging Inspection Through Novel Explainable AI Metrics
Shajib Ghosh, Antika Roy, Md Mahfuz Al Hasan, Patrick Craig, Nitin Varshney, Sanjeev J. Koppal, Navid Asadizanjani - University of Florida

Effective Heat Dissipation of White Laser Diodes by Welding Metallized Phosphor-Sapphire on Ceramic Substrate With 3D Metal Dam
Zikang Yu, Jiuzhou Zhao, Qing Wang, Yang Peng, Mingxiang Chen - Huazhong University of Science and Technology

2024 ECTC EXHIBITION

The ECTC 2024 Exhibition is pleased to showcase dozens of companies and organizations representing the full spectrum of materials, services, equipment, and products for the electronic packaging industry. Complementing the strength of the ECTC technical program, the Exhibition provides an unparalleled opportunity for engineers and decision makers to discuss and collaborate with representatives from leading electronic packaging companies. With scheduled refreshment breaks and social events that will take place in the Exhibition space, exhibitors and attendees will enjoy continual interactions with conference attendees. We are also excited to again offer the ECTC Lounge, where attendees and exhibitors can take a few minutes to relax or converse with colleagues. Exhibit hours will be from 9:00 AM to 12:30 PM and 2:00 PM to 6:30 PM on Wednesday, May 29, 2024, and 9:00 AM to 12:30 PM and 2:00 PM to 4:00 PM on Thursday, May 30, 2024. Exhibit booths for 2024 are currently on a waitlist. The 2024 Exhibit waitlist signup can be found at www.ectc.net and by clicking the "Exhibits" link. For additional information or questions, please contact Sam Karikalan, ECTC Exhibits Chair at +1-949-529-4802 or email samkarikalan@ieee.org and exhibits@ectc.net

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HOW TO REGISTER FOR ECTC:

By Internet: Submit your registration electronically via www.ectc.net. Your registration must be received by the cutoff date, May 3, 2024, to qualify for the early registration discounts.

You may contact our registration staff at registration@ectc.net for additional information. Payment can be made by Visa, Mastercard, or American Express.

HOTEL RESERVATIONS

Gaylord Rockies Resort & Convention Center
6700 N Gaylord Rockies Blvd., Aurora, CO 80019

Hotel reservations for ECTC 2024 can be made in one of two ways:

1) Contact the Gaylord Rockies Resort & Convention Center at +1-720-452-6900 and reference the ECTC Conference to receive the conference rate of US$229 per night, unless the reserved room block for the conference is fully booked.

or

2) Log onto www.ectc.net and click on the "Location" tab near the top of the page to find a special online hotel registration link.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2024 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2024 from 3rd party companies. These emails and sites are not to be trusted. There are scam artists out there and if it's too good to be true it likely is. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC emailings to subscribers or ECTC emails from our Executive Committee. **ECTC's only authorized site** for reserving a room is through our website (www.ectc.net). You may, however, want to use other trusted sites to book travel. Should you have any questions about booking a hotel room please contact ECTC staff at lrenzi@renziandco.com.

74th Electronic Components & Technology Conference

2024 ECTC REGISTRATION INFORMATION			
Conference Registration		**Advance Registration Until May 3**	**Door Registration Starting May 4**
IEEE Member	Attendee (full ECTC conference)	US $1100	US $1265
	Attendee (Joint ECTC + ITHERM conferences)	$1430	$1665
	Attendee One-Day Registration	$835	$835
	Speaker or Chair (full ECTC conference)	$935	$1135
	Speaker or Chair One-Day Registration	$735	$735
Non-IEEE Member	Attendee (full ECTC conference)	$1365	$1530
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	Attendee One-Day Registration	$835	$835
	Speaker or Chair (full ECTC conference)	$935	$1135
	Speaker or Chair One-Day Registration	$735	$735
Student	Attendee or Speaker (full conference)	$455	$455
Professional Development Courses (PDCs) Note: all PDCs include a luncheon			
IEEE Member	Full PDC (both a.m. and p.m.)	$625	$625
	Single PDC (a.m. or p.m.)	$440	$440
Non-IEEE Member	Full PDC (both a.m. and p.m.)	$675	$675
	Single PDC (a.m. or p.m.)	$490	$490
Student	Full PDC (both a.m. and p.m.) or Single PDC	$150	$150
Other Registration Options			
Extra Luncheon Tickets		$100	$100
Cancellation Fee		$100	$100

Please note that we are no longer offering the purchase of extra proceedings. Additionally, the various exhibit registration types are no longer available for the general public.

Please log onto www.ectc.net/registration to register for 2024 ECTC.

There will be no refunds or cancellations after May 3, 2024. Please note that a $100 cancellation fee will be in effect for all cancellations made on or prior to May 3, 2024. Substitutions can be made at any time.

For additional information about registration or ECTC please contact us at:

ECTC Registration
% Renzi & Company, Inc. Management
Email: registration@ectc.net

If you join IEEE **BEFORE you register for the 2024 ECTC you can save on registration fees and get the Electronics Packaging Society (EPS) add-on membership free for the reminder of 2024!*

To take advantage of this offer, simply go to: https://www.ieee.org/membership-application/public/join.html

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CONFERENCE OVERVIEW

Tuesday, May 28, 2024

Morning Professional Development Courses
8:00 a.m. - 12:00 p.m.

1. High Reliability Soldering in Semiconductor Packaging
2. Photonic Technologies for Communication, Sensing, and Displays
3. From Wafer to Panel Level Packaging
4. Eliminating Failure Mechanisms in Advanced Packages
5. Navigating Thermal and Reliability Challenges in Chip Components for Automotive High-Performance Compute Systems
6. Polymers for Advanced Packages
7. Flip Chip Technologies
8. Reliable Integrated Thermal Packaging for Power Electronics

ECTC Special Session on Industry-Government Co-Investments for Advanced Packaging
8:30 a.m. - 10:00 a.m.
Exploring the Impact of Industry-Government Co-Investments for the Advanced Electronics Sector in North America, Asia and Europe

ECTC Special Session on Advanced Metrology
10:30 a.m. - 12:00 p.m.
Challenges and Opportunities in Advancing Metrology for Next-Generation Microelectronics

Afternoon Professional Development Courses
1:30 p.m. - 5:30 p.m.

9. Additive Flexible Hybrid Electronics – Manufacturing and Reliability
10. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel Level and Advanced RF Packages
11. Fan-Out Packaging and Chiplet Heterogeneous Integration
12. Analysis of Fracture and Delamination in Microelectronic Packages
13. Advanced Packaging for MEMS and Sensors
14. Nano Materials and Polymer Composites for Electronic Packaging
15. Design-On-Simulation for Advanced Packaging Reliability and Life Prediction
16. Thermal Spreading and Contact Resistance

ECTC Special Session on Thermal Management
1:30 p.m. - 3:00 p.m.
Efficient and Innovative Thermal Management for Power Hungry AI/ML Applications: Challenges and Opportunities

ECTC Special Session on RF Packaging
3:30 p.m. - 5:00 p.m.
RF Packaging for Communication and Sensing Applications above 100 GHz – Technologies, Design Challenges and Emerging Solutions

Young Professionals Networking Panel
7:00 p.m. - 7:45 p.m.

ECTC EPS Seminar
7:45 p.m. - 9:15 p.m.
Challenges of Chiplets on Large Substrates

Wednesday, May 29, 2024

ECTC Keynote
8:00 a.m. - 9:15 a.m.
Petascale photonic chip connectivity for energy efficient AI computing

Technical Sessions
9:30 a.m. - 12:35 p.m.

1. Advances in Fan-Out, Wafer Level, and Panel-Level Packaging Technologies Enabling New Applications
2. Advanced Die-to-Wafer Hybrid Bonding for Heterogeneous Integration
3. Co-Packaged Optics
4. Reliability of Advanced Substrates and Interconnects
5. Digital Health Care: Wearable Sensors, and Flexible Electronics
6. Thermal-Mechanical Reliability Simulations

Interactive Presentation Session 37
10:00 a.m. - 12:00 p.m.

Wednesday Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

7. Heterogeneous Integration: Systems Design, Signal & Power Delivery, and Process Optimization
8. Sub-Micron Scaling in Wafer-to-Wafer Hybrid Bonding
9. Advanced Processes for Chip Stacking
10. Novel 3D Integration and Hybrid Bonding Solutions
11. Next-Generation Artificial Intelligence, Quantum Computing, and Secure Packaging
12. Artificial Intelligence and Advanced Modeling Approaches

Interactive Presentation Session 38
2:30 p.m. - 4:20 p.m.

ECTC/ITHERM Diversity and Reception
6:30 p.m. - 7:30 p.m.
Best Practices to Attract, Hire and Retain a Diverse Workforce

Thursday, May 30, 2024

ECTC Plenary Session on Emerging Start-ups
8:00 a.m. - 9:15 a.m.
The Future of the Semiconductor Industry. Emerging Start-ups and Technologies for Advanced Packaging

Technical Sessions
9:30 a.m. - 12:35 p.m.

13. Next-Generation Substrate Manufacturing Technologies
14. Breakthrough Ultra-Fine Pitch Redistribution Layer and Solder Bumping Technologies
15. Novel Materials and Process for Hybrid Bonding
16. Reliability of High-Density and High-Power Packages
17. Advanced Additive Manufacturing for Printed Electronics and Integrated Systems
18. Radio Frequency Antenna-in-Package and Component Design

Interactive Presentation Session 39
10:00 a.m. - 12:00 p.m.

EPS Awards Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

19. 3D Integration Copper-Copper Hybrid Bonding
20. Novel High-Density 3D & Thru-Via Structures and Processes
21. Innovations in Polymer Packaging Materials
22. Signal & Power Integrity for Advanced Packages and Systems
23. Novel Bonding Technology for Advanced Assembly Substrates and Integration
24. Advances on Flex and Redistribution Layer Technologies and Warpage

Interactive Presentation Session 40
2:30 p.m. - 4:20 p.m.

Friday, May 31, 2024

ECTC EPS President Panel Session on Education and Workforce Development
8:00 a.m. - 9:15 a.m.
Challenges in Education and Workforce Development in the New Chips Economy

Technical Sessions
9:30 a.m. - 12:35 p.m.

25. High-Performance Computing, Design Challenges, and Solutions
26. Chiplet Interconnect Design and Validation
27. Advanced Die Bond and Board Level Reliability
28. Optical Interconnections
29. Reliability in Harsh Environments Including Automotive
30. Process and Hybrid Bonding Modeling and Characterization

Student Interactive Presentations Session 41
10:00 a.m. - 12:00 p.m.

Raffle Prize Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.

31. Advances in Flip Chip and Chip Scale Packages
32. Advancement in Copper Hybrid Bonding Technologies Common to Multiple Applications
33. Fine-Pitch Materials and Processes
34. Photonics Integration, Materials, and Processes
35. Reliability and Current Stressing of Solder Interconnections
36. Thermal Management and Cooling Solutions

Session Summary by Interest Area

Packaging Technologies
S1, S7, S13, S19, S25, S31

Applied Reliability
S4, S16, S29, S35

Assembly & Manufacturing Technology
S10, S23, S27

Emerging Technologies
S5, S11, S17

RF, High-Speed Components & Systems
S18, S22, S26

Interconnections
S2, S8, S14, S20, S26, S32

Materials & Processing
S9, S15, S21, S27, S33

Thermal/Mechanical Simulation & Characterization
S6, S12, S24, S30, S36

Photonics
S3, S28, S34

Interactive Presentations
S37, S38, S39, S40, S41

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