Copper Hybrid Bond Interconnections for Chip-On-Wafer Applications

Tuesday, May 30, 2023, 10:30 a.m. – 12:00 p.m.

Chairs: Thomas Gregorich (Infinera) and Chaoqi Zhang (Qualcomm)

Moderator: Jan Vardaman (TechSearch International)

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Thomas Gregorich
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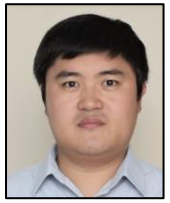

Chair
Chaoqi Zhang
Qualcomm

Moderator
Jan Vardaman
TechSearch International

Speaker
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Besi

Speaker
Xavier Brun
Intel

Copper Hybrid Bond Interconnections for Chip-On-Wafer Applications

As one of the primary building-blocks of IC packages, electrical interconnections are evolving rapidly to address increasing ultra-high bandwidth requirements. Copper Hybrid Bonds deliver the highest-density chip-to-chip interconnect and are seen as a key enabling technology for ultra-high bandwidth devices/systems such as vertically-stacked chiplets.

This Special Session will explore the applications, requirements, and challenges of Copper Hybrid Bonds (CHB) for Chip-to-Wafer (C2W) applications. Wafer-to-wafer CHB has been in HVM for many years and continues to expand. While C2W is in production, challenges remain. This panel will discuss challenges and solutions for the expanded use of C2W Copper Hybrid Bonds.

Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications

Xavier F. Brun

Intel Corporation, Assembly Test Technology Development

Chandler, AZ, United States

Ack. Sai A., Pooya T., Kaladhar R., Adel E., AP&PL Team

Heterogeneous Packaging Requirements

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High efficiency power delivery architectures

High efficiency VR, Low IR drop

Power-efficient, High Bandwidth On-Package IO

Ultrafine bump pitches, Fine L/S

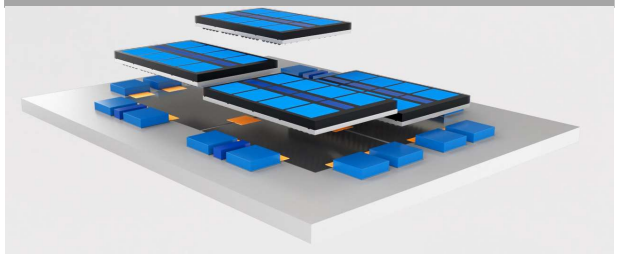
Diverse application functionality

On-package multi-IP Integration

Disaggregation (i.e L2 cache, etc.)

& Standardization of Interfaces

HPC - AI / Datacenter Advanced Packaging



Manage increasing cooling demands

Si-package co-design and materials for improved thermals

System Compatible Form Factors

Die stacking, Tight die-die spacing, Large complexes

High Yield, perf /$

Die disaggregation

Design/architect for yield

High speed IO over long distance

Optical signaling on package

High reliability

Design, process, architecture, materials for reliability

Copper Hybrid Bonding (CHB) performance benefits drives adoption in HPC AI / Datacenter applications

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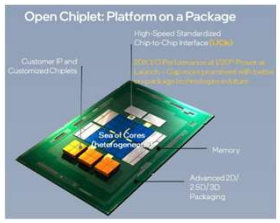
CHB HI Challenges & Opportunities

External IP/die/pkg Integration Challenge

- Standardization of Bond Interface (enabling mix-foundry HI)
- Design rule/ Design co-optimization
- 3D HBI protocol standardization

Ponte Vecchio

Source: WCCF TECH INC.

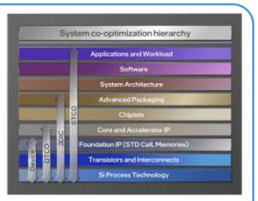


Universal Chiplet Interconnect Express

Source: UCIe

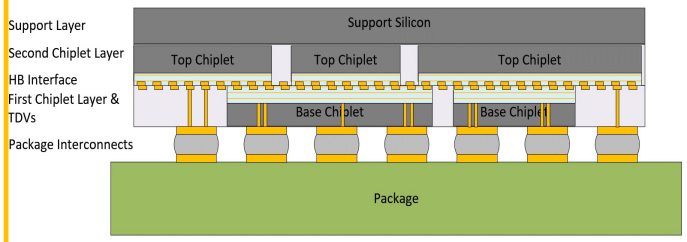
Cost Challenge

- Current C2W HB cost limits wide product adoption (logic) vs. solder solution
- Standardization / Supplier Ecosystem
- System technology co-optimization (STCO)



Source: A. Kelleher IEDM'22

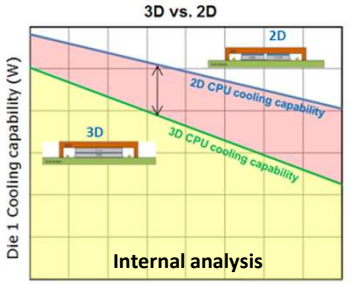
HI with Hybrid Bonding [Quasi-Monolithic Chips (QMC)]

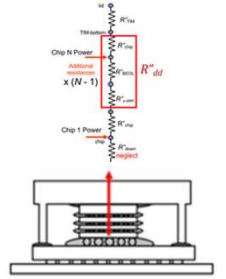


Elsherbini, A., et al. "Enabling Next Generation 3D Heterogeneous Integration Architectures on Intel Process." 2022 IEDM. IEEE, 2022.

Thermal Challenge

- Lower 3D pkg cooling capability





Source: Heterogeneous Integration Roadmap Chapter 20

C2W HBI Yield Challenge

- Die-Wafer, Stack Die- Substrate
- Improved alignment accuracy for pitch scalability
- Controlled wafer/die warpage and stress
- Stacked die coplanarity

New Material Challenge

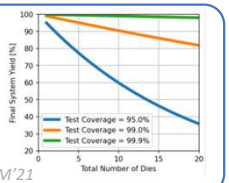
- Low cost/reliable Die to Die fill materials
- Bonding surface protection material
- Carrier materials / clean or PL chemistries
- Thermal interface materials

Power delivery Challenge

- 3D stacking (active on active)
- Need EDA tools

Test Challenge

- New test strategy for fine pitch
- Need better test coverage



Source: A. Elsherbini, IEDM'21

Need 3D HBI interface standardization to help CHB adoption
System technology co-optimization key to HI with C2W Hybrid Bonding

C2W Hybrid Bonding Technology Challenges

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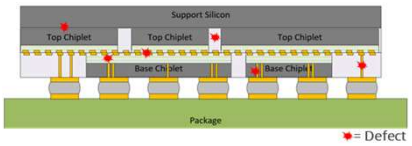
Metrology Challenge

- In-line metrology & inspection for real time process feedback

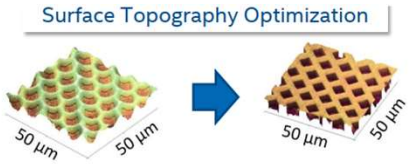
- AI/ML Training Integration for High-Precision, High TPT Recess Metrology

- High Speed, Localized, Non-destructive Defect Detection

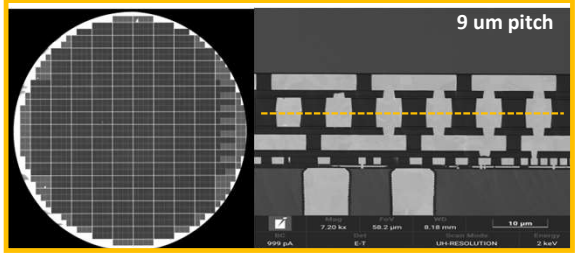


Process & Thermal Mechanical Challenges

- CMP for Cu dishing control
- Clean singulation solution
- Sit time control for plasma activation
- Thermal budget for the process flow
- Control overall stress of the package

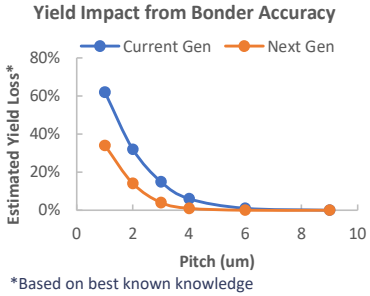


Void-Free Bonding with Extremely High Placement Accuracy (<< 1um)

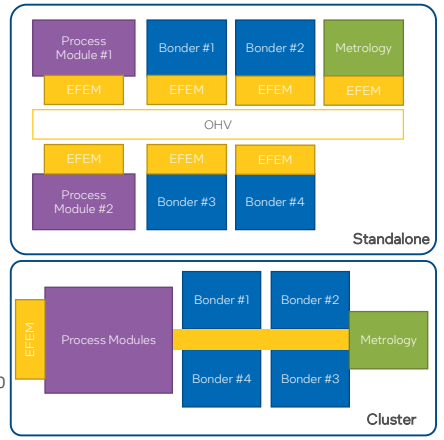


C2W Equipment Challenge

- Scalability for Reducing Pitch
- Cleanliness Control
- Active Thermal Control
- Run Rate Optimization

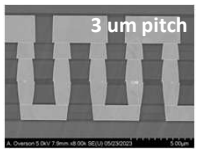


*Based on best known knowledge



Test & Reliability Challenges

- New test strategy with tight pitch pads
- Reliability for hybrid bonding (Cu-Cu & dielectric bond strength)



Innovations needed to solve process scalability/reliability and metrology challenges in CHB

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 This document contains information on products and/or processes in development.

Die-to-Wafer Hybrid bonding Technology Roadmap

Eric Beyne, imec

System-level benefits drive microelectronic scaling

This is also the Main driver for 2.5D and 3D integration technologies:

- Increasing system complexity
- Increasing need for heterogeneous integration – not only SOC
- Increasing die-to-die interconnect data bandwidth:
  - more interconnect channels,
  - higher interconnect speeds per interconnect

  } Very high aggregate bandwidth
- Reducing die-to-die interconnect energy:
  - Shorter distance interconnect
  - Scaled, lower capacitance interconnects
  - Lower voltage

$\Rightarrow$ It is not about the number of interconnects but rather the available (local) interconnect density enabled by interconnect pitch scaling

Die-to-Die interconnect technology today

- Solder µbump technology: 50 ⇒25 µm pitch today

- Wafer-to-Wafer Hybrid bonding: 10⇒ 1 µm pitch today

Die-to-Die interconnect technology today

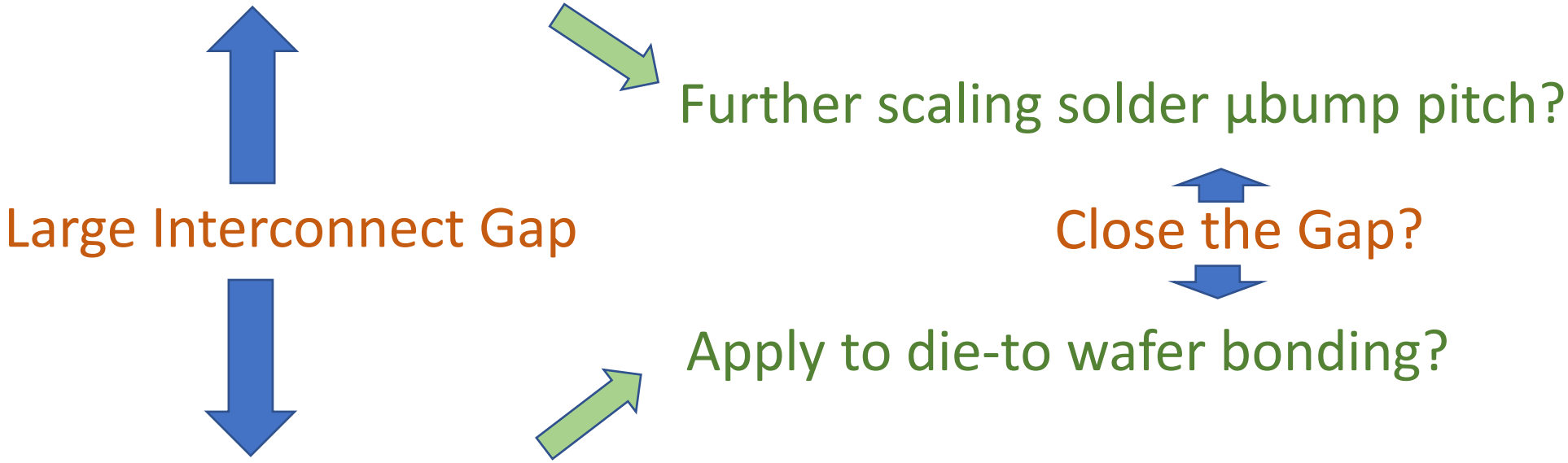
- Solder µbump technology: 50 ⇒25 µm pitch today

Large Interconnect Gap

- Wafer-to-Wafer Hybrid bonding: 10⇒ 1 µm pitch today

Die-to-Die interconnect technology today

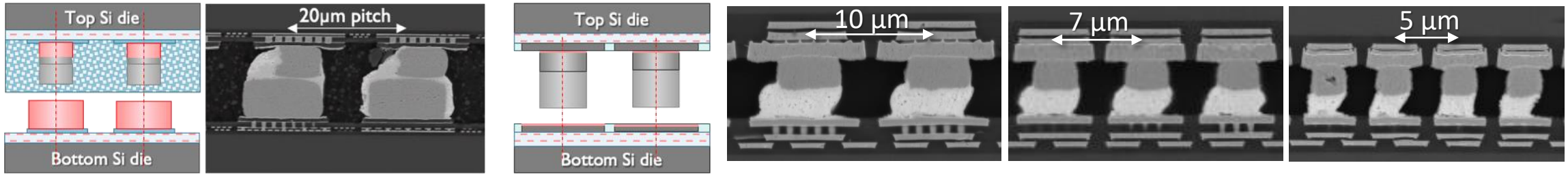
- Solder µbump technology: 50 ⇒25 µm pitch today



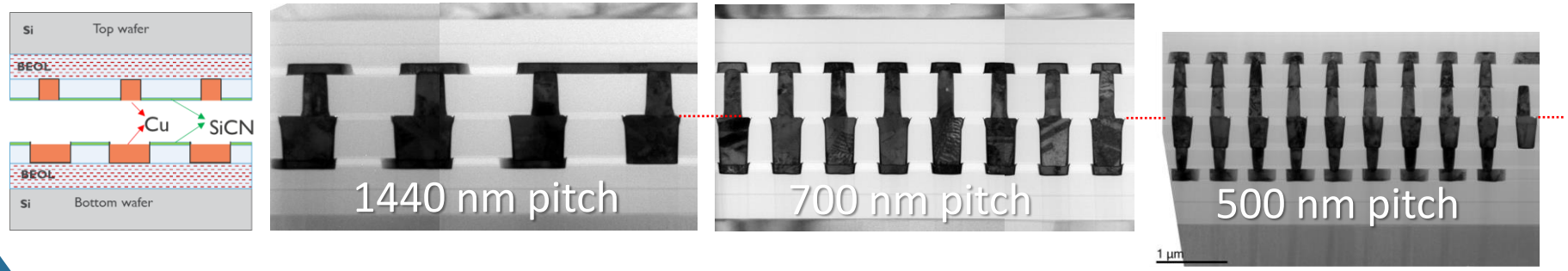
- Wafer-to-Wafer Hybrid bonding: 10⇒ 1 µm pitch today

Die-to-Die interconnect R&D @ imec

- Solder µbump technology: 20 ⇒10 ⇒7 ⇒5 µm pitch



- Wafer-to-Wafer Hybrid bonding: 2 µm ⇒ 700nm ⇒ 500nm pitch



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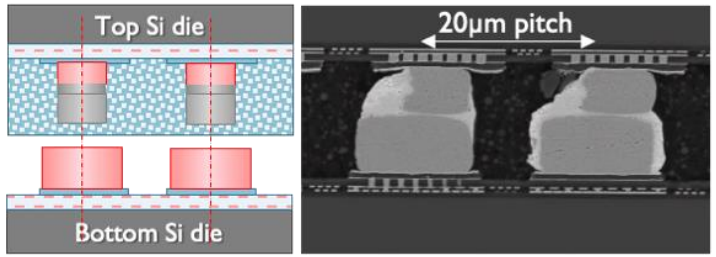
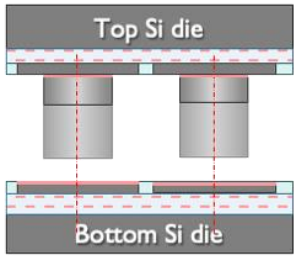
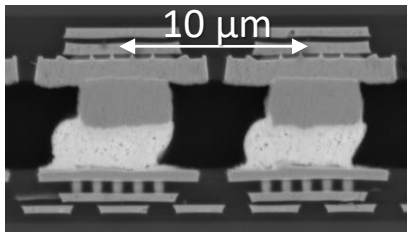
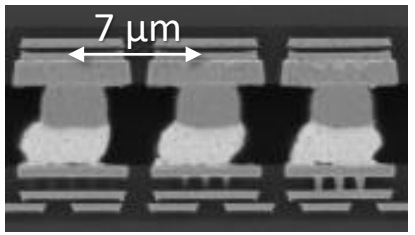
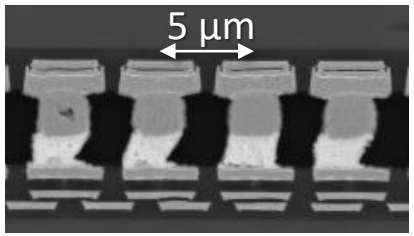


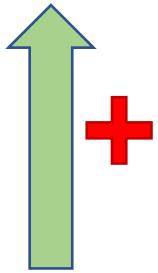




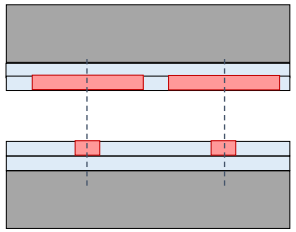


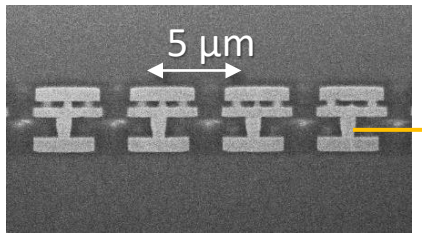


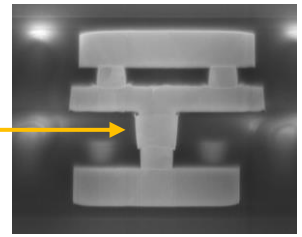
- Die-to wafer Hybrid bonding: 10 ⇒5 ⇒2 µm pitch

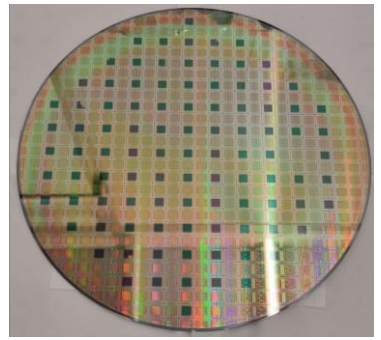


➢Ultra clean dicing
➢Post dicing die cleaning
➢Ultra-clean, High precision, High UPH D2W placement

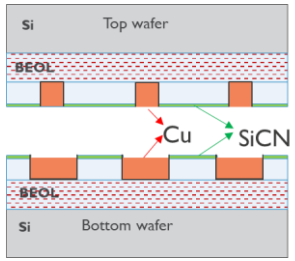


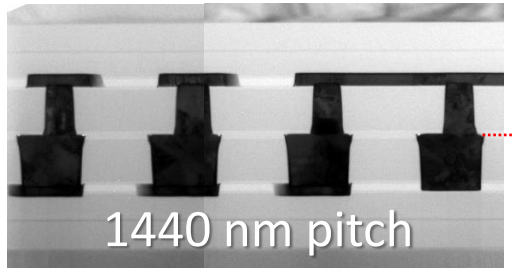


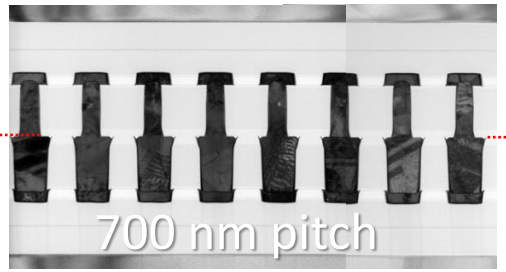


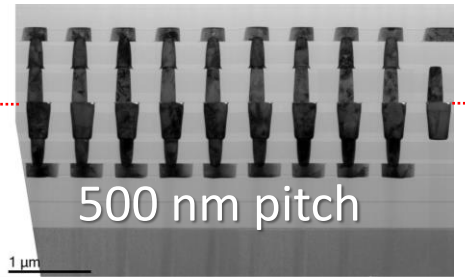


- Wafer-to-Wafer Hybrid bonding: 2 µm ⇒ 700nm ⇒ 500nm pitch

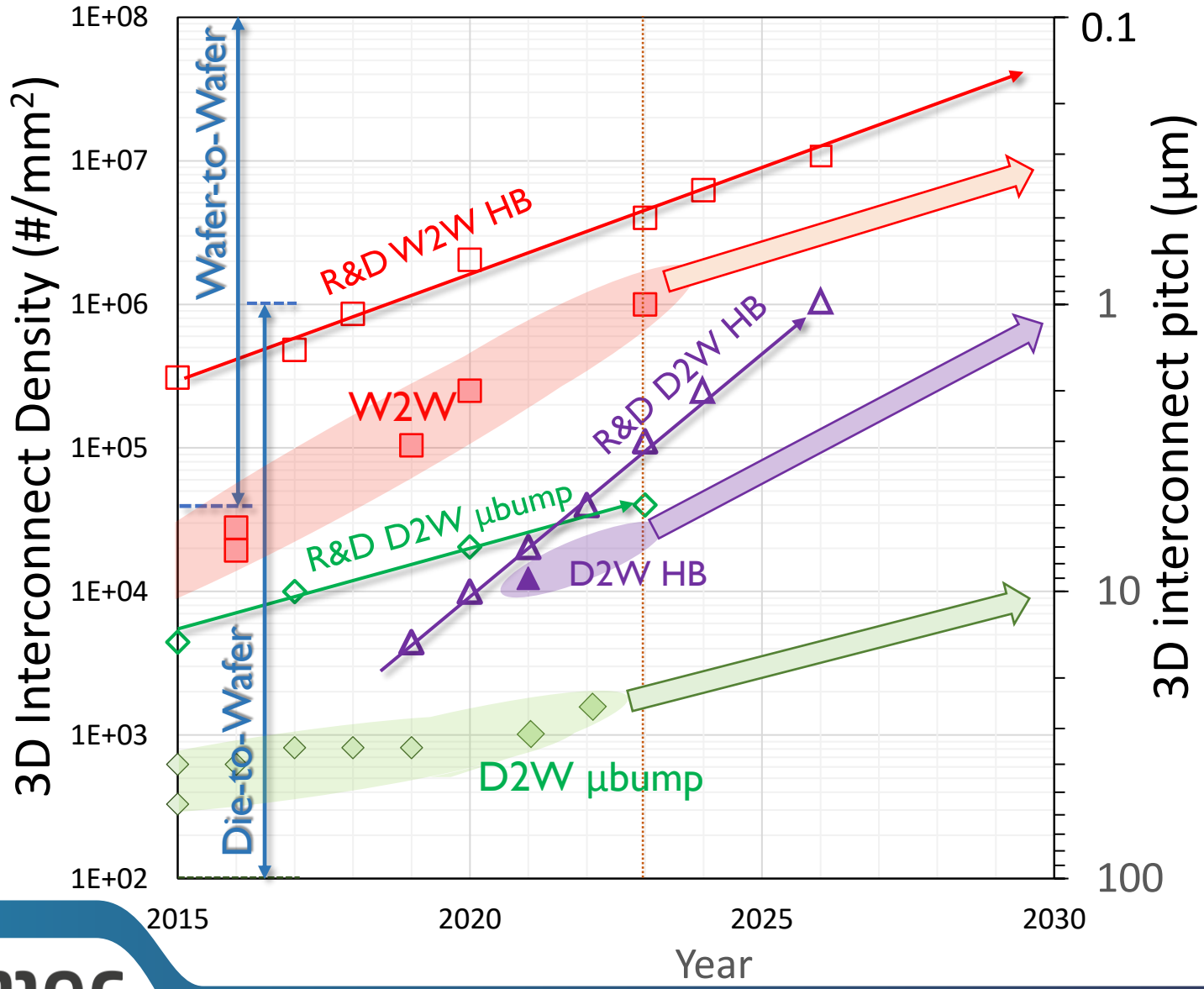








3D Interconnect Roadmap – imec R&D & Industry



R&D roadmap 5 to 10 year ahead of industry adoption

D2W Hybrid bonding will fill the 10 to 1 µm pitch gap between µBump bonding and W2W HB bonding

- W2W HB - imec R&D
- W2W HB - industry
- D2W HB - imec R&D
- D2W HB - industry
- D2W µBump - imec R&D
- D2W µBump - industry

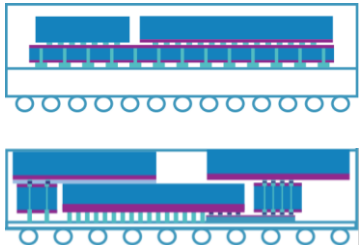
D2W= Die-to-wafer bonding
W2W= Wafer-to-Wafer bonding
HB= Hybrid bonding

The 3D Interconnect Technology Landscape

3D-SIP

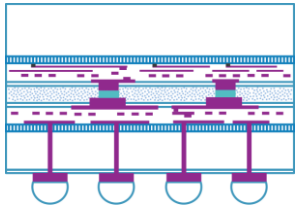
Package stacking

- Multi-die Packaging
- Interposer "2.5D"
- Embedded Die

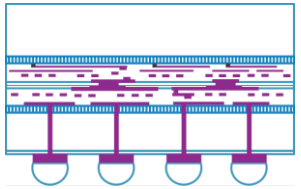


3D-SIC

Die Stacking µbump

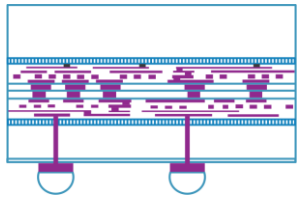


Die Stacking Hybrid bonding



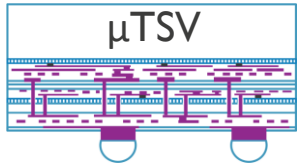
3D-SOC

Wafer-to-Wafer Hybrid bonding

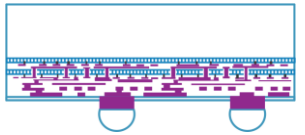


Dielectric bonding

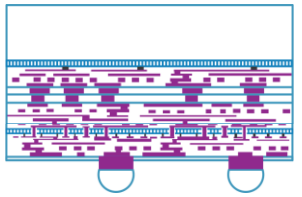
µTSV



Wafer-to-Wafer Sequential

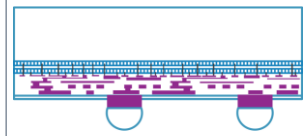


BSPDN



3D-IC

Transistor Stacking



3D Interconnect Pitch scaling

1mm 400µm 100 µm 40µm 20µm 10 µm 4µm 2µm 1µm 500nm 100nm

3D Interconnect Density (#/mm²)

1 10 10^2 10^3 10^4 10^5 10^6 10^7 10^8

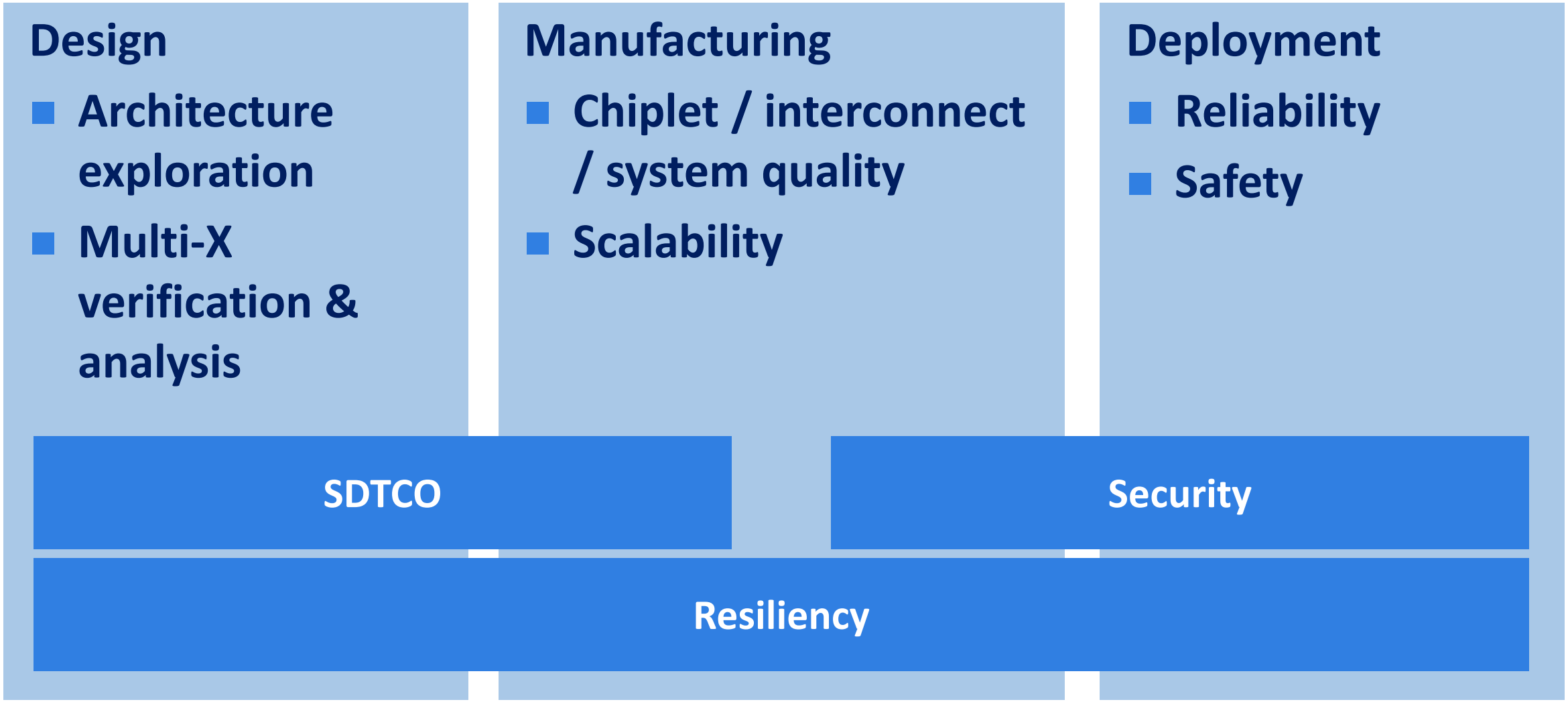
PDF/SOLUTIONS™

Confidential Information

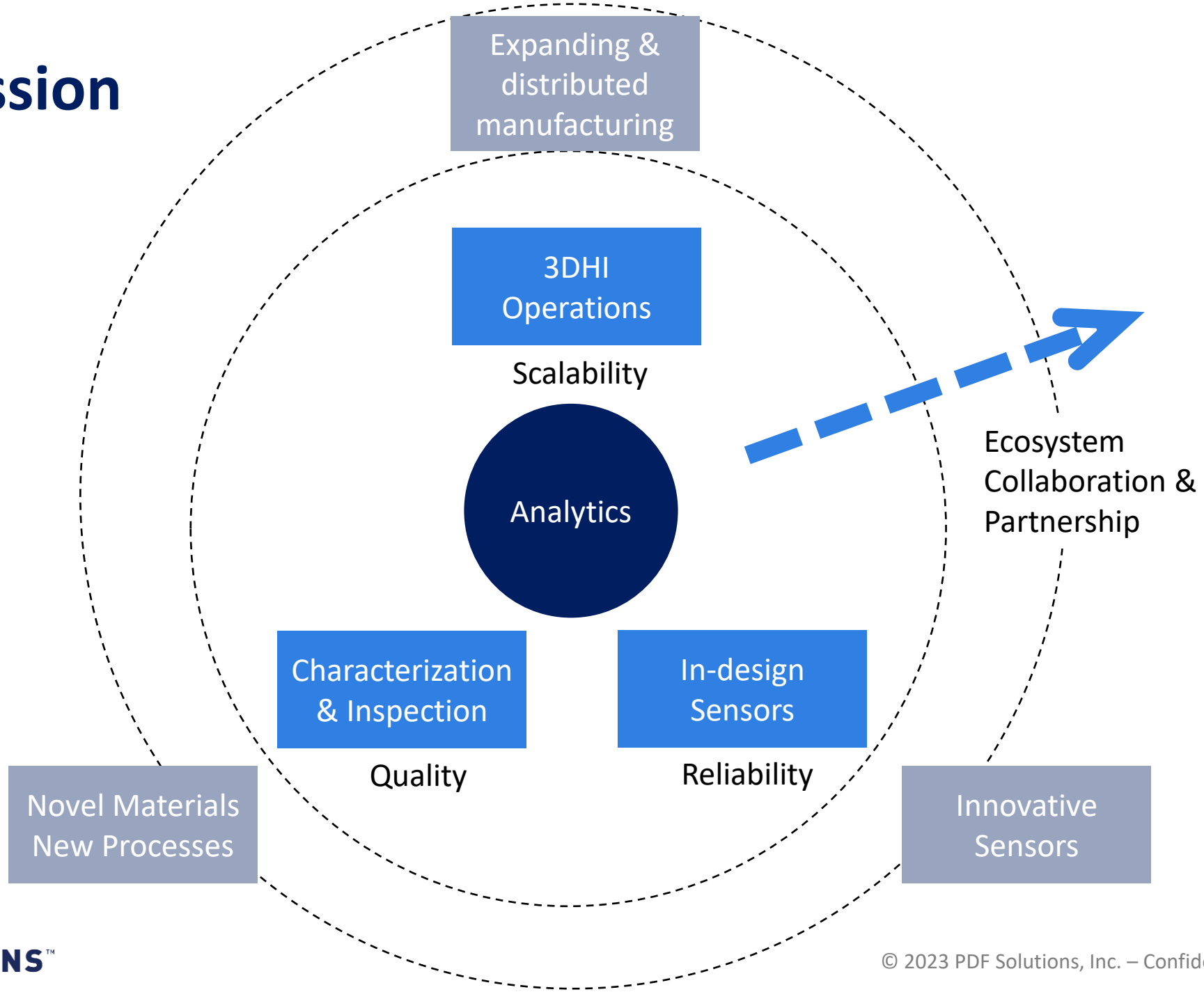
Enabling Robust 3DHI Products:

A Quality and Reliability Perspective

Broader 3DHI Challenges



PDF Mission



PDF Capabilities: Hybrid Bonding Use Cases

Design → Ramp → Production → Deployment

exensio

Process Control
+ Assembly Ops
+ Test Ops

Real-time 3DHI operations and test control
E142 Single device traceability

exensio

Manufacturing Analytics

End-to-end, anywhere to anywhere, correlation & problem-solving

DirectScan (ebeam)
+
Characterization Vehicle Infrastructure (probed)

Massively parallel characterization of alignment / resistivity / performance …

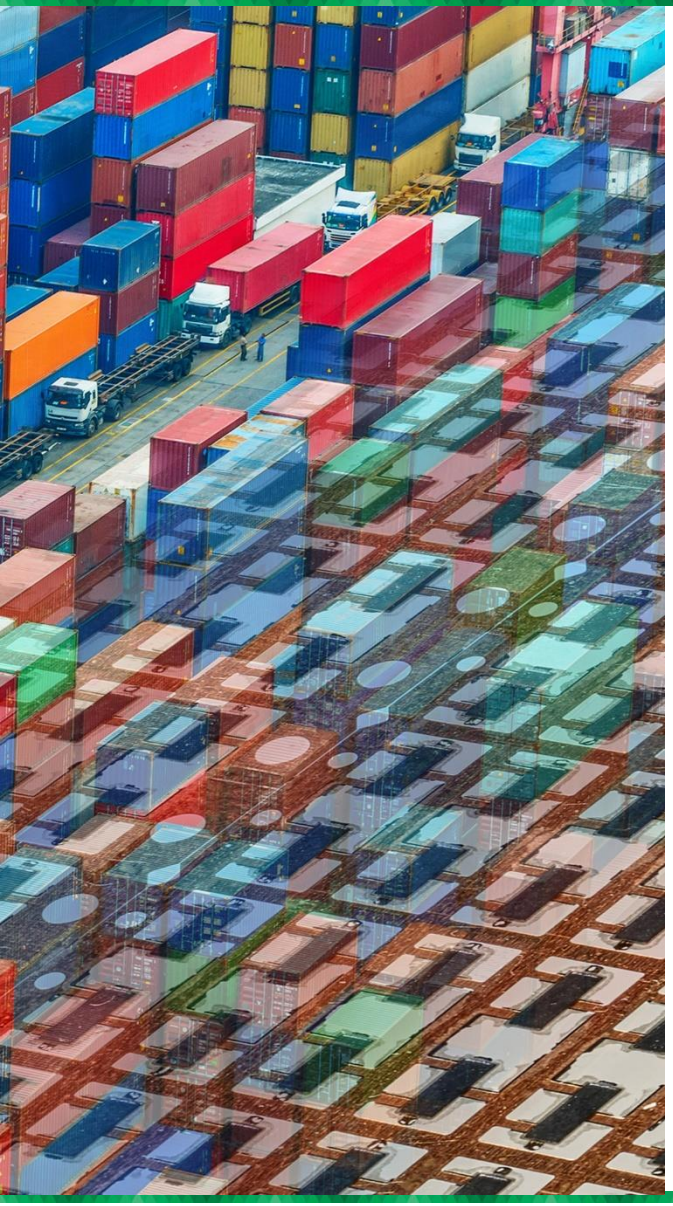
In-circuit sensors and control

Pre/post-assembly stress
Burn-in / in-field aging

Software

Hardware

PDF/SOLUTIONS™

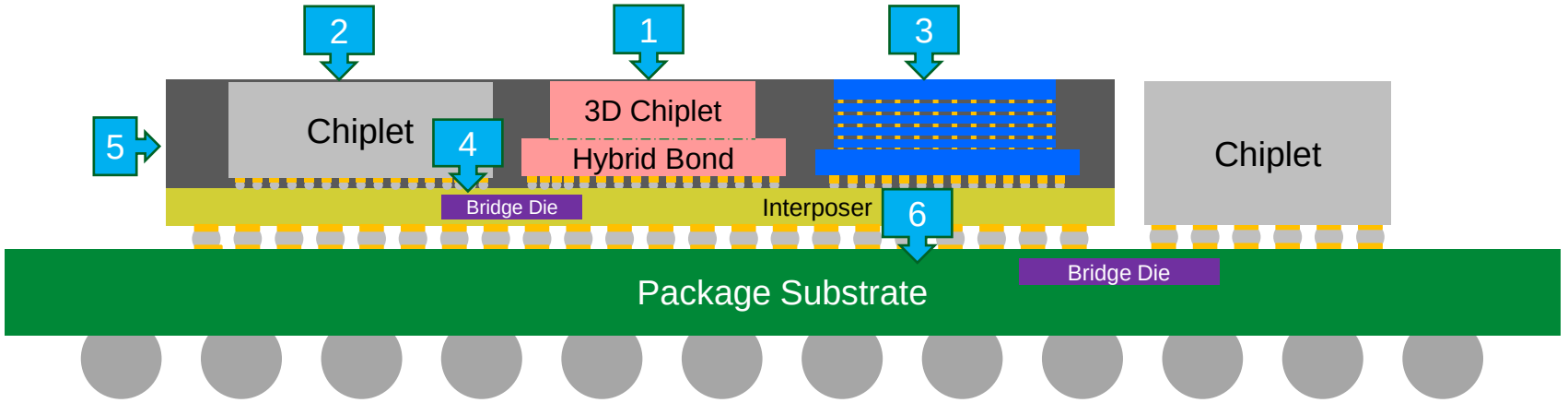


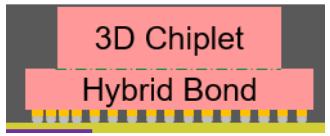
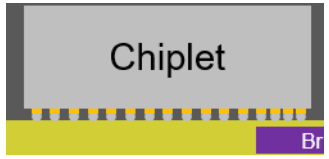
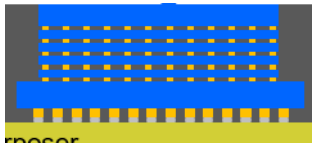
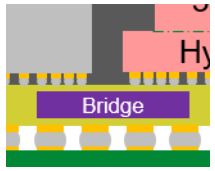
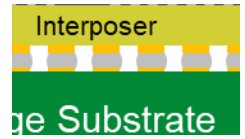
Chip-to-Wafer Hybrid Bonding Opportunities and Challenges

2023 ECTC Special Session on Copper Hybrid Bonds

Chris Scanlan
SVP Technology, Besi

New 3D Chiplet Structures Use Variety of Processes



1	2	3	4	5	6
Hybrid Bonding	Chip to Wafer TCB	High Bandwidth Memory Stacking	Embedded Bridge Die Attach	Wafer Level Die Molding	HD Interposer to Substrate
					
8800 CHAMEO Ultra Plus	9800 TC Next C2W	8800 CHAMEO Ultra Plus 8800 TC Advanced	8800 Chameo Ultra	FML	2200 evo

Hybrid Bonding Extends Moore's Law by 3D System Scaling

Enables faster, more complex devices with submicron placement accuracy.

Direct Cu-Cu Interconnect in 3D

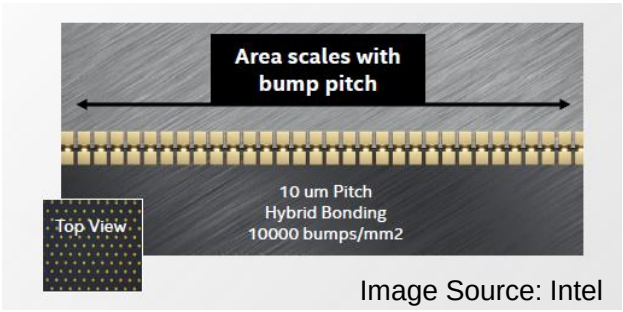


Image Source: Intel

1000x increase in contact density

Heterogeneous integration of chiplets

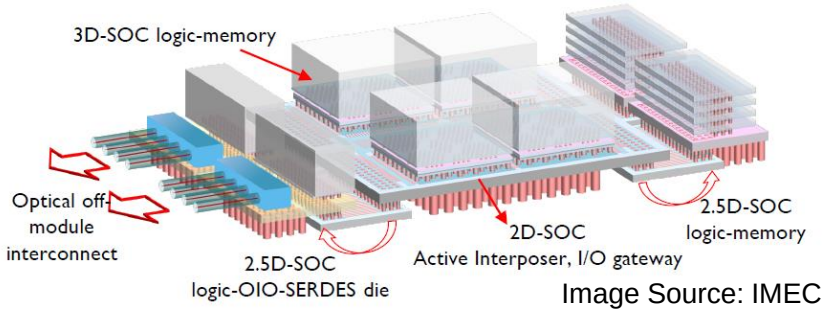


Image Source: IMEC

More transistors per package

Increased Performance

- Increased data transfer
- Higher bandwidth
- Higher speed

Lower Cost of Ownership

- Higher die yield
- Lower energy per bit
- Lower cost per contact
- Lower heat dissipation

Design Flexibility

- New 3D chiplets
- Fab node optimization
- Customized designs
- Highly configurable

8800 Chameo Ultra Plus Chip-to-Wafer Hybrid Bonder

First high-volume die-to-wafer hybrid bonder

In production since Q1 2022

200 nm alignment accuracy

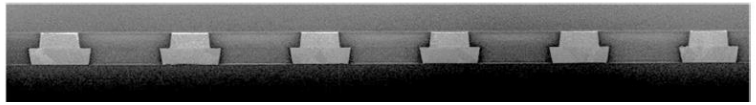
At high speed of up to 2000 UPH

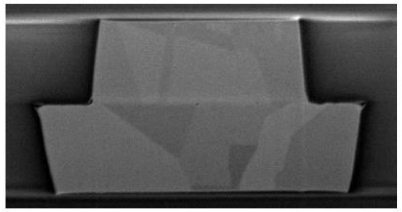
Designed for use in front-end fab environment

Optional cluster line integration via collaboration with AMAT

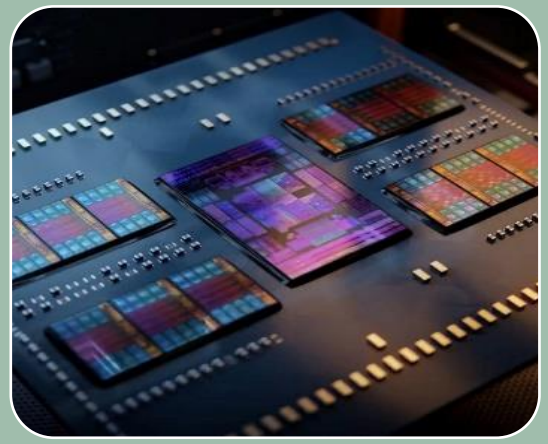
100 nm accuracy machine available in 2023

Roadmap to 50 nm accuracy





Hybrid Bonding Potential Applications

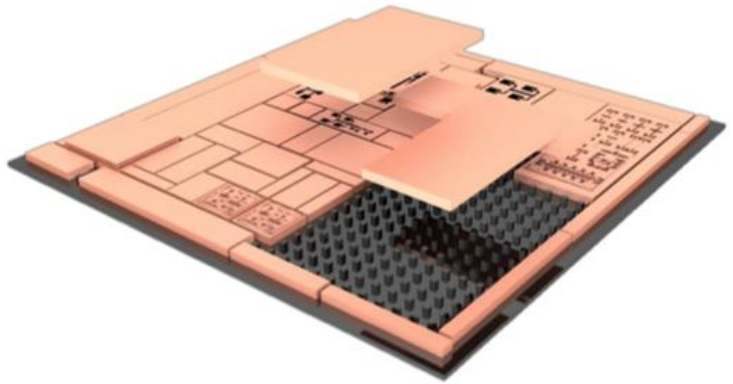
HPC	Advanced Memory	Mobile	Sensors and Photonics
			
Logic + Memory Core on Core	**Advanced Memory Stacking**	**Application Processors mmWave RF**	**Integrated Silicon Photonics**
AI Datacenters Gaming	HBM4 DRAM	Smartphones	Image Sensors AR/VR Display

Challenges to Broad Adoption of Interoperable Chiplets

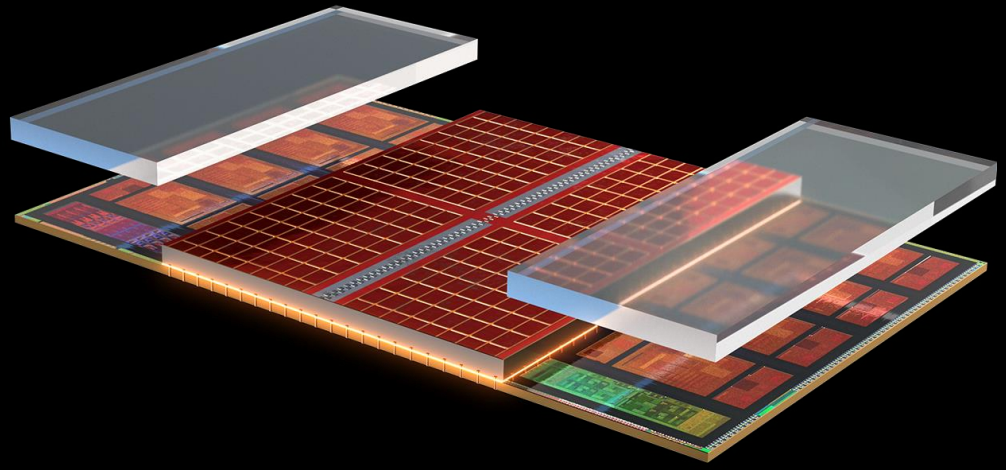
Chiplets promise to allow integration of functional blocks from multiple companies into a single device, speeding development and reducing development cost

But several challenges must be addressed to integrate chiplets from different companies:

- Control and compatibility of the bonding surfaces
- Standardization of communication protocols and physical interfaces (e.g. UCIe)
- EDA tools and design flows
- Testability and verification of the individual chiplets and the assembly
- Performance binning and matching
- Yield ownership
- Failure analysis methods and ownership
- Product liability and allocation of risk
- Margin stacking
- Supply-chain management and logistics

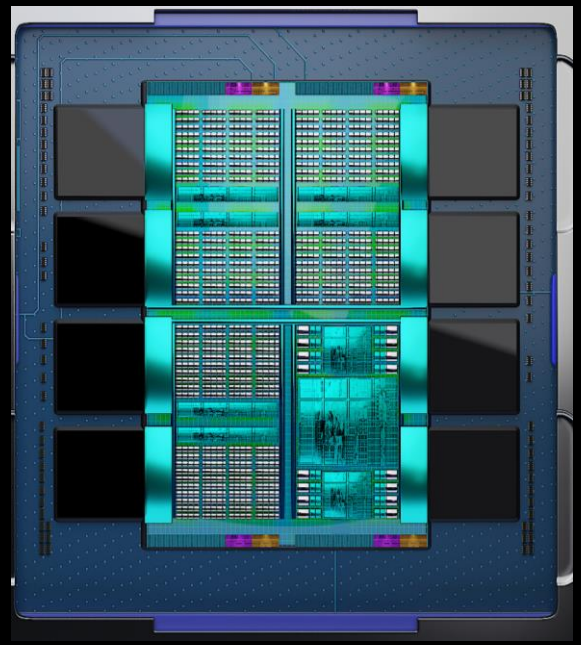


AMD



3D ADVANCED PACKAGING ENABLING MOORE'S LAW'S NEXT FRONTIER

HYBRID BONDING COMES ALIVE TO ENABLE THE FUTURE OF HIGH- PERFORMANCE & AI COMPUTING



RAJA SWAMINATHAN

AMD CORPORATE VP

ADVANCED PACKAGING LEADER

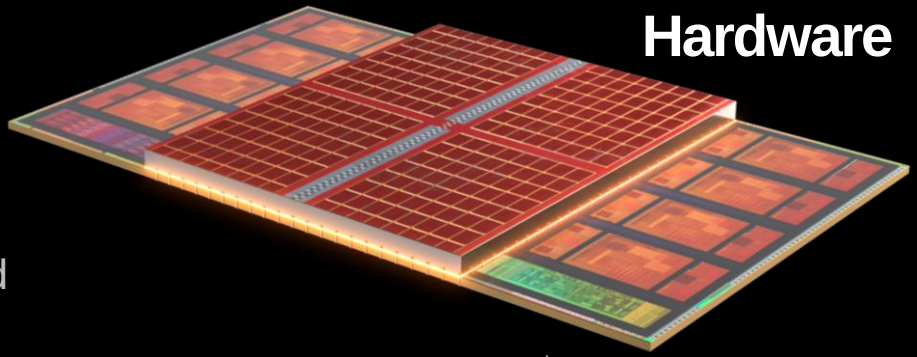
CAUTIONARY STATEMENT

This presentation contains forward-looking statements concerning Advanced Micro Devices, Inc. (AMD) such as the features, functionality, performance, availability, timing and expected benefits of AMD products; TAM for data center, PCs, embedded and gaming; and technology trends, innovation and roadmaps, which are made pursuant to the Safe Harbor provisions of the Private Securities Litigation Reform Act of 1995. Forward-looking statements are commonly identified by words such as "would," "may," "expects," "believes," "plans," "intends," "projects" and other terms with similar meaning. Investors are cautioned that the forward-looking statements in this presentation are based on current beliefs, assumptions and expectations, speak only as of the date of this presentation and involve risks and uncertainties that could cause actual results to differ materially from current expectations. Such statements are subject to certain known and unknown risks and uncertainties, many of which are difficult to predict and generally beyond AMD's control, that could cause actual results and other future events to differ materially from those expressed in, or implied or projected by, the forward-looking information and statements. Investors are urged to review in detail the risks and uncertainties in AMD’s Securities and Exchange Commission filings, including but not limited to AMD’s most recent reports on Forms 10-K and 10-Q.

AMD does not assume, and hereby disclaims, any obligation to update forward-looking statements made in this presentation, except as may be required by law.

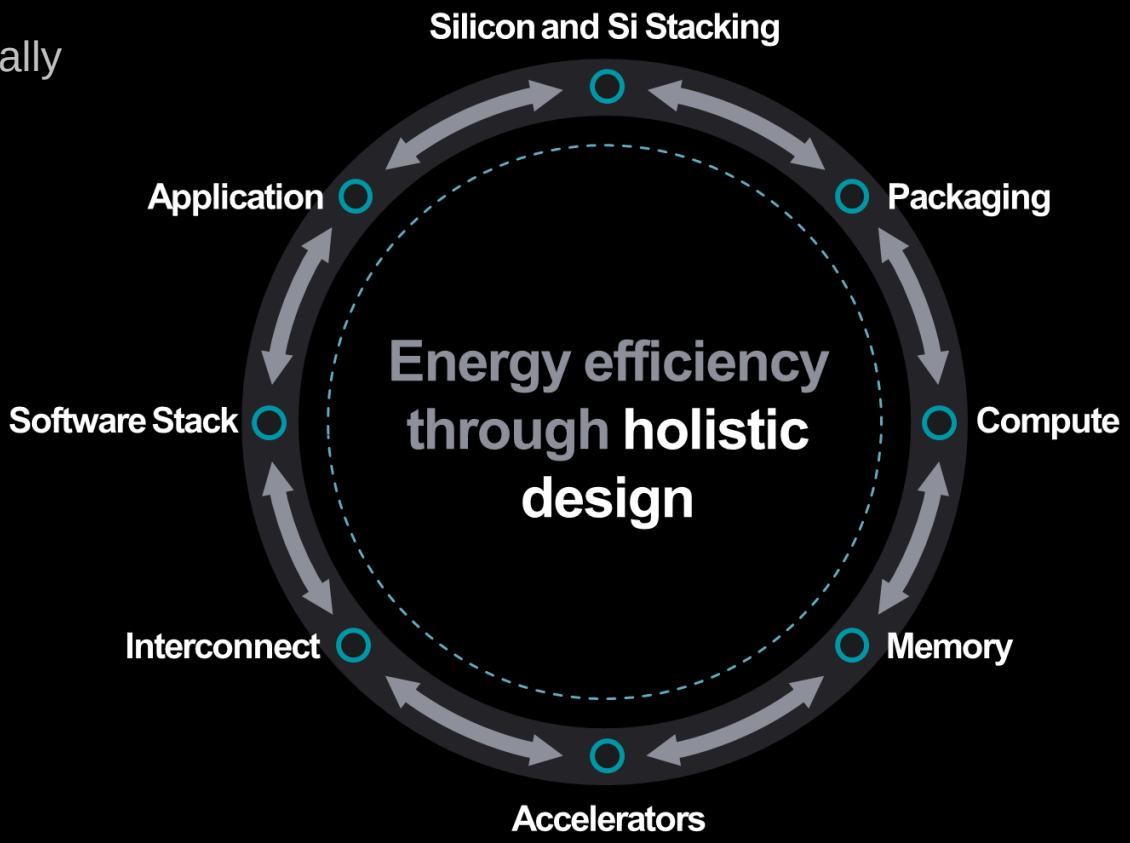
Energy efficiency requires holistic innovation

- Energy efficiency is the primary limiter. We must innovate in new dimensions:
  - System-level optimizations; Domain-specific heterogeneous architecture
  - Tight integration of compute and memory with chiplet architectures, advanced packaging, new interconnects
  - Leveraging AI holistically



Hardware

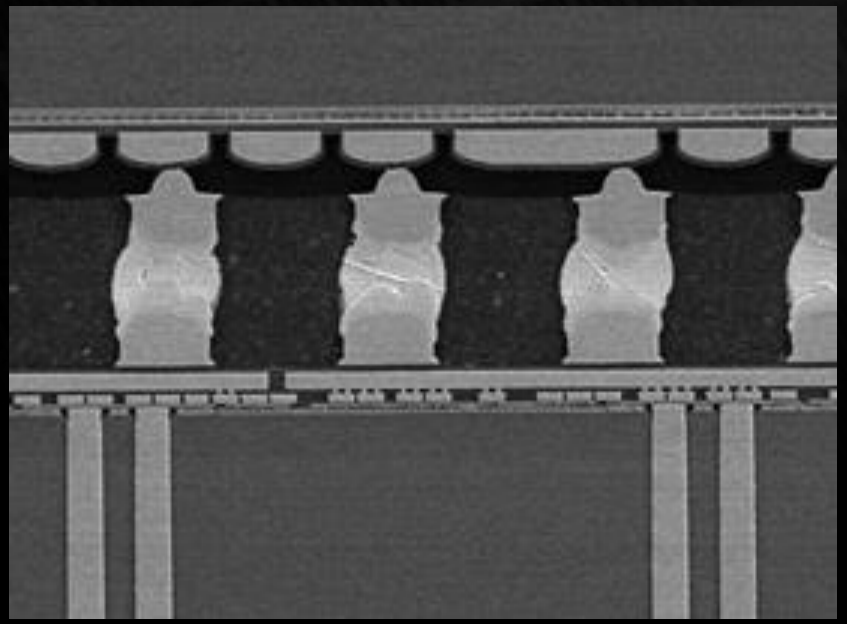
Software and Applications

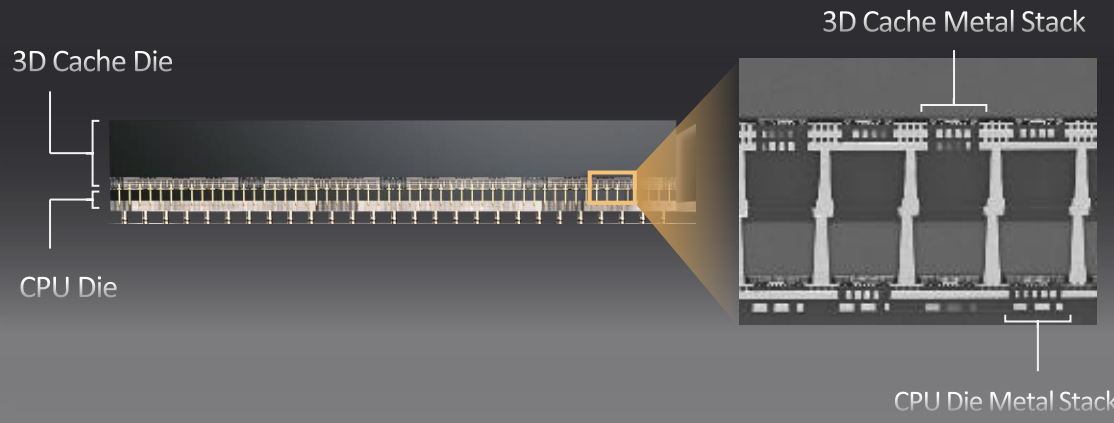


3D ARCHITECTURES

HYBRID BONDING DRIVING MOORE'S LAW SCALING

Other 3D Architectures





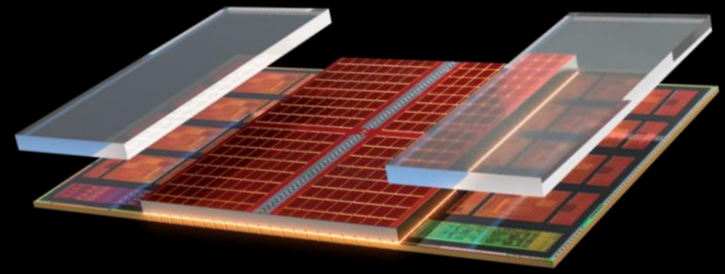
3D Hybrid Bonding

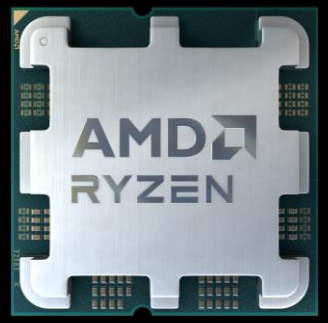
> 3X
Interconnect Energy Efficiency
Compared to Micro Bump 3D

> 15X
Interconnect Density
Compared to Micro Bump 3D

Based on AMD engineering internal analysis, May 2021 See endnotes.

AMD RYZEN™ 7 7800X3D



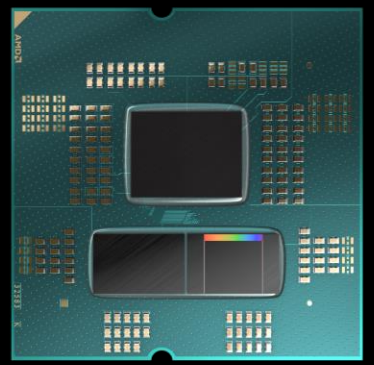


up to	up to	up to	
8 Cores 16 Threads	5.0 GHz Boost	104 MB L2+L3 Cache	120W+ TDP

ZEN 4 **Processor architecture** 5nm **Technology**

AMD RYZEN™ 9 7950X3D

Ultimate processor for gamers and creators



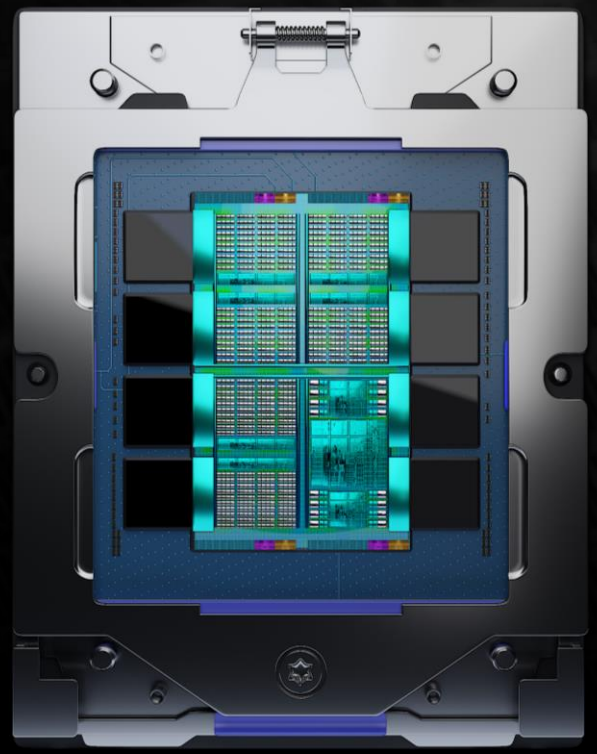
up to	up to	up to	
16 Cores 32 Threads	5.7 GHz Boost	144 MB L2+L3 Cache	120W TDP

ZEN 4 **Processor architecture** 5nm **Technology**

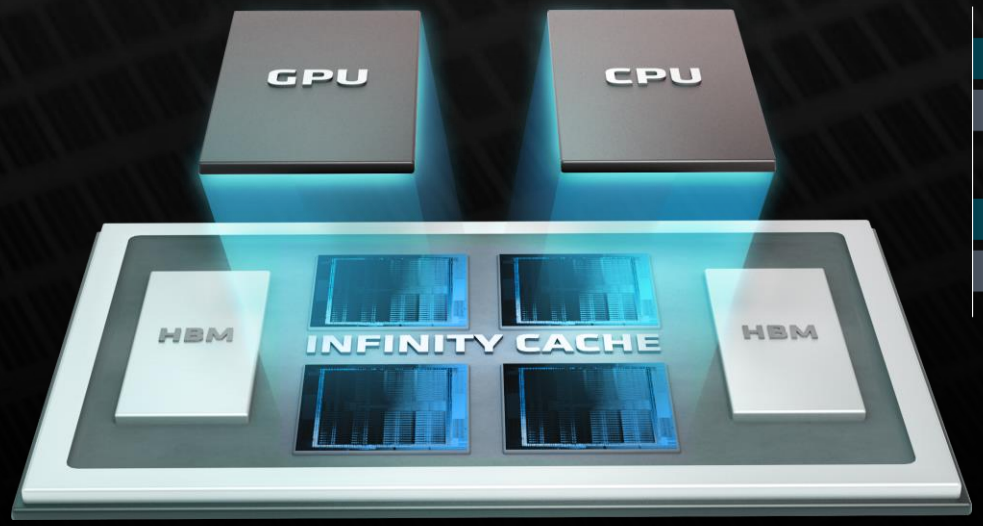
See endnotes R5K-107, GD-150, RPL-041

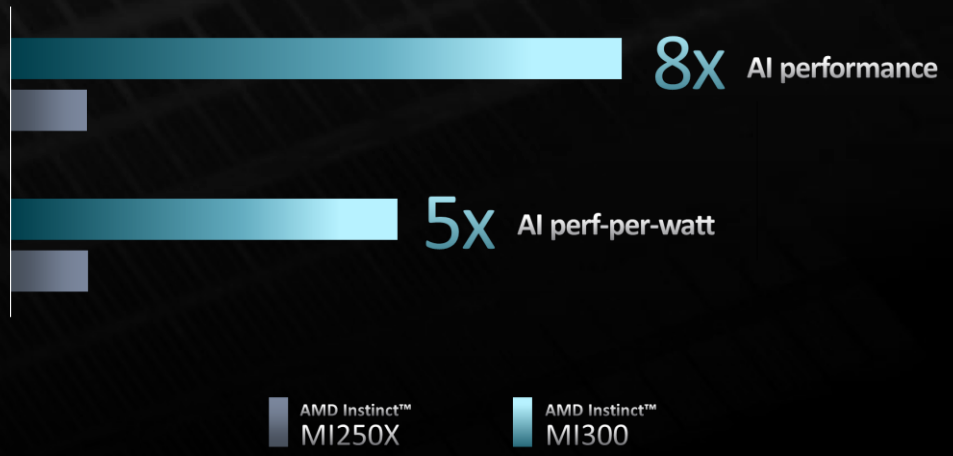
AMD INSTINCT™ MI300

The world's first data center integrated CPU + GPU



AMD CDNA™ 3 Unified Memory APU Architecture





146B
Transistors

128GB
HBM3

AMD CDNA 3 Next-Gen Accelerator Architecture

ZEN 4 24 Leadership Data Center CPU cores

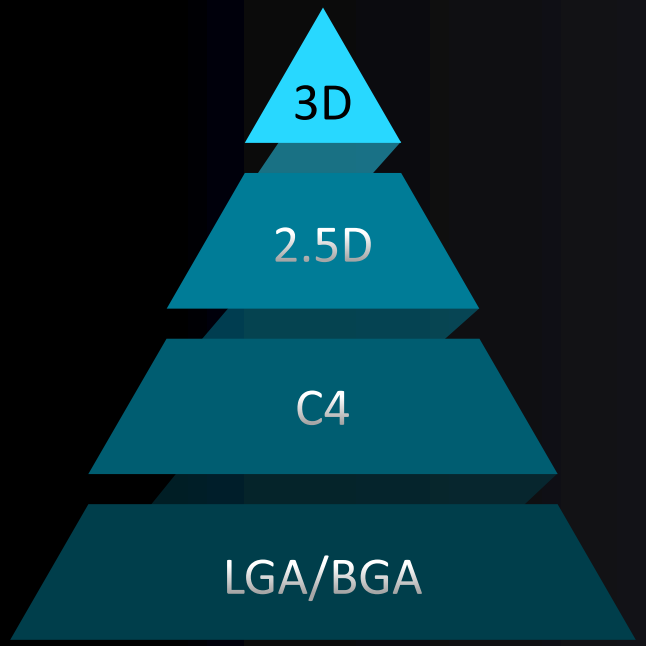
Enabled By

3D

Advanced Chiplet Packaging

See Endnote MI300-03

DESIGN AUTOMATION OPPORTUNITIES



3DIC Stack Construction Efficiency and Cycle time

3DIC Thermal Analyses for early feedback

3DIC Static EMIR analyses for early feedback

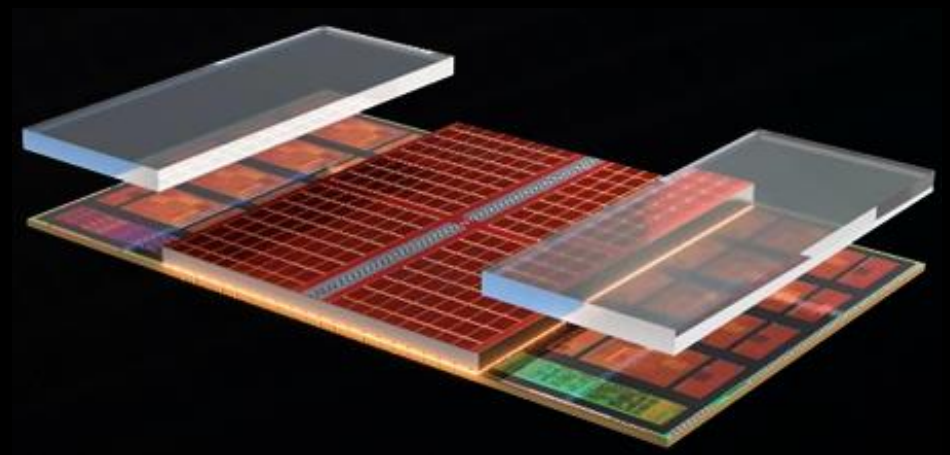
Si interposer/ Fanout D2D/HBM routing

MULTI-SCALE DESIGN/PROCESS OPTIMIZATION NEEDED TO MANAGE WARPAGE AND INTERCONNECT RELIABILITY

NEXT GEN 3D ARCH REQUIRES NEXT GEN EDA TOOLS

1) STANDARDIZE DRC TOOL SET

DRC decks spanning all design components in 2.5D/3D architectures



2) ENABLE TRUE SILICON-PACAKGE CO-DESIGN

Proliferate common tool platform across silicon and package designs

3) STANDARDIZE FILE FORMATS

Create a seamless tool-to-tool interaction from design to analysis

4) INCREASE TOOL CAPACITY

EDA tools to stay lockstep with design pin count increases

EDA TOOL ECOSYSTEM NEEDS TO MERGE SILICON AND PACKAGE TOOLCHAINS

FUTURE OF 3D STACKING

TSV Pitch

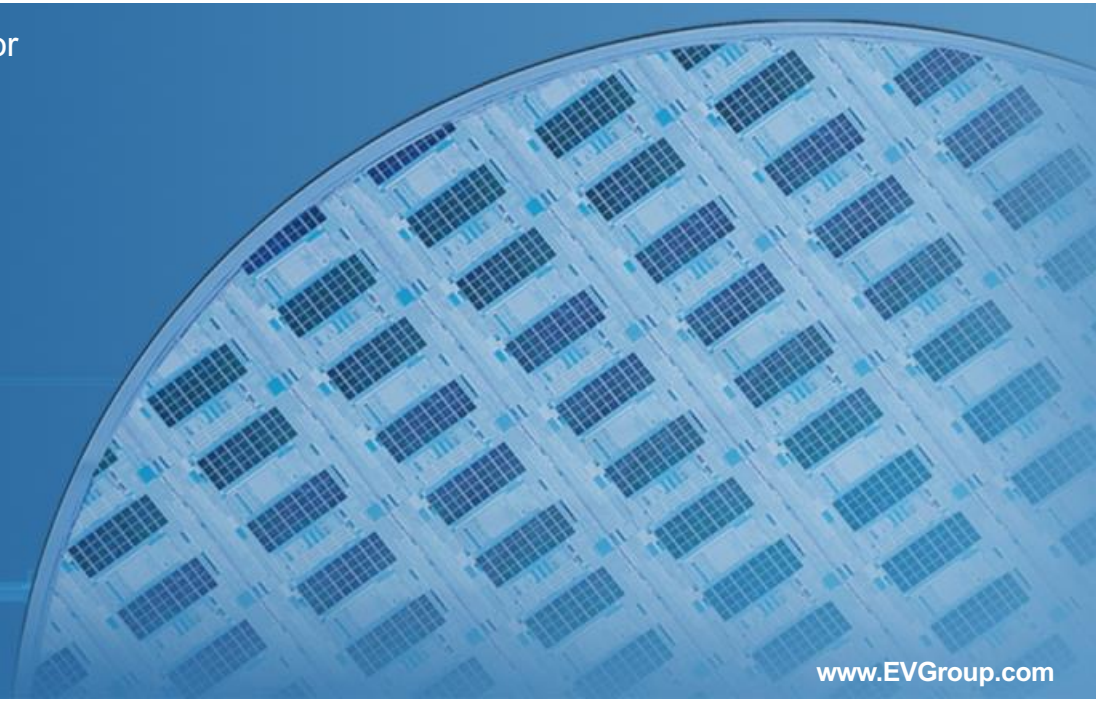
FULL DIE-TO-DIE | IP ON IP | MACRO IN MACRO | IP FOLDING/SPLITTING | CIRCUIT SLICING

ADVANCED PACKAGING CAN ENABLE INTEGRATION SCHEMES
NOT POSSIBLE WITH MONOLITHIC DESIGNS

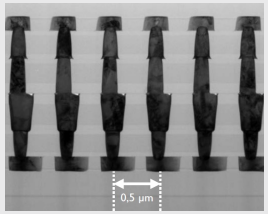
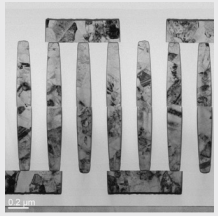
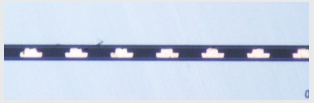
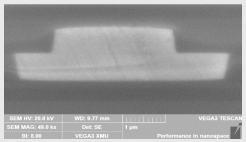
2023 ECTC Panel Discussion

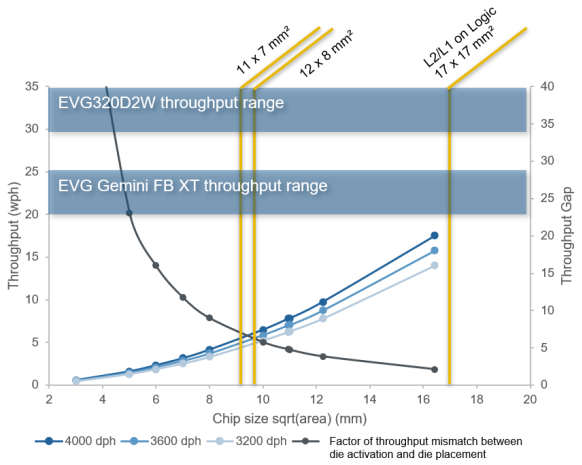
D2W Considerations

Dr. Thomas Uhrmann | Business Development Director



D2W vs W2W Hybrid Bonding

	Hybrid W2W Bonding	Hybrid D2W Bonding
Maturity	Wafer Bonding Equipment and Process are matured since 2010	Process and Equipment maturity is starting to yield but still many difficulties
Contact Pitch	<1µm pitch in production <500nm in development  	Currently 9µm pitch in production Roadmap for 2023: 2µm  
Equipment Capability	Alignment: <50nm (3s) Post Bond Overlay: <75nm (3s)	Alignment: <150nm Post Bond Overlay: ~350nm
Die Size	Die Size and Grid Matching required	No limitations in die size and system segmentation
Segmentation	Each bonding layer consist of one node	Each chiplet can consist of a different node
Yield	Cumulative yield of each bonded layer	Cumulative yield can be avoided by testing
Throughput	>25 bonds per hour	Related to chip size and amount of chiplets per system



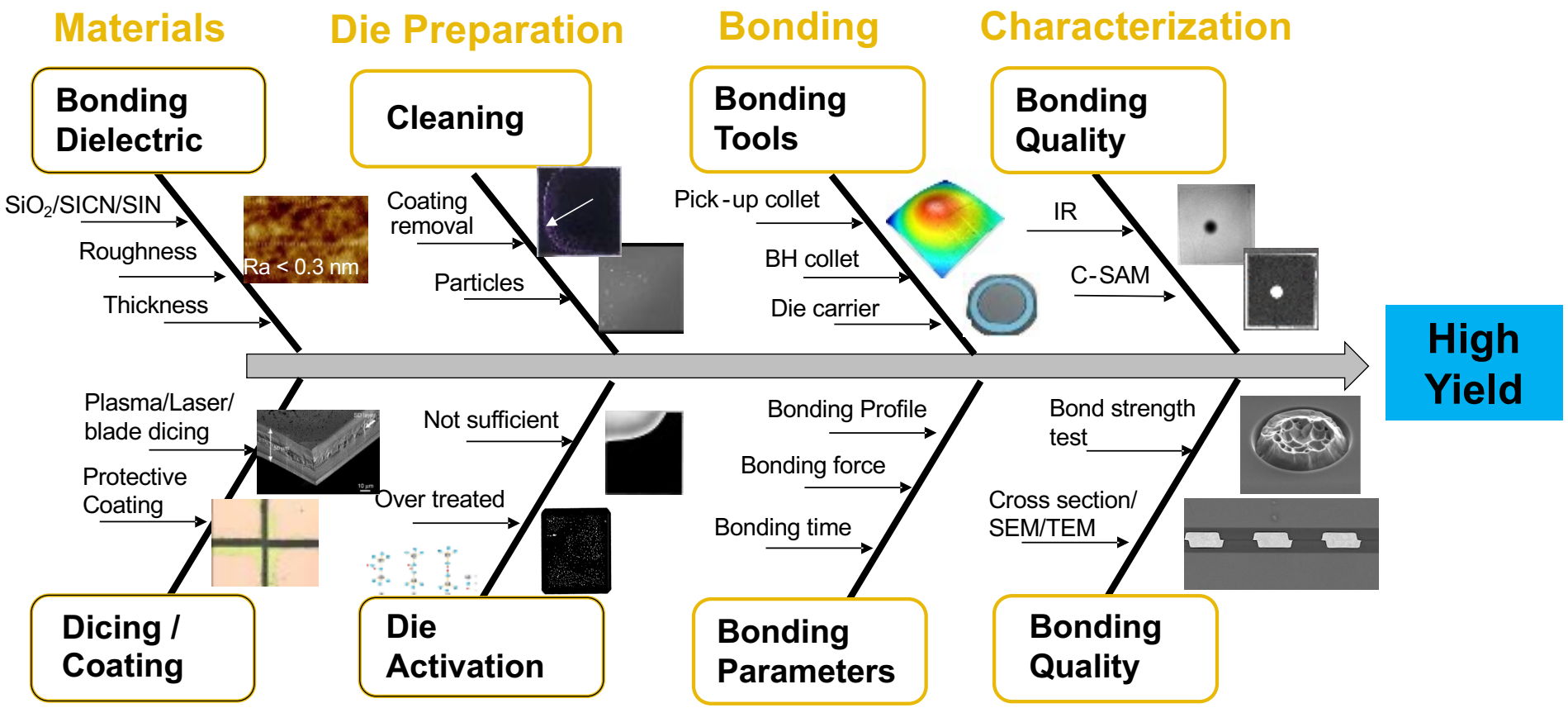
- Direct placement throughput matching is impossible to achieve, as pre-processing and die placement show a throughput difference between 2x to 10x for standard die sizes
- For small dies of less than 6x6mm² D2W bonding cost is strongly increasing
- W2W bonding can offer improved cost / yield ratio

D2W Hybrid Bonding | Many ways to succeed…

	Co-D2W	Reconstructed W2W	DP-D2W	SA-D2W
Transfer Method	Collective Bonding (Die Level Bonding)	Reconstructed W2W (Anorganic Fill Process)	Direct placement of activated dies using Flip Chip Bonder	Self Assembly on hydrophilic guiding pads
Pro's	• Proven technology • Die Activation and cleaning equivalent to W2W hybrid bonding • Oxide management • Rework on carrier feasible	• Proven process • High yield, clean process • All based on standardized wafer-based manufacturing equipment	• Versatile method • Die thickness invariant	• Avoids high precision flip chip bonder and potential cost saving • Die thickness invariant
Con's	• Error propagation of D2W + W2W alignment • Cost of carrier prep, utilization and clean • Die thickness needs to be in narrow range	• W2W bonding process is heavily impacted by die grid and filling factor between dies	• Bonding interface needs to be touched • Die handling especially for multi die stacks such as SRAM, DRAM • Particle management during die placement	• High precision die preparation using chemical treated zones • Dicing potentially affects placement • Die strain is affecting self alignment results
Maturity	Limited volume production proven for several years	Limited volume production	Limited volume production	Experimental results available, Feasibility testing ongoing

Combination of known good dies on carrier with anorganic wafer level pre processing, post processing and W2W bonding

D2W Hybrid Bonding | Process Considerations



Source: ASMPT / EVG Paper "Direct Die to Wafer Cu Hybrid Bonding for Volume Production" – Session 3

SYNOPSYS®

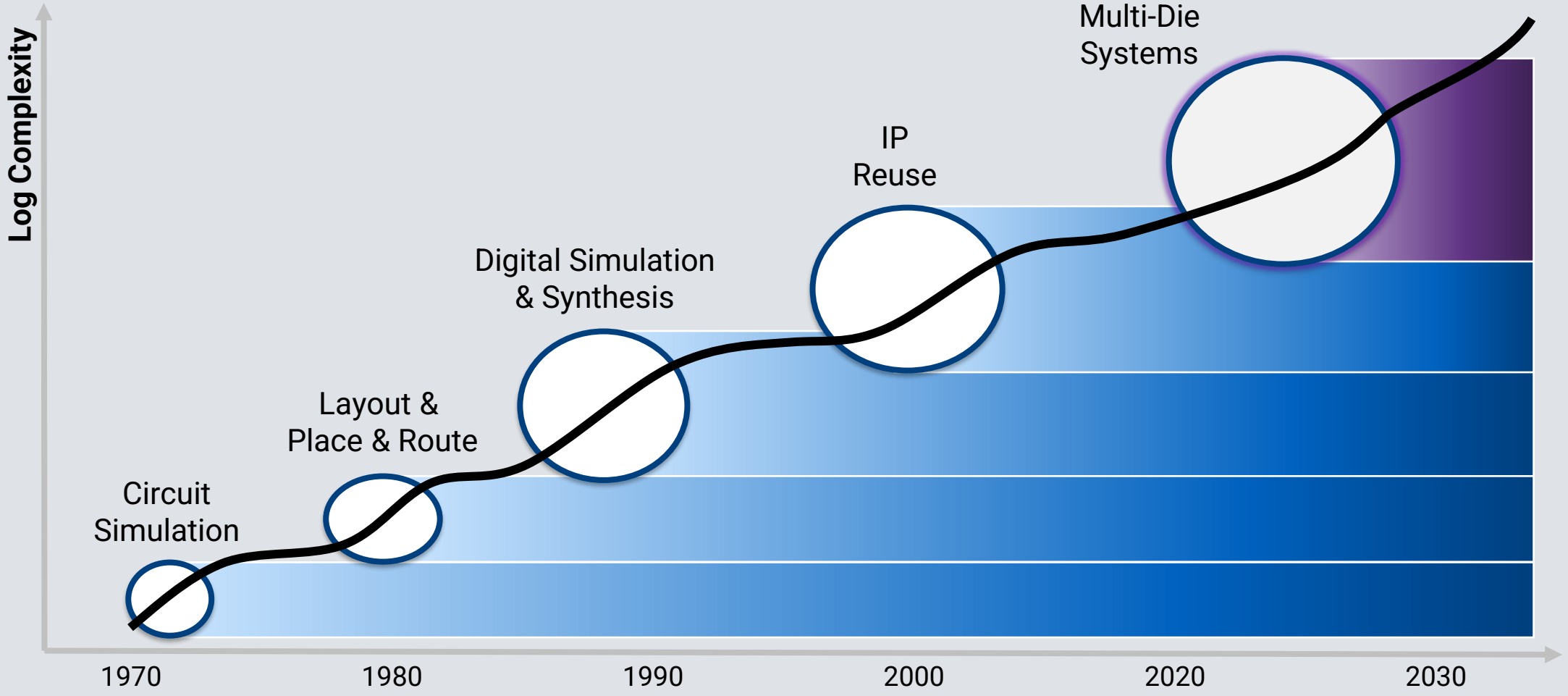
C2W Cu Hybrid Bonding

Design and EDA Perspective

Abhijeet Chakraborty, VP Engineering, Synopsys Inc

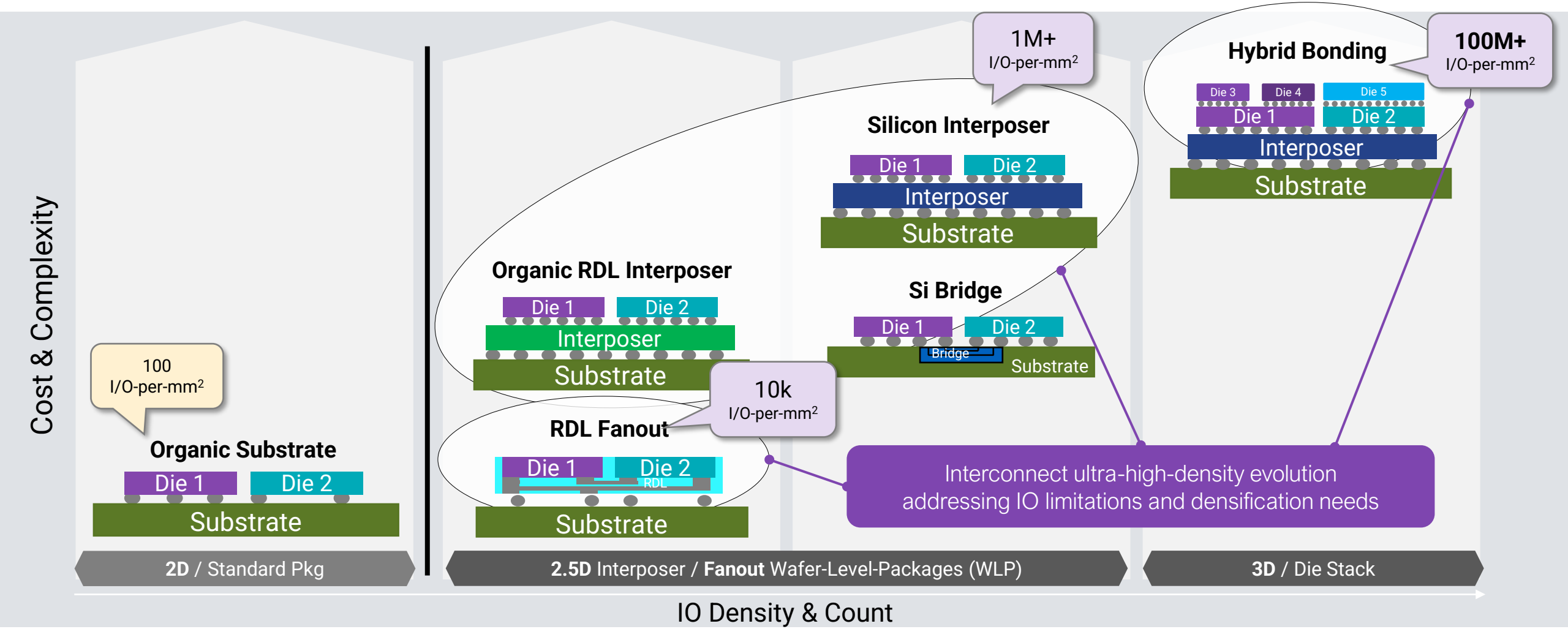
May 30, 2023

Semiconductor Design Productivity Waves



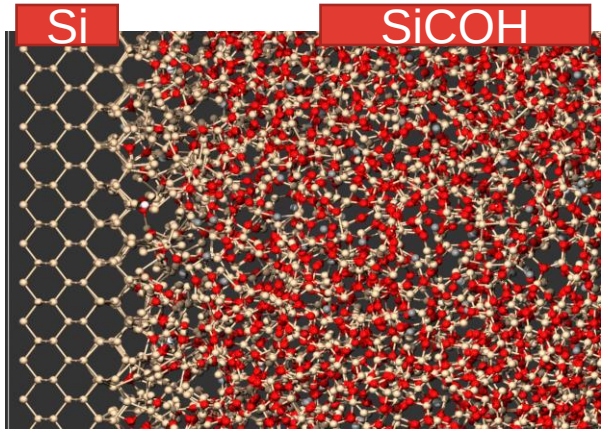
System Optimization

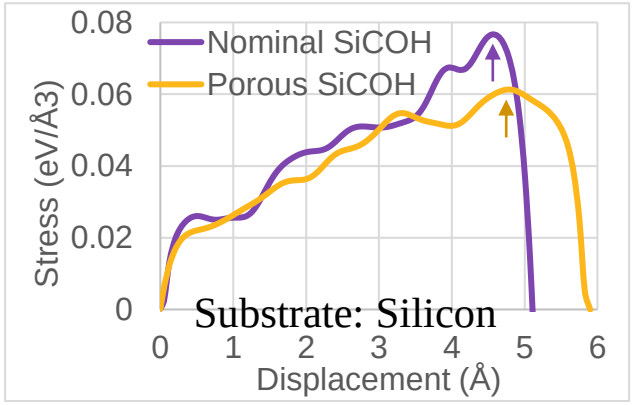
Choice is driven by power/performance/form-factor/cost/time



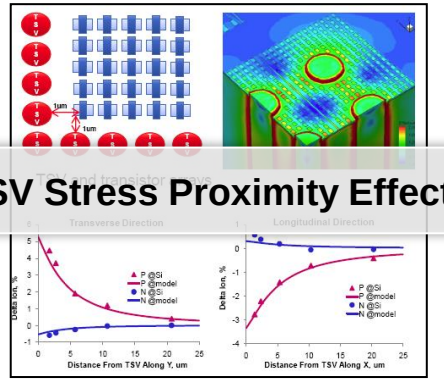
Multi-Domain, Multi-Physics Analysis

Mechanical Reliability

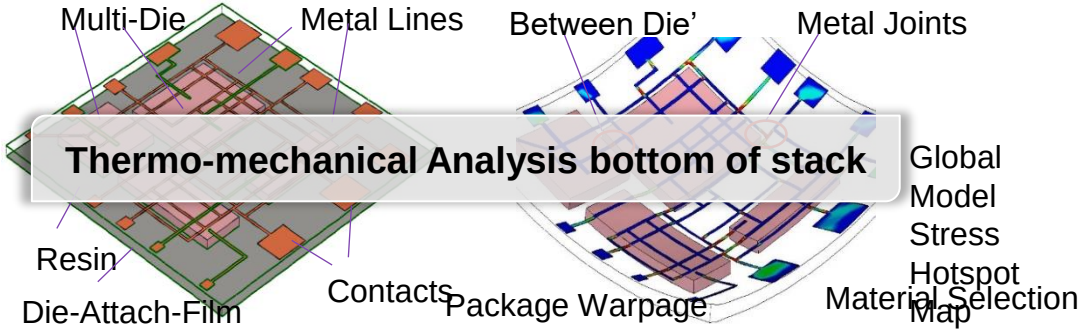




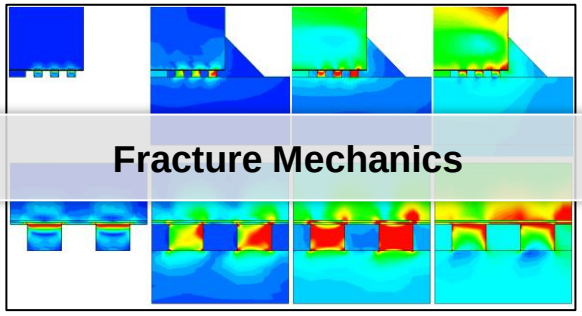
The interface bonding strength between a substrate and a complex material system, such as SiCOH, can be analyzed by molecular dynamics method with Synopsys QuantumATK



TSV Stress Proximity Effects



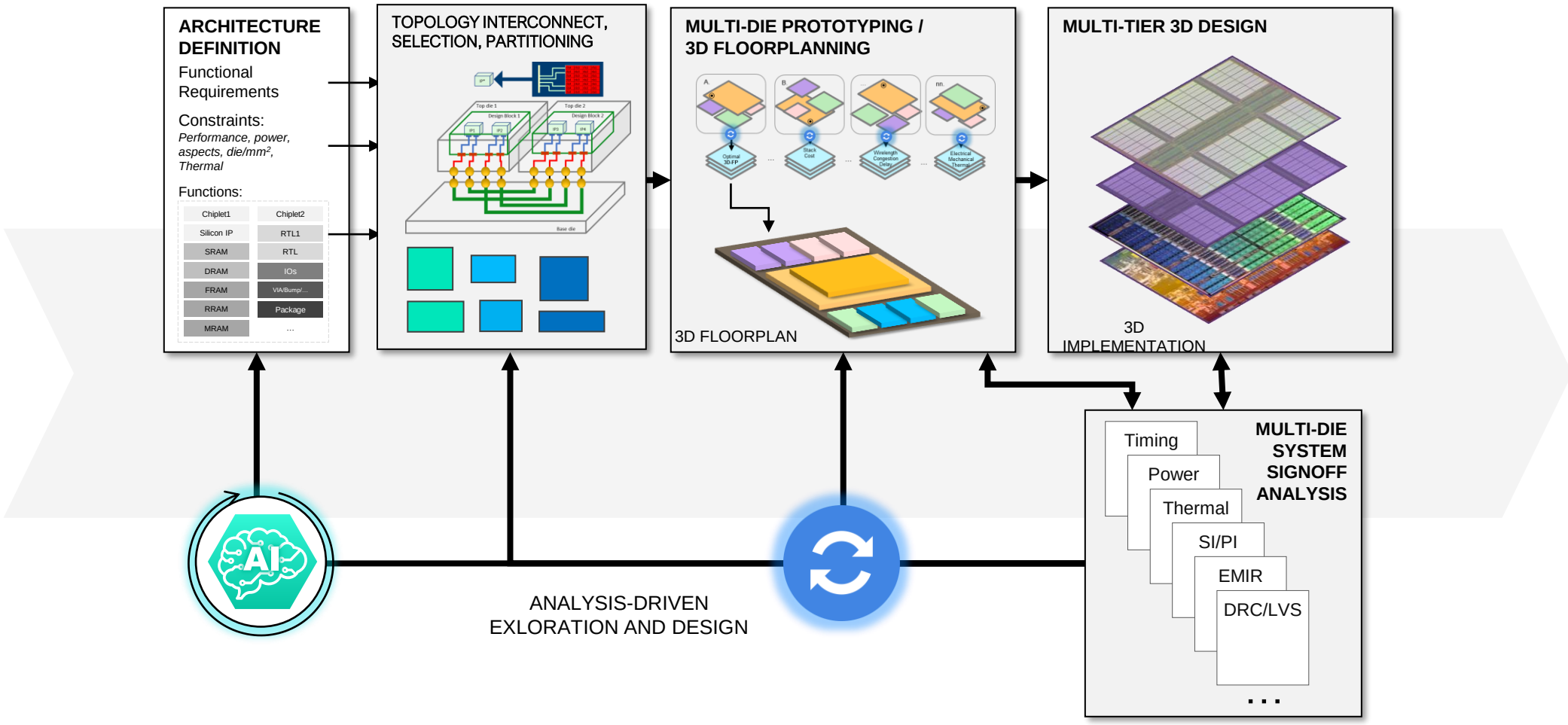
Thermo-mechanical Analysis bottom of stack



Fracture Mechanics

Scalable Design Closure

Addressing massive systemic complexity of heterogeneous system

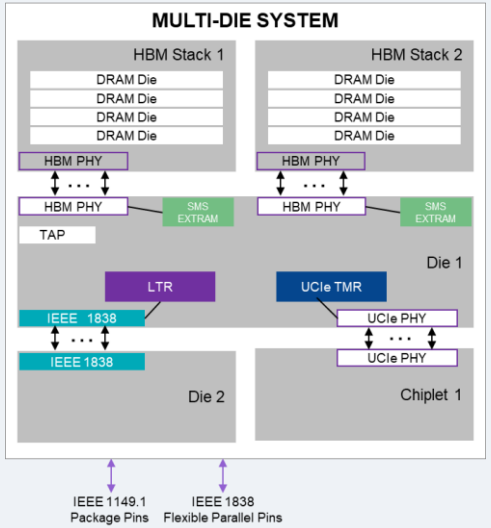


Manufacturing Ramp and Product Reliability

Synopsys' TestMAX and the SLM Family of products

Multi-Die System Test & Repair

Product Quality (KGD, Package, System)



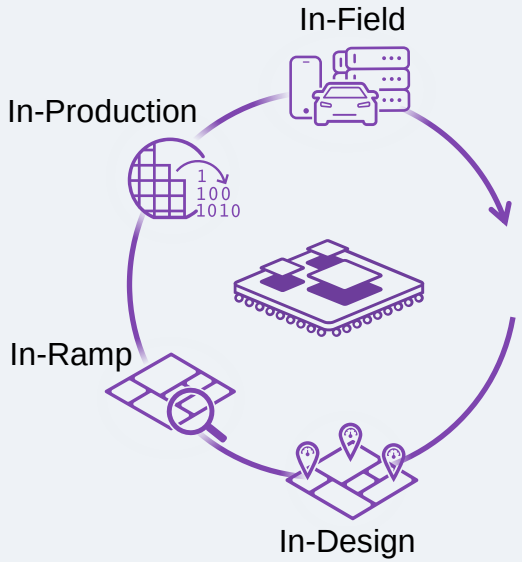
Ensure quality with comprehensive test, debug, repair for multi-die systems

Integrated Test for:
Multiple Dies, Memories, Interconnects, and Full-system

Test Access	Logic-to-Logic	Logic-to-Memory	Via / Bump / Interconnect
IEEE 1838	PHY Monitor, Test & Repair	Ext. Memory BIST & Repair	High volume Lane Test & Repair

Silicon Lifecycle Management E

Reliability, Yield, Health



Enhance multi-die system operational metrics through environmental, structural, functional monitoring

Solution Comprises:
Silicon IP, EDA Software, and Analytics Insights

In-Design	In-Ramp	In-Production	In-Field
Power/ Performance Optimization	Yield, Failure Analysis	Volume Test, Quality and Traceability	Optimization, Safety, Security, Maintenance

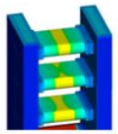
STCO For Design And Process Optimization

Design Kits for Multi-Die Systems

DTCO
Design Technology Co-Optimization

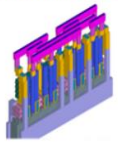
Materials, devices, process integration w
Sentaurus TCAD

Transistor



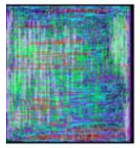
- FinFET
- GAA
- CFET …

Standard cell



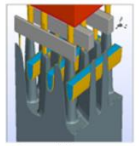
- Fin depopulation
- Std cell height
- BS-PDN

Chip



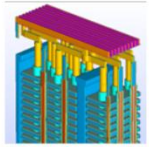
- PPAC eval

DRAM



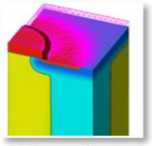
- Scaling
- Sensing margin
- tREF

3D NAND



- Stacking
- QLC, PLC
- Reliability

Power / RF

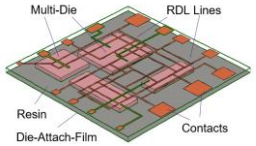


- Transistor
- Module
- R_{on} vs. V_b
- P_o vs. f

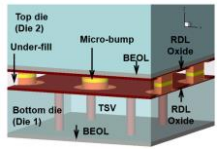
PTCO
Package Technology Co-Optimization

Substrates, devices, package integration w
Sentaurus Interconnect

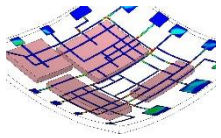
Materials



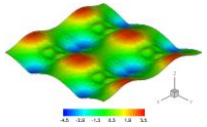
Via, Bump scaling



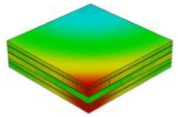
Spacing/Density



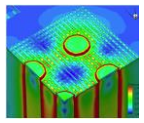
Mobility / KOZ



CTE Mismatch



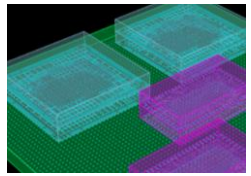
Array Density



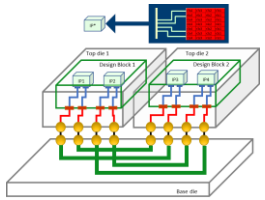
STCO
System Technology Co-Optimization

Architectures, devices, system integration w
3DIC Compiler

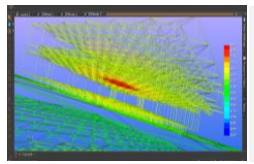
3D Stack / Multi-Die Pkg



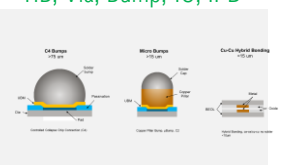
Interconnect Topology and cut assessment



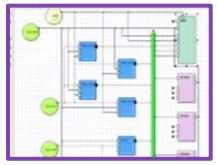
Thermal / Warp / Stress

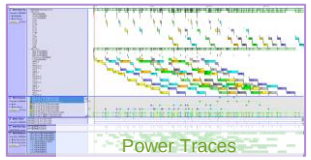


HB, Via, Bump, IO, IPD



Functional aspect



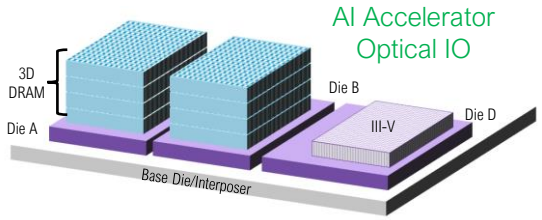


3DHI Design Kit
Heterogeneous Integration

System PDKs (Die/Pkg), Design Rules, Ref. Designs, Flow and Collaterals

Rapid Prototyping and Evaluation

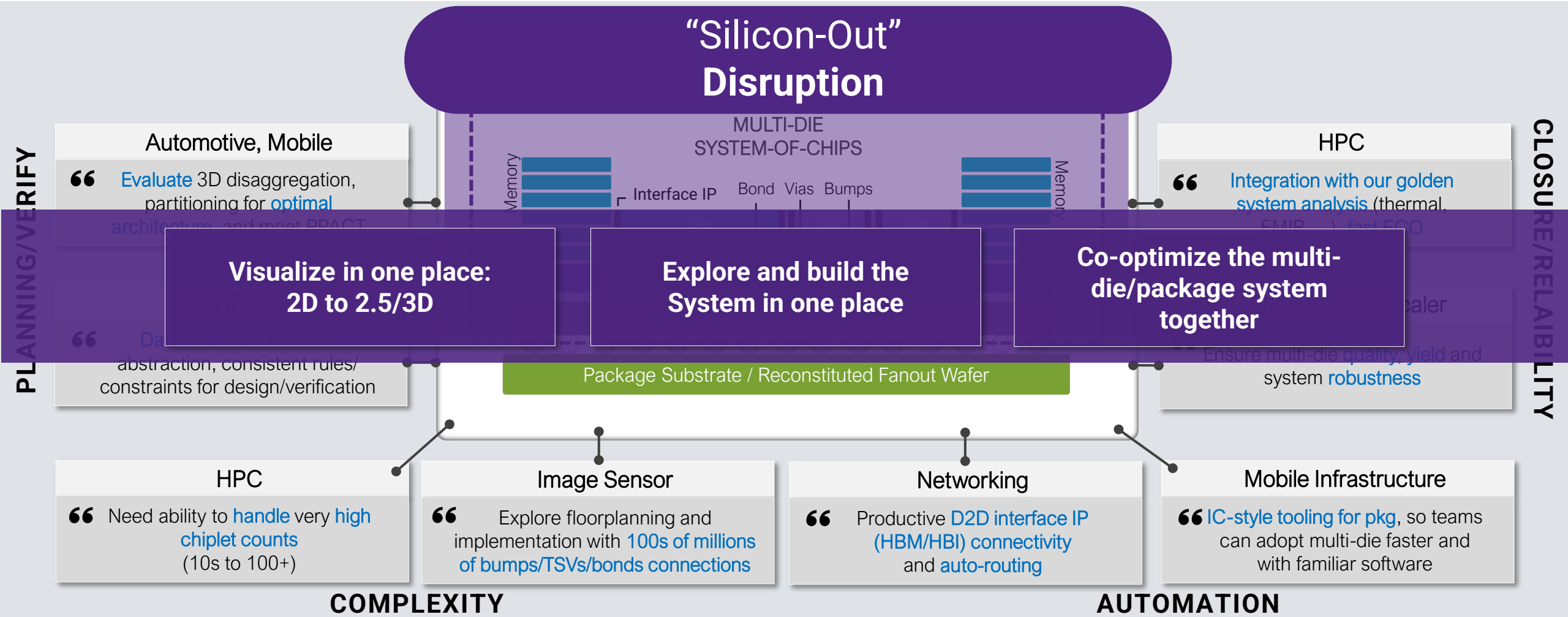
- 3D Stacking and multi-die packaging
- System interconnect scaling
- Package materials



Unified delivery of 3DHI Design Kit

- Package tech files, Via, Bump, IO libs
- Interconnects/interposer L/S DR,ER
- Multi-layer / build-up substrate
- MDXF system design and assembly rules
- Multiphysics models, D2D and I/F IP
- Templates

C2W Cu Hybrid Bonding: Opportunities and Challenges



Thank You