The Future of High-density Substrates – Towards Submicron Technology

Tuesday, May 30, 2023, 7:45 p.m. – 9:15 p.m.

Chairs: Takashi Hisada (IBM) and Yasumitsu Orii (Rapidus)

We cordially thank our Special Session sponsor

Chair
Takashi Hisada
IBM

Chair
Yasumitsu Orii
Rapidus

Panelist
Yasushi Araki
Shinko

Panelist
Yu-Hua Chen
Unimicron

Panelist
Satoru Kuramochi
Dai Nippon Printing (DNP)

Panelist
Madhavan Swaminathan
Pennsylvania State University

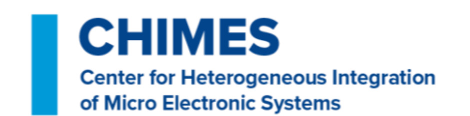
Panelist
Griselda Bonilla
IBM

The Future of High-density Substrates – Towards Submicron Technology

Chiplets and Heterogeneous Integration (HI) technologies are expected to drive performance and efficiency enhancement of semiconductor modules while Si scaling is slowing down. One of the key attributes of chiplets and HI technologies is the bandwidth of interconnection between chips within the same package. A very short-distance and high-density interconnection from one chip to another enables high-speed data transmission with low energy loss. High-density chip carrier substrate is the core technology driving the evolution of chiplets and HI technologies.
In this session, we will discuss ultra-fine-pitch substrate technologies towards submicron ground rule for Chiplets and Heterogeneous Integration.

High Density Glass Substrates for Heterogeneous Integration

Madhavan Swaminathan
Dept. Head Electrical Engineering
William E. Leonhard Endowed Chair
Director, CHIMES (an SRC JUMP 2.0 Center)
The Pennsylvania State University
Emeritus Professor, ECE & MSE, Georgia Tech
Former Director, 3D Systems Packaging Research Center (NSF-ERC), Georgia Tech



Heterogeneous Integration Options (2D/2.5D/3D)

2D/2.5D integration	Silicon			Organic		Glass Interposer (Mukhopadhyay, et al. '19)
	TSV Interposer (Martwick, et al, 2016)	Si Bridge (EMIB) (Mahajan, et al, 2019)	Silicon IF (Jangam, et al, 2018)	Organic Interposer (Turner, et al, 18)	Chip-last Fanout (Wang, et al 2019)	
Status	Commercial	Commercial	Research	Commercial	Development	Research
Dielectric constant	3.9	3.9*	3.9	3.0*	3.2	2.5-3.0
IO pitch	50 µm	45 µm	10 µm	55 µm	40	55 µm
Interconnect length	5 mm	5 mm	0.5 mm	6 mm	1 mm	2.5 mm
Interconnect density	250 IO/mm/layer	300 IO/mm/layer	n/a	25 IO/mm/layer	500 IO/mm/layer	250 IO/mm/layer
V_{swing}	1.2 V	1 V	1 V	0.15 V	1 V	1 V
$R_{on}/C_{Tx}/C_{Rx}$ (Ω/F/F)	39/0.4p/0.4p	50/0.5p/0.5p	30/50f/50f	n/a	50/0.4pF/0.4pF	30/0.3pF/0.3pF
Data rate/IO	2 Gbps	5 Gbps	4.21 Gbps	20 Gbps	9.5 Gbps	9.2 Gbps
Bandwidth density	500 Gbps/mm	1500 Gbps/mm	1300 Gbps/mm	500 Gbps/mm*	4750 Gbps/mm	2300 Gbps/mm
Energy-per-bit	1.025 pJ/bit*	1.2* pJ/bit	0.4 pJ/bit	0.58 pJ/bit	0.78 pJ/bit*	0.36 pJ/bit

Derived metric

3D Integration	TSV-based		Non-TSV
	3D IC /w TSV [Zhang, et al. '18]	Hybrid Bonding [Chen, et al, '19]	3D Glass Embedding [Ravichandran, et al, '19]
Status	Commercial	Commercial	Research
Dielectric Constant	3.9*	3.9*	2.5-3
IO pitch	40 µm	10 µm	20 µm
Interconnect length	75 µm*	50 µm*	35-50 µm
Interconnect density (IO/mm^2)	625	10000	2500
V_{swing}	0.7 V*	1 V*	1 V
$R_{on}/C_{Tx}/C_{Rx}$ (Ω/F/F)	n/a	n/a	50/50f/50f
Data rate/IO	1.69 Gbps	n/a	1.86 Gbps
Bandwidth density	1.76 $Tbps/mm^2$*	n/a	4.65 $Tbps/mm^2$
Energy-per-bit	76.2 fJ/bit	7 fJ/bit*	11.2 fJ/bit

Derived metric

- ❑ Energy-per-bit (EPB) an important metric to achieve energy efficiencies.
- ❑ Bandwidth density needs to scale to enable communication between logic & memory.
- ❑ Both 2D & 3D Integration necessary for HI.

S. Ravichandran and M. Swaminathan, Chip Scale Review (2022)

Embedded Die Glass Substrates

Disaggregation & Reaggregation of dies

placement

Logic 1

Logic 2

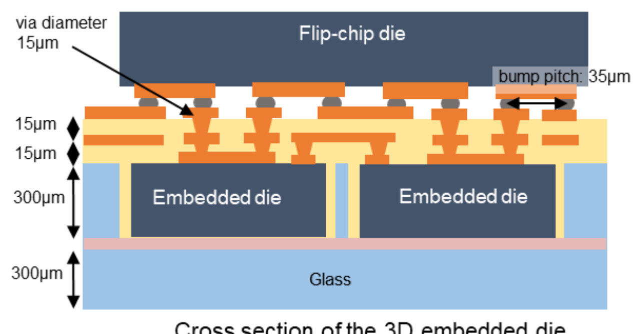
Mem 2

TOP

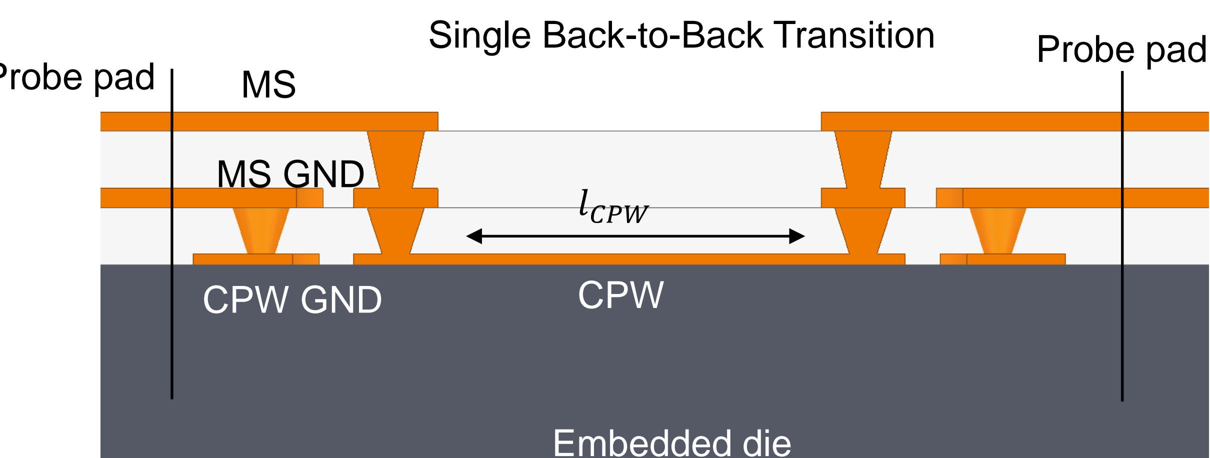
BOT

routing

3D (glass Interposer)



Cross section of the 3D embedded die with die-to-die interconnects

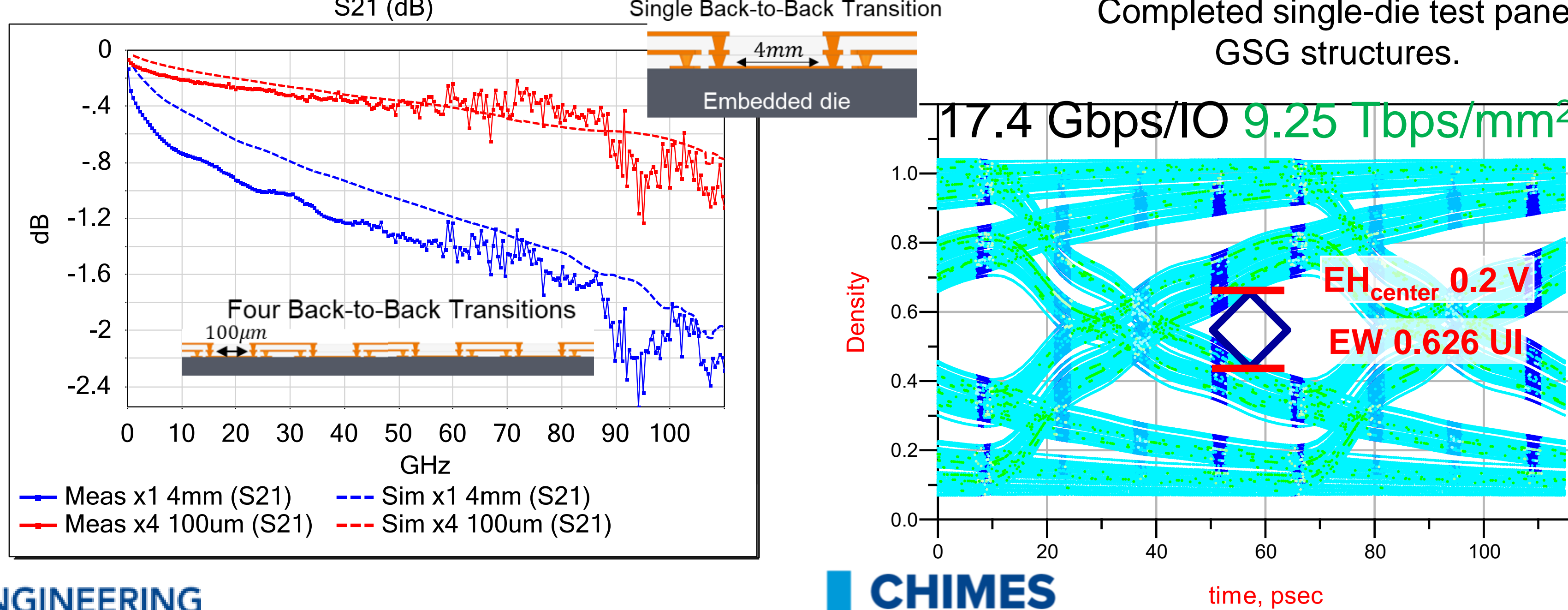


Georgia Tech PACKAGING RESEARCH CENTER

6.1 mm

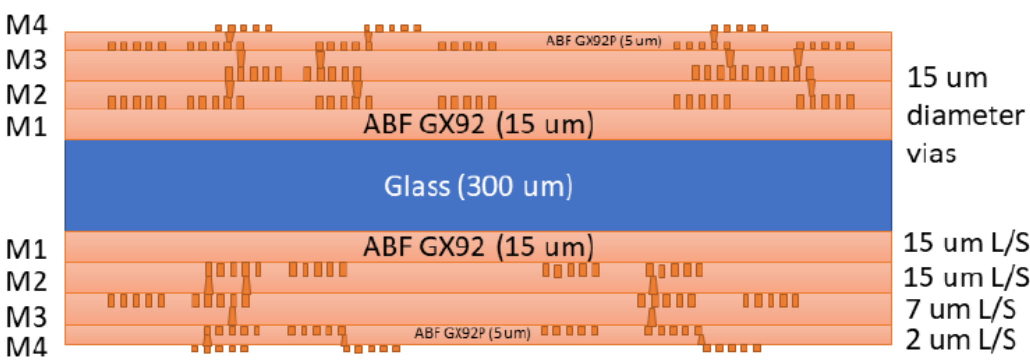
6.1 mm

Completed single-die test panel GSG structures.



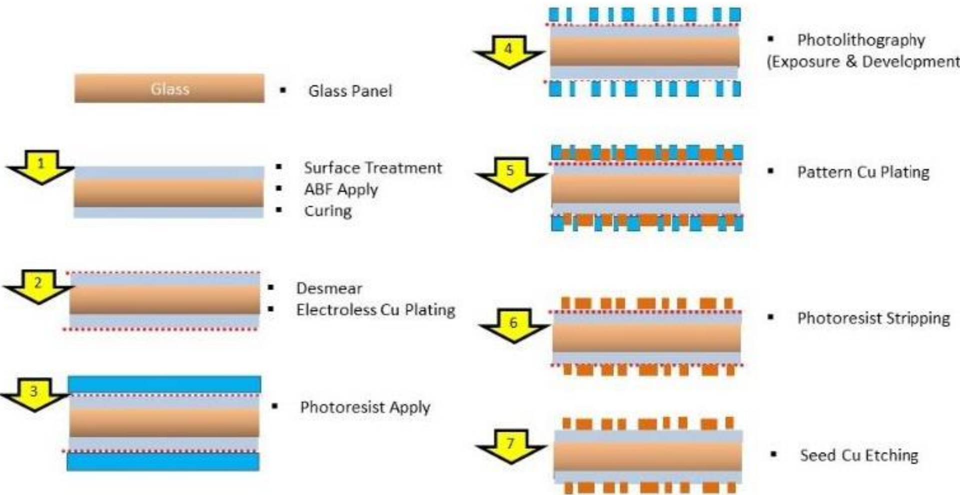
Courtesy: E. Erdogan, GT-PRC

Eight Metal Layer Process for Glass Substrates



15 um diameter vias

15 um L/S
15 um L/S
7 um L/S
2 um L/S



Christopher Blancher, Mohanalingam Kathaperumal, Fuhan Liu, and Madhavan Swaminathan, ECTC 2023

Fig. 3. 15 µm L/S on M1 of 8ML panel

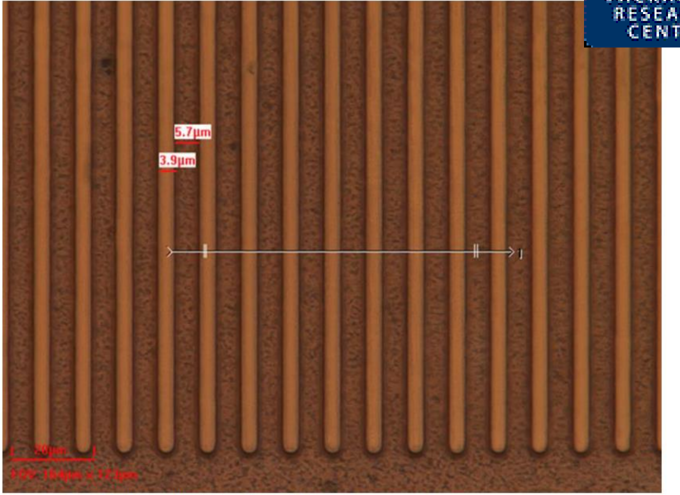


Fig. 5. 5 µm half-pitch wiring from M3

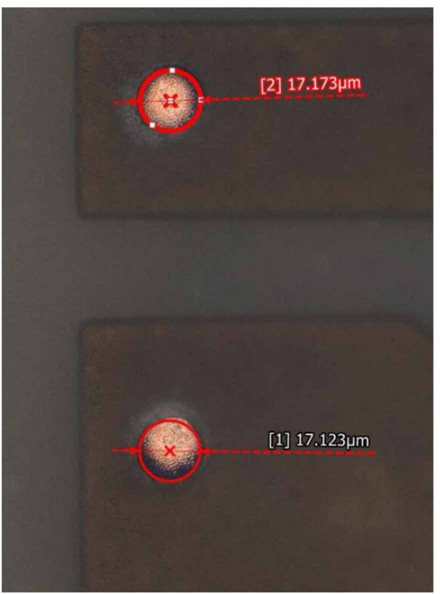


Fig. 4. Microvias from M2 to M1 on 8ML panel

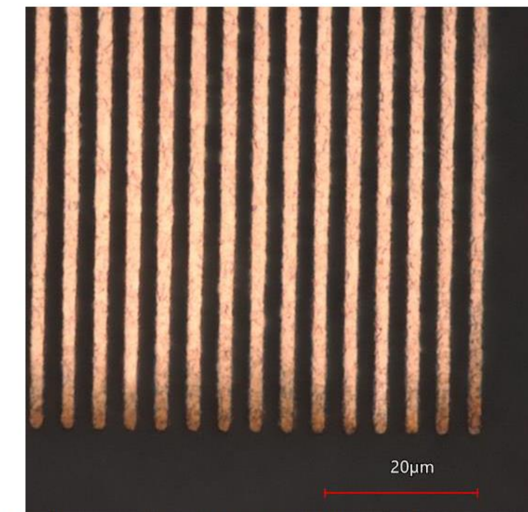
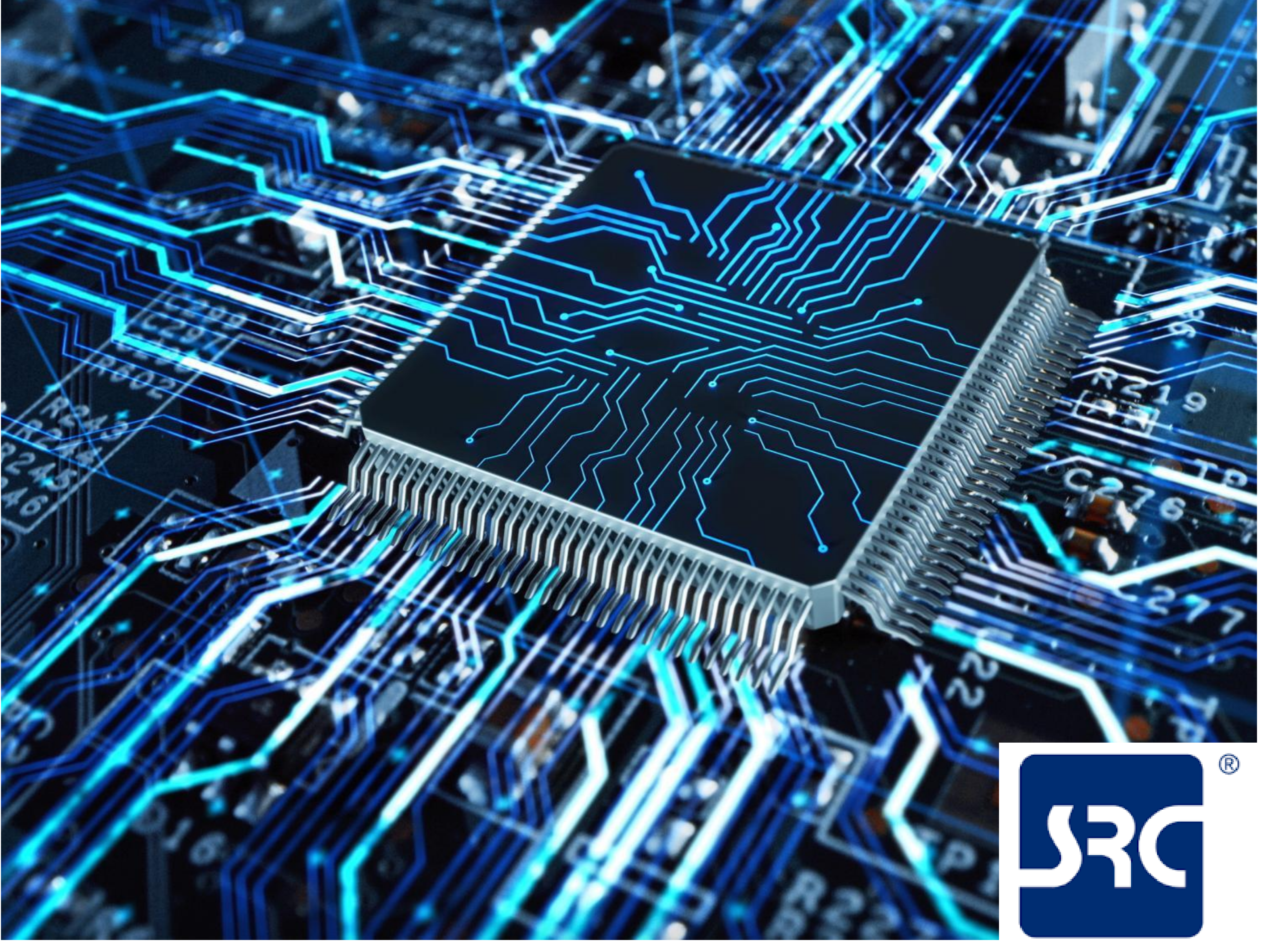


Fig. 6. Optical image of 2 µm L/S after seed layer etch

JUMP 2.0 Center @ Penn State (14 Univ. Partners)

Penn State leads semiconductor packaging, heterogeneous integration center



- Center for Heterogeneous Integration of Micro Electronic Systems (CHIMES)
- Supported by the Semiconductor Research Corporation (SRC)'s Joint University Microelectronics Program 2.0 (JUMP 2.0), a consortium of industrial partners in cooperation with the Defense Advanced Research Projects Agency (DARPA)

https://www.psu.edu/news/engineering/story/penn-state-leads-semiconductor-packaging-heterogeneous-integration-center/

Ultra-dense Heterogeneous Integration Platform – A Futuristic Outlook

1 & 7 **IC PARALLELISM ICS FOR HI INTEGRATION**

- Blurred on-chip vs. off-chip connectivity
- Metallic Fine pitch wires & in-fill dielectrics
- 100nm fine-pitch chiplets alignment
- Massive memory access of DRAM and PIMs

5 **RECONFIGURABLE CIRCUITS & AI ACCELERATORS**

- Fourier-Theorem Convolution Ops
- ps MAC Ops
- Zero-power Multiplication
- Algorithm-hardware Co-Design
- Co-packaged laser

4 **PHOTONIC/OPTIC INTER/INTRA ICS**

- Vertical optical TSVs
- Adiabatic coupling
- M3D Connectivity

3 **RF/MM-WAVE**

- RF-Electronic integration
- Massive 2D Arrays
- IoT-relevant THz freq

6 **ACTIVE & PASSIVE DEVICES FOR HETEROGENEOUS INTEGRATION**

- Emerging materials for photonic ICs
- Low-loss Waveguides and WDM filter
- Passive waveguides with integrated EO modulators

2 **COOLING**

- In-package cooling
- High-ratio thermal capacitance materials
- Emerging heat management materials

M3D THEME II

Passive Light Delivery

Gain Integration + Controllers

Heat Sink

Strata 1 Die 1

Strata 2 Die 1

Strata 3 Die 1

Bump Pillar

Electronic Photonic Chiplets

Laser

Antenna

ULK Dielectric

Inductor

Embedded RF

CORE

Micro-cooler

IVR

Thermal Insulator

RF CMOS

InP

Thermal Interface Material

Heat Spreader

2 **POWER DELIVERY & THERMAL MANAGEMENT**

- Efficient vertical delivery.
- Embedded IVR & inductors

www.chimes.psu.edu

Interposers Fabricated using 2-μm-Pitch Semi-Additive Process for Heterogenous Integration

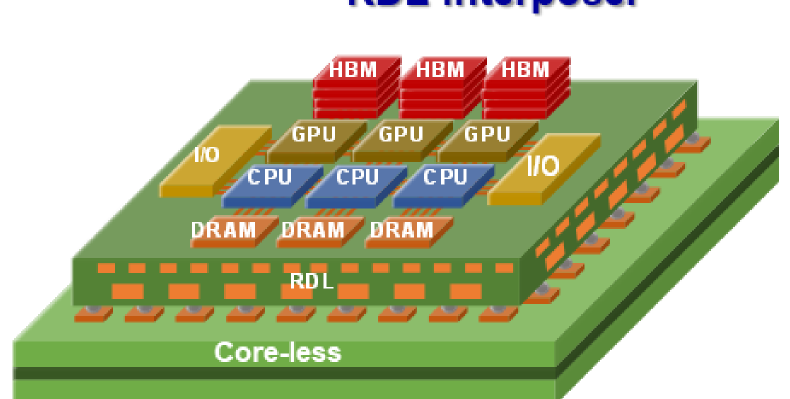
Satoru Kuramochi

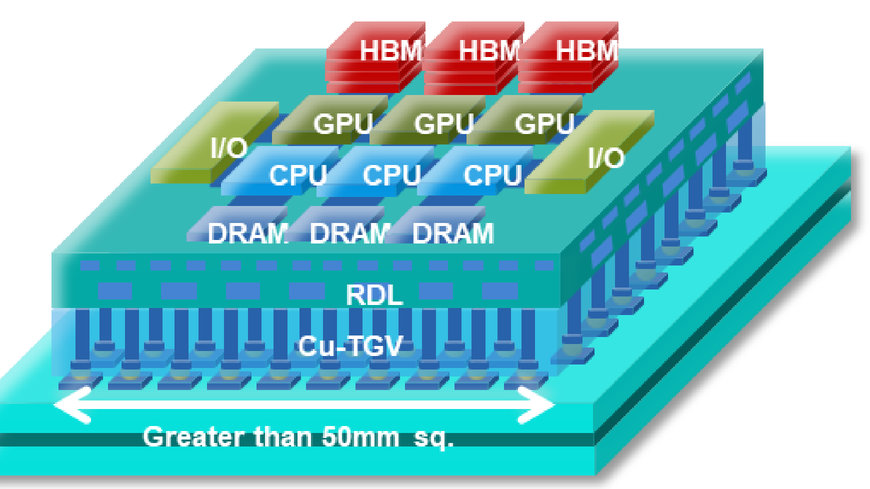
Dai Nippon Printing (DNP) Co., Ltd., Japan

Outline

- Introduction
- Glass Interposer
- RDL Interposer
- Summary

RDL and Glass Interposers for Heterogeneous Chiplet-Based Integrations

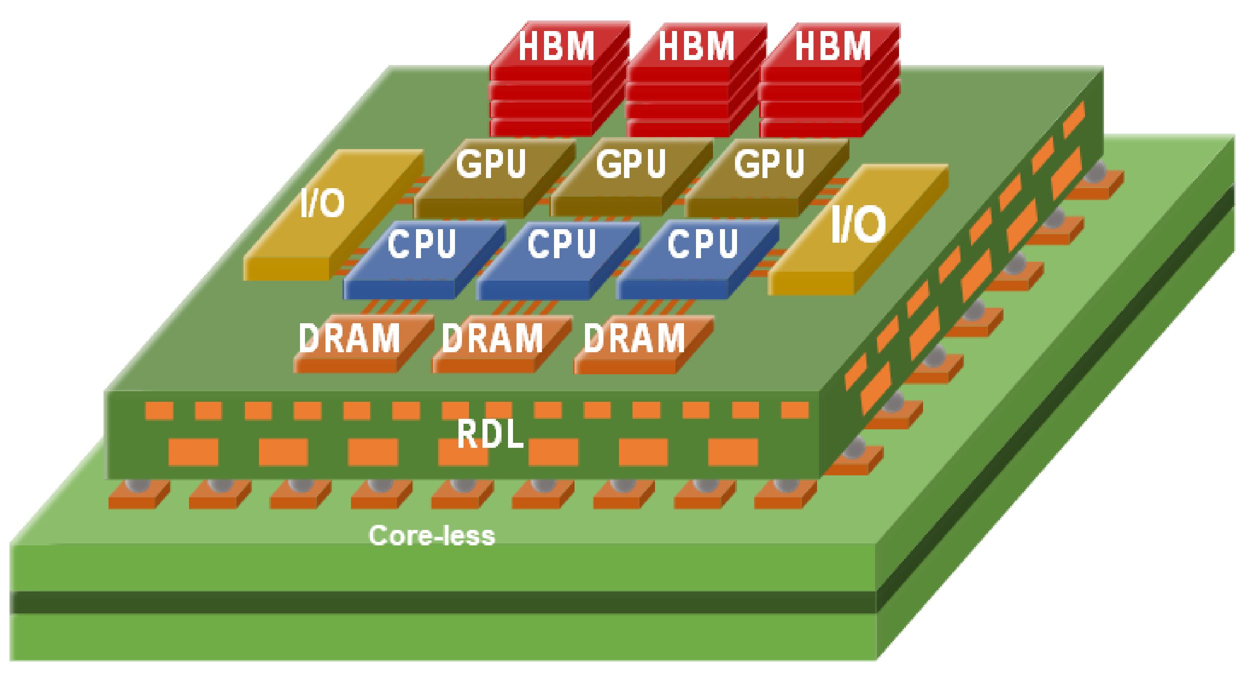




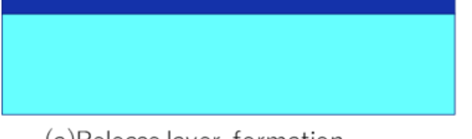
Products	RDL interposer	Glass interposer
Applications	General purpose ・PC ・Mobile ・Switching, etc.	High-performance ・A.I. computing ・Graphics ・Game, etc.
Advantage	Cost effective	Larger size (>50mm sq.)

RDL interposer

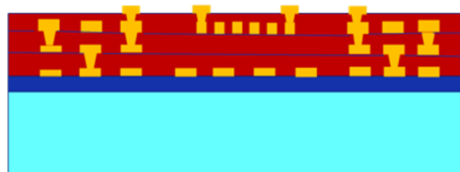
2.5D-RDL Interposer



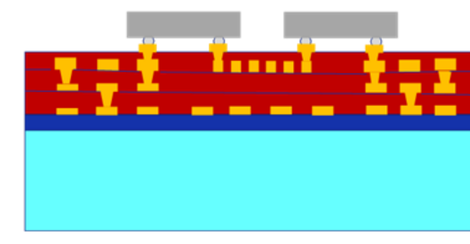
Process flow of RDL Interposer



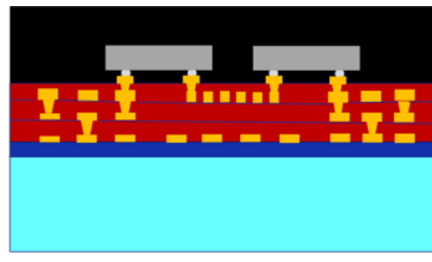
(a)Release layer formation



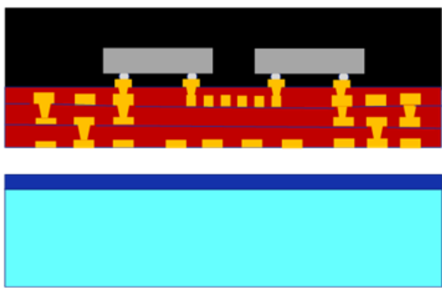
(b)RDLs formation



(c) Chips mount



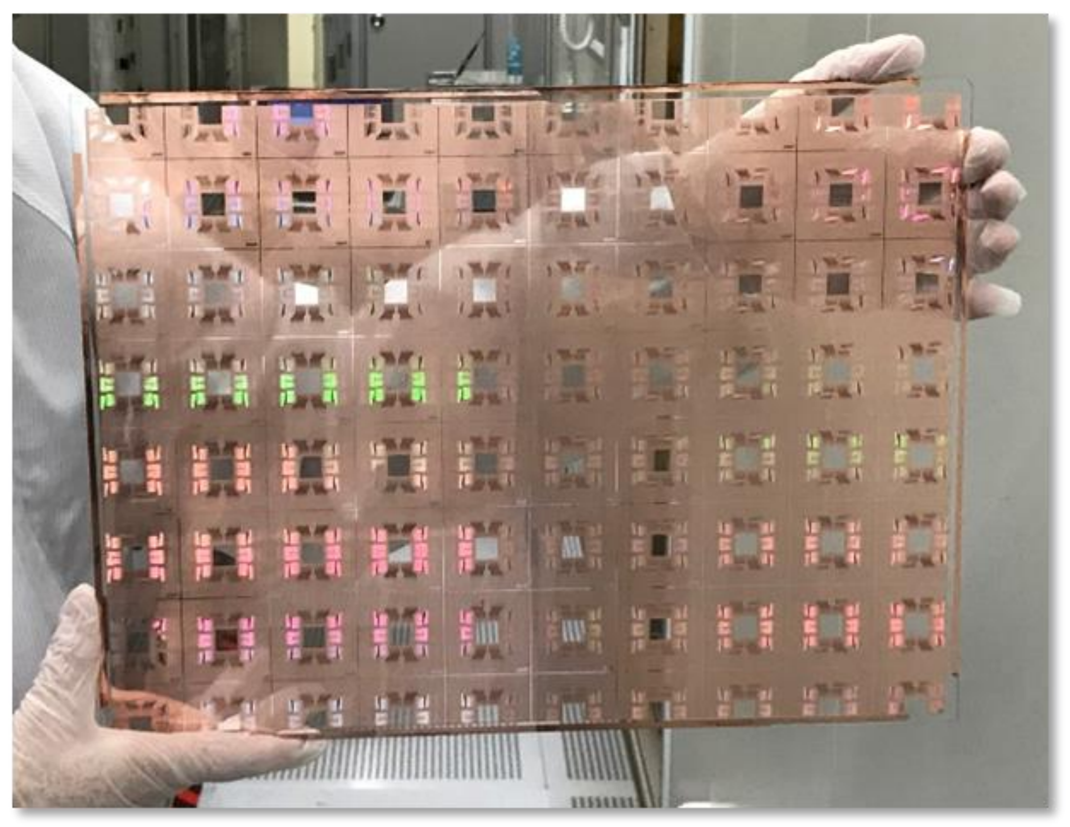
(d) Mold on Chips

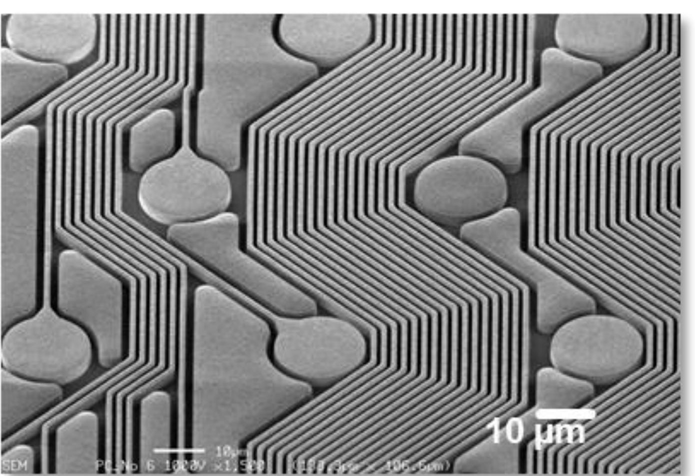


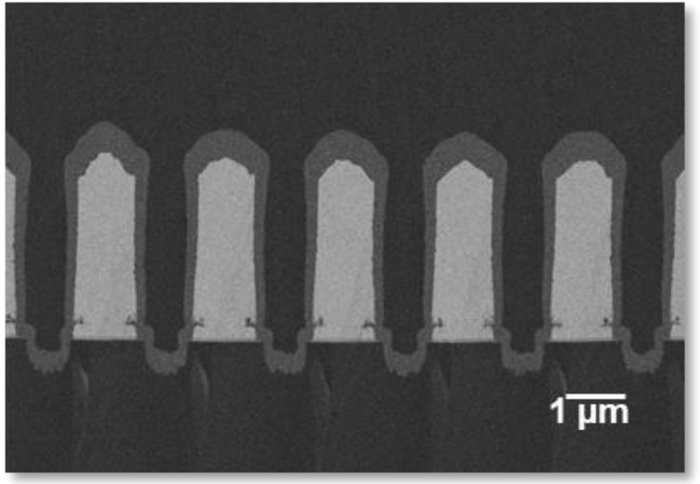
(e) Release carrier glass

DNP

SAP process for fine wiring





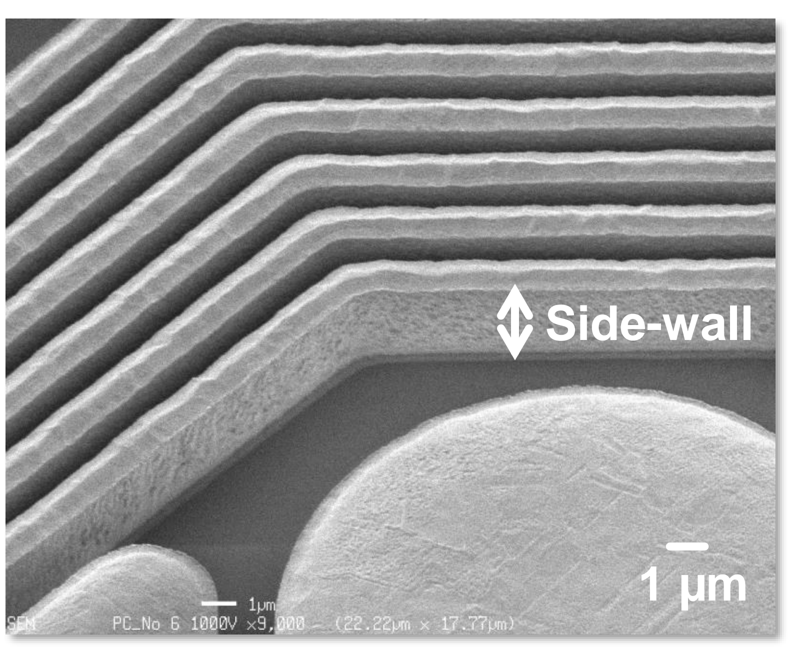


2-µm-pitch Cu trace

2-µm-Pitch Cu Traces in HBM I/O Area

10 µm

10µm
SEM PC_No 6 1000V ×1,500 (133.3µm × 106.6µm)



Close-up image

- No trace-width shift; any type of failure (trace peeling/deformation) was not detected .
- Trace side-wall with aspect ratio as high as 3, is almost a right angle (90°) .

DNP

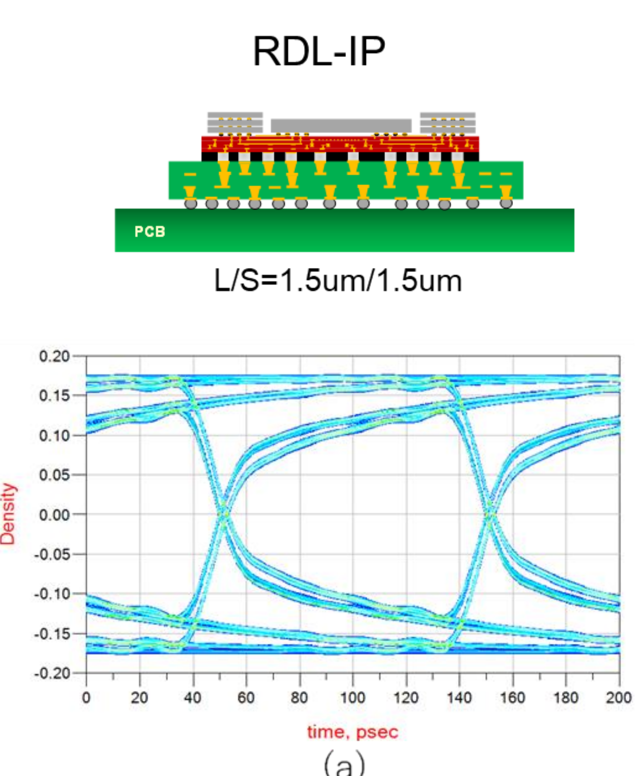
TEM Images of Biased-HAST Stressed Comb Monitors

- There was no Cu diffusion for the enhanced RDL sample.
- The control sample clearly shows that Cu migrated into the polyimide.

©Dai Nippon Printing *Presented at Pan pacific 2023*

Modeling high frequency transmission

Transmission speed 10Gbps will be used next generations HBM standard



(a)

10Gbps

L/S=0.5/0.5um

Density

time, psec

(a)

L/S=2.0/2.0um

Density

time, psec

(c)

L/S=0.75/0.75um

Density

time, psec

(b)

L/S=10/10um

Density

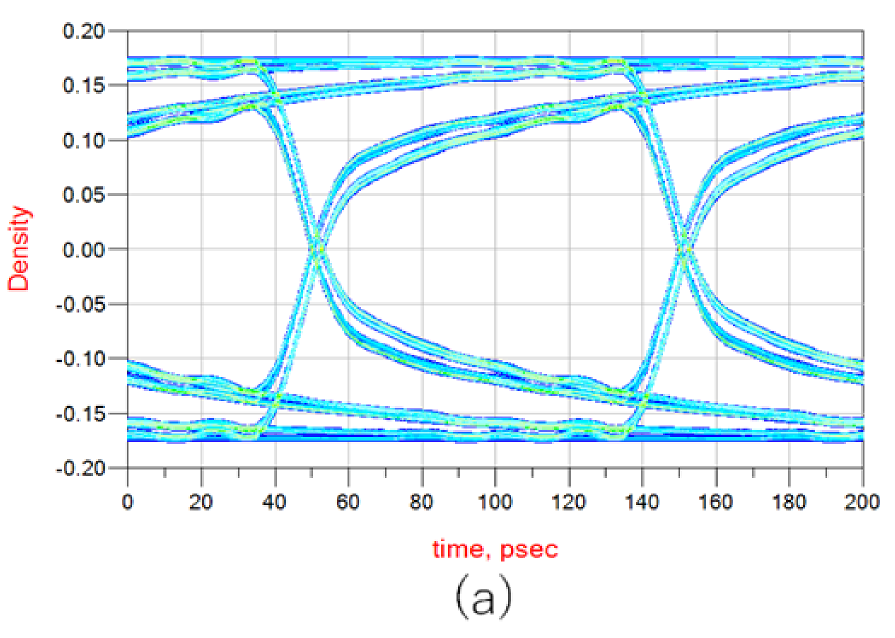
time, psec

(d)

DNP

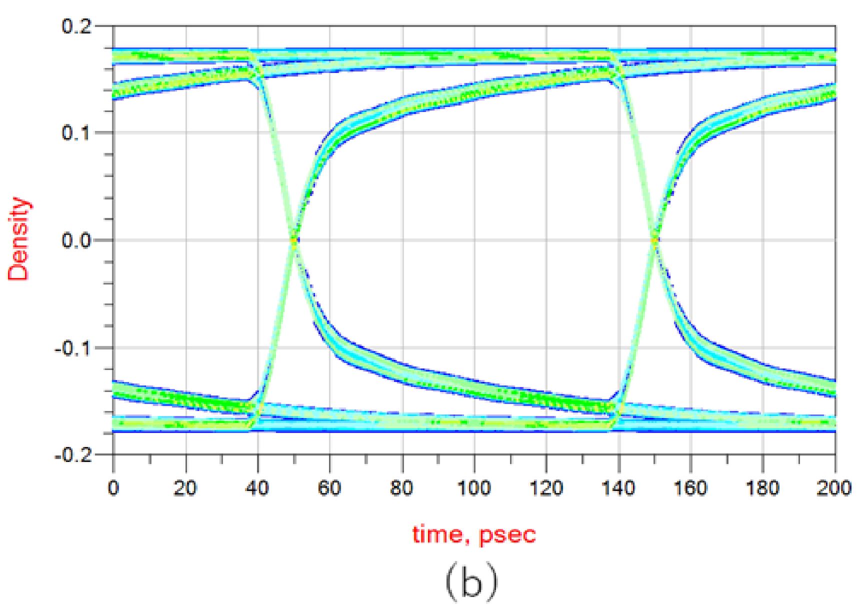
Modeling high speed transmission

L/S=1.5/1.5 um tanδ=0.02 dielectrics



(a)

L/S=1.5/1.5um tanδ=0.002dielectrics



(b)

Table 4

Model	Eye height(V)	Rising time(psec)
CPW tanδ=0.002 dielectrics	0.25	16.6
CPW tanδ=0.02 dielectrics	0.20	28.5

Simulated Eye Diagram at 32 Gbps

GSG

1.0 µm 1.0 µm
S G S G S
3.0 µm
Polyimide
4.0 µm
G
3.0 µm

SSG

1.0 µm 1.0 µm
X
S S G S
3.0 µm
I/O section: X=6.0 µm
Middle section: X=6.0 µm
4.0 µm
G
3.0 µm

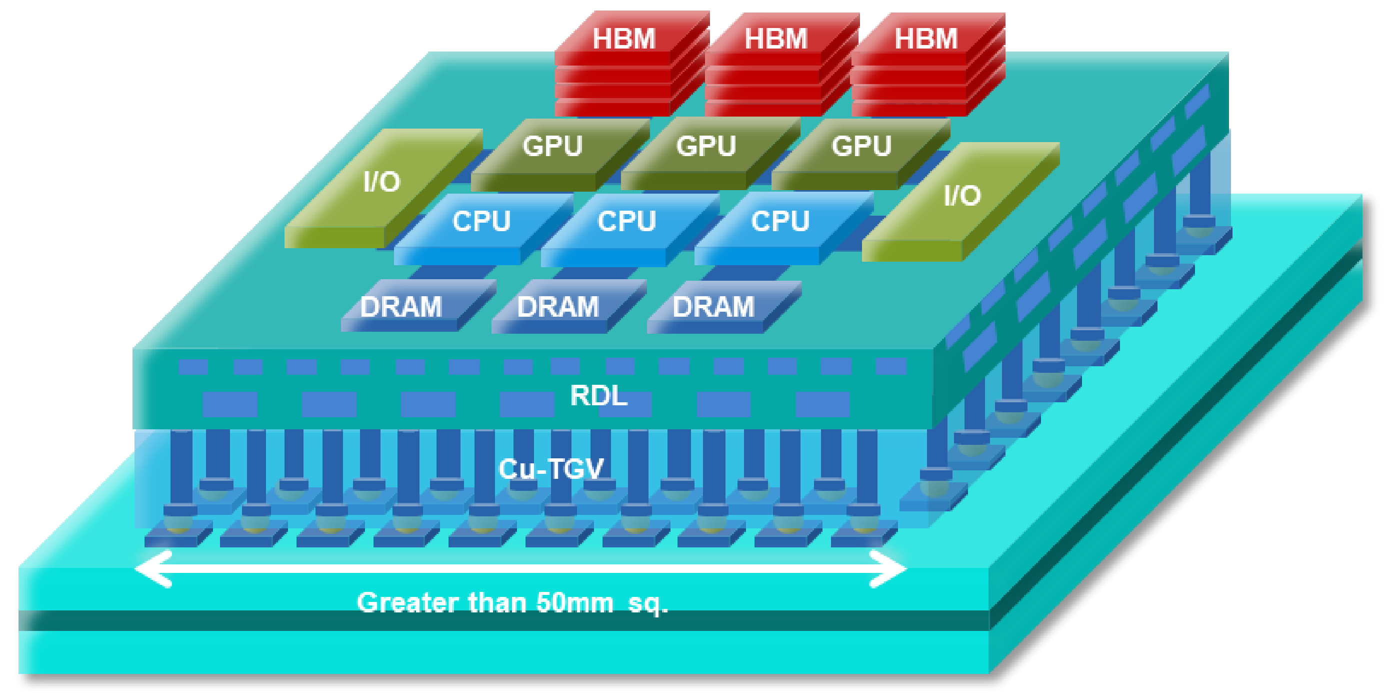
SSS

2.0 µm
X X
S S S
2.0 µm
I/O section: X=3.5 µm
Middle section: X=3.5 µm
4.0 µm
G
2.0 µm

Voltage (V): 0.5, 0.4, 0.3, 0.2, 0.1, 0.0, -0.1, -0.2
Time (psec): 0, 10, 20, 30, 40, 50, 60
Keep-out area

Glass interposer

2.1D-Glass Interposer

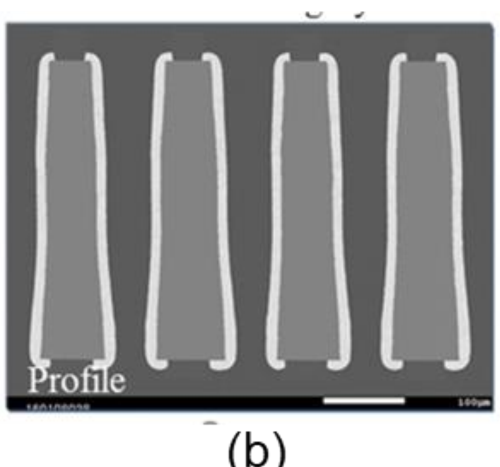


©Dai Nippon Printing
Presented at Pan pacific 2023

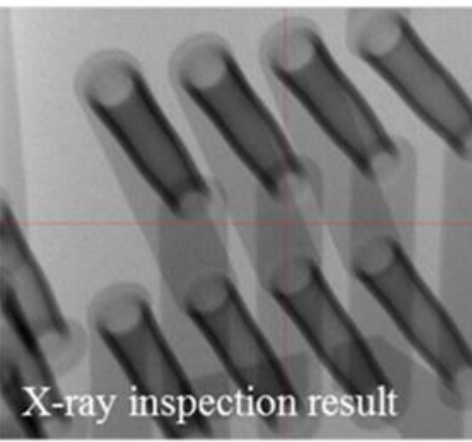
TGV with 300x400㎜ Glass Panel

400 mm

(a)



(b)



(c)

Takano et al., "3D IPD on Thru Glass Via Substrate using panel Manufacturing Technology, " Proceedings International Micro electoonics and Packaging Society 2017. pp. 102

Measurement result of transmission line with TGV

80umΦ TGV
400umt
L=10mm, W 30um

80umΦ TGV
400umt
L=10mm, W 30um

40umΦ TGV
400umt
L=10mm, W 30um

Filled Type | **Conformal Type** | **Partial fill Type**

(a) S21(dB) vs. Frequency (GHz): CPW, CPW+TGV — 0.23dB @30GHz

(b) S21(dB) vs. Frequency (GHz): CPW, CPW+TGV — 0.48dB @30GHz

(c) S21(dB) vs. Frequency (GHz): CPW, CPW+TGV — 0.34dB @30GHz

There are difference depend on metalize,
However loss are very lower than surface wiring loss.

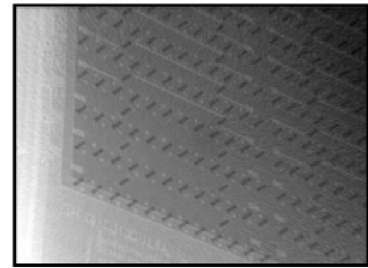
©Dai Nippon Printing
Presented at Pan pacific 2023

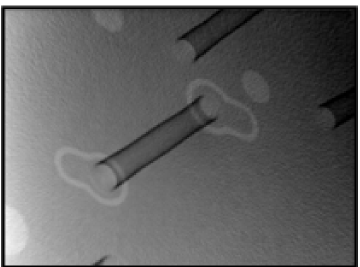
DNP

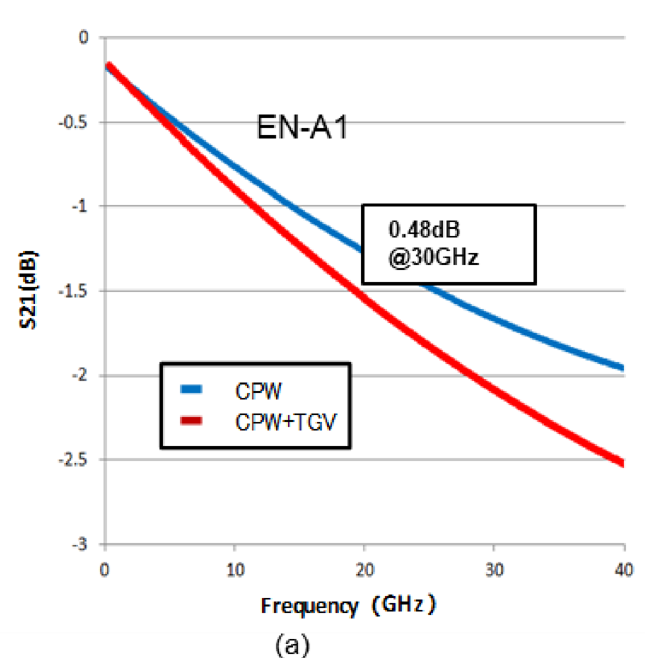
Glass material property

	Dielectric constant	Dielectric loss
Alkali-free Glass (EN-A1)	5.8	0.006@10GHz
Synthetic fused Quartz Glass (AQ)	3.8	0.0002@10GHz

Conventional glass

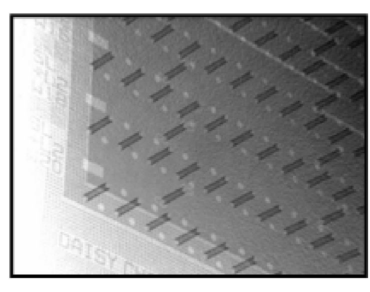


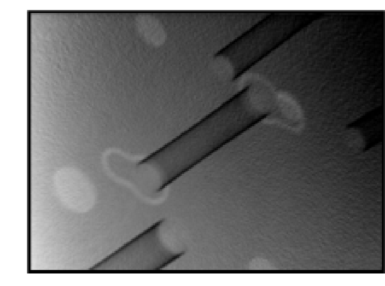


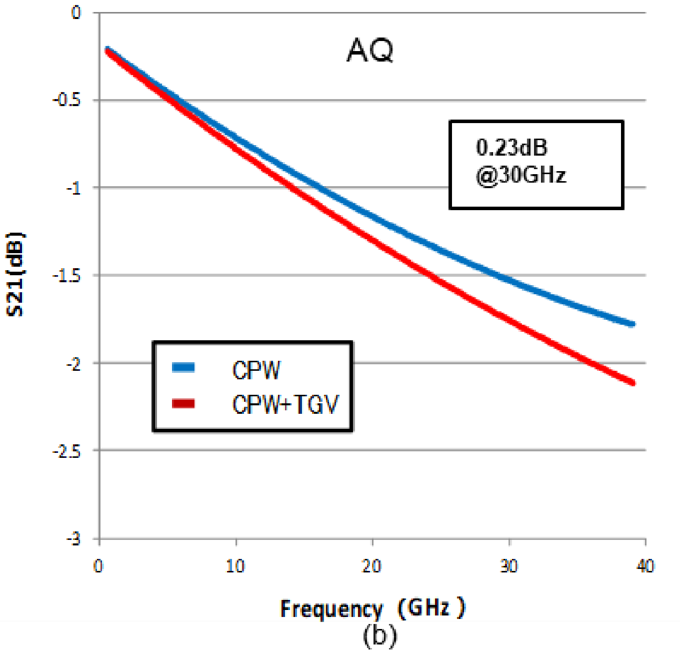


(a)

Synthetic fused quartz Glass





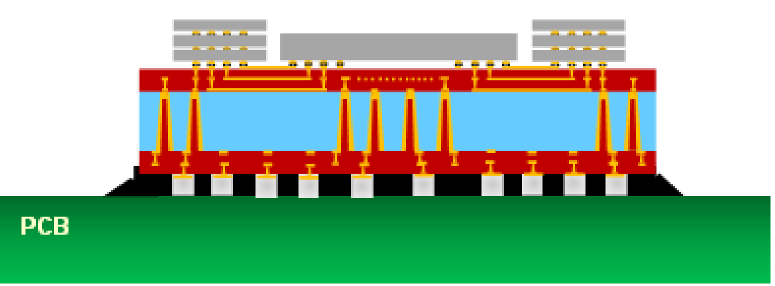


(b)

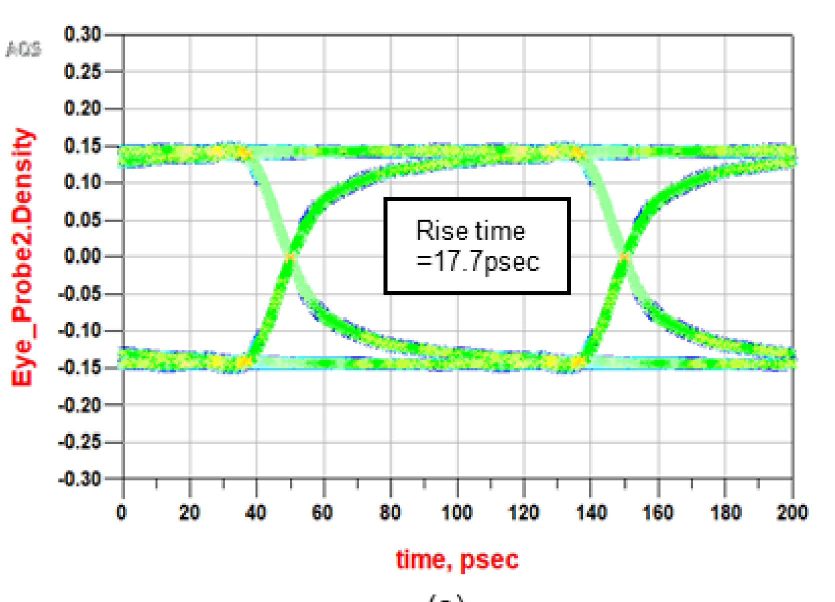
©Dai Nippon Printing *Presented at Pan pacific 2023*

Comparison characteristics with interconnection

2.1D

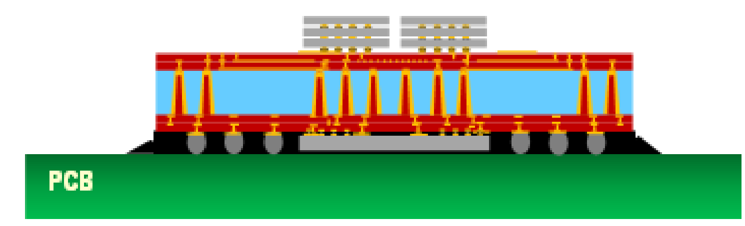


L/S=1.5/1.5um fine line

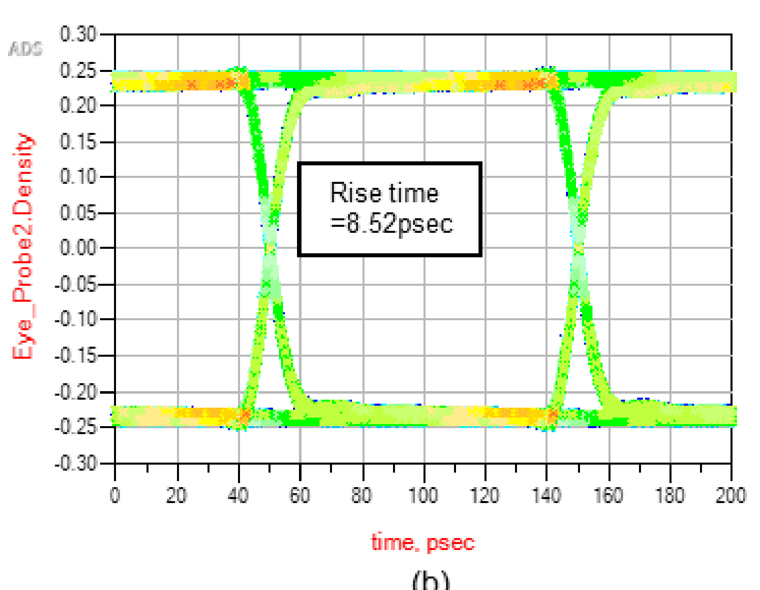


(a)

3D



TGV=40um fine via



(b)

©Dai Nippon Printing

Presented at Pan pacific 2023

Summary

- Fine wiring L/S=1.0/1.0um demonstrated using Semi-Additive-Process for RDL. Excellent transmission characteristics obtain fine pitch area using GSG.

- Low loss types has advantage on the high-speed transmission.

- Three types of TGV were demonstrated and measured high frequency characteristics. All three types, TGV itself are very low loss.

- Quartz glass has a very small insertion loss of -0.23dB at 30GHz. Quartz glass has small loss comparing with the alkali-free glass.

©Dai Nippon Printing

Semiconductor Package Development Trends Driving Heterogeneous Integration

~ 2.3D i-THOP® : integrated - Thin film High density Organic Package ~

Shota Miki

SHINKO ELECTRIC INDUSTRIES CO., LTD.
Research & Development Div.

e-mail : sy.miki@shinko.co.jp

Contents

- Motivation
- Application & Configuration
- 2.3D i-THOP®
    - Structure and Design rules
    - TV Demonstration
    - Electrical Performance
    - Future
- Summary

Motivation

Memory bandwidth, I/O density (Relative)

Optical WG

2D → 2.3D/2.5D

Si IP + TSV(3D)

2.3D i-THOP®
High-density
Organic Interposer

HBM pad pitch: 55µm

DLL® (MCP)

DLL® = BU substrate

~2010

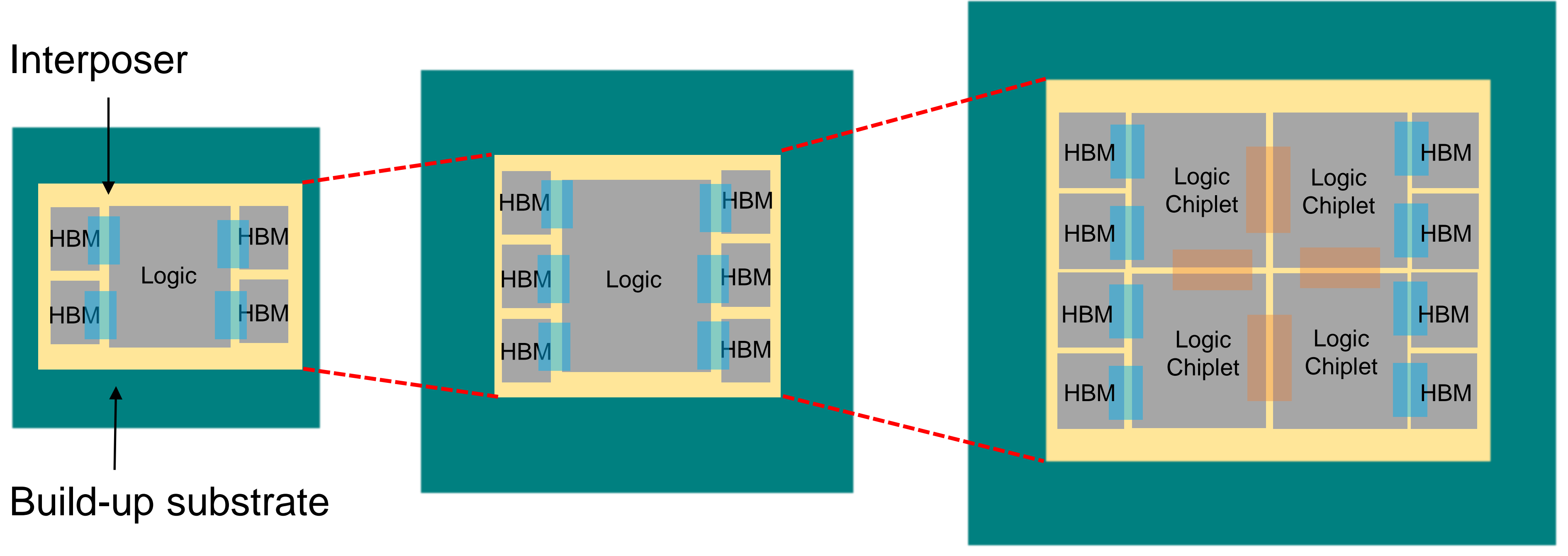
2016~

- Required higher density IO connections such as HBM and Chiplets
- i-THOP® targeting advanced solution to current Si interposer technology

* i-THOP and DLL are registered trademark of SHINKO ELECTRIC INDUSTRIES CO., LTD

Application & Configuration

- ✓ **Application: AI, HPC, Networking etc.**
- ✓ **Expected Configuration: Large sized interposer with increased HBM & Chiplets integration**



- ✓ Further interposer area expansion is expected to improve system performance.
- ✓ Fine and high-density interposer is key technology for interconnecting HBM and Chiplets.

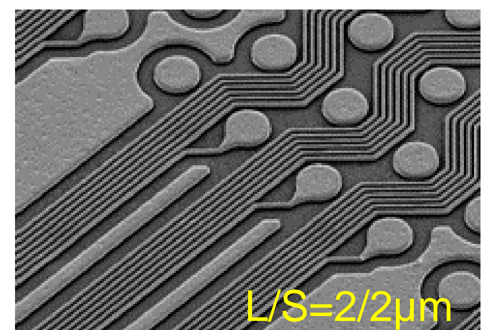
Structure & Design rules

FC-pad

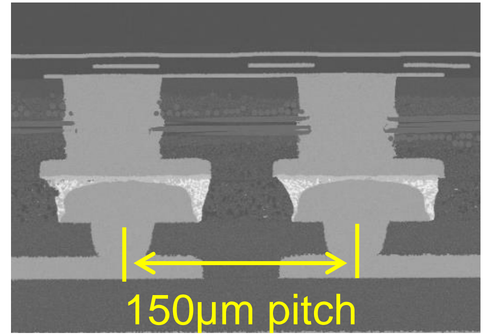
40µm pitch

Rigid layer

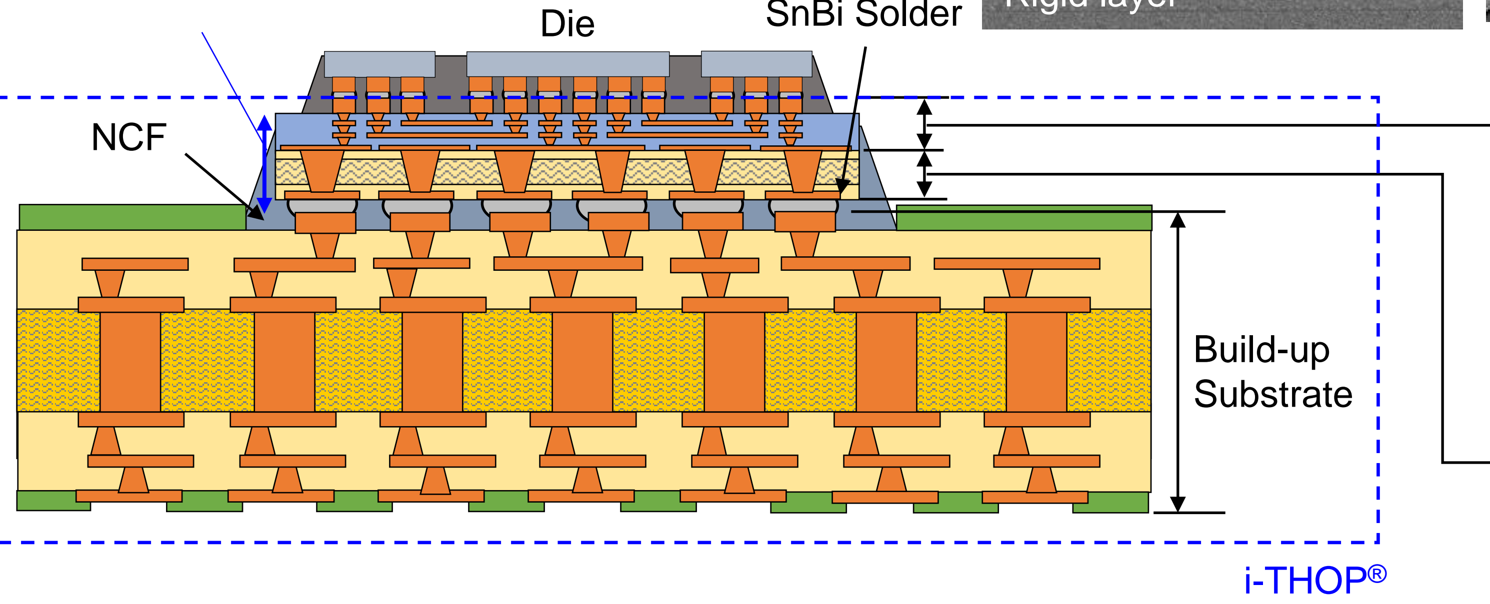
Fine trace



Interposer joint



Organic Interposer
Thickness: <100µm



Thin Film Layer

Min. FC pad pitch	40 µm
Min. Line and Space	2 / 2 µm
Micro Via / Via land diameter	12 / 21 µm
Metal thickness	2 µm
Insulation thickness	5 µm

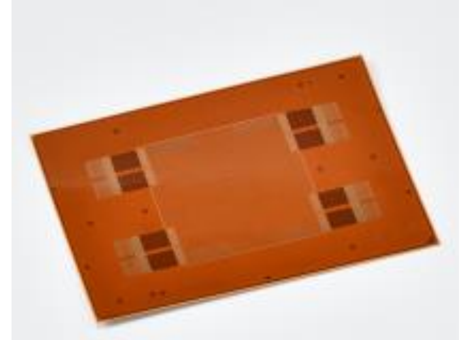
Core-less Layer

Via diameter	70 µm
Min. Interposer joint pitch	150 µm

" Design and detail dimensions are subject to change."

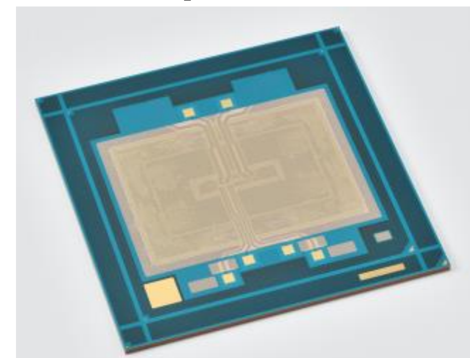
2.3D i-THOP® | TV Demonstration

Organic interposer



Size : 44 x 31 x 0.094 mm

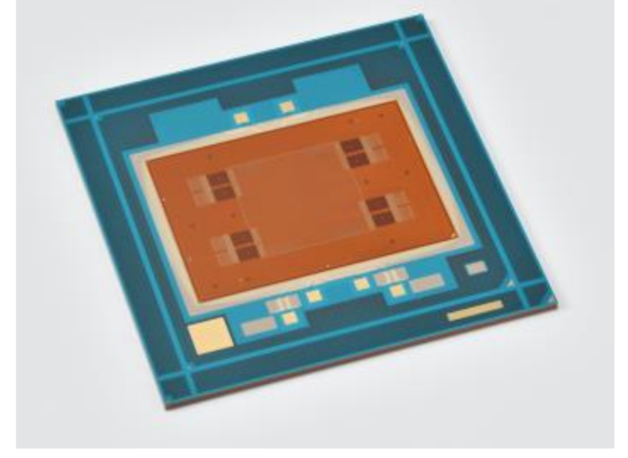
Build-up Substrate



Size : 65 x 65 x 1.45 mm

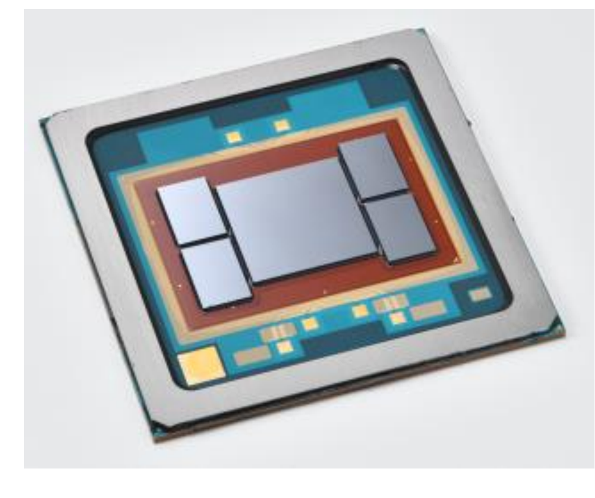
Interposer assembly

2.3D i-THOP®



Die assembly & Stiffener attach

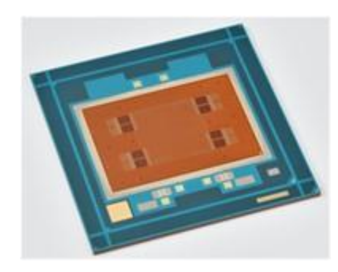
2.3D i-THOP® Module

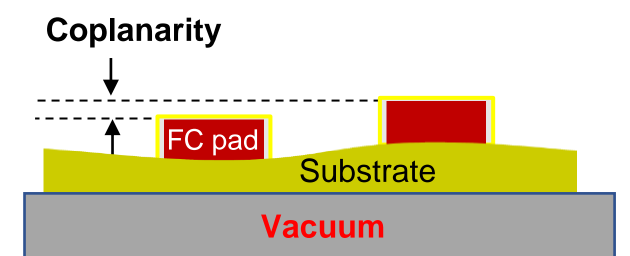


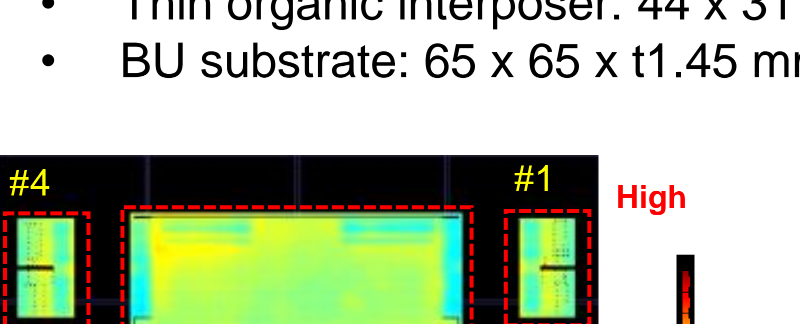
✓ Organic interposer and BU substrate are pre-assembled for following “die last” assembly.

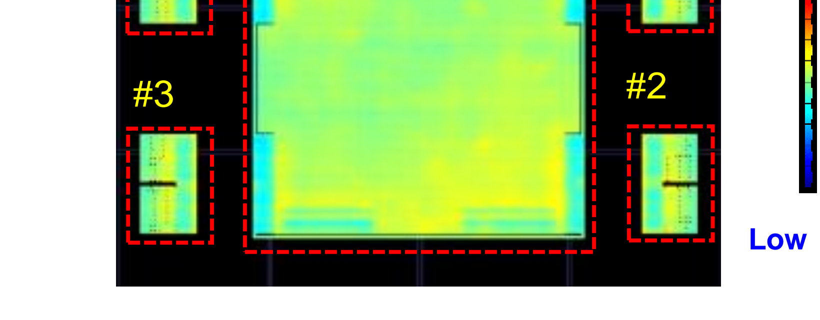
FC-pad Coplanarity

- Sample
  - Thin organic interposer: 44 x 31 mm
  - BU substrate: 65 x 65 x t1.45 mm

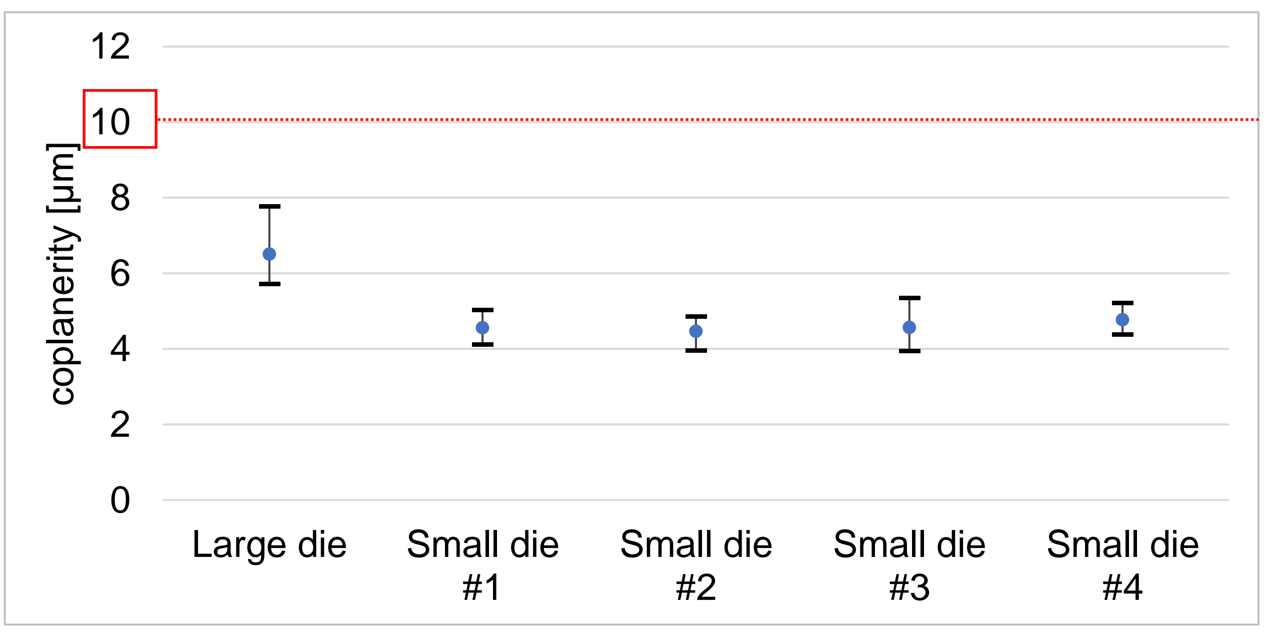








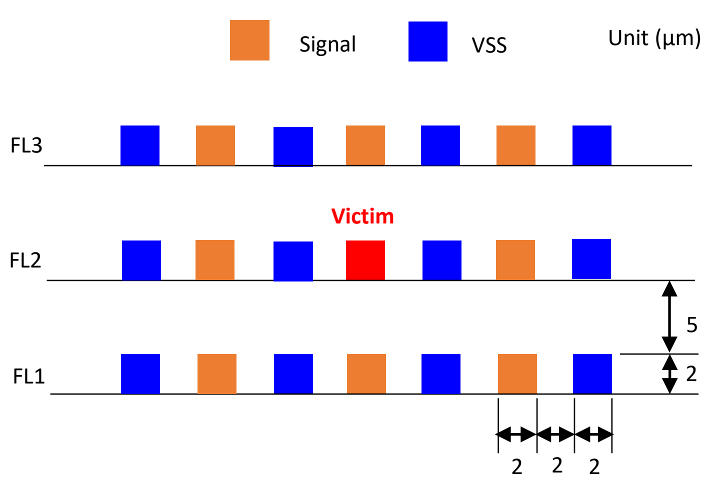
- ✓ Large die : 20 x 20 mm size, 41,378bumps
- ✓ Small die : 7.75 x 11.87 mm size, 4,942bumps



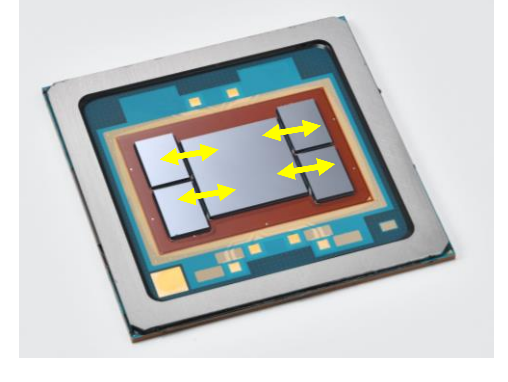
✓ FC-pad coplanarity is under 10μm in large and small dies areas.

- **Signal Integrity Analysis of Logic-HBM wiring**

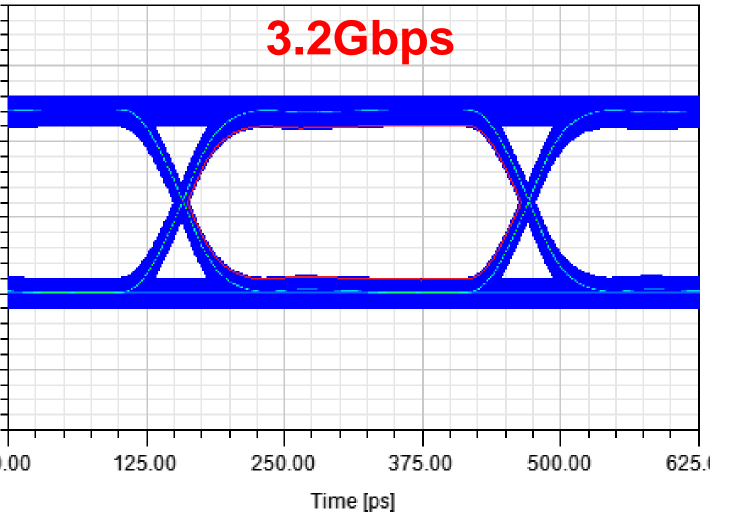
Coplanar structure wiring model
(X-sectional view)

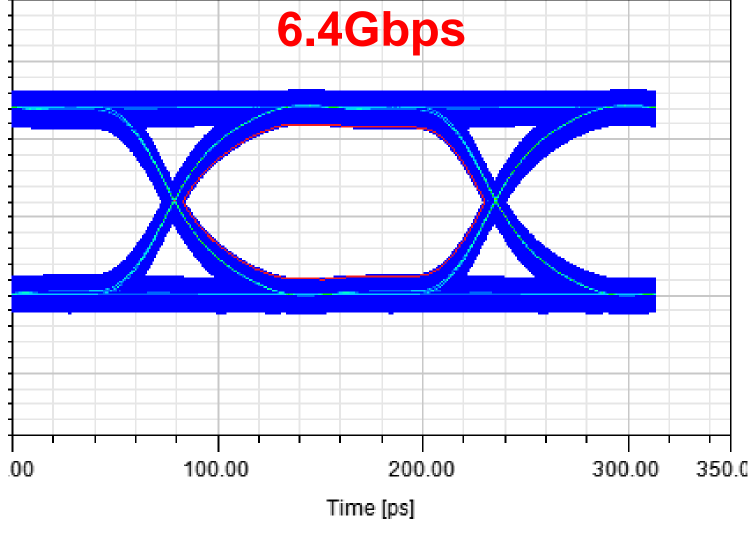


- ✓ L/S=2/2μm
- ✓ 3 routing layers
- ✓ Line length (Victim) = 4.27mm



Eye pattern





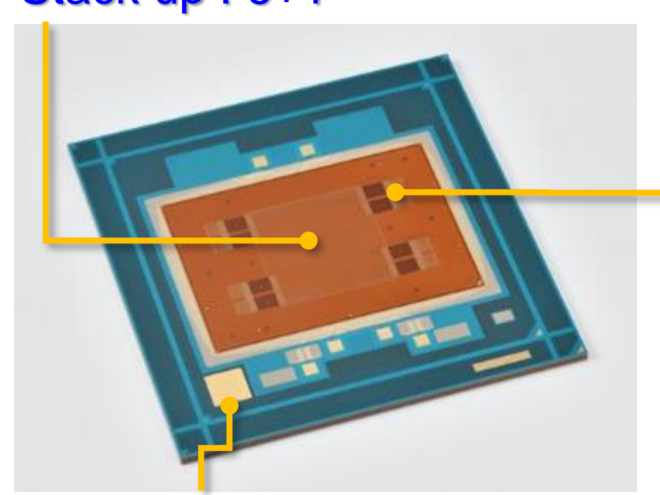
✓ Potential to support HBM2E and HBM3 transmission speeds with good eye pattern was confirmed.

2.3D i-THOP® | Future

Increase in Thin Film Layer Count

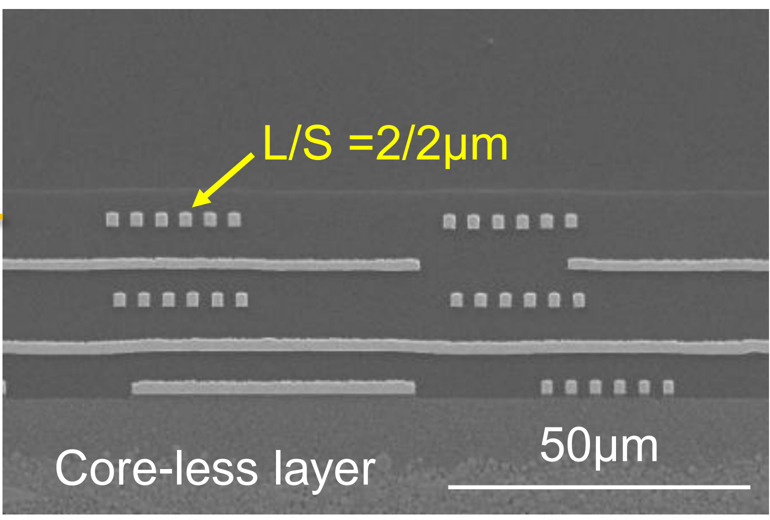
- **Maximum Interposer stack-up : 6 + 1 (under evaluation)**

Organic Interposer
44 x 31 mm
Stack up : 6+1

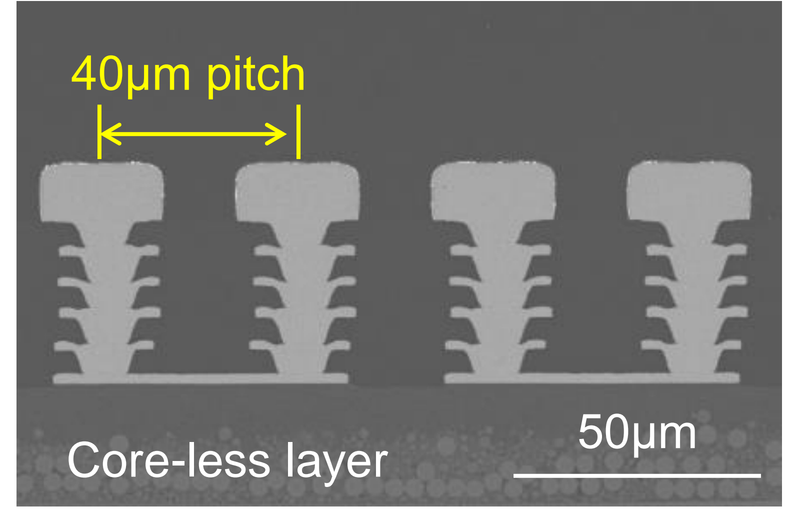


Build-up substrate
65 x 65 mm

Min. L/S=2/2μm traces



Micro via stacked in 5 layers



✓ L/S=2/2μm traces and five stacked vias could be formed successfully.

Large Sized Organic Interposer Development

- **Maximum Interposer Size : 70x70mm (under evaluation)**

Organic Interposer
70 x 70 mm
Stack up : 4+1

BU substrate
100 x 100 mm

After die assembly

4 x Logic Chiplet
20 x 20 mm

12 x Small chip

Note: Routing area for L/S = 2/2 µm is within 55 x 55 mm.

✓ 2.3D i-THOP® was fabricated using large sized interposer.

Technology Roadmap

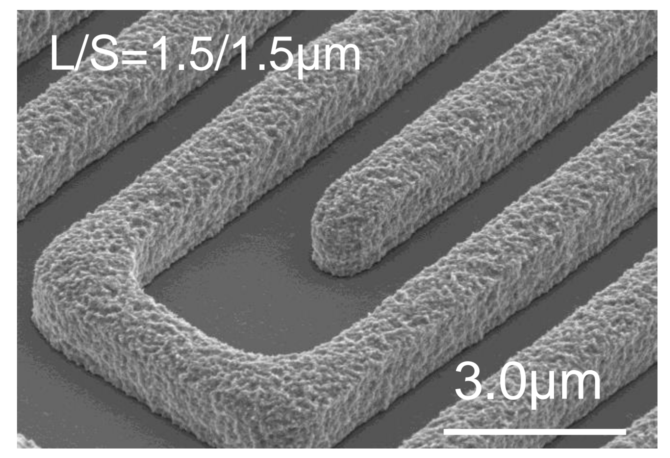
Item		Design Rule	2022	2023	2024	2025		Equipment dependent *1
Thin film layer	Min. Line/Space	2/2µm	2/2µm		1.5/1.5µm			1/1µm
	Min. Via/Land dia.	12µm/21µm	12µm/21µm		8µm/17µm			5/13µm
	Max. Via dia.	12µm	12µm		18µm			
	Min. FC Pad pitch	40µm	40µm		35µm			30µm
Coreless layer	Min. Interposer joint pitch	150µm	150µm		130µm			

" Design and package architecture roadmap targets are subject to change. "

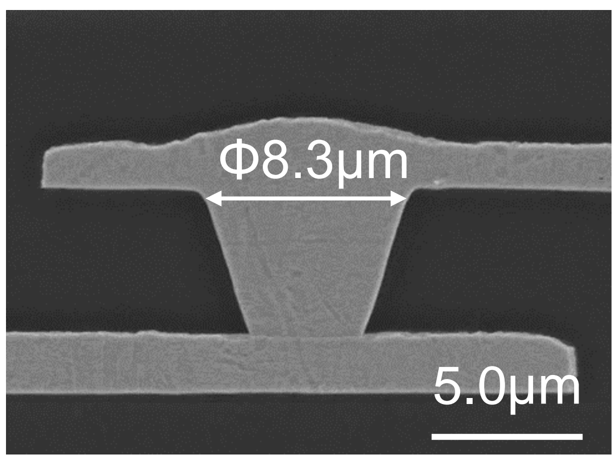
*1 These will require new equipment development. We will consider whether to proceed with development depending on customer needs.

Fine Design Technology

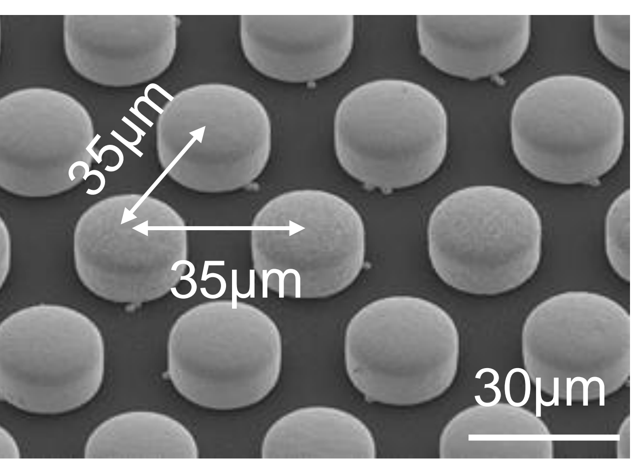
Fine trace



Micro via



FC-pad



✓ Process condition is under evaluation for technology roadmap.

Summary

- 2.3D i-THOP® targets advanced solutions to current Si interposer technology.
- 2.3D i-THOP® has advantage to die last process because of low coplanarity package structure.
- Good signal integrity to support HBM2E and HBM3 transmission speed was confirmed.
- Shinko continues to develop fine and heigh-density technologies for Heterogeneous Integration.

Thank you for your attention!

Brightening the Future

Since 1946

1st Level Packaging: Considerations for HPC: A system perspective

Dale McHerron, PhD
Sr Manager and STSM, IBM Research

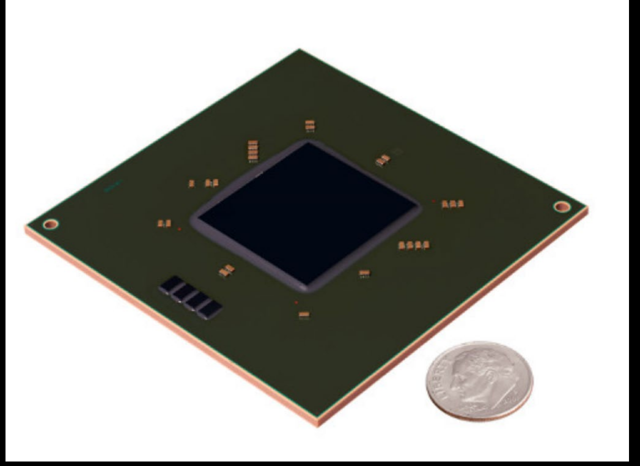
© 2022 IBM Corporation

IBM Z System 1st Level Packaging: Single Chip Module (SCM)

SCM Key Attributes:

- Deliver power to CPU (lots!)
- Off Module I/O
- High Reliability
  - Z system: Guaranteed 3s downtime / yr
- Known good substrate
  - Full Test coverage before assembly
  - CPU cost >>>> Substrate cost
- Support Land grid array (LGA)
  - Enable system swap out
  - High Clamping forces
- Support Thermal Solution

Z15 Heatsink

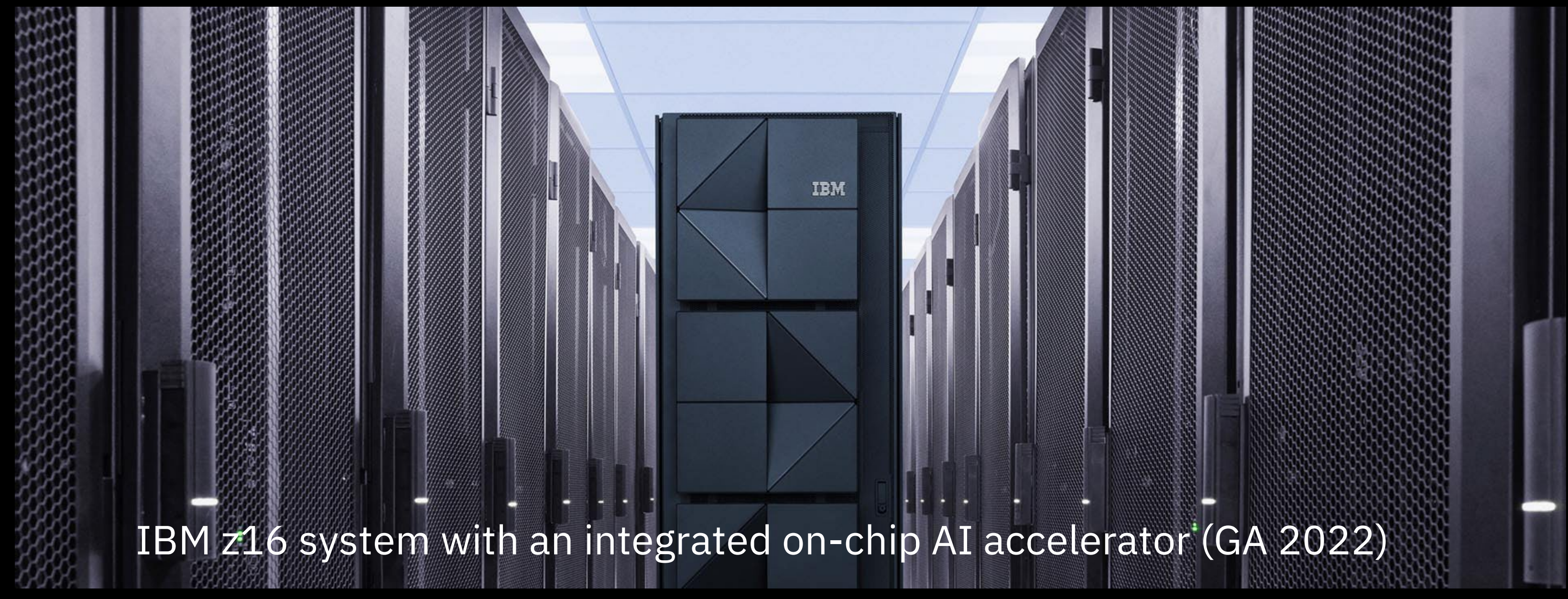


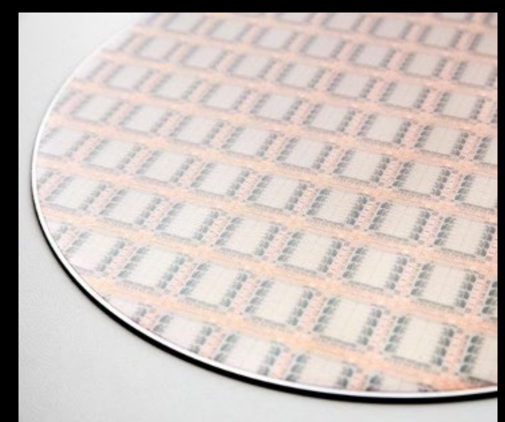
Z15 SCM (2019)

IBM **Research**

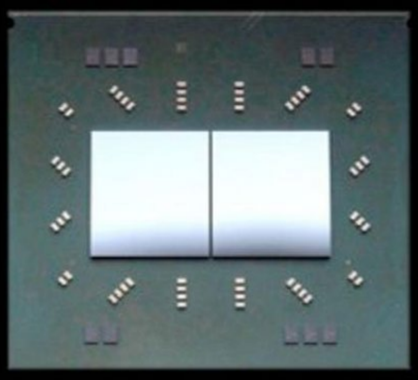
© 2022 IBM Corporation

IBM Z16 packaging: Dual chip module on organic substrate

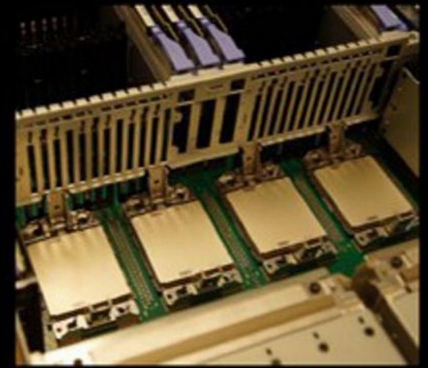




300mm wafer w/ IBM Telum Processor: 7nm technology, 8 cores, 5+ GHz, 256MB L2 cache and AI accelerator



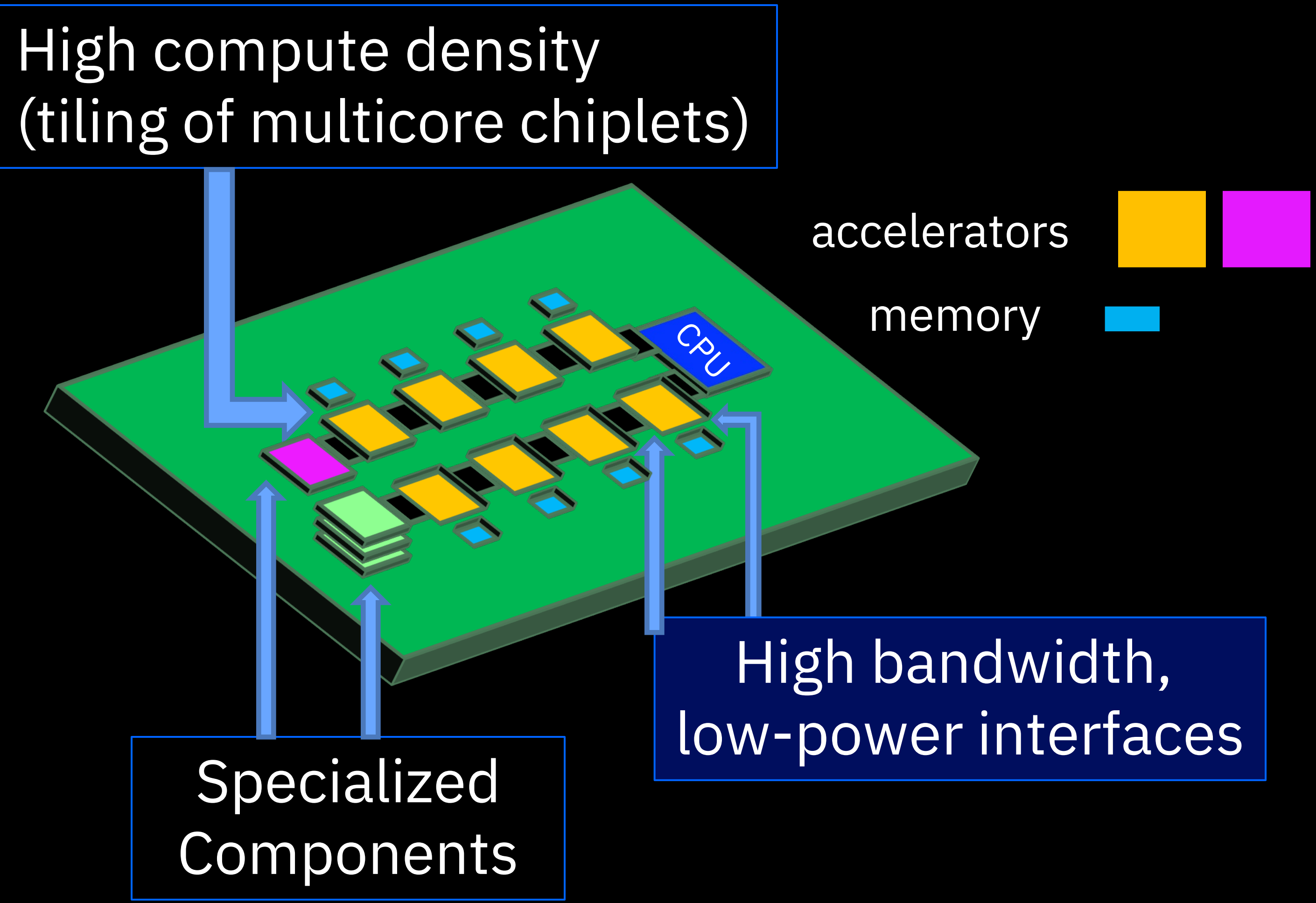
Dual chip module
2chips, 512 MB L2 cache, >500W/chip



4 socket drawer
4 DCMs, 2GB L2 Cache

© 2022 IBM Corporation

Chiplet Platform for HPC & AI



What's needed From the Package:

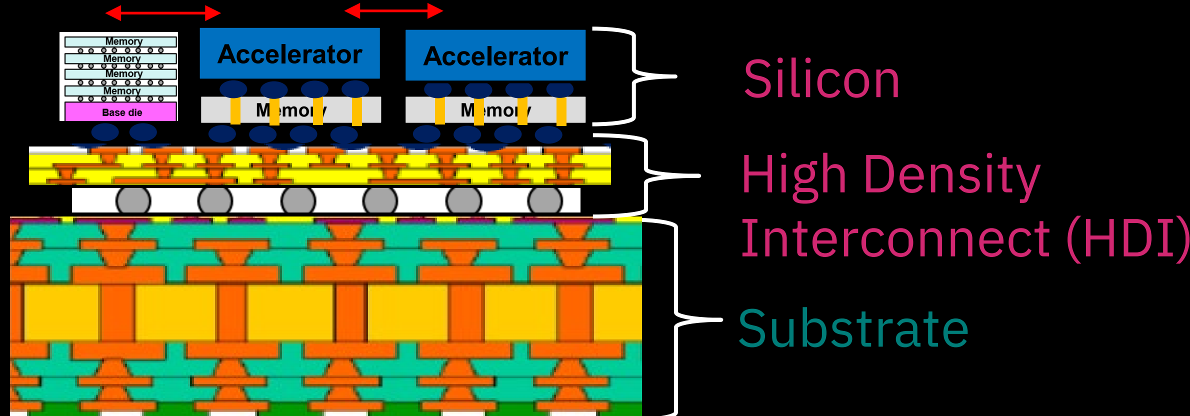
- Interfaces between components
  - High bandwidth (Gbps/mm)
  - Energy-efficient (pJ/bit)
  - Area-efficient (Gbps/mm^2)
  - Standards to allow connectivity between wide variety of components
- Technology Elements
  - Scaled interconnects
  - Fine pitch wiring
  - Power Delivery
  - Large(r) form factors

Dale McHerron, ICEP2021

© 2021 IBM Corporation

Packaging Considerations for HPC

- ✓ Low volume
- ✓ High complexity
- ✓ Expensive
- ✓ High reliability / long lifetime



Silicon:

- Continue to innovate on chiplets and connectivity
  - 3DI, bump scaling, hybrid bonding, interfaces, Si partitioning

HDI:

- Leverage Si fab capabilities
  - Drive density scaling
  - Utilize existing infrastructure / technology
- Continue to innovate
  - Interposers, bridges, FO, RDL, etc
- Enable customization at this level
  - Address application specific PI / SI requirements

Substrate:

- Drive standards to minimize product mix
- Innovate on new technologies