Photonic Integrated Circuit Packaging : challenges, pathfinding and technology adoption

Tuesday, May 30, 2023, 1:30 p.m. – 3:00 p.m.

Chairs: Stéphane Bernabé (CEA Leti) and Hiren Thacker (Cisco)

ECTC 2023 Special Session 3

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Photonic Integrated Circuit Packaging : challenges, pathfinding and technology adoption

Photonic integrated circuit (PIC) technologies are proliferating into many application spaces; from hyperscale data center, High Performance Computing to sensing including LiDAR. Packaging remains the greatest challenge to high volume manufacturing at high throughput and yield. The main challenges are: optical coupling, TSV integration for chiplet or photonic interposer approaches, laser integration, thermal management, manufacturability and reliability. While there are currently only limited standardization activities (OIF, COBO, IEC SC86C/WG4) addressing these challenges, the need for innovative solutions is growing to merge semiconductor 3D packaging technologies and photonics. This session will feature leading practitioners who are actively driving PIC packaging innovation and technology adoption towards high-volume reality.

Photonic Integrated Circuit Packaging: Challenges, Pathfinding and Technology adoption

Gianlorenzo Masini

30May2023

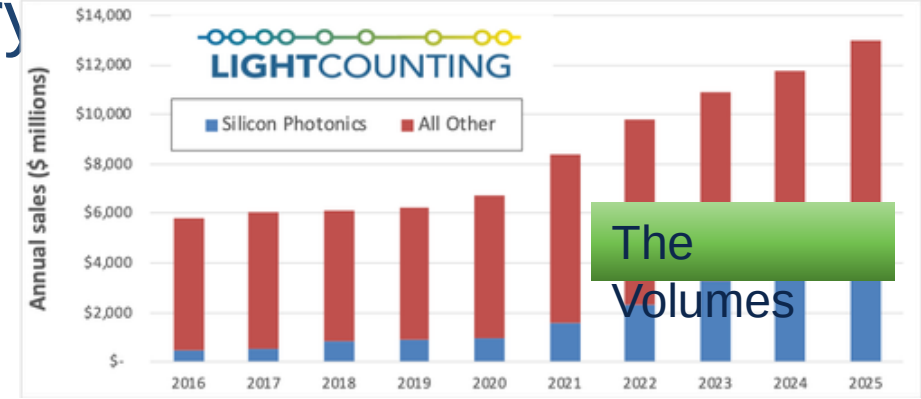
Agenda

- Photonics @ Cisco
- Photonics packaging challenges
- Module solutions
- Co-packaging avenues
- Conclusions

The silicon photonics industry today

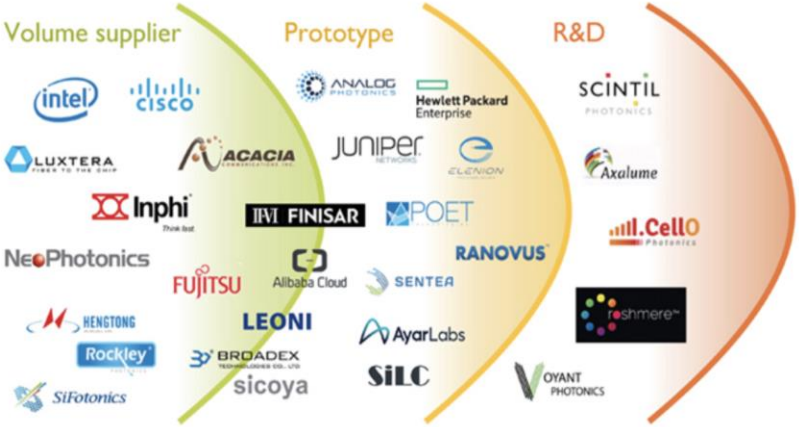
- Mature technology with multiple industrial players, and slightly diversified market
  - Most of the volume in short haul applications, in which it competes with EML-based “classic optics” solutions
- Numerous emerging applications

Figure: Global market for optical transceivers, AOCs and EOMs by technolo

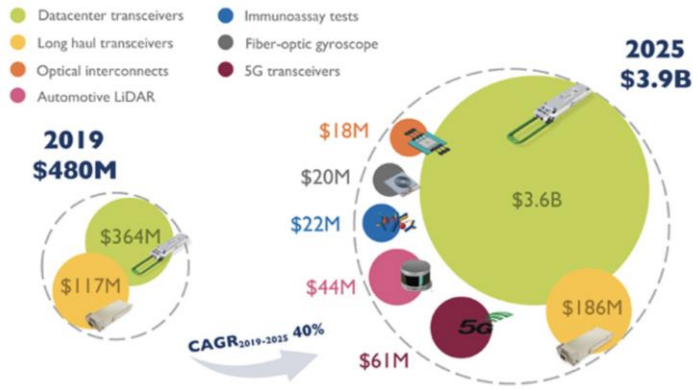


The Volumes

The Players



The Applications

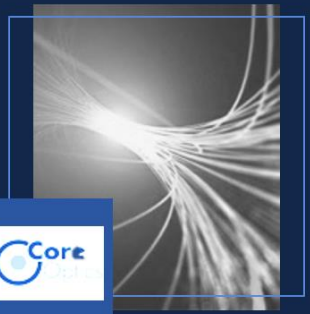


Readiness levels of silicon photonics players: volume, prototype or research. Source: Silicon Photonics Market & Technology 2020 report by Yole Développement.

Silicon photonics 2019-2025 market forecast by applications. Source: Silicon Photonics Market & Technology 2020 report, by Yole Développement.

Cisco Investments in Silicon & Optics

Inorganic Investments in Optics and Silicon



CORE OPTICS

Innovator in coherent optical technologies

JULY 2010

LIGHTWIRE

Innovator in Direct Detect silicon photonics

MARCH 2012

LEABA

Next Gen Silicon One for Routing/Switching

MARCH 2016

LUXTERA

Leading automation of Direct Detect SiP manufacturing process

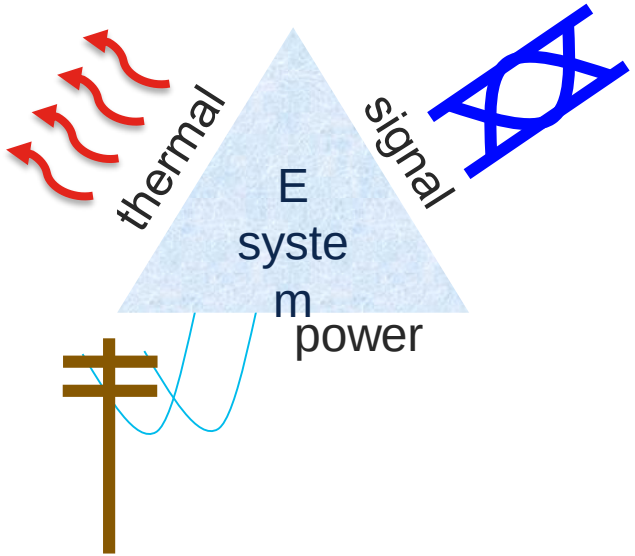
FEBRUARY 2019

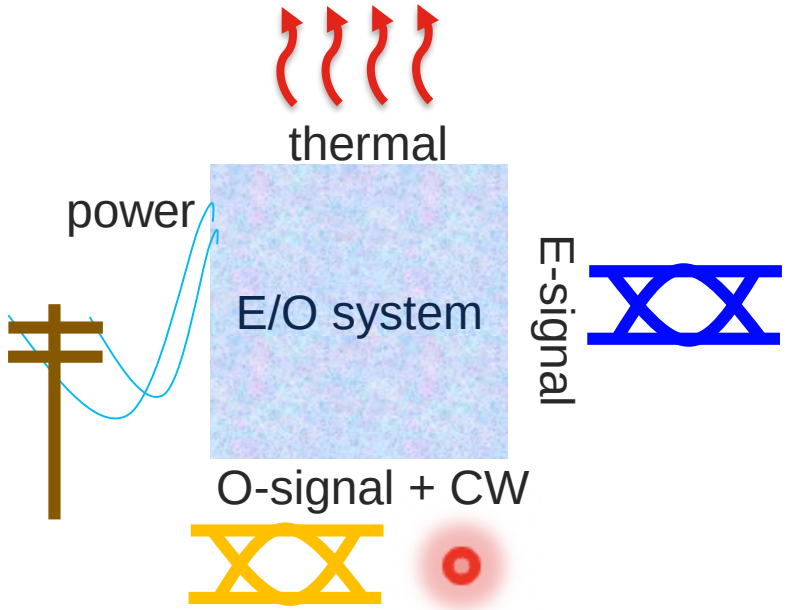
ACACIA

Innovative high-speed Coherent optics

MARCH 2021

The interfaces

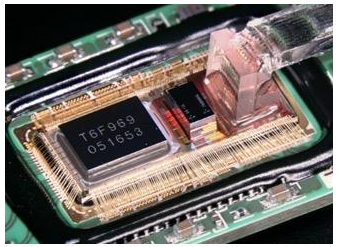




- Photonics adds the need for a 4th packaging interface beyond the 3 classic ones used by electronic systems:
  - Power, Signal, Thermal
  - + optical (“power” and signal)

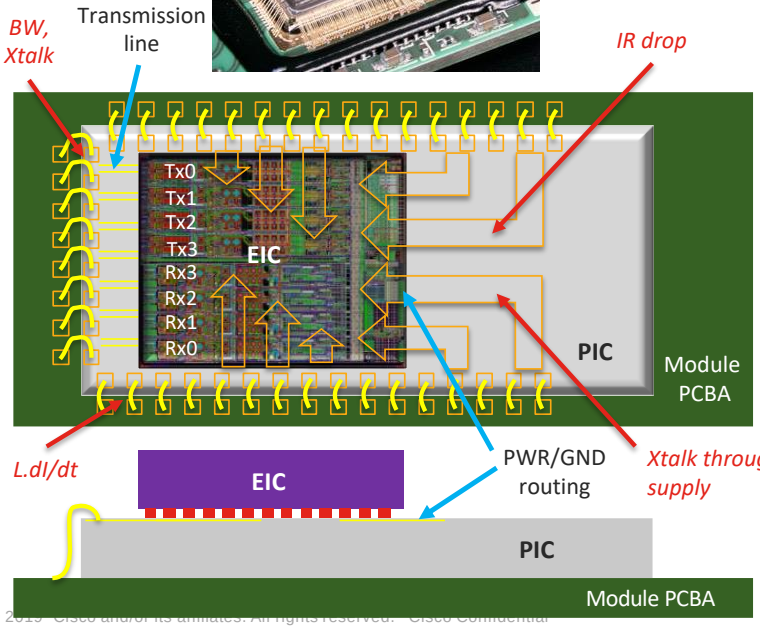
All to be implemented in “quasi-2D” assembly as electronics packages typically are

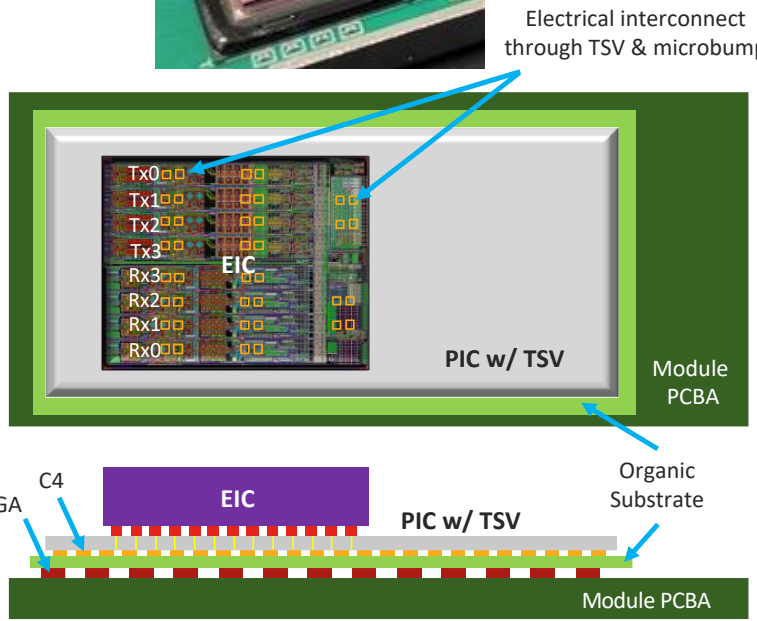
Importance of Packaging: Power Supply



100 Gbps Engine

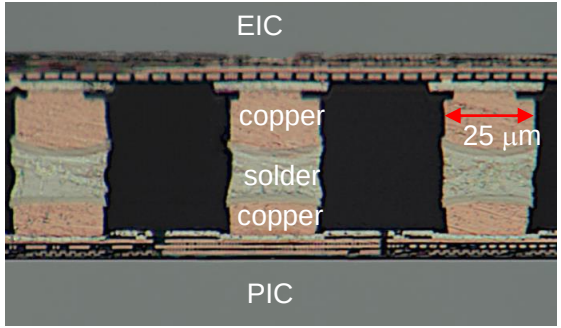
400 Gbps Engine

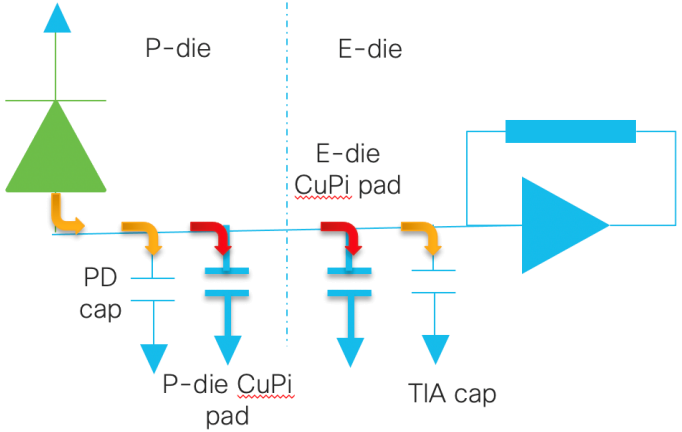




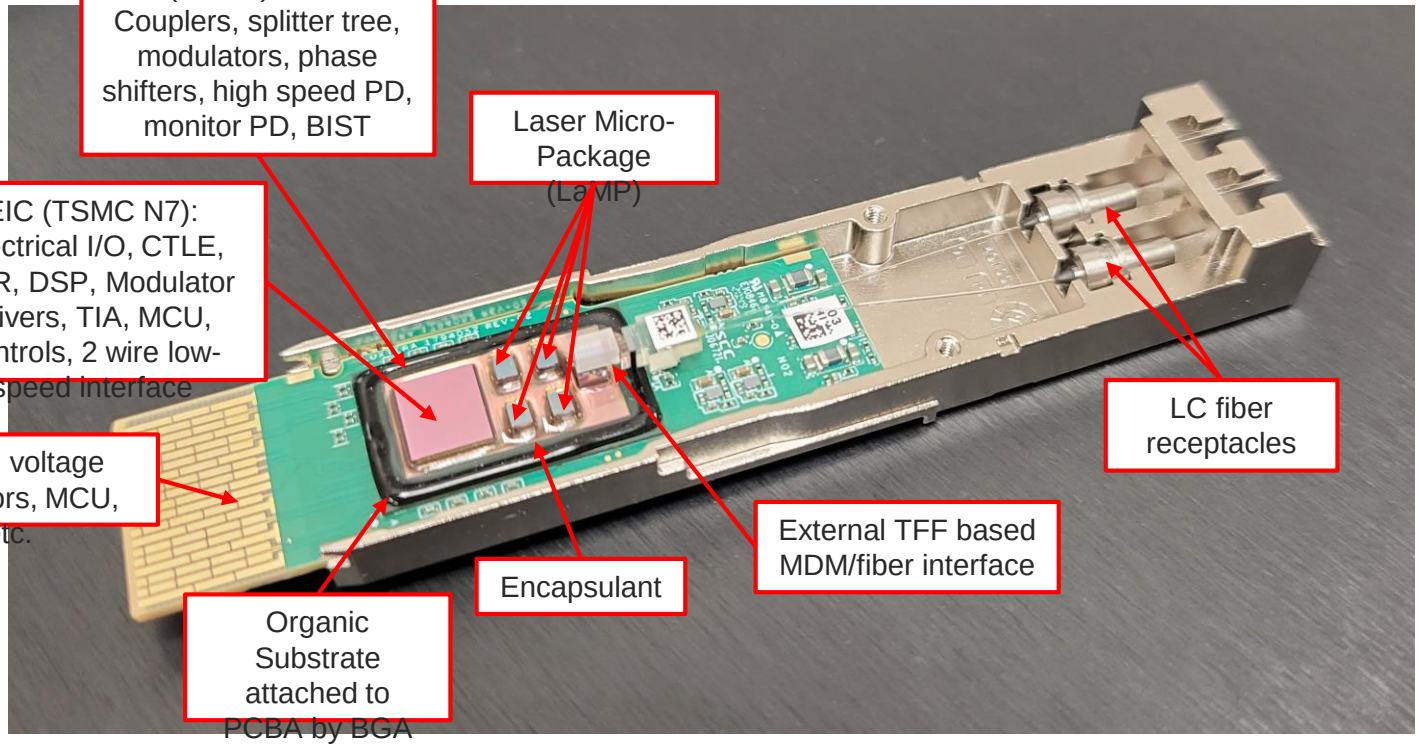
Importance of Packaging: Impact on RX sensitivity

- Receiver sensitivity is determined by transimpedance gain/noise vs bandwidth tradeoff:
  - Strongly affected by parasitic capacitance at the input of the TIA
  - This tradeoff gets even more important at higher data rates
- Hybrid integration between EIC and PIC by means of micro-bumps (CuPi):
  - TIA input capacitance composed of: C_{PD}, C_{pad1}, C_{pad2}, input cap TIA
  - Cu Pi interconnect has ~2 x capacitance of the photodetector
- Mitigation paths:
  - Tuning out parasitics with inductors
  - Reduce micro-bump/pad size, bump-less bonding?
  - Monolithic integration?

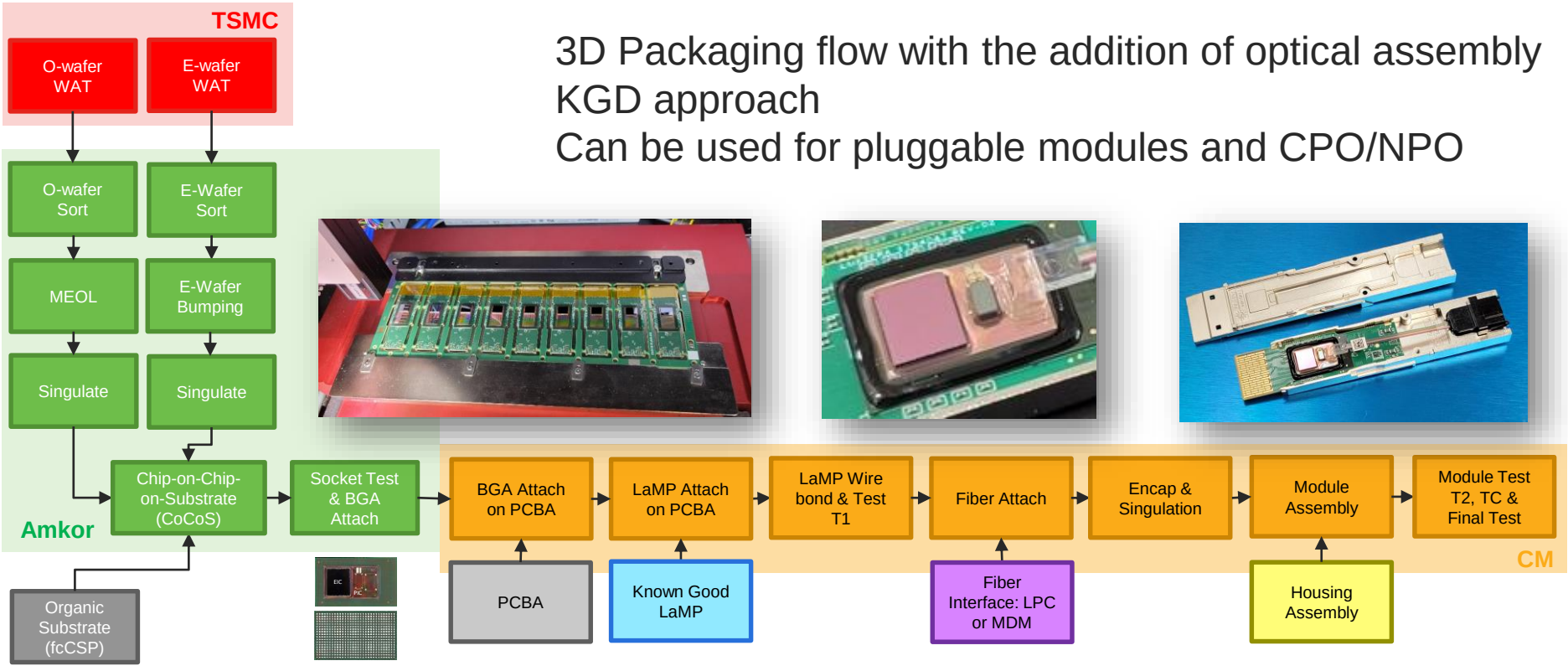




3D Silicon Photonics 400G-FR4 QSFP-DD Module



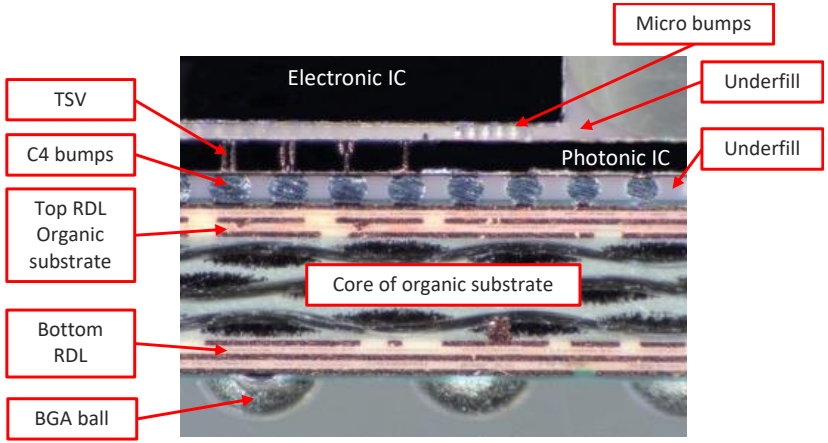
3D Silicon Photonics Manufacturing Flow

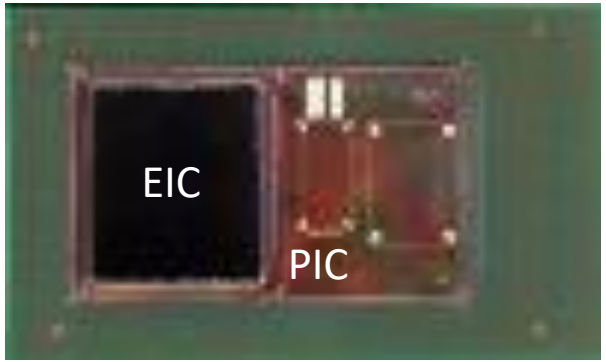


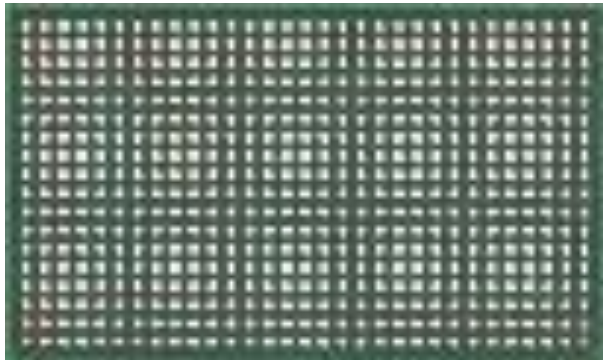
3D Packaging flow with the addition of optical assembly
KGD approach
Can be used for pluggable modules and CPO/NPO

3D Silicon Photonics Technology Platform

- CoCoS: Organic substrate with PIC and EIC
- PIC has Through Substrate Vias (TSV) allowing electrical interconnect through the PIC
- EIC bonded to PIC by micro bumps
- PIC bonded to organic substrate by C4 bumps





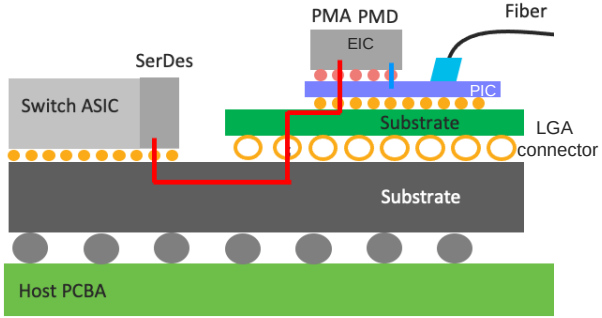


Silicon Photonics Technology Requirements for Current and Future Transceiver Applications

Product Requirements	Technology Requirements
Increasing electrical and optical bit rate: • Electrical: 28 G -> 56 G -> 112 G -> 224 G • Optical: 25 G -> 100 G -> 200G -> 400G	• High BW modulators & photo detectors (50GHz -> 100 GHz) • Support advanced CMOS N7 -> N5 -> N3 • Lower parasitics (R, L, C): TSV/TDV, smaller bumps, bump-less
Increasing integration level (cumulative data rate / chipset): • Larger number of channels and optical I/Os • Higher density: Gb/mm2 • Higher density of power dissipation: heat sink challenge	• Denser interconnect (smaller bumps, bump-less, dense TSV/TDV) • Support larger P-die size (1x reticle sizes or more) & multiple E-die on P-die • Improved thermal interfaces • Support advanced CMOS N7 -> N5 -> N3
Increasing optical device performance requirements: • Support higher link penalties • More extensive use of WDM • High-power, low-noise light source (internal/external)	• Continue reducing insertion losses: grating & edge couplers, waveguides, passive devices • Integrated/external mux/demux • Efficient external light source
Manufacturing requirements: • High-volume, low-cost manufacturing • Time to market	• Leverage mature approaches & technologies • Automation • Minimize complexity

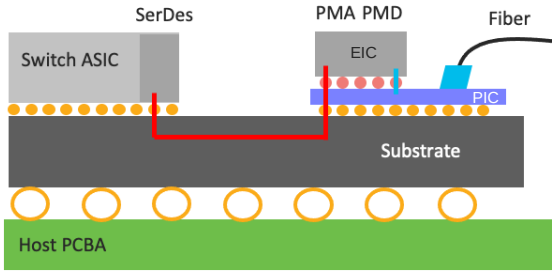
Options for 3D silicon Photonics Co-Packaged Optics

”Near Packaged” Optics by Optical Modules



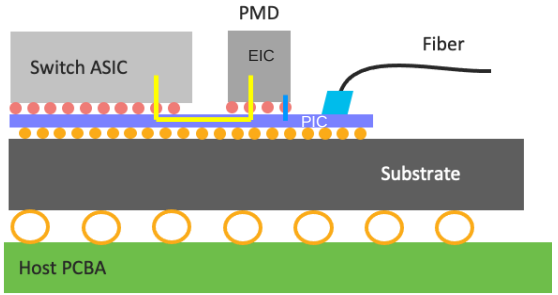
- Optical module: multiple suppliers
- Complex system integration: connectors, size constraints
- Longer traces + connector, not lowest power solution

Co-Packaged Optics by Electro-Optic MCM



- Leveraging existing technologies
- Integration at OSAT
- Shorter traces on substrate no connector, should allow lower power

Co-Packaged Optics by Silicon Photonic Interposer



- Leveraging existing technologies
- Integration at OSAT
- Shortest traces on silicon interposer, should allow lowest power

Summary

- Over the last decade Silicon Photonics has gained significant momentum in HV production of optical transceivers addressing Hyperscale DC, High-Performance computing, Mobile and Enterprise applications.
- As data rates per lane keep increasing: 25 G/l, 100 G/l, 200G/l, 400G/l, the technology needs to to be augmented by introducing more advanced optoelectronic devices and new packaging technologies.
- Silicon photonics in combination with 3D advanced packaging can support the data rate and density optical interconnect roadmaps demanded by the industry.

Acknowledgement

This presentation contains work of
the Cisco teams and its technology partners,
their contributions are greatly acknowledged.

Thank you for your interest

Integration of advanced 3D packaging technologies and Silicon interposers for heterogeneous PIC and EIC integration

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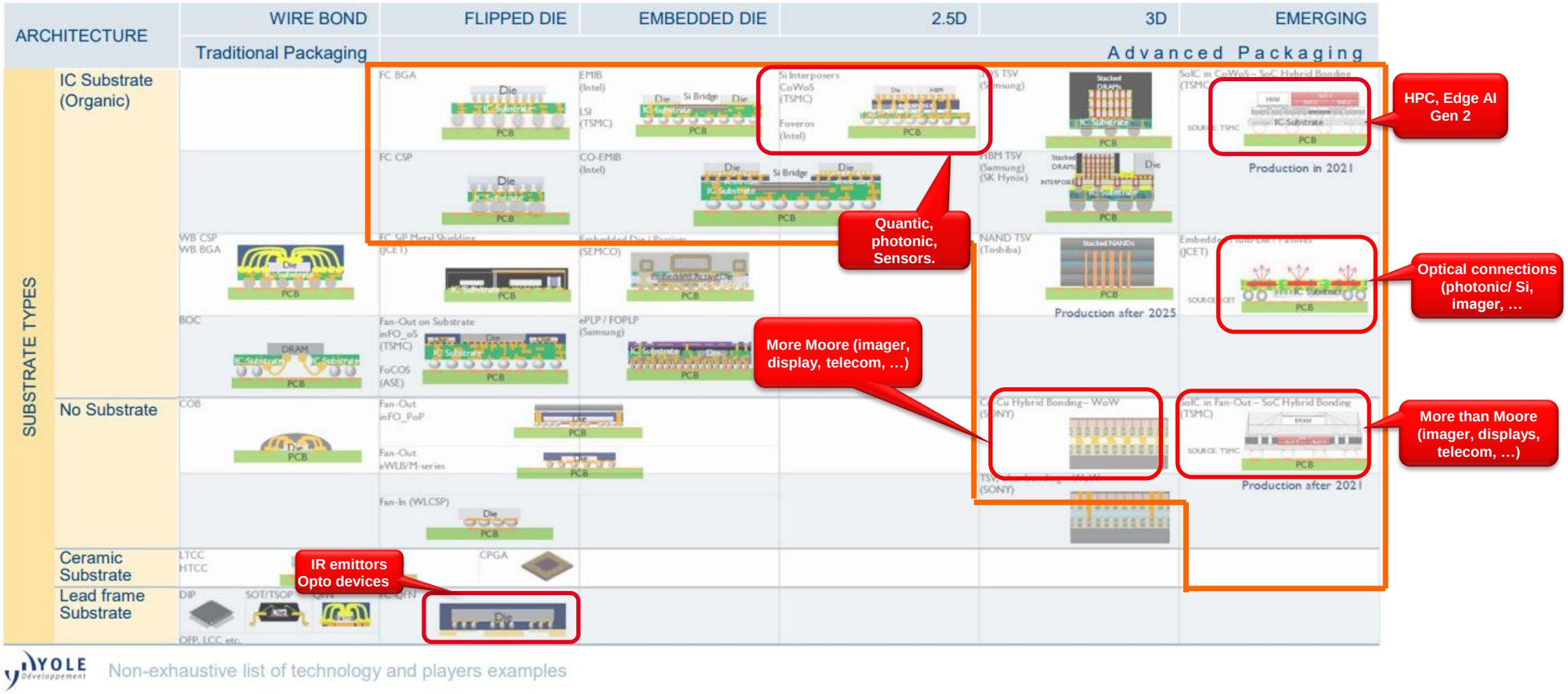
Summary

- ✓ **Introduction**
  - Technological trend overview
  - 3D integration and photonics requirements
    - Technological 3D packaging toolbox
- ✓ **Examples of Photonic devices 3D integration**
  - High speed transceivers
  - Lidar integration
  - Photonic interposer for multichip heterogenous integration

3D Packaging technology overview



3D Packaging is becoming a key integration path for photonic devices integration

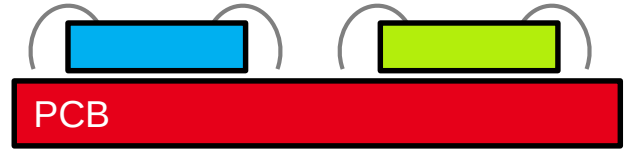
Why 3D packaging

3D Integration General advantages :

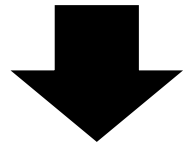
- Smaller I/O pitch
- Density (substrate floor plan reduction)
- Matrix of connections instead of pad rings
- Low L and R (performances and power)

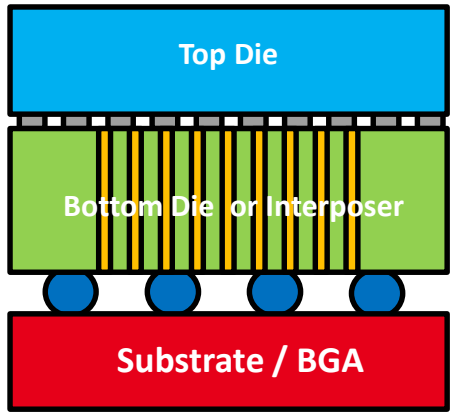
For photonic integration using Si interposer :

- Flexible Heterogeneous dies integration
- Collective fabrication (lower cost)
- Embedded passives
- Thermal spreading



Standard wire bonding





Rerouting layer (Damascene)

Redistribution layer (RDL)

Interconnections (Micro Pillars / Bumps, Hybrid Bonding)

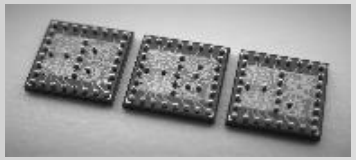
Intra-connections (Through silicon vias)

XY connections

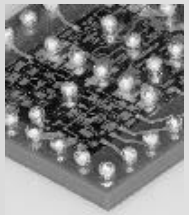
Z connections

A generic toolbox to enable 3D integration

Rebuild Wafers

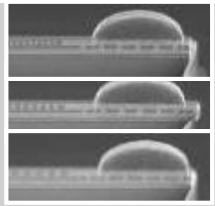


Multi-Die molded
Rebuilt Dies

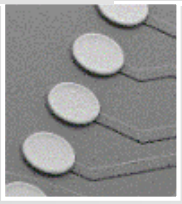


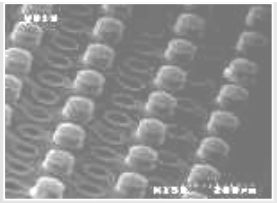
Wafer level Overmolding

Routing

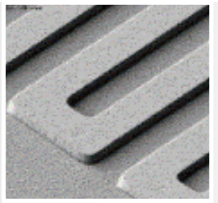


Front-side Cu damascene



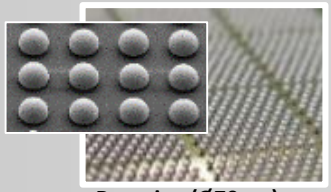


Back-side RDL co-integration (Pitch 20µm) with UBM & BUMP

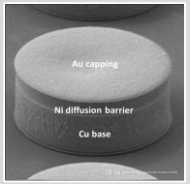


Superconductive traces

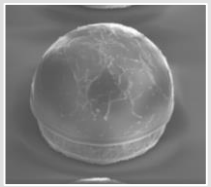
Connecting
Interconnections



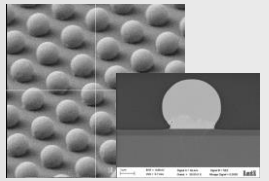
Bumping (Ø70µm)
Balling (Ø300µm)



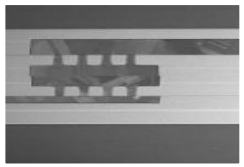
Copper pillars
(Ø10µm)



SnAg Copper bumps
(Ø10µm)

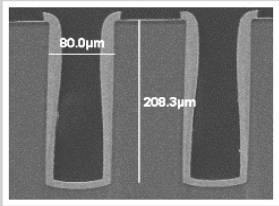


In Balls
(<Ø5 µm)

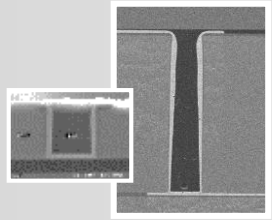


Hybrid bonding

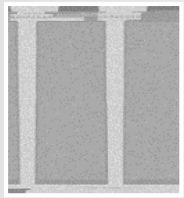
TSV (Through Silicon Vias)
Intraconnections



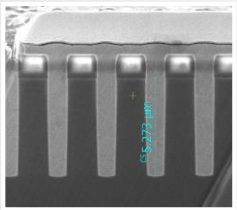
TSV last power (thick Cu-liner)



TSV last process AR 0,5 → 5



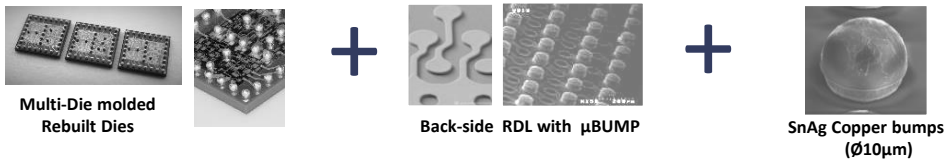
TSV mid Process Ø10µm



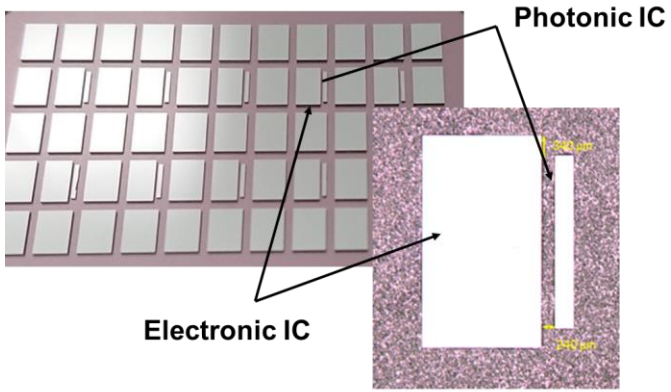
High Density TSV Ø1µm

Compatible with integration on a silicon interposer – chosen depending on final integrated device requirements

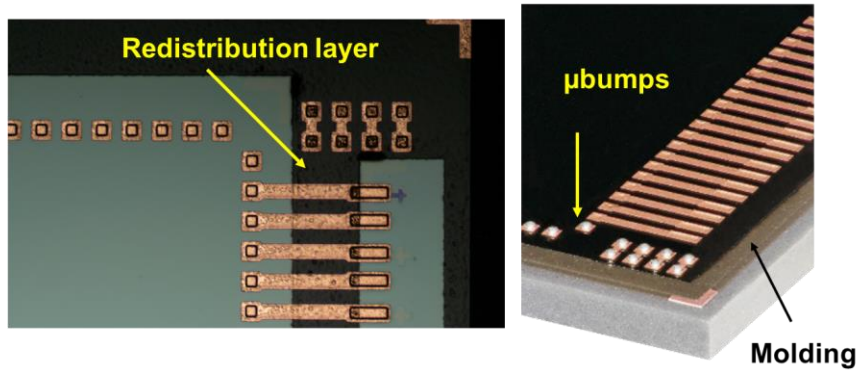
Example 1
Photonic die co-integration and integration on Si interposer



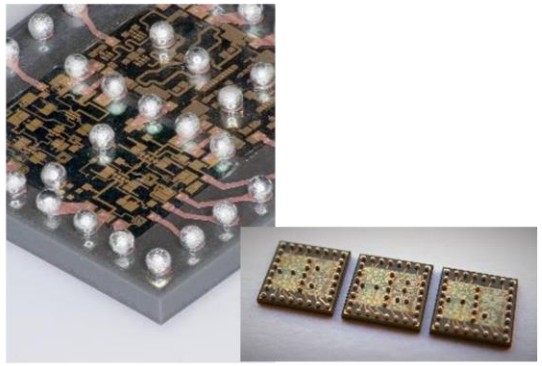
- **High speed tranceivers**
  - ✓ Reconstruction of Electronic (command) and Photonic (Sensor) die for accurate alignment to a fiber array in X,Y and Z



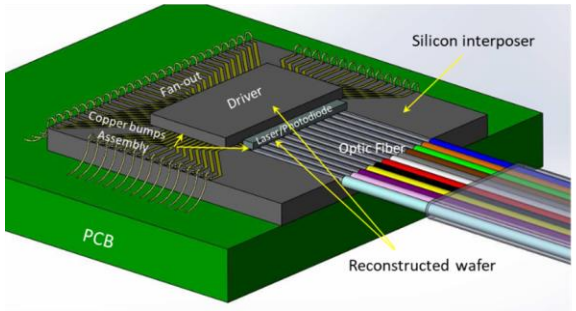
Pick and Place

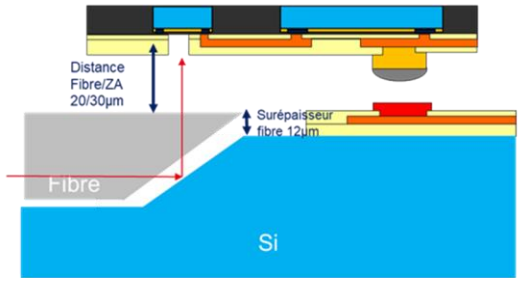


Wafer rebuilding process



Singulation in heterogeneous modules



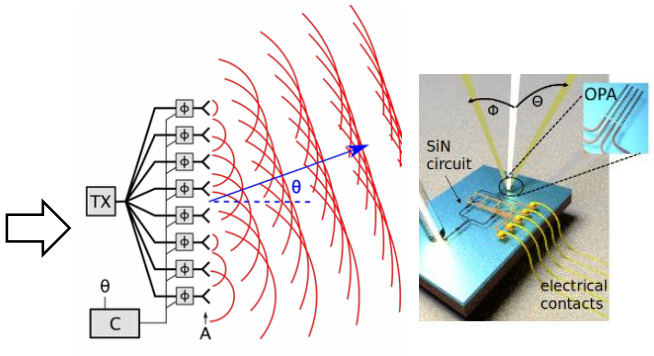


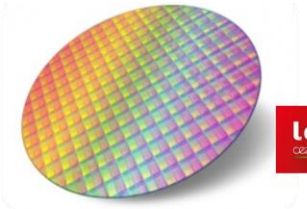
Flip chip of reconstructed module on a Si interposer including V-Grooves and Fan-Out for perfect alignment of light beam with photonic sensor active area

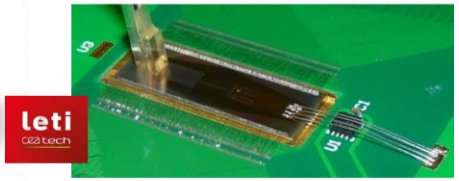
Courtesy of Perceval Coudrain – CEA LETI

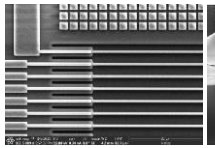
Example 2
Density increase – Next generation of Solid State Lidars

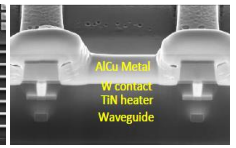
- **LiDAR for autonomous driving necessitates high accuracy and wide angle at long distance**
  - ✓ Mechanical steering devices are much too large and energy consuming for automotive application
  - ✓ Introduction of Silicon based technology : Optical Phase Array





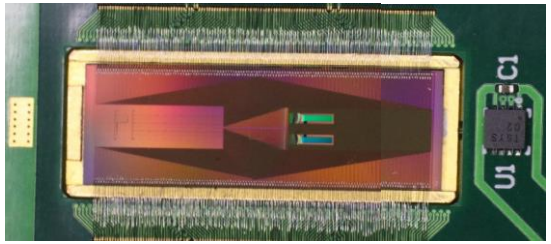


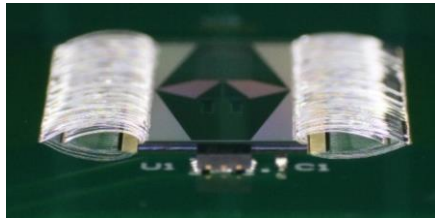


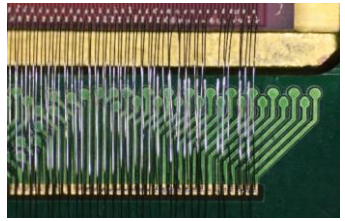


256 channels solid state Optical Phase Array

OPA BEAM STEERING





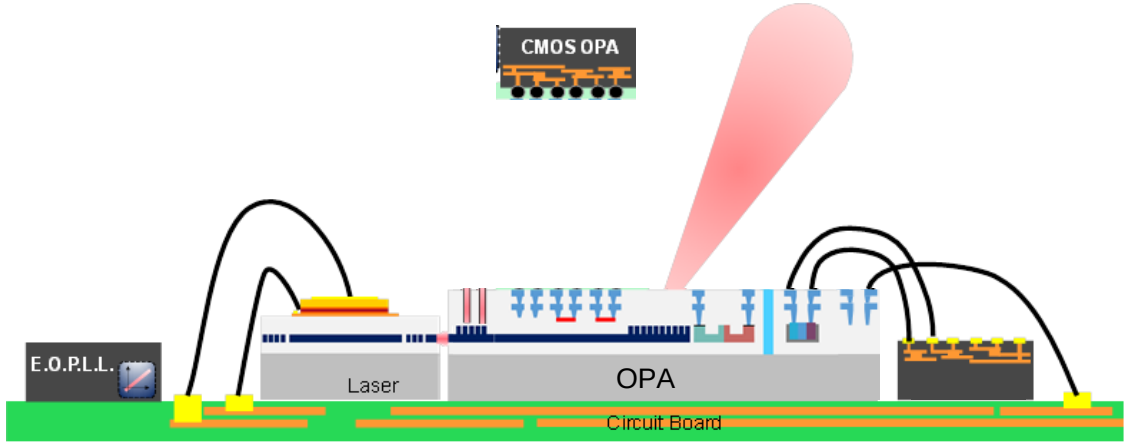


- **Photonics is ready for manufacturing**
- **Challenge is coming from high number of connexions in packaging**

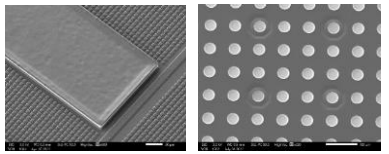
D. Fowler and Al : Journal of Lightwave Technology 2022

Example 2
Density increase – Next generation of Solid State Lidars

- **Solution :** Introduce 3D Advanced Packaging technologies with the right ratio between complexity and performances
- **Solution 1** : Introducing flip chip and RDL routing
  - ✓ The OPA will acts as interposer
  - ✓ Outsourced CMOS command chip hybridized on OPA using lead free solder
  - ✓ Reduction of connections from OPA to command and reception
  - ✓ Higher integration
  - ✓ Keep the surface for laser input and beam steering

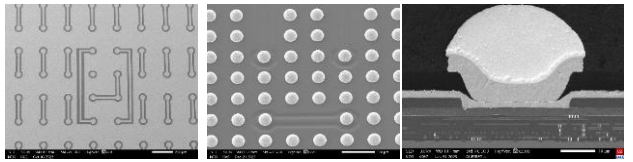


OPA

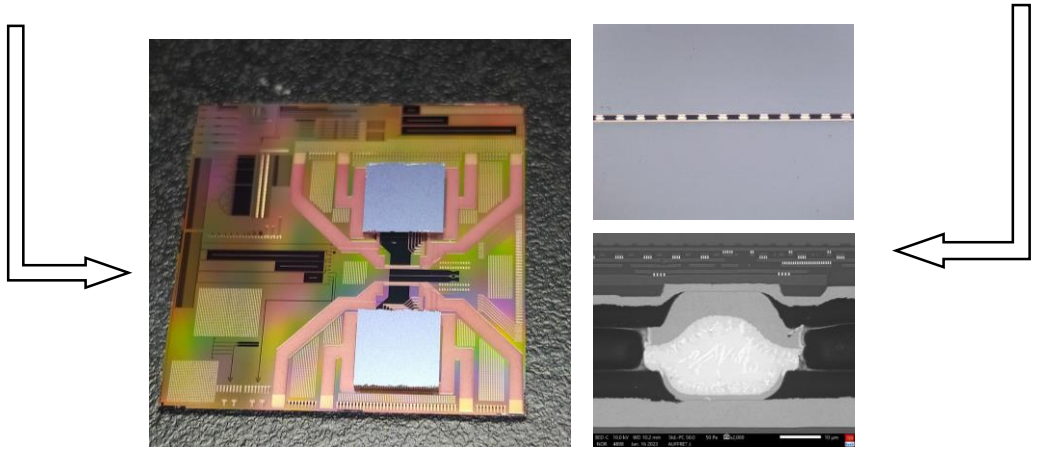


Cu RDL ***Under Bump Metallization***

CMOS



Cu RDL ***CuNiSnAg µbumps***

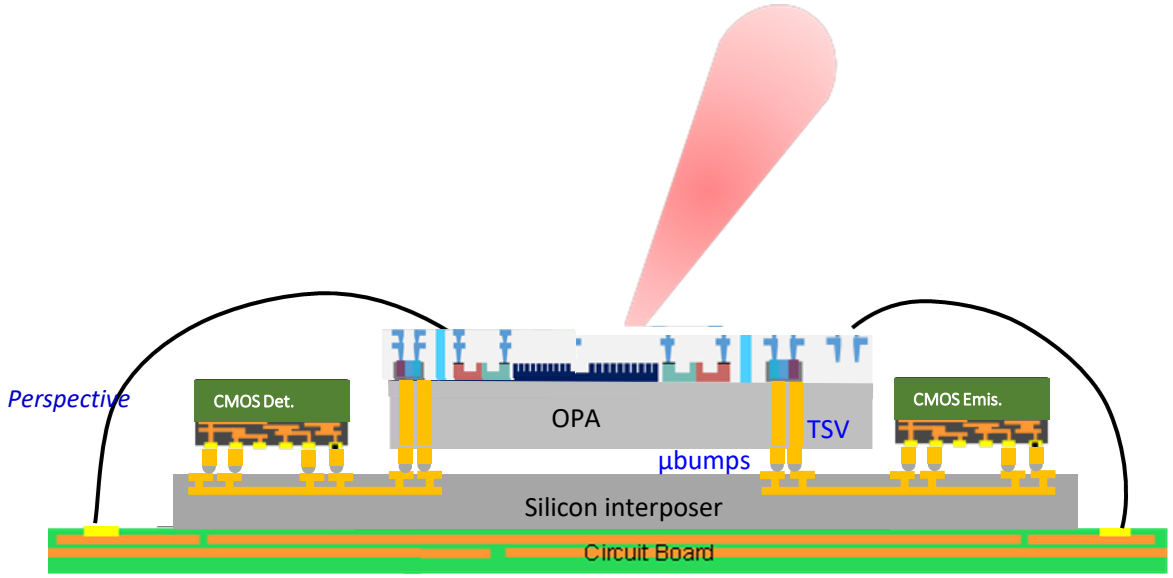


2 CMOS flip chip on Photonic Die (Φ40µm bumps) ***J. Auffret**: IITC 2023*

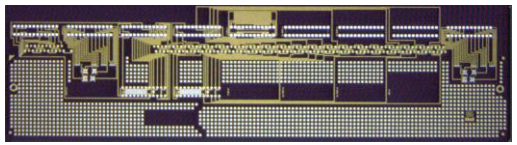
Example 2
Density increase – Next generation of Solid State Lidars

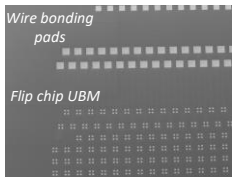
- **Solution 2** : Introducing TSV and Flip chip
  - ✓ Si interposer to route heterogeneous circuit
  - ✓ Mid process TSV combined to fine pitch flip chip to allow further full integration

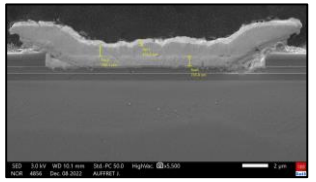
  - ✓ Distribution of all interconnections and routing to photonic die back side
  - ✓ Much higher integration enabled
  - ✓ Keep the Photonic die surface free for laser input and beam steering
  - ✓ Potential integration of multiple heterogeneous dies on interposer



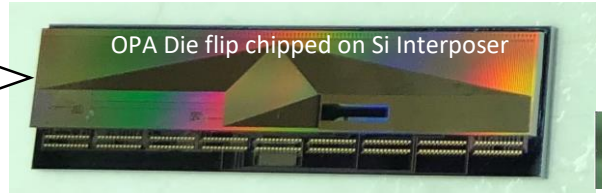
Si Interposer



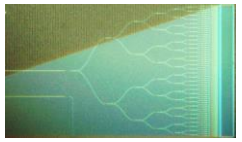


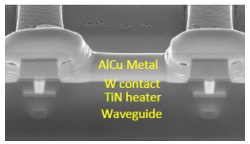


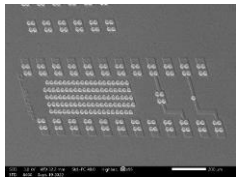
Under Bump metallization *Φ 20 µm UBM*

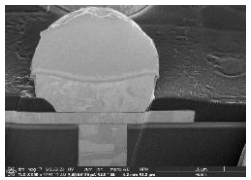


Photonic die

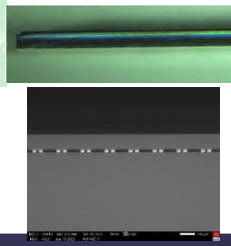


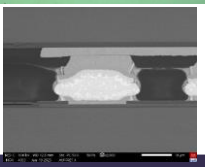






Thinned OPA



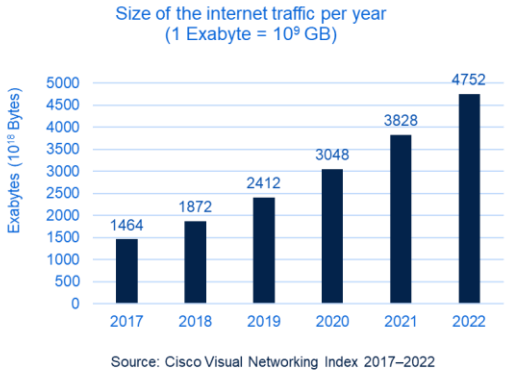


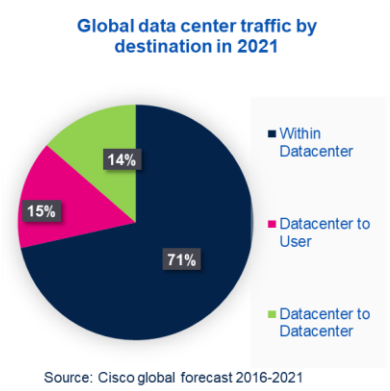
TINKER

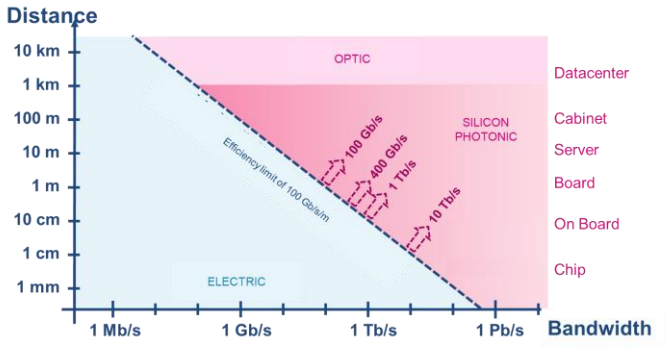
T. Mourier and Al *: "Advanced 3D integration TSV and flip chip technologies evaluation for the packaging of a mobile LiDAR 256 channels beam steering device designed for autonomous driving application" – ECTC 2023 session 6 (May 31st)*

Example 3
Performance increase – Multichip integration on photonic interposer

- **HPC requires increased data transmission and lower latency**
- Integration of multiple chiplets on a silicon interposer have already been developped and reported
- Next phase consists in transmitting the data through the interposer by light

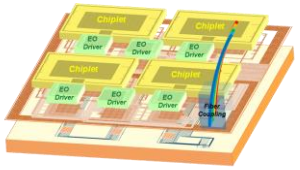


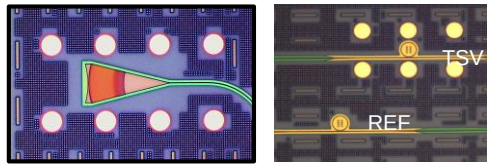




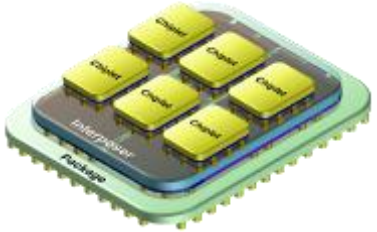
Optical links are faster and more power efficient than electrical links at high speed

Performances / Complexity

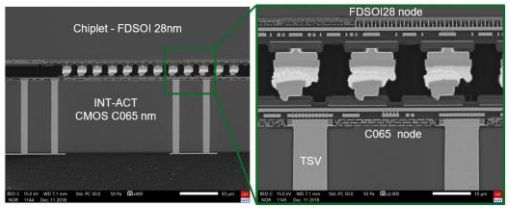




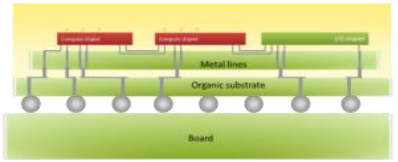
Photonic on Silicon



Active interposer



TSV and Flip Chip



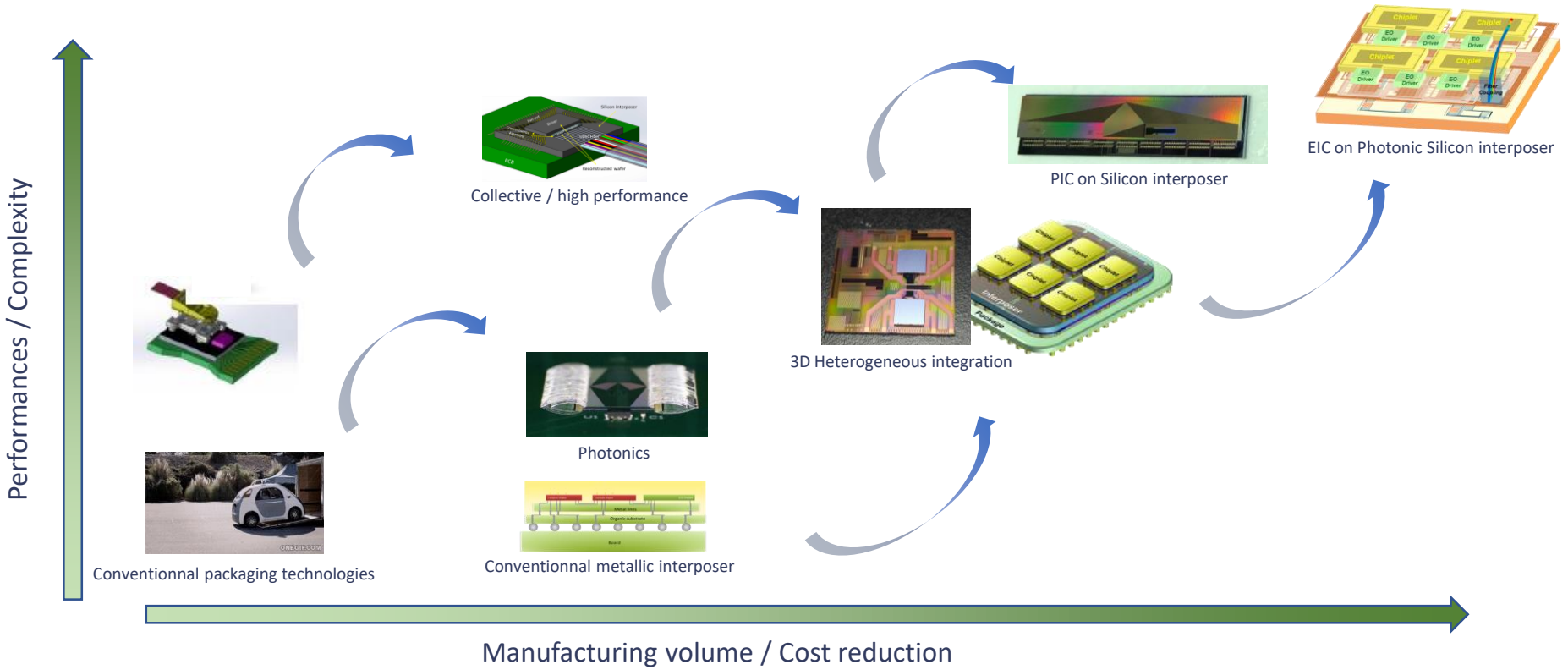
Metallic interposer

Conventionnal packaging

S. Malhouitre and Al *: "Process Integration of Photonic Interposer for Chiplet-based 3D Systems"*
ECTC 2023 – session 1 (May 31st)

Conclusion

- **These are only examples on our developments but trends are clear**
  - Need for heterogeneous integration ➔ 3D integration
  - Need for photonics integration ➔ 3D advanced Packaging
  - Fulfill the market requirements ➔ Trade off between the added complexity, performances, volume and COO

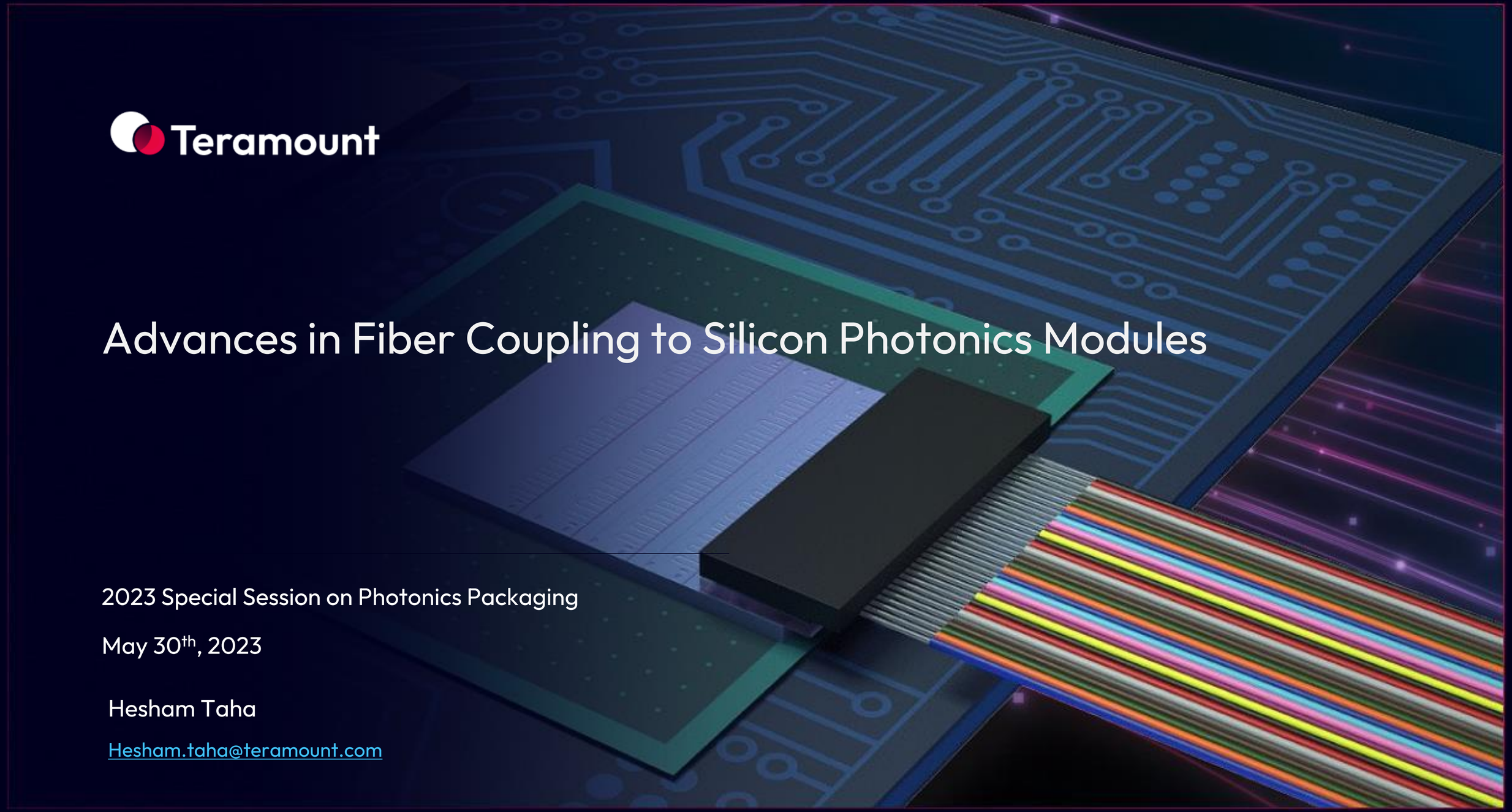


It is just the beginning of the story …

Aknowledgements

- I would like to aknowledge all LETI people involved in the works presented here and the French Miccado Carnot project and the TINKER European project for supporting their realization

THANKS FOR YOUR ATTENTION



Advances in Fiber Coupling to Silicon Photonics Modules

2023 Special Session on Photonics Packaging

May 30th, 2023

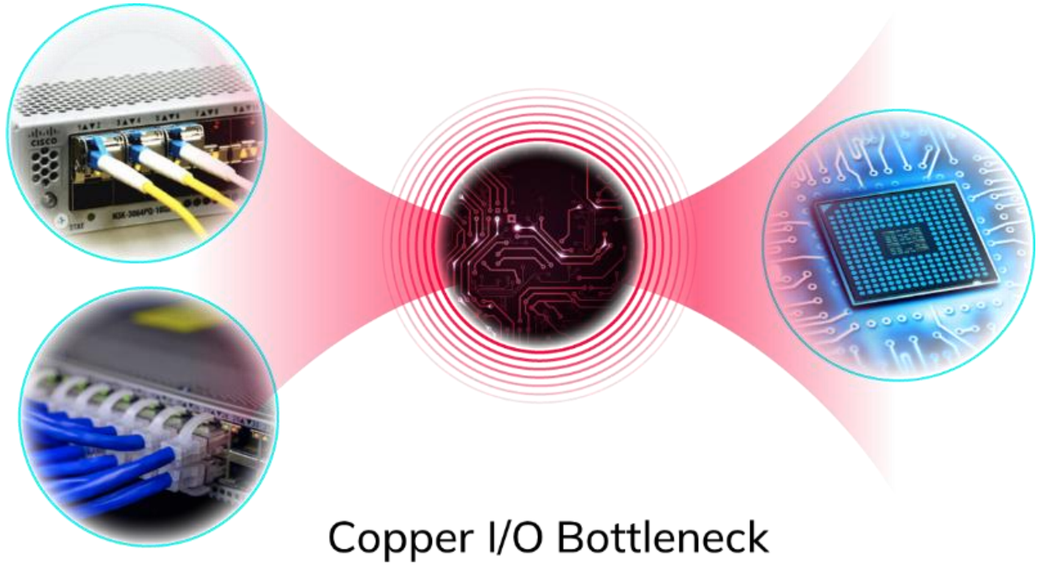
Hesham Taha

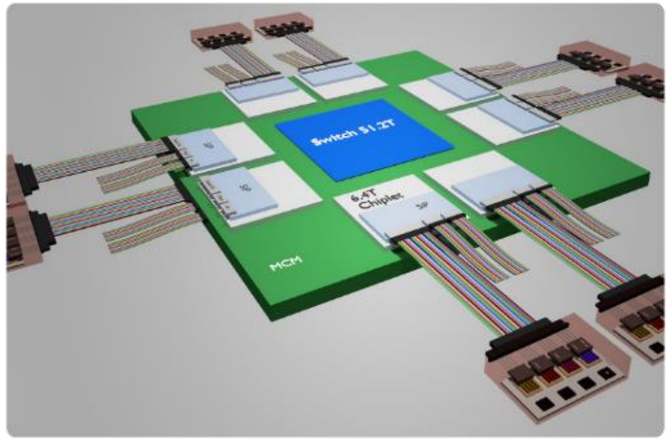
Hesham.taha@teramount.com

Ever-growing bandwidth demand

- Advanced computing and networking applications are limited by copper connectivity

- **Optical connectivity is the ultimate solution for high-speed data transfer, low power and low latency**





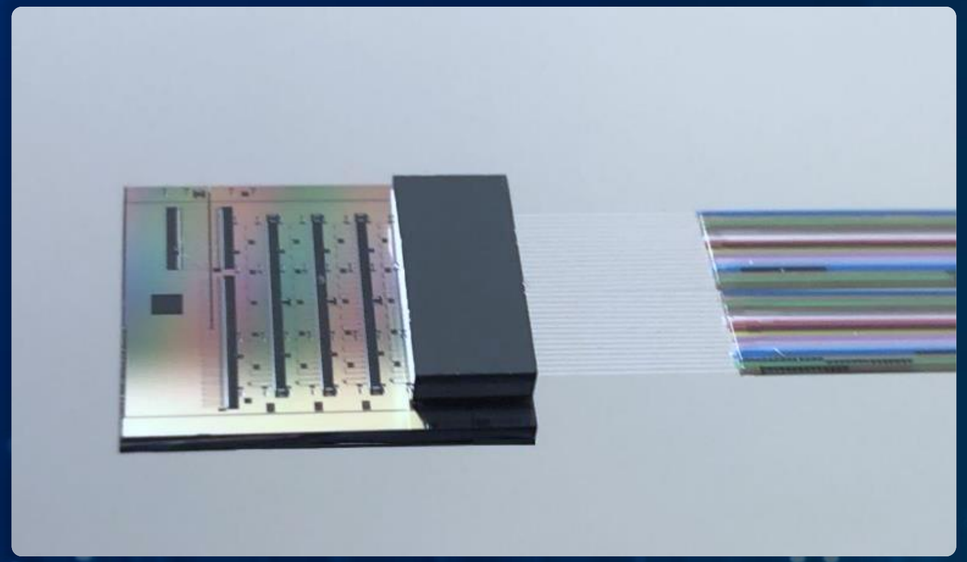
Advanced photonics and electronics packaging requires:

- Use of right building blocks for aligning photonics with standard semiconductor manufacturing and packaging flow

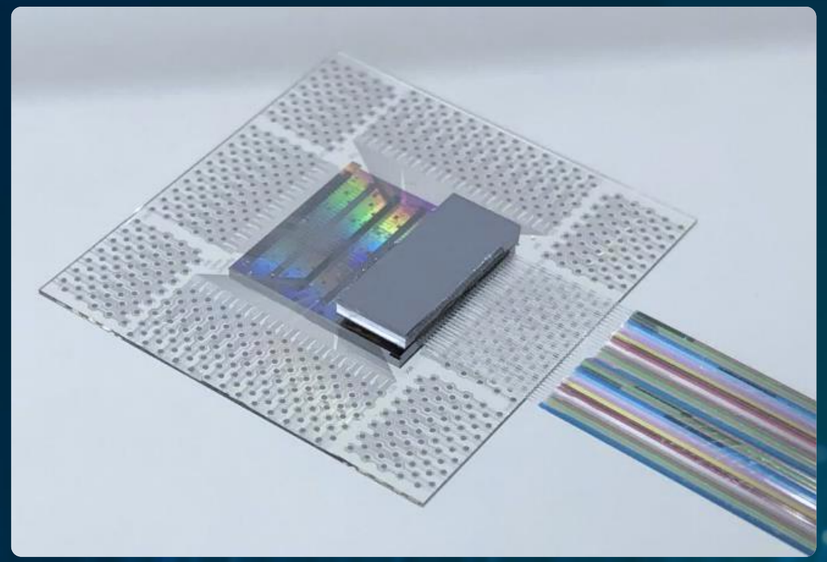
Universal Photonic Coupler

Scalable photonics and electronics packaging

Photonic-Plug: Scalable fiber to SiPh chip packaging



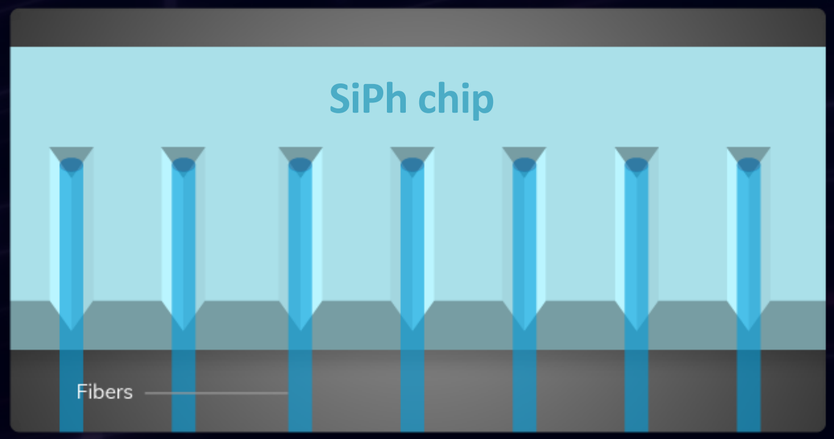
Photonic-Plug: Optical and Electrical packaging



Compatible with standard semiconductor high-volume manufacturing

Current fiber packaging limitations

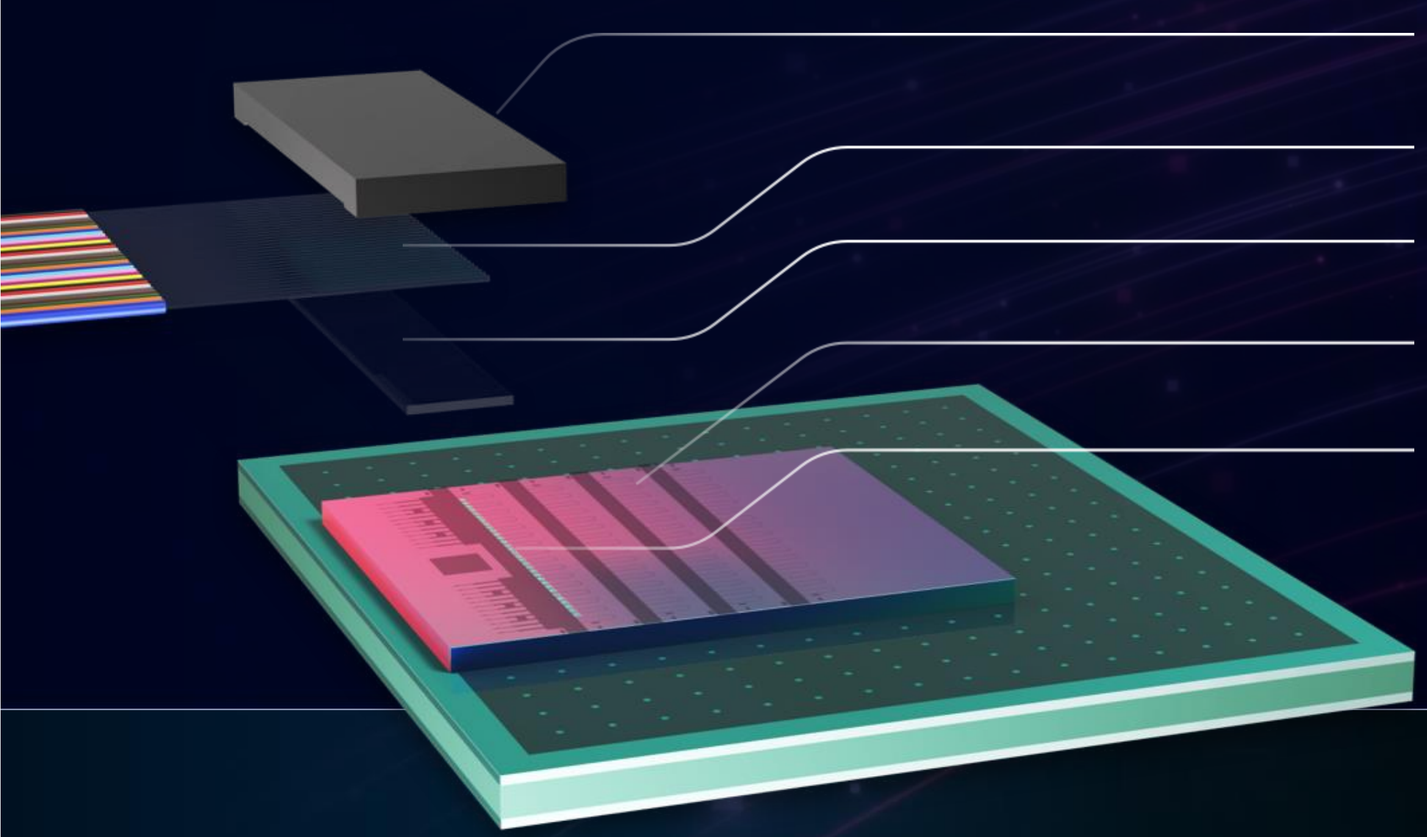
- In-plane (of SiPh chip) fiber assembly – Yield and Serviceability iusses
- Side-coupling geometry – Limits fiber count and wafer level testing
- Reflow compatibility challenges
- In-compatible with 2.5/3D interposer geometries



Direct fiber bonding on SiPh plane

Fibers must be separated from SiPh plane for enabling HVM

UNIVERSAL PHOTONIC COUPLER: PHOTONIC-PLUG + PHOTONIC-BUMP



Self-aligning Optics die

SM and PM fiber ribbon

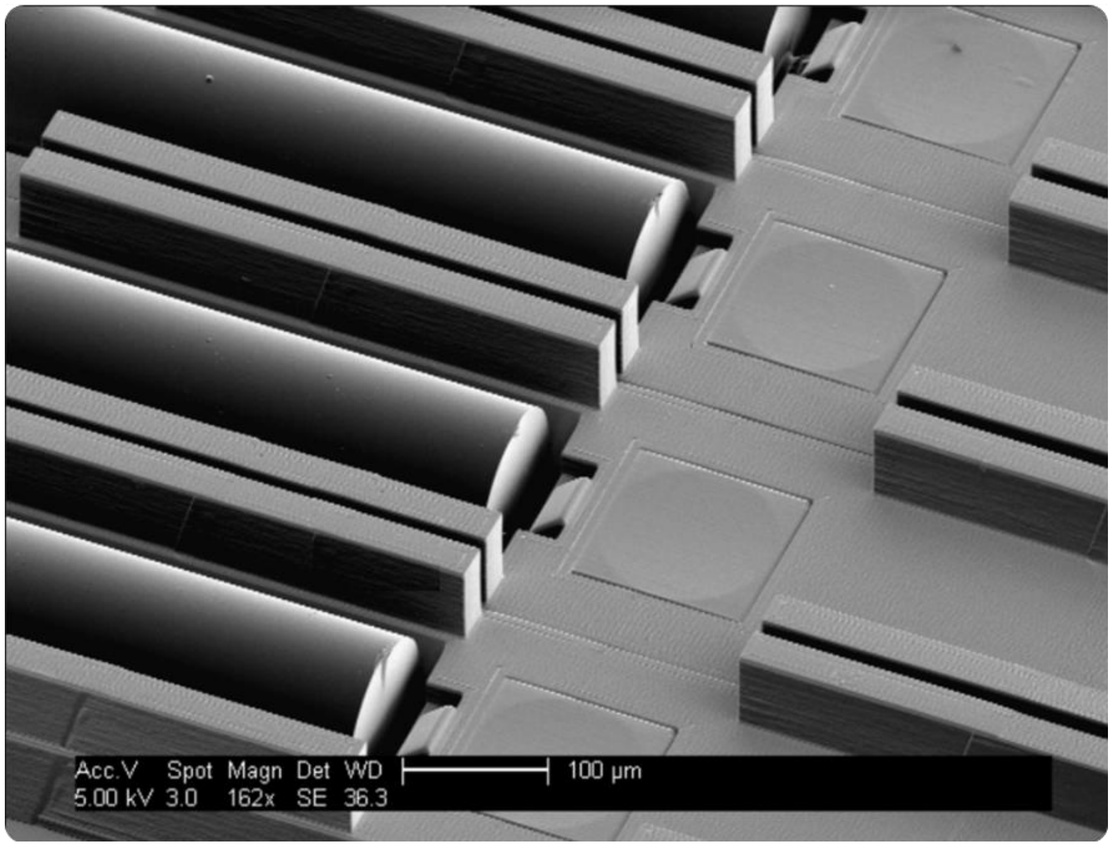
Glass Spacer

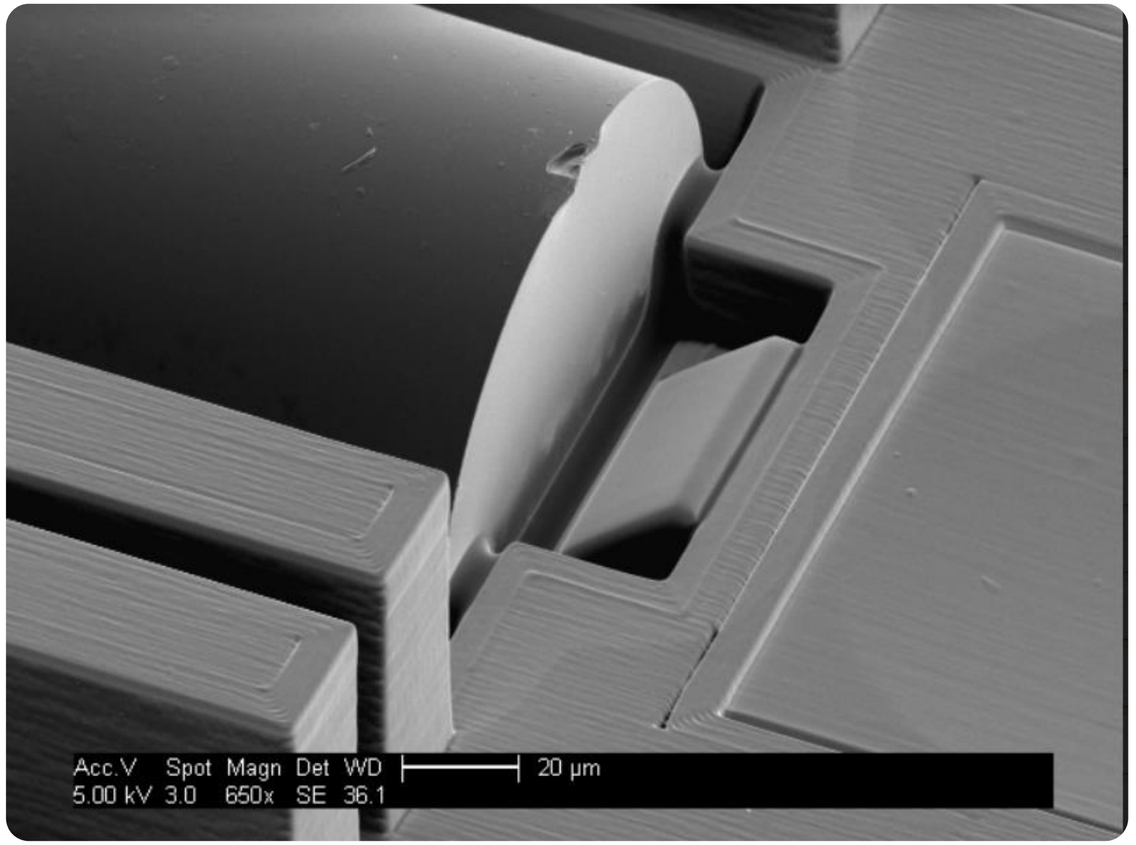
Teramount Photonic-Plug®

Silicon Photonic chip

Teramount Photonic-Bump®

Photonic-Plug – utilizes wafer level fabrication processes

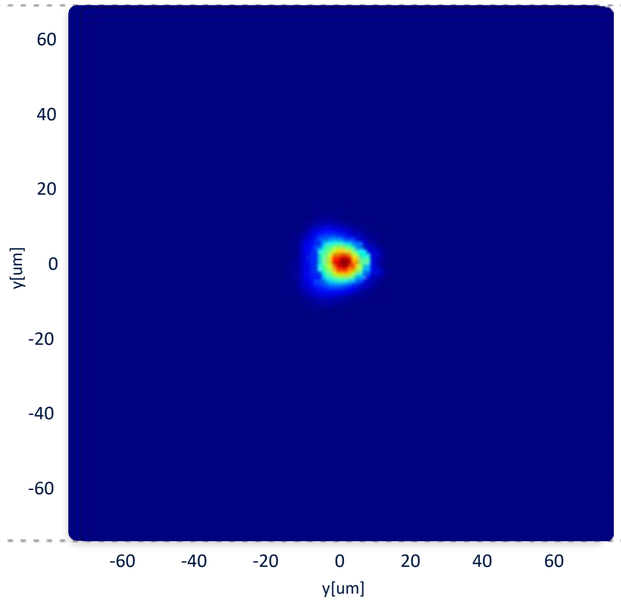




Single-mode and Polarization Maintaining fiber connector

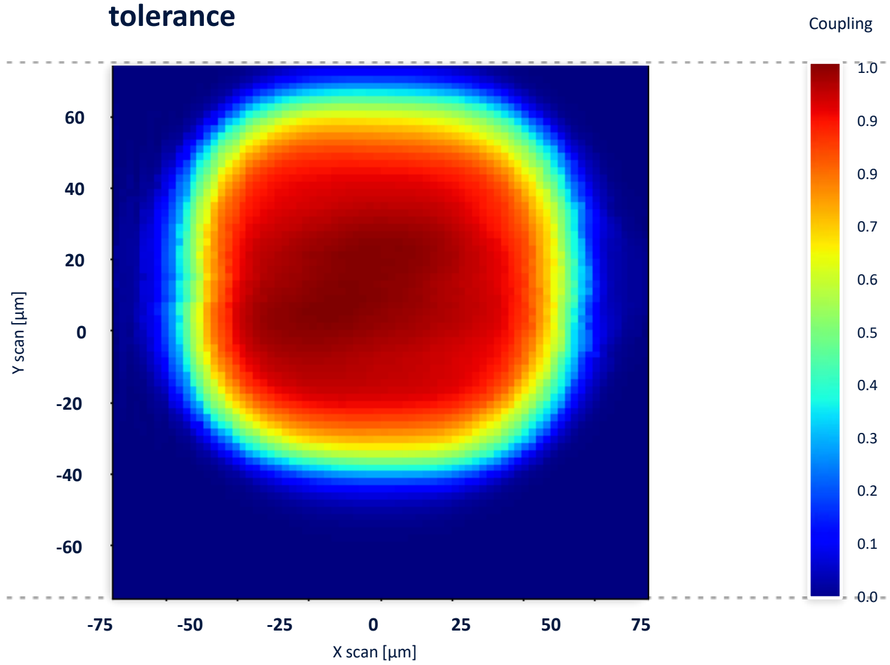
Assembly tolerance comparison

Typical single mode fiber tolerance



Tight tolerance requires Active alignment

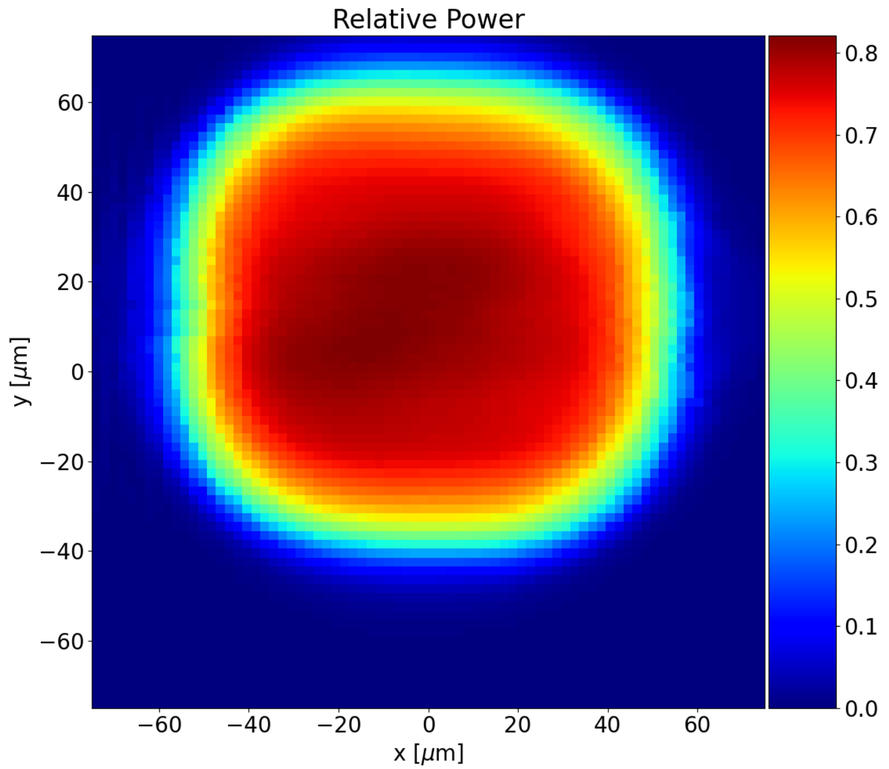
PhotonicPlug measured tolerance



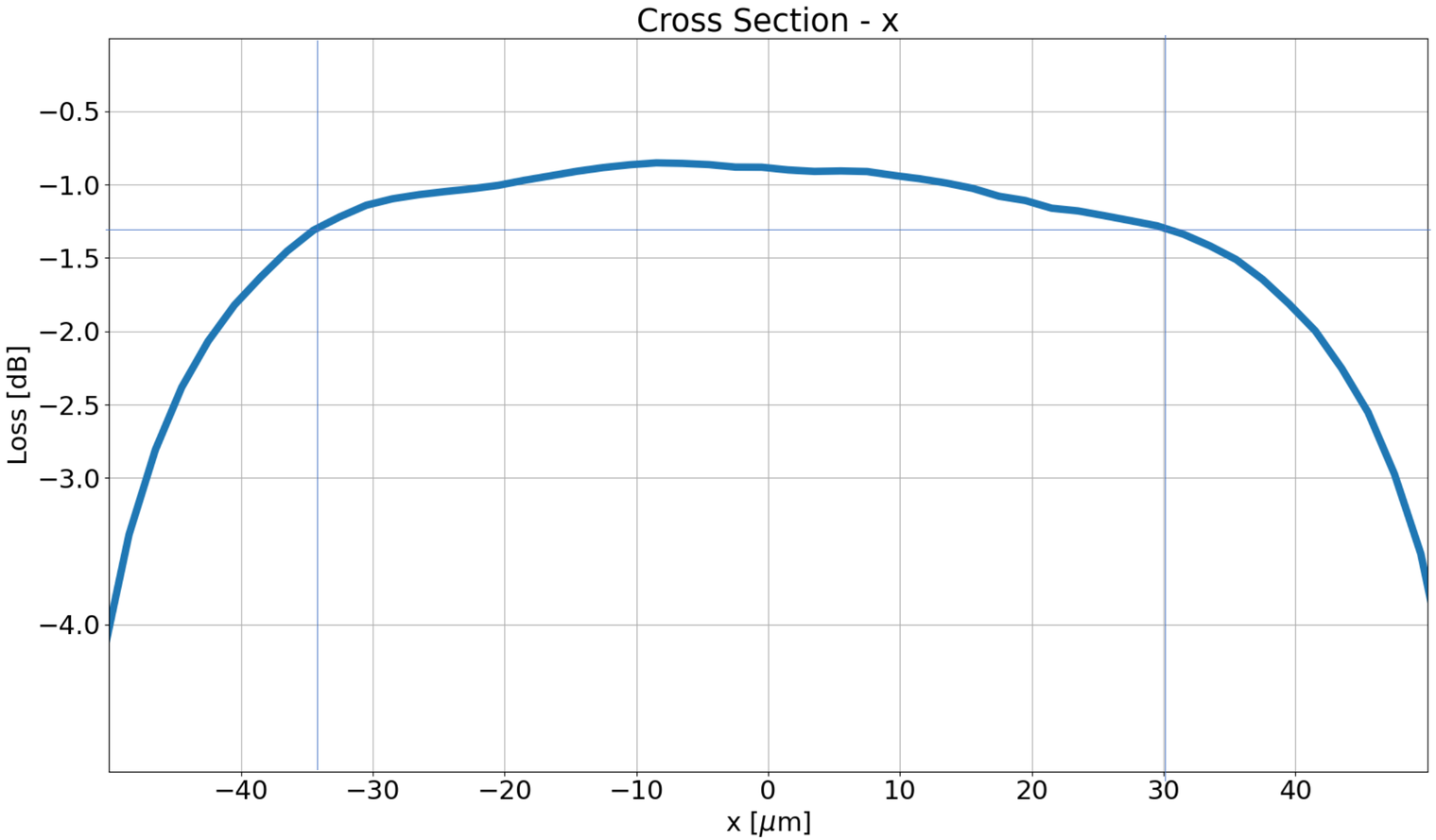
PhotonicPlug large tolerance for Passive alignment

Photonic-Plug: >100x unprecedented tolerance improvement

Assembly tolerance >± 30µm/0.5dB



PhotonicPlug XY measured tolerance map

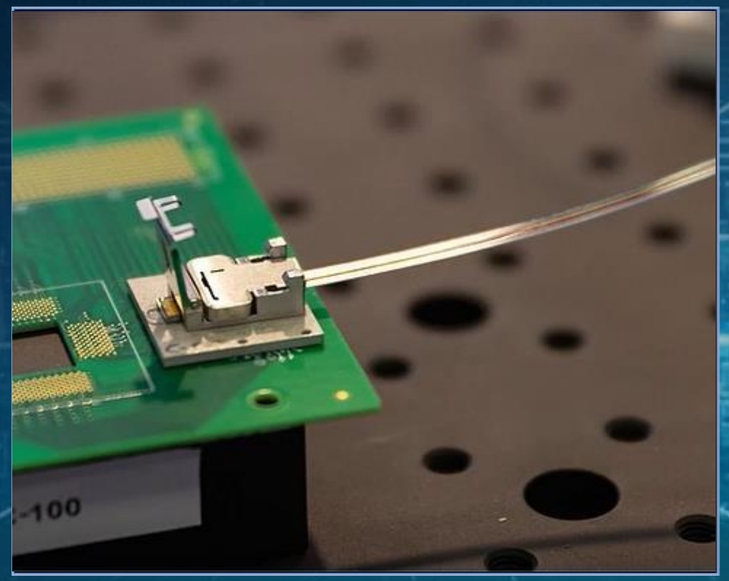


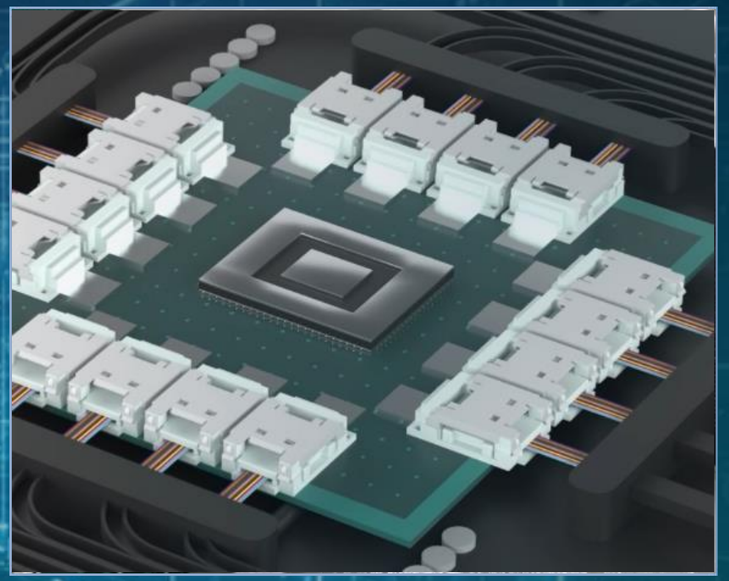
Cross section shows misalignment tolerance

8

Teramount

Detachable PhotonicPlug: Game changer for co-package optics





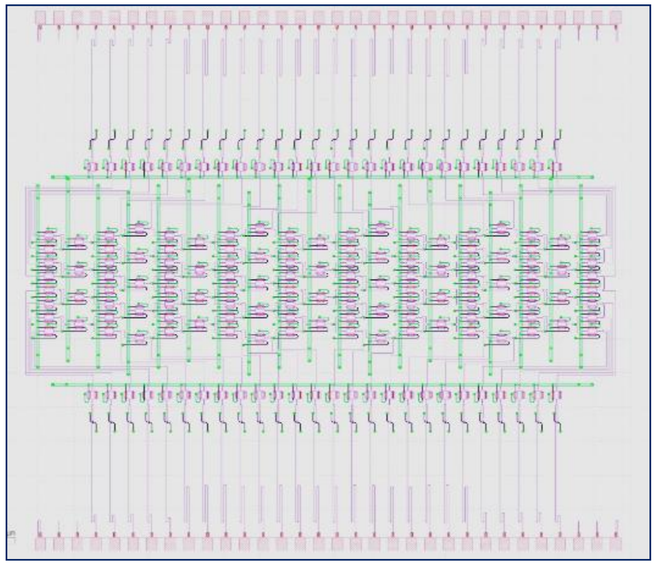
- Detachable/Serviceable fiber connector
- Post reflow fiber assembly
- Simple reworkable connectivity for CPO

Eco-system enablement

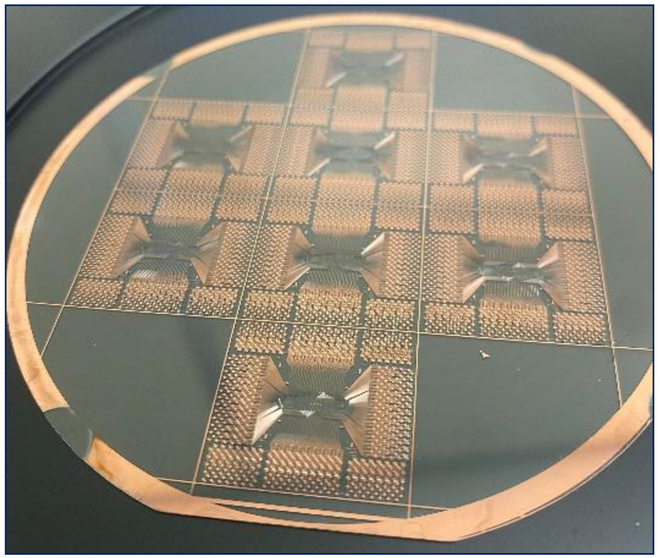
Photonic-Bump ready wafers announcement:

Photonic-Bump and Detachability extend fabless model to silicon photonics

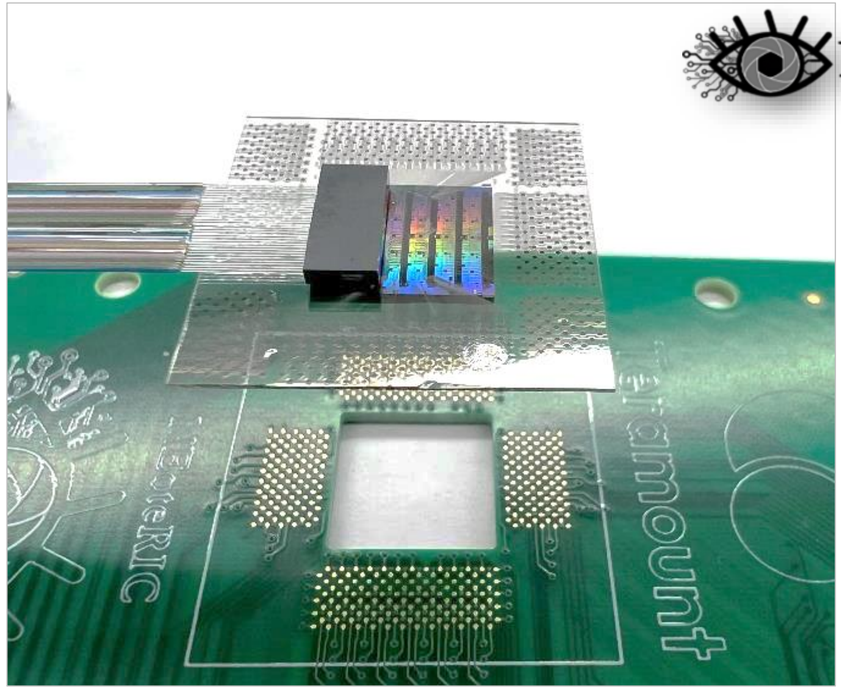
Silicon Photonic die with 64 “Photonic Bumps” and 450 Electrical bumps



Bumped SiPh wafer



Fan-out Glass Interposer

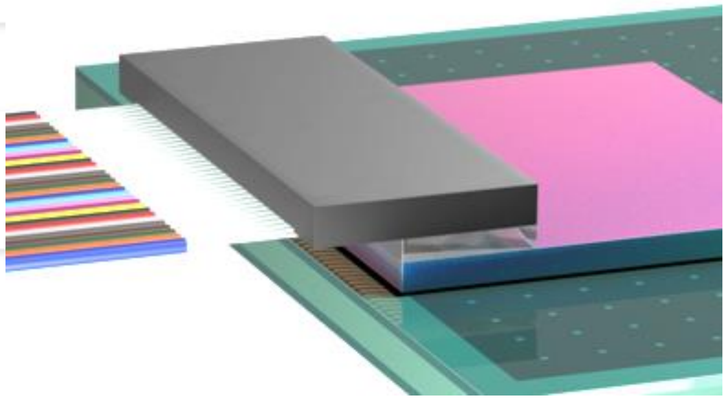


Photonic-Plug, Glass Interposer and Bumped SiPh die

All optical and electrical I/Os are connected by one flip-chip assembly

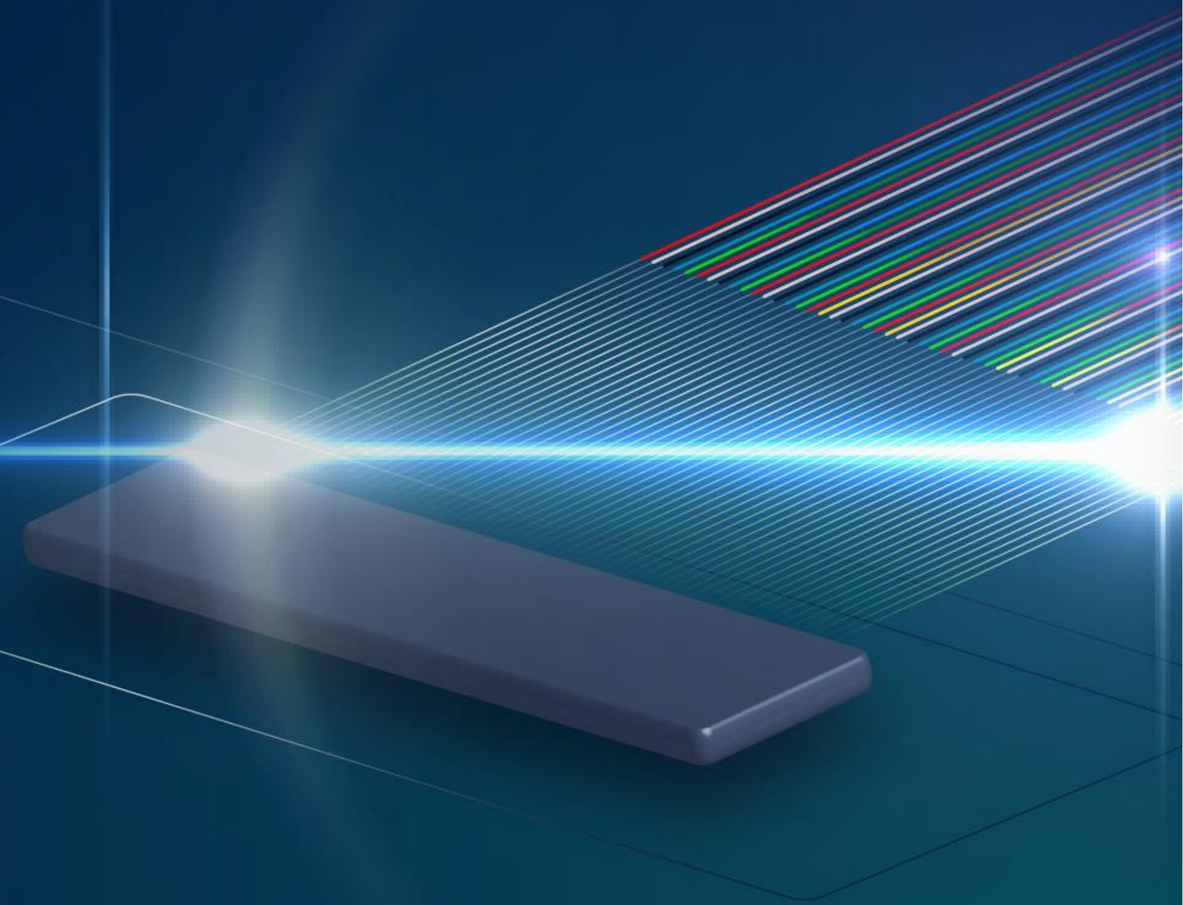
Photonic-Plug and Photonic-Bump integration

- **Fiber planner separation:** Interposer geometry & TSVs
- **Surface coupling:** Photonic-Bump wide-band surface coupling; wafer and die test
- **Wafer level optics:** Large assembly tolerances – standard packaging flow
- **Serviceability:** Detachable and post-reflow fiber assembly



Teramount

Thank you



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Advanced Photonic packaging and system integration for CPO

Laser-PIC coupling the ultimate challenge

Alexander Janta-Polczynski

IBM Bromont – Semiconductor Assembly and Test

ajantapo@ca.ibm.com

Booth #211

IBM Bromont Advanced Packaging / HI Infrastructure

IBM Albany Research Advanced HI R&D.

- Class 1000 Cleanroom space
- State of the art HI Line
- Focused on 3DHI technology
- Hybrid bonding, HD substrate, DBHi technology, …
- Transfer of technologies to IBM Bromont for production

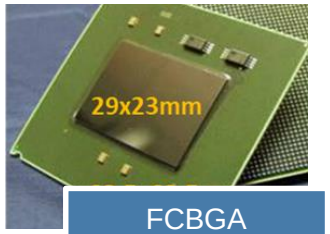
IBM Bromont / C2MI Development and HVM capability

- 50 yr Packaging facility serving both IBM and non-IBM customers (majority) for advanced flip chip, SIP and test production
- Partnered with C2MI technology incubator
- Massive expansion planned in both capability and capacity supported by Canadian Government funding

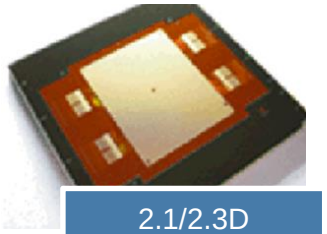
North-East Advanced Corridor play to address NA Supply Chain needs.

- IBM Albany R&D capabilities and alliances/ network
- IBM Bromont production capacity
- Packaging Development ecosystem with C2MI
- Addresses the lack of advanced packaging capabilities in North America (weakest link of supply chain)

IBM Bromont - Advanced Packaging

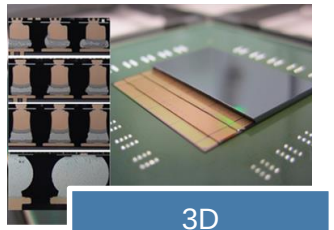


FCBGA

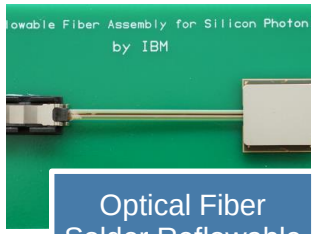


2.1/2.3D

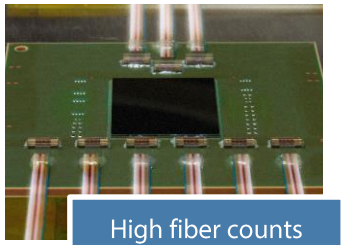
2.5D



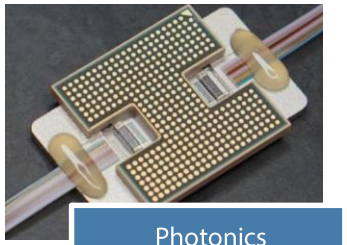
3D



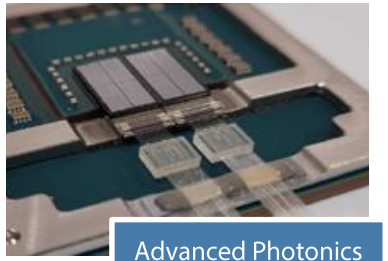
Optical Fiber Solder Reflowable



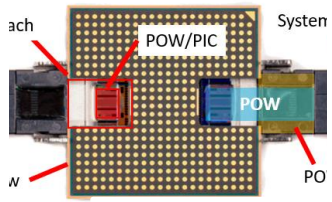
High fiber counts



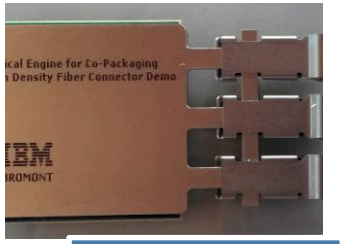
Photonics



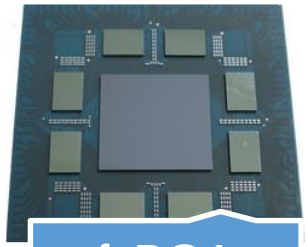
Advanced Photonics



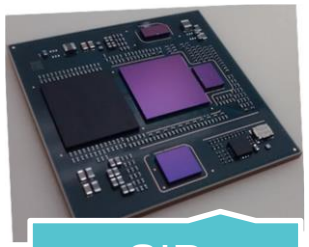
High density optical ports counts



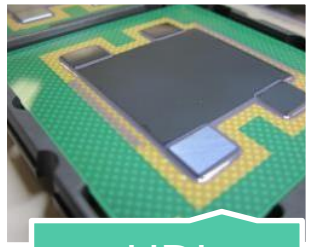
Integration



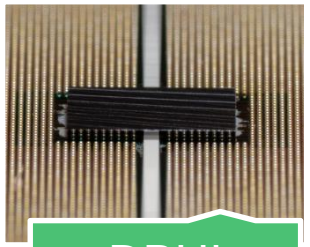
fcBGA



SIP



HDI

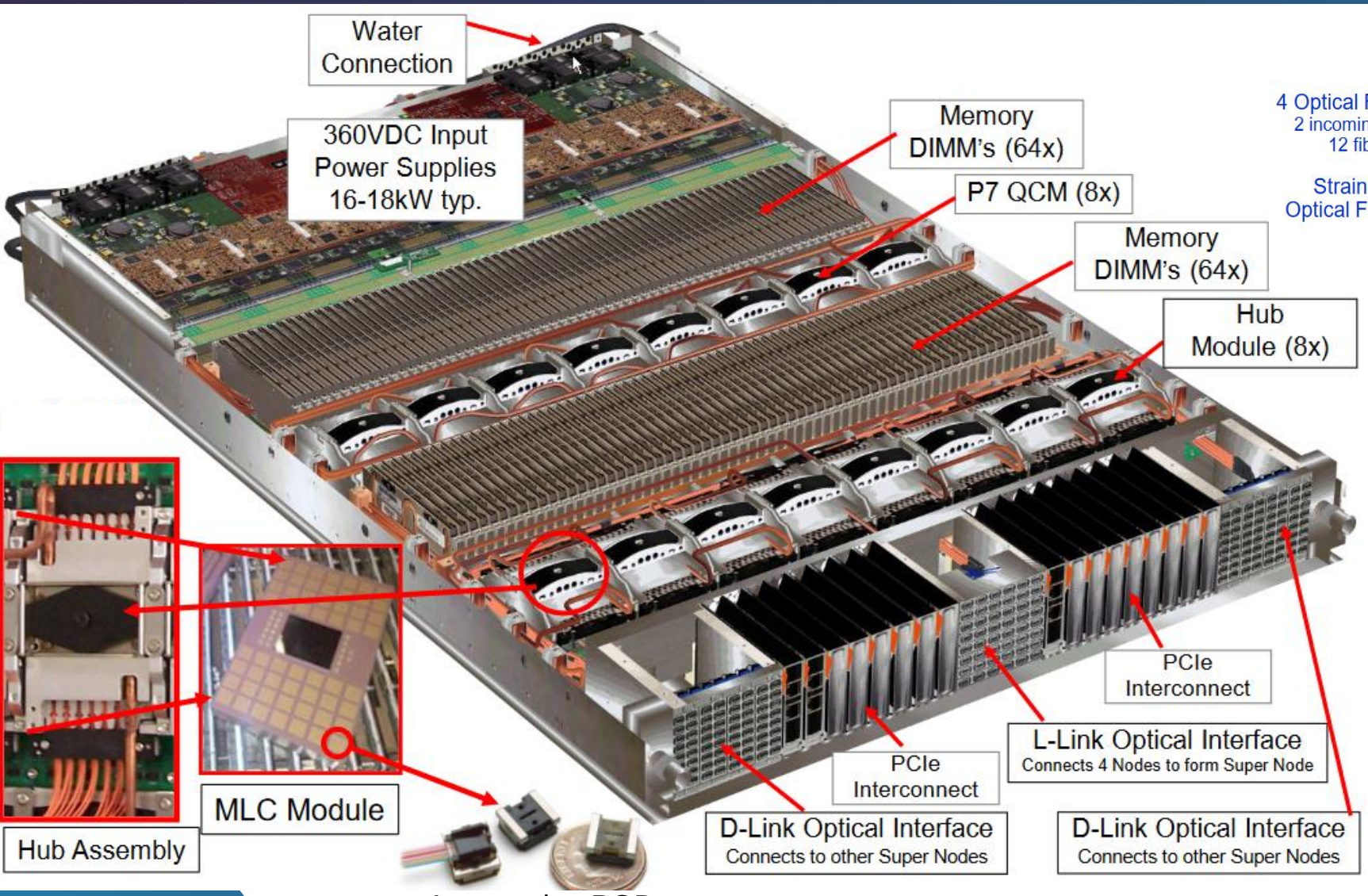


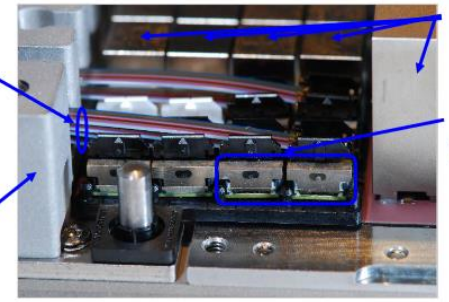
DBHI

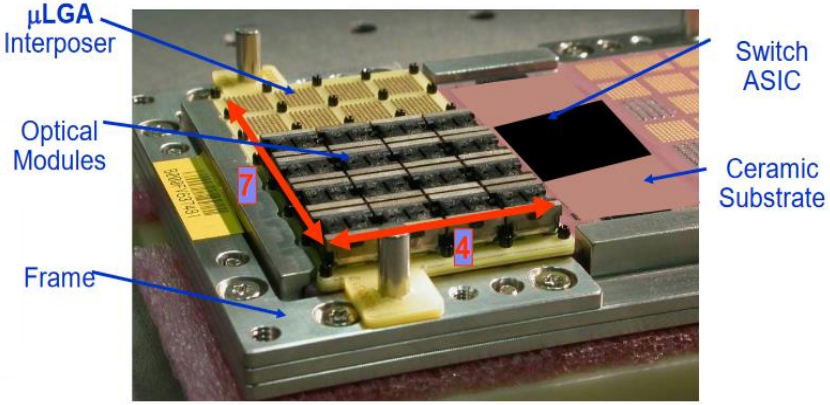
CPO MOM

CPO MOM

IBM Power 775: 1st Commercial CPO







24+24 Tbs from drawer

IBM expertise in system integration

Made in Bromont

CPO Benefits

- **Increasing BW towards ASIC**
  - Electrical IO constraints
  - Bandwidth X distance metric
  - IO on both sides of package
- **Reduction in Power Consumption**
  - Proximity = Lower power SERDES
  - Change the power envelop trade-off
- **Expansion of ASIC performance**
  - Chiplet partitioning with HI
  - Reduction in Cost
- **Advance cooling strategies**
  - CPO MCM/HI increase density
  - ~10x reduction in floor space

Full Wall plug efficiency must include light source !!

Bandwidth scaling = Increase Radix

study from HPC area

- 4.2x more servers per 1st-level switch
- Reduce a hop level
  - improved network locality
  - fewer switch modules 86%
- 4x higher bisection bandwidth
  - packet deliveries
  - less network contention
  - faster and more energy efficient

POWER Efficiency

Type	pJ/bit
FPP	20-30
OBO	~15
NPO	~12
Socket	~5-7
CPO Today	5-10
CPO Next Gen1	2-4
CPO Next Gen2	< 1+light source

CPO plan 50% more efficient than PCIe6

Optical links < 1pJ/bit ! **laser

Laser approaches

Laser Heterogeneous Integration

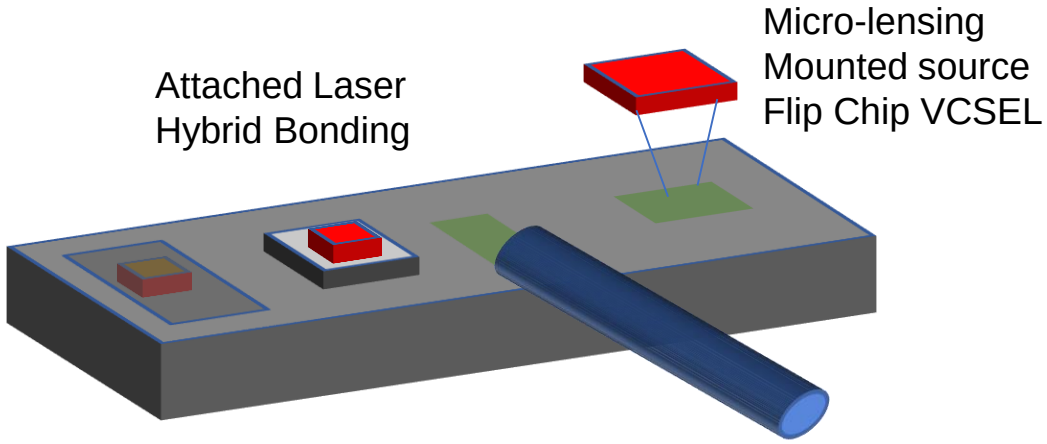
III-V laser in in Silicon Photonics option

- Monolithic: Hetero-epitaxy
- Direct wafer bonding
- Micro-Transfer Printing
- Hybrid: Flip-chip bonding
  Thermocompression bonding
  Laser assist bonding

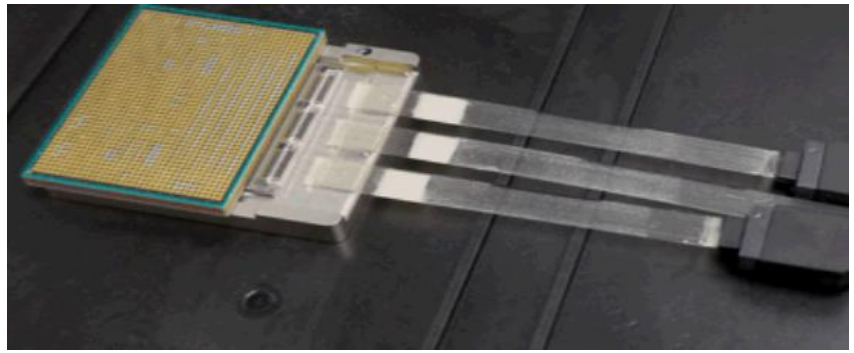
Laser injection :

Coupling element for light

- Additional Fibers to ELS (PM)
- Micro Lensing (VCSEL & SiPh)
- Grating Coupler (Loss)
- Edge coupling (Better for WDM)
- Spotsize coupler design for manufacturing
- Multiple stable wavelengths in one source



Photonics assembly with 3 fiber array (including PM)



Laser types for co-packaging

	Pro	Cons
Hetero-epitaxy	Fully integrated	III-V material in wafer process Development cost of wafer Laser Thermal stability / Reliability
Hybrid bonding	Populate good sites Enable self optical test	High precision placement Laser Thermal stability / Reliability
VCSEL	Proven low cost technology High efficency laser, lower cost	Fail management Thermal sensitvity (High speed)
External Light Source (ELS) Additional Fibers	Laser far from hot ASIC Weakest point of failure out of package Field replaceable (laser banks)	Mating for optical test Use of additional PM fibers Coupling loss Laser safety

Challenges:

- Laser Thermal management
- Current feedback loop for laser stability
- Optical isolation for laser quality
- System integration optimisation
- Reliability : Field Replacement and serviceability
- Final Yield : Who is responsibe?
- Assembly flow, component integration, test sequence
- Standardisation & Technologies compatibility

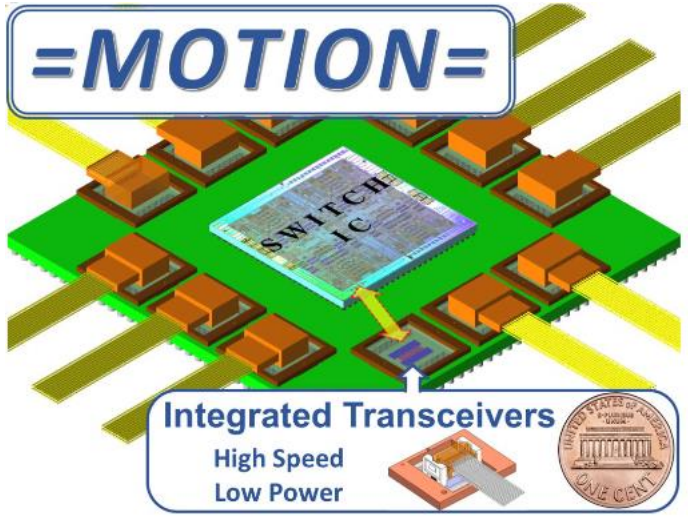
VCSEL CPO example : ARPA-e MOTION

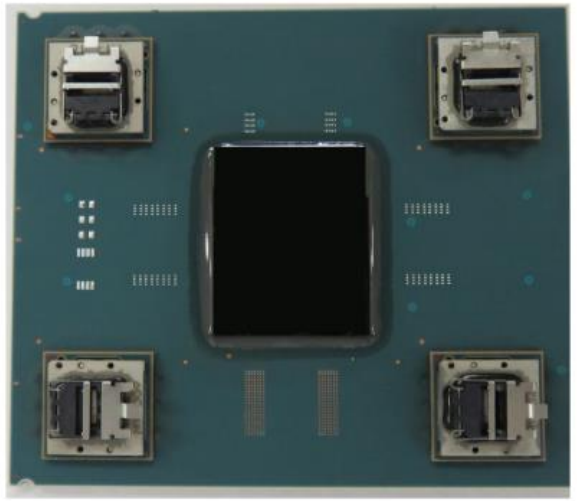
MOTION
Multi-wavelength Optical Transceivers Integrated on Node

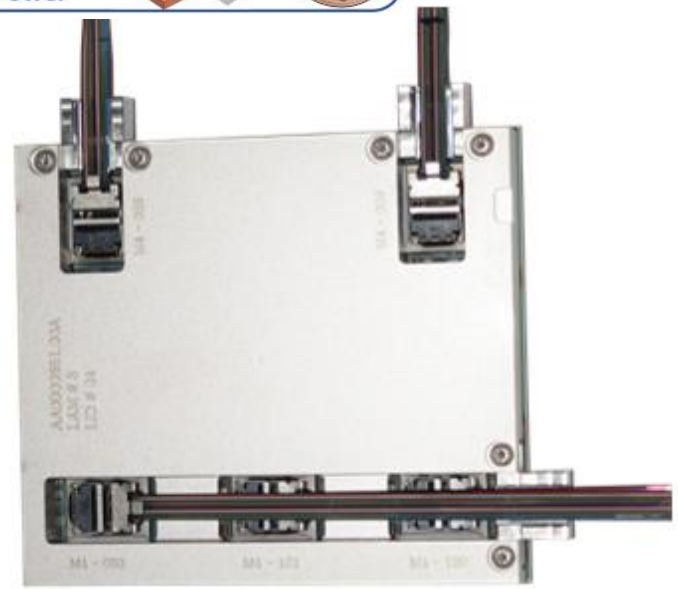
Co-packaging for CPU/GPU High-level Specifications

- ARPA-E Sponsored Project on co-packaging
- IBM and Coherent(Finisar) collaboration
- Demonstrating a viable path to system integration
  using established IBM Server Group processes
- 56GBd NRZ; BER tested to <1E-12 pre-FEC → PAM4
- 0C to 70C Case
- 6dB (electrical) link budget (XSR-like)
- 2 dB optical link margin (30m w/connectors)
- Solderable onto ASIC 1 st level substrate
- Power efficiency <4 pJ/bit → < 2pJ/bit
- Size13mm x D:13mm x H:4mm
  3.2W, 16 channels → 32 channels
- Target < 25¢/Gb/s

- Low Power consumption
- High reliability
- Roadmap to > 3.2 Tb/s

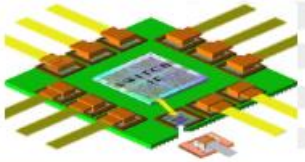




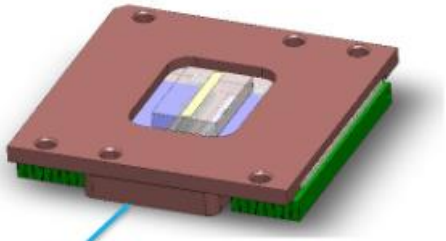


Acknowledgment: "The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000846. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof."

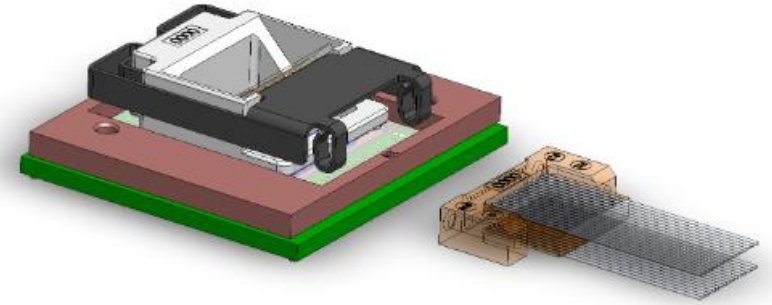
MOTION Transceiver Package Overview



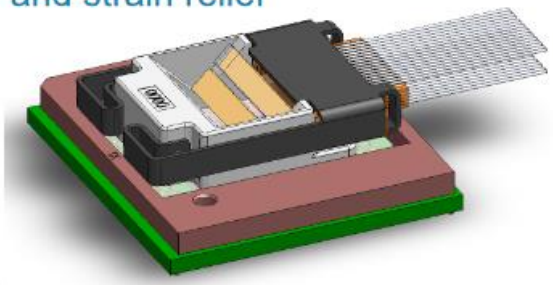
Chip-Scale Optical Package (CSOP)



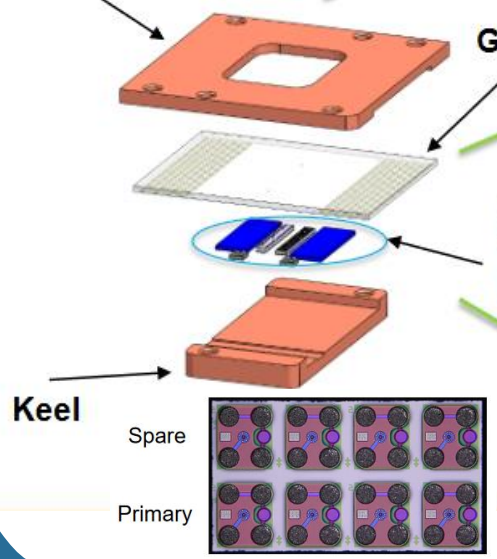
Final Assembly with lens and clip attached

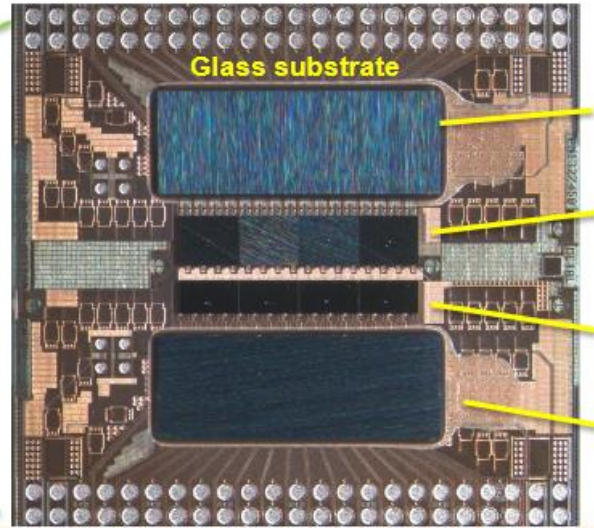


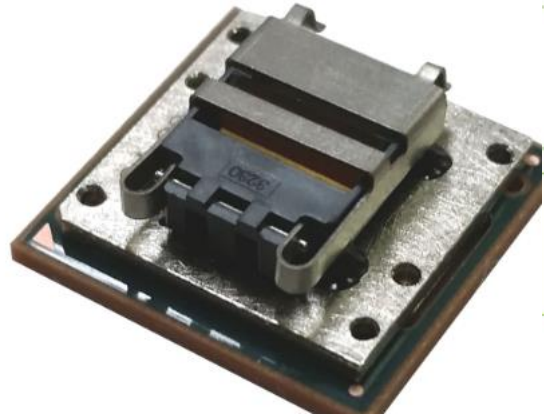
Fully Assembled with fiber cable and strain relief



4mm total height







VCSEL redundancy

Assembled in Bromont

MOTION Performance

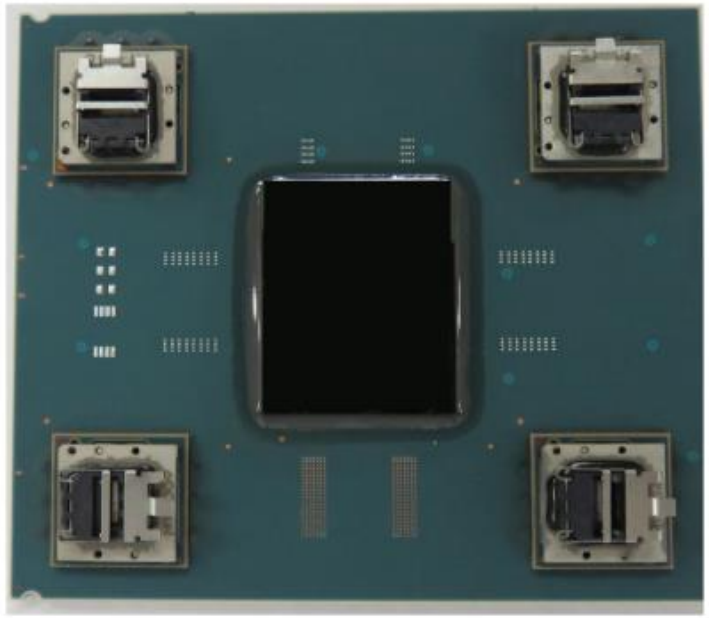
- Low Power consumption
- High reliability
- Roadmap to > 3.2 Tb/s

Tx Power Consumption

Power supply	Data mode	PRBS mode
1.8 V	820 mA	1.6 A
3.3 V	256 mA	256 mA
Total power	2.3 W	3.7 W
Energy efficiency	2.5 pJ/bit	4.1 pJ/bit

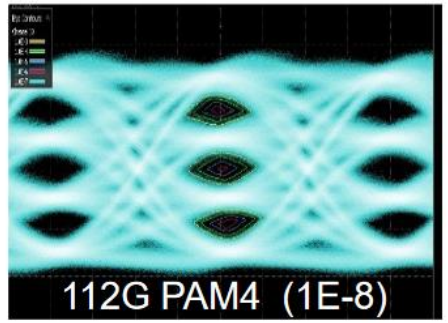
Rx Power Consumption

Power supply	Data mode	PRBS mode
1.8 V	480 mA	1.2 A
3.3 V	120 mA	130 mA
Total power	1.3 W	2.7 W
Energy efficiency	1.5 pJ/bit	3 pJ/bit



MCM of a Processor surrounded with
4 MOTION devices w/o heat spreader

Extended to 112G PAM4



Reliability Package with 4 optical engine

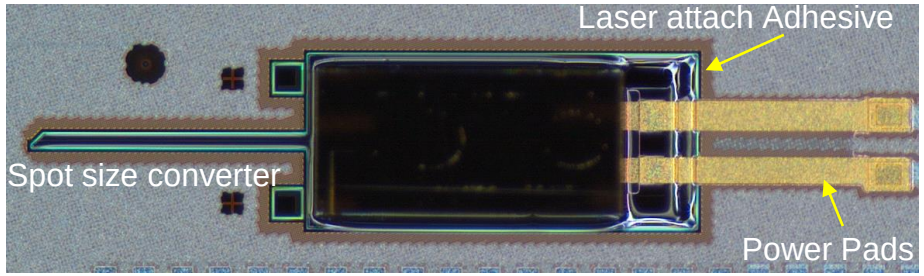
Stress	Samples	T/S -40/60°C	Time 0	Readout 1	Readout 2	Readout 3	Readout 4	Readout 5	Readout 6
DTC -40/125°C	5	5X	T, R	250 c	500 c	750 c	1000 c	1250 c	1500 c
ATC 0/100°C	5	5X	T, R	500 c	1000 c	1500 c	2000 c	2500 c	3000 c
HTS 125°C	5	5X	T	494 hrs.	989 hrs.	1486 hrs.	2009 hrs.		
T&H 85°C/85% RH	5	5X	T	279 hrs.	438 hrs.	721 hrs.	1002 hrs.		

Laser Attach - Hybrid bonding

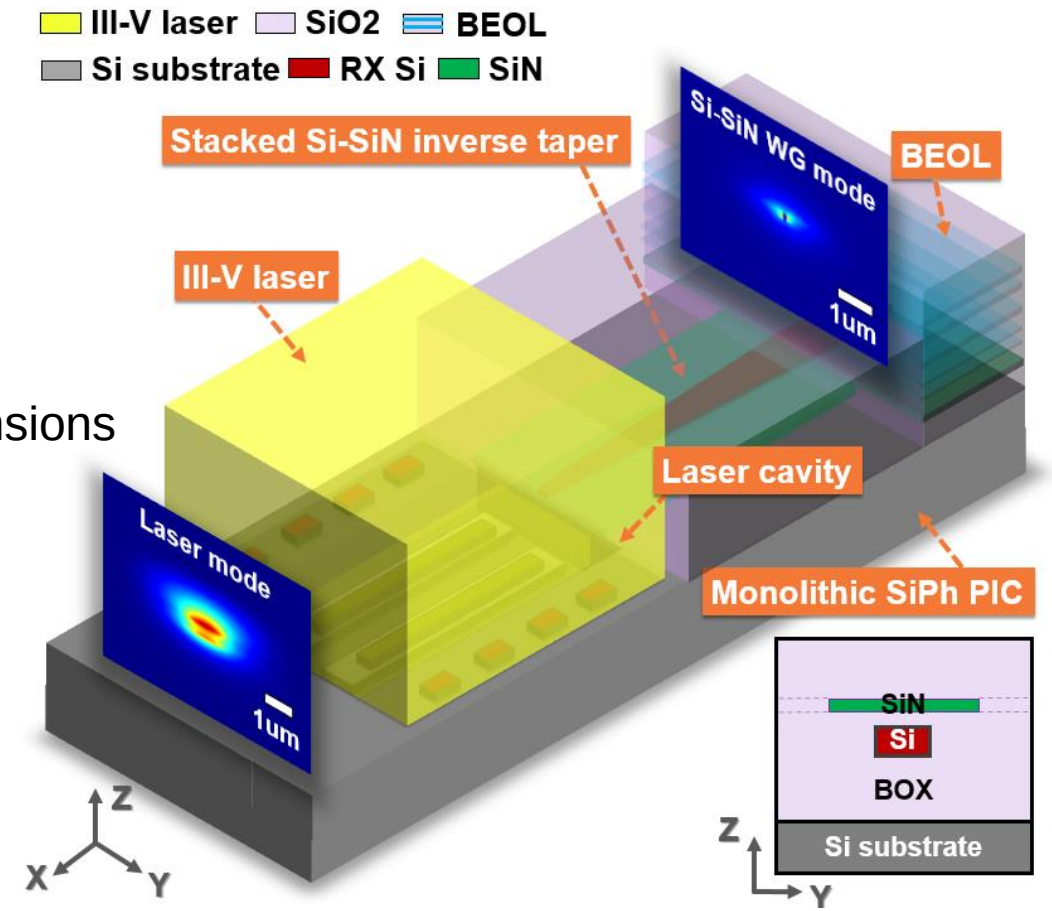
III-V laser flip-chip bonded and co-integrated into Silicon Photonics die

Significant mode mismatch
Large divergence of III-V laser
Low couling loss Spot size converter design
Precise mechanical stops for alignment in all dimensions

Laser-to-PIC coupling >12 dBm output power



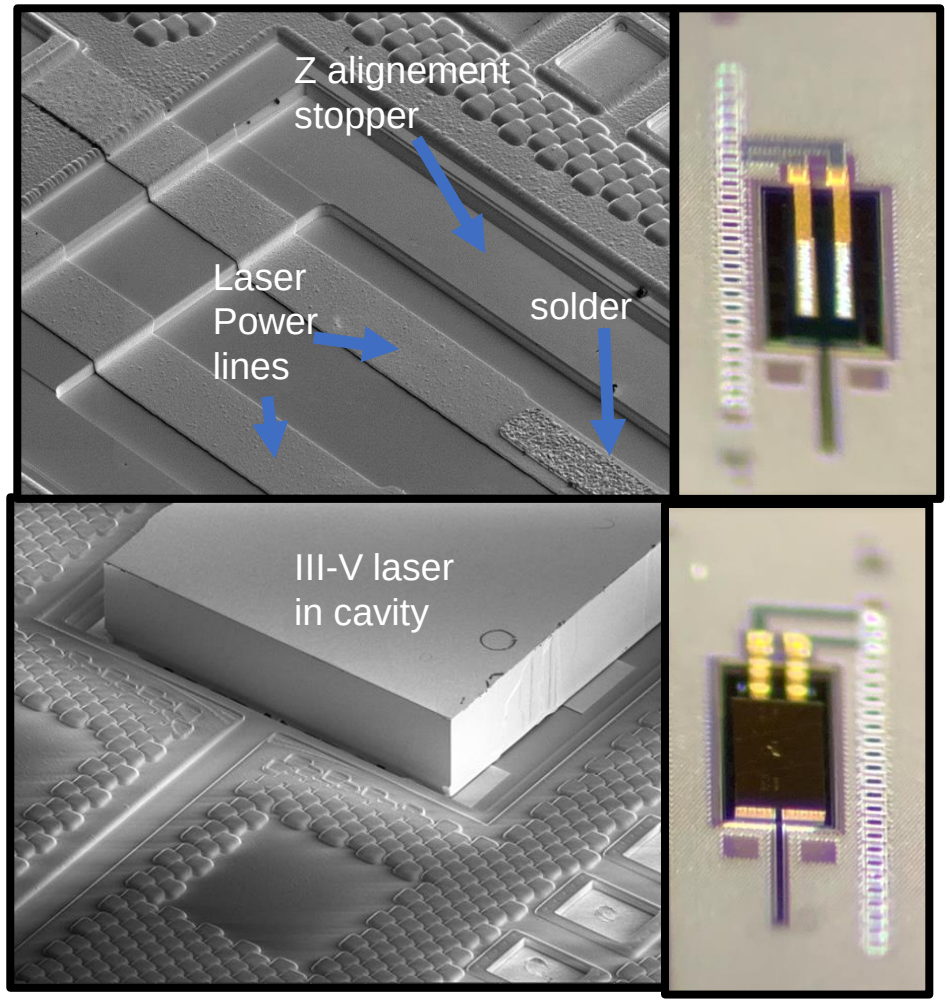
Assembly of a III-V Laser into a Silicon Photonics Cavity
Aging and reliability vehicle for laser attach

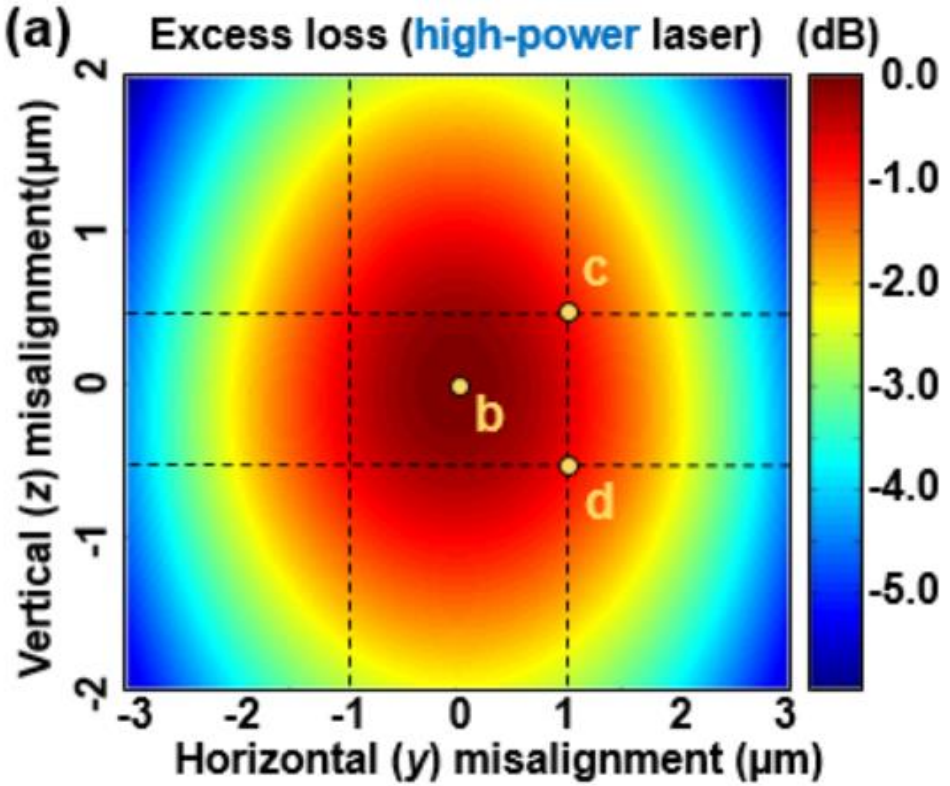


Y.Bian et al. "Integrated Laser Attach Technology on a Monolithic Silicon Photonics Platform", 71th ECTC 2021

Laser Attach - Hybrid bonding

Stopper and alignement feature to achieve laser to PIC optical coupling

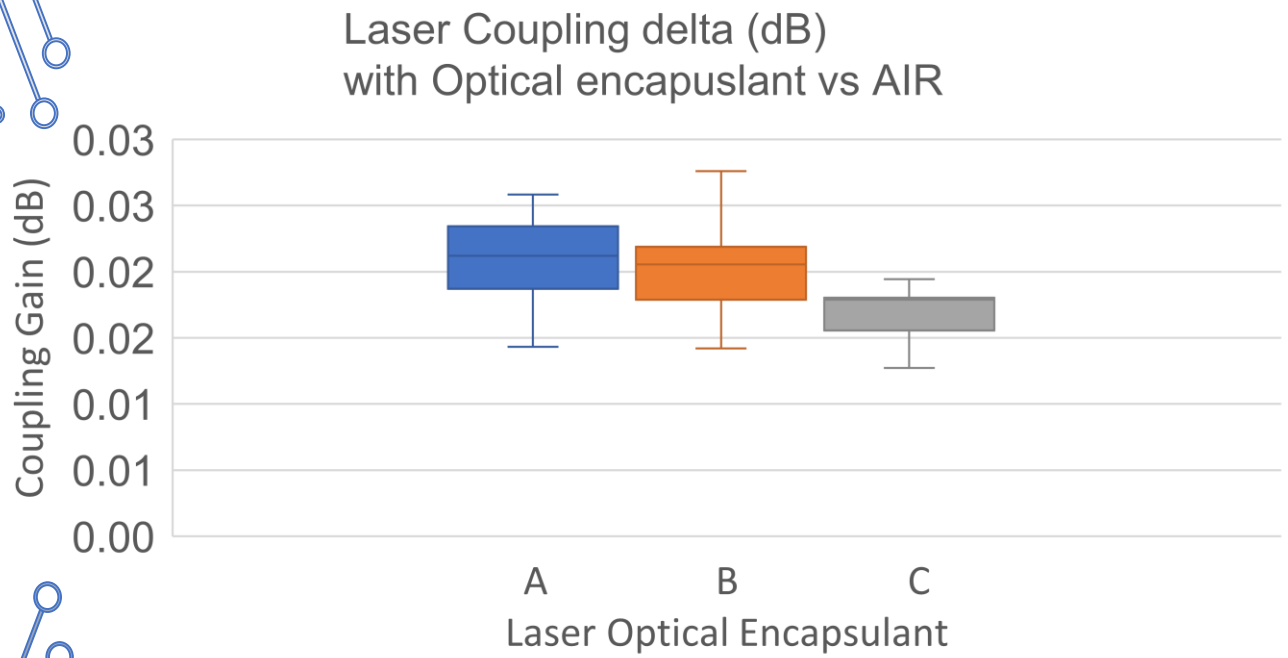




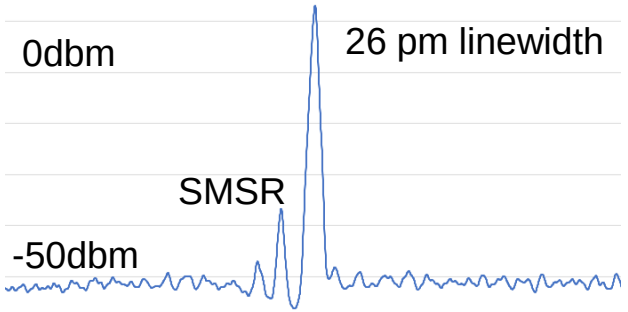
Y.Bian et al. "Integrated Laser Attach Technology on a Monolithic Silicon Photonics Platform", 71th ECTC 2021

Laser Optical Adhesive Performance

Laser Optical Encapsulant



O-HTOL Aging	Readout	Cumulative
High power Laser through optical adhesive and temperature	T1000hrs @ 85C +T1000hrs @125C +T1000hrs @125C	T3000 PASS



Track laser spectral behavior with temperature or along aging,

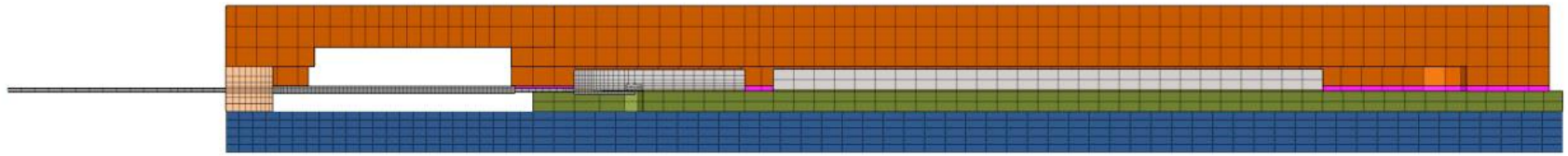
Laser optical adhesive aging : Optical HTOL Test

- High-temperature operating life with laser power-on
- High optical power density through optical adhesive
- Laser Thermal stabilisation

Additional PM fibers in package

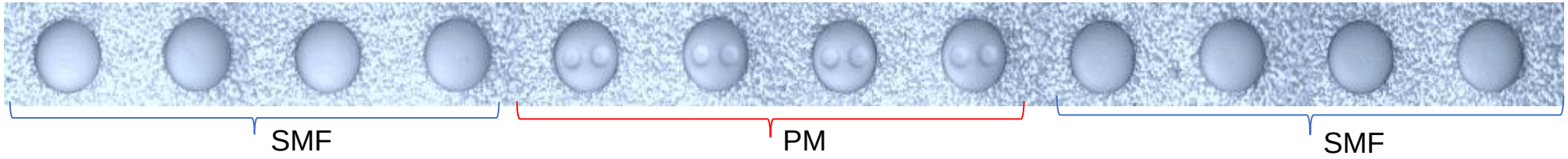
Integration of Fiber array within the photonic package

Controlled Fiber bending inside package due to large CTE mismatch
Amplified deformation scaling for emphasis – notice the multiple optical fibers bends
Cooling from curing to room temp – animation video



***Optical Fiber* Pigtails Integration in Co-package. ECTC2022**

Mix of SMF and PM fibers in a fiber Array for PIC assembly. Preclock PM fiber are used to inject ELS into the PIC.



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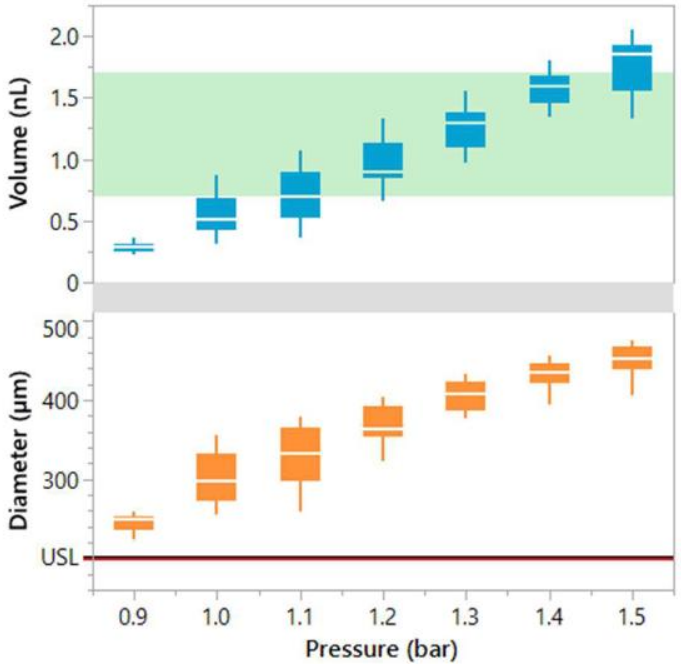
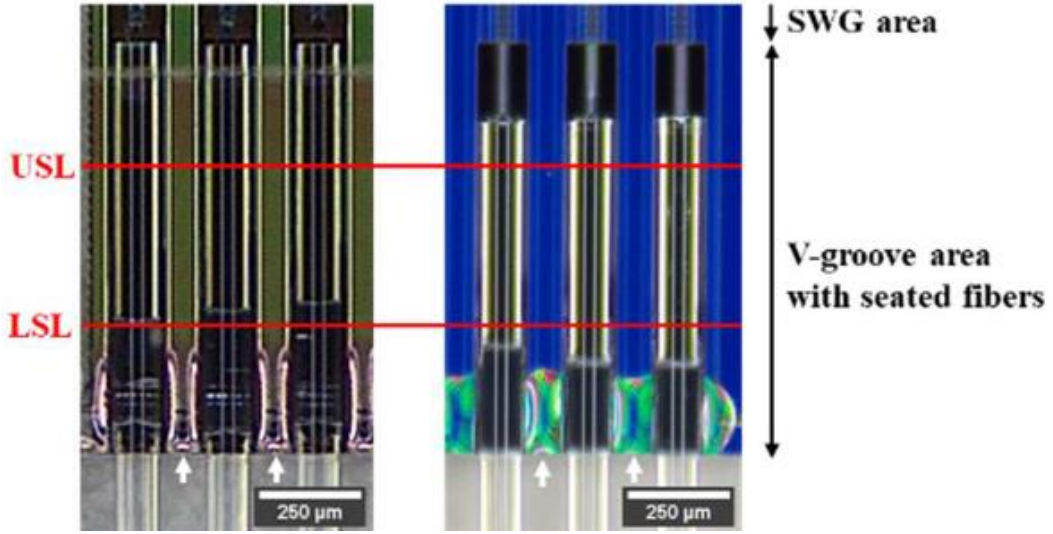
Adhesive Process and Dispense challenges

Dot Volume : Between 0.6 and 1.7 nL
Dot Diameter : 40 and 200 µm

Pushed towards **nano-dispense** technics !

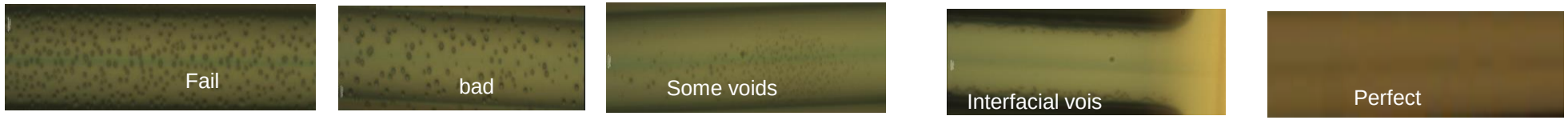


- Time-pressure
- Pin transfer
- Non-contact Jet



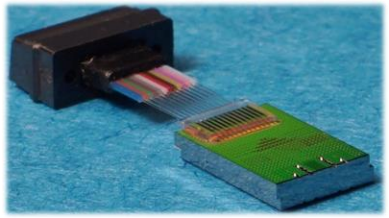
Example of advance dispensiing control for photonic package.
Picture of structural adhesive inside Vgroove
to hold the optical fiber array (solder reflowable)

IBM expertise in process flow, surface preparation and adhesive selection

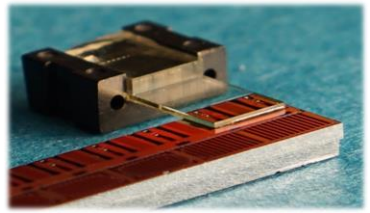


High resolution microscopy images of waveguide with optical adhesive
Process flow and curing parameter affect adhesive behavior – Process control for no adhesive bubble and defect

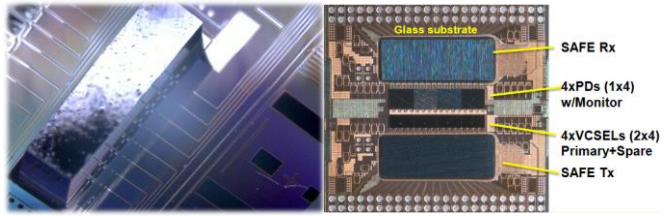
Advanced packaging leader for HI, MCM, SiP and CPO



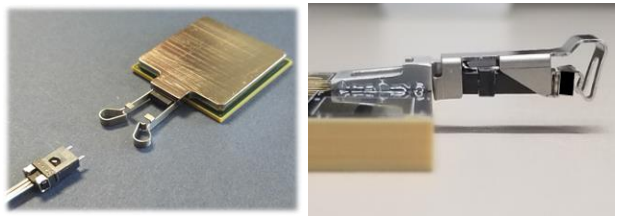
Fiber Attach



Polymer Attach



Laser, VCSEL/PD Attach



Advanced CPO integration

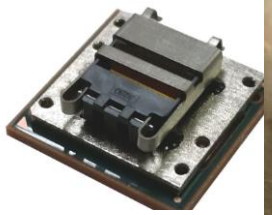
IBM Bromont

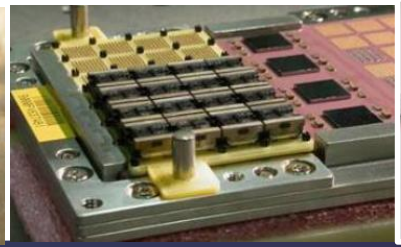
Booth #211

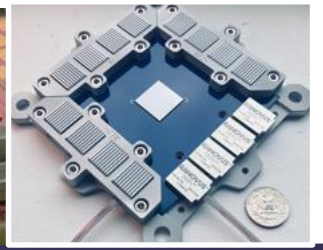
OSAT manufacturer

Engagement from prototyping to production.
Standardization in packaging: Effective models
Supply chain: proven ecosystem

- Heterogenous Integration
- Complex MCM / SiP / CPO
- Proven material sets for high performance
- Designs acceleration (Benefit from existing models)
- Streamlined manufacturing flow
- Integrated supply chain
- Design for effective High Volume manufacturing
- “Assembly Design Kit = Packaging PDK”
- Solder reflowable photonics
- Prototyping to high volume manufacturing
- High Mix production lines flexibility (effective manufacturing)







Next Gen Silicon Photonics Transceivers: From design challenges to pilot line fabrication

Presenter: Grace O'Malley
Vice President of Technical and Project Operations
iNEMI

Project Chair: Kamil Gradkowski
Senior Researcher
Photonics Packaging Tyndall National Institute,

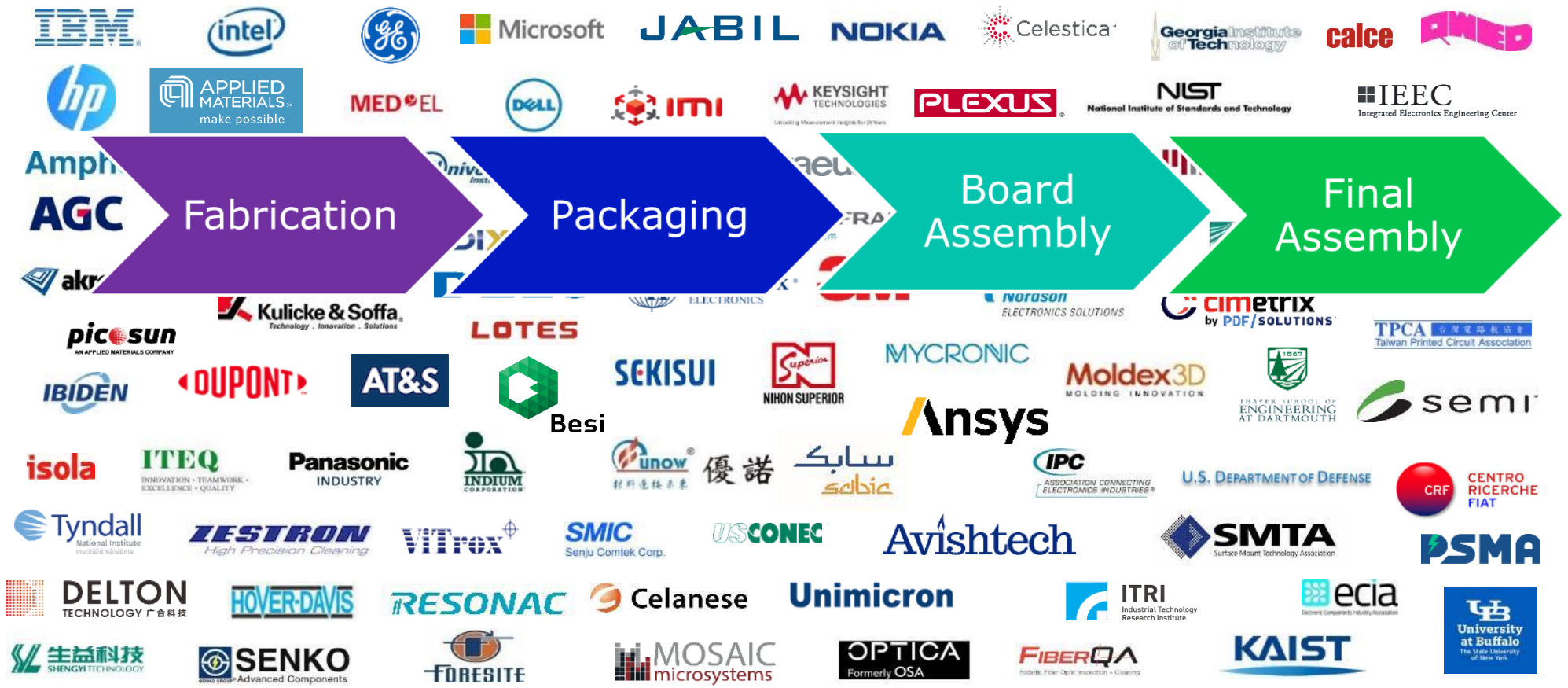
May 30, 2023

Tyndall National Institute

iNEMI
Advancing manufacturing technology

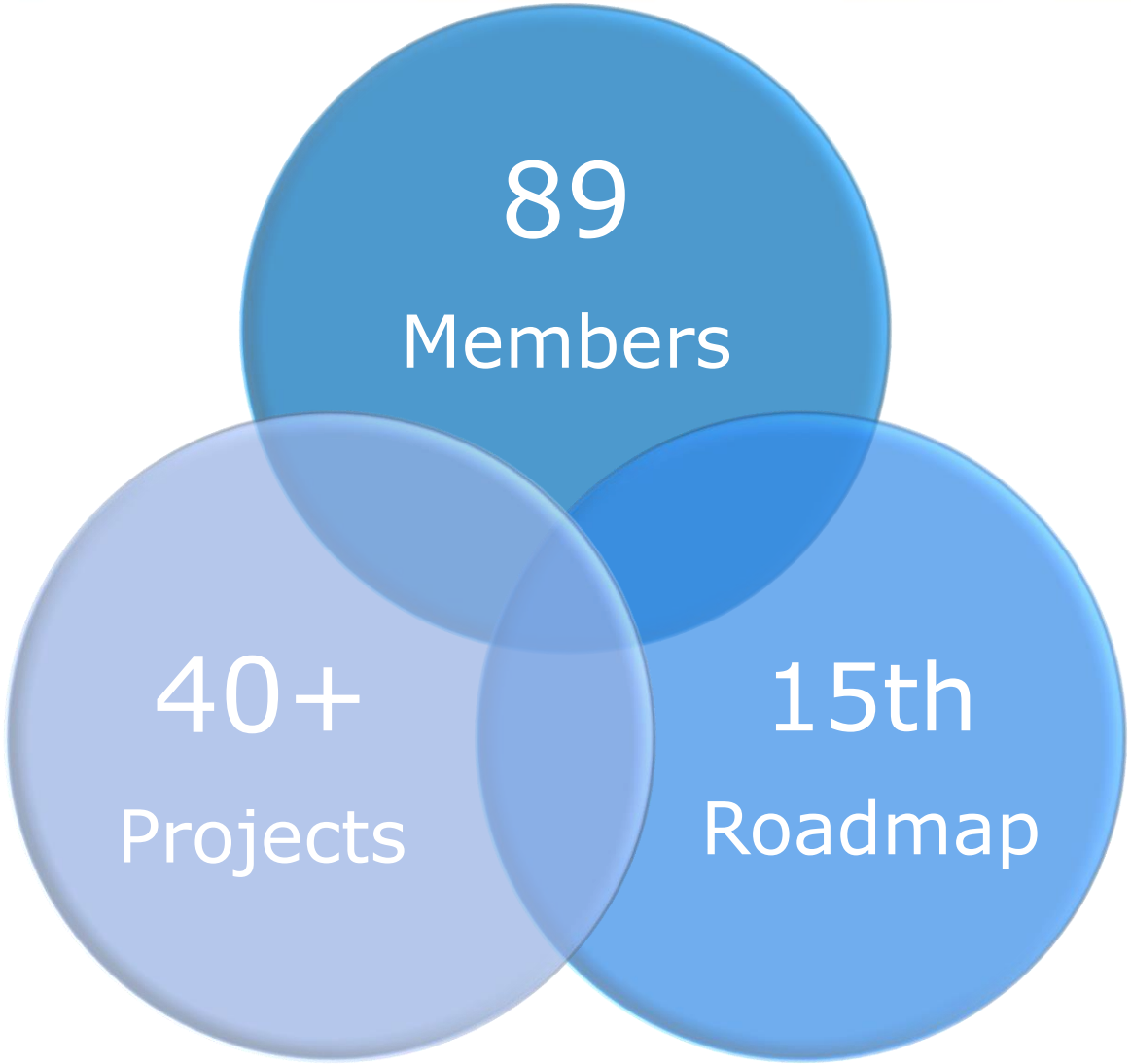
iNEMI – The Premier Collaboration Forum for the Electronics Manufacturing Value Chain

iNEMI since 1996, gives its members the ability to anticipate and shape industry needs, ensure supply chain readiness and accelerate innovation.



iNEMI – The Premier Collaboration Forum for the Electronics Manufacturing Value Chain

- **Think strategically** by roadmapping future technology needs
- **Collaborate wisely,** working with a network of technical leaders to identify and focus on common industry challenges
- **Solve creatively** through collaborative technical projects that amplify any one individual organization's expertise and resources



Photonic Packaging Group

Fibre Packaging

Flip-chip Packaging

Solder Jetting

Micro-optic Packaging

Fibre Array Packaging

Wirebonding

Flip-chip Packaging

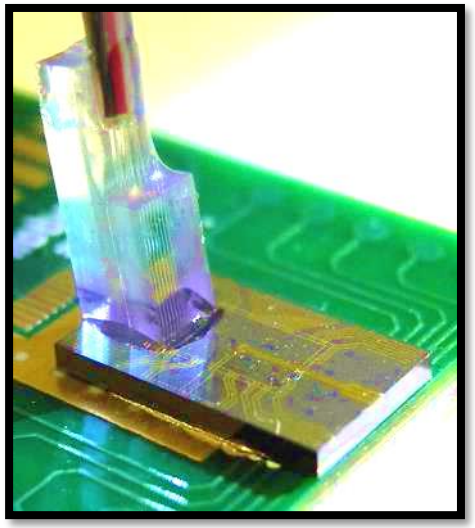
Package Design

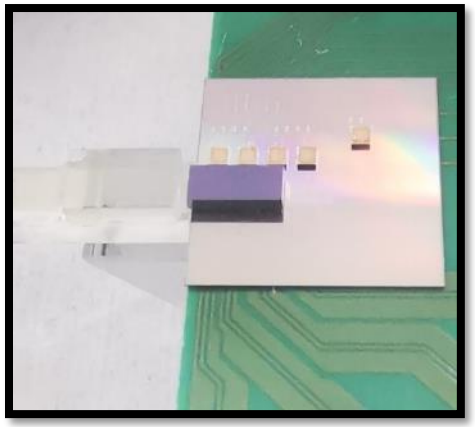
Project Motivation

Module with Separable Single-Mode Expanded-Beam Optical Interface for Edge-Coupled PIC Optics

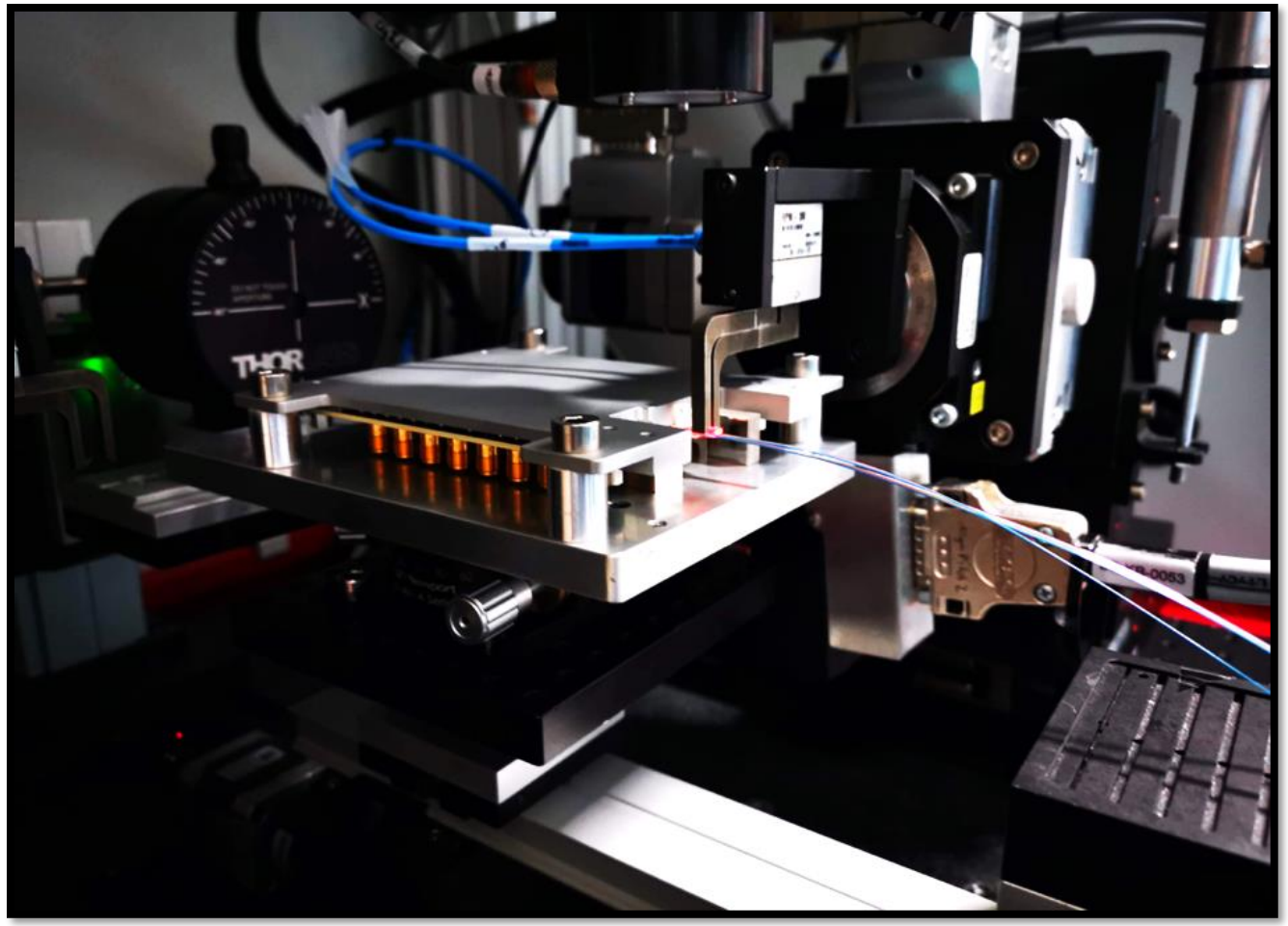
- Industry Roadmaps predict that silicon-photonics-based transceiver modules will provide the most cost-effective and energy-efficient solutions for on-board interconnect.
- Silicon Photonic Integrated Circuits (PICs) are single-mode (SM) devices, and require SM interconnect media (e.g. fiber) for optimum performance.
- Efficient and repeatable SM optical coupling between fibers and PIC waveguides requires mechanical alignment accuracies to better than 1 micron. This makes optical coupling aspects of PIC packaging difficult and expensive.
- Optical coupling to PICs is now typically achieved by direct bonding of fiber to the PIC package, resulting in a "pigtailed" package. The presence of the fiber cable on the module complicates handling and board placement.
- Use of conventional physical contact SM connectors on PIC modules requires that the cable connector and PIC module receptacle achieve submicron alignment of the fiber cores, and that there is adequate mating force to assure optical contact of cores.

State-of-the-Art in Photonic Packaging





Permanent bond between PIC and Fibre Array



Serial process, difficult to scale

Package-level

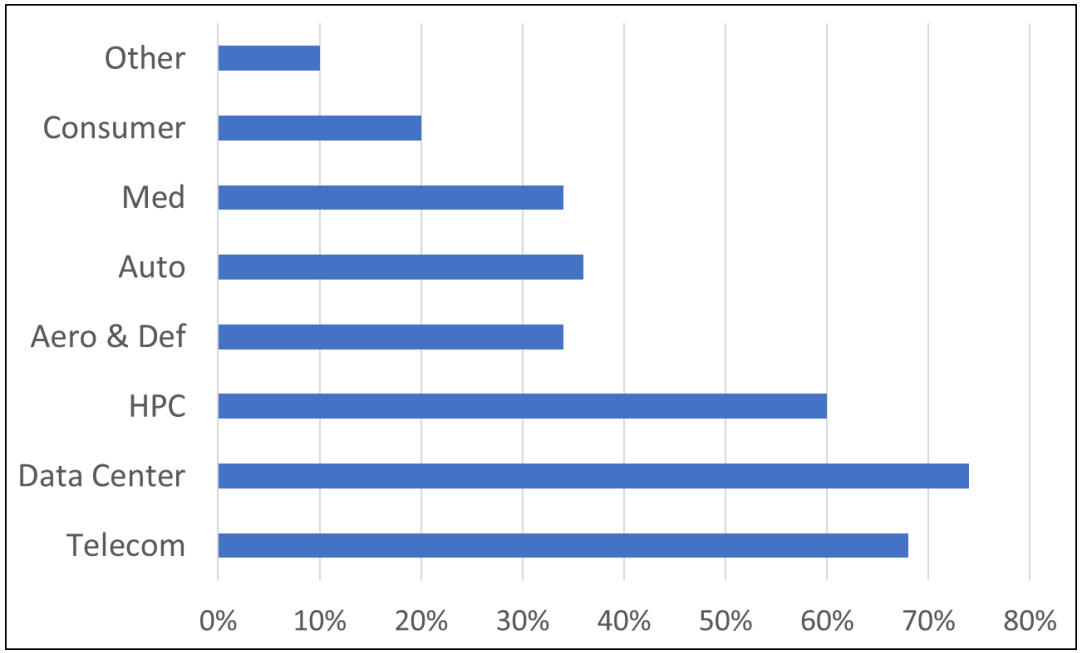
Project Objectives

Module with Separable Single-Mode Expanded-Beam Optical Interface for Edge-Coupled PIC Optics

- Demonstrate the principles of a separable single-mode (SM) expanded-beam optical connector to chip interface by assembling a demonstrator module and verifying optical performance.

- Identify manufacturability and assembly issues for such separable optical interconnect systems, e.g. micro-optics assembly, tolerance considerations, materials.

Industry survey helped define project



Require coupling single-mode optical fiber to PICs in the next 3 to 5 years?

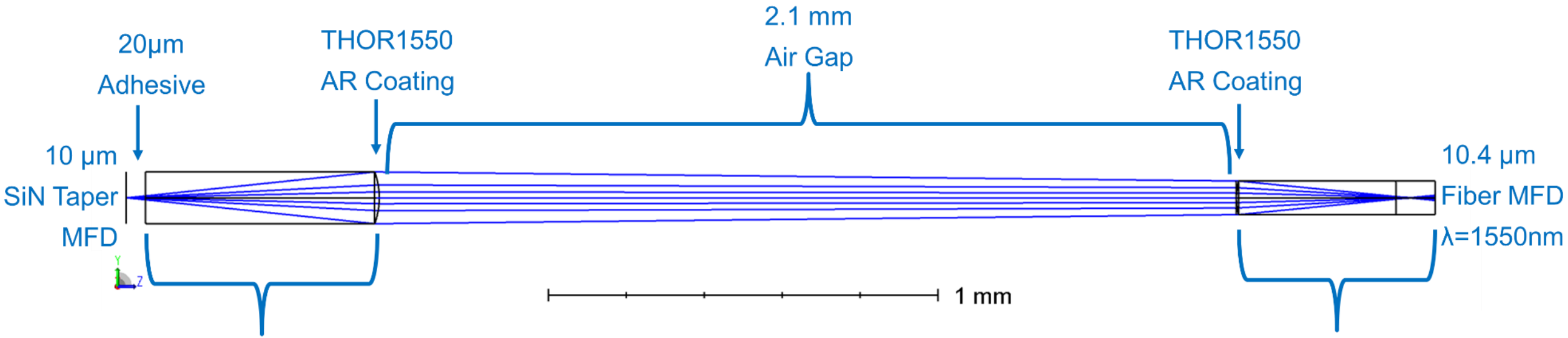
Survey Driven Requirements

- Pluggable SM expanded-beam interface.
- Optical coupling at edge of PIC
- Less than 2 dB waveguide to (standard) fiber cable coupling loss.
- Horizontal mating of connector to PIC module
- Fiber exit parallel to the board
- Non-hermetic
- PIC compatible with testing at wafer level
- Reflow compatible (260°C)

Mating Connector & Cable Availability

- 8 channels of optical signal
- 250 micron pitch fiber cable
- 12 fiber ribbon cable

Optical Design of the Demonstrator



SUSS Lens Array #18-00997

https://shop.suss-microoptics.com/collections/couplers-collimators-1

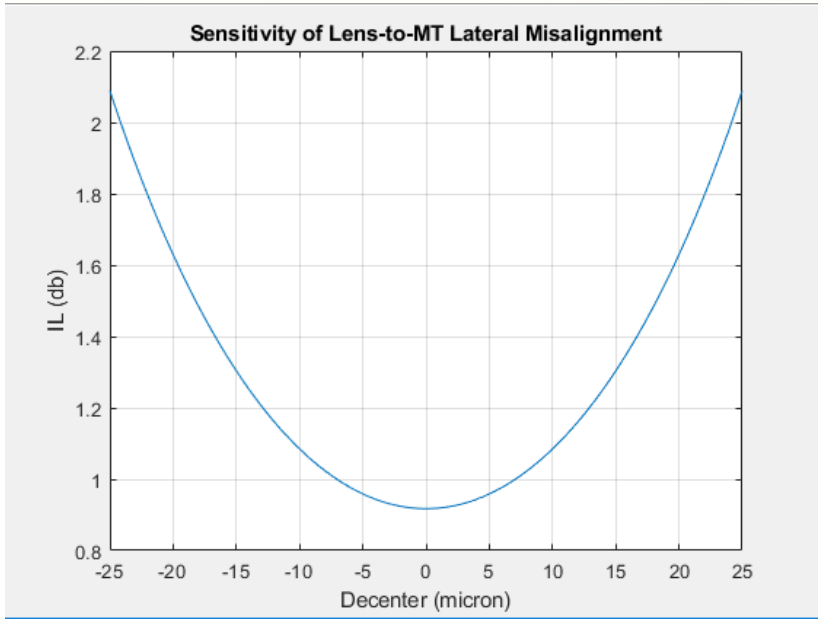
Fused Silica

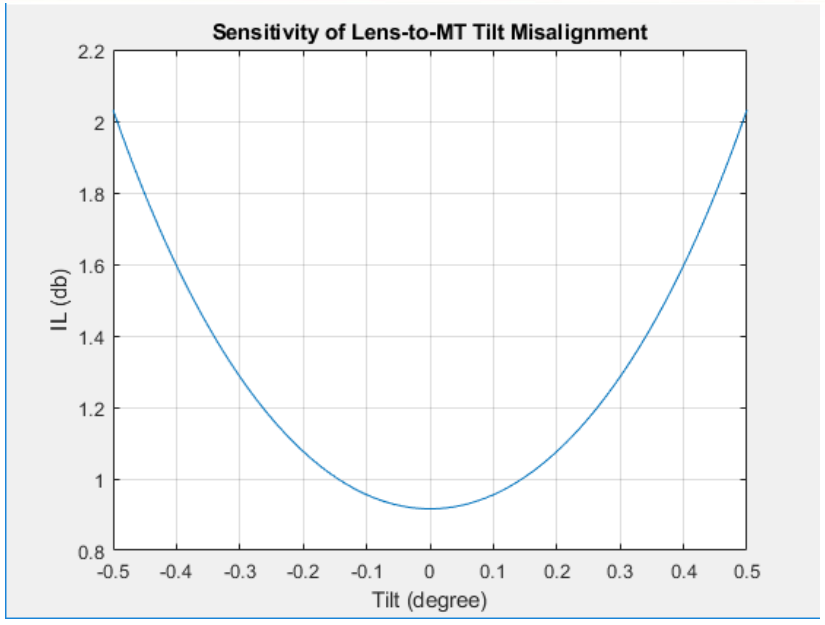
Thickness=0.6mm

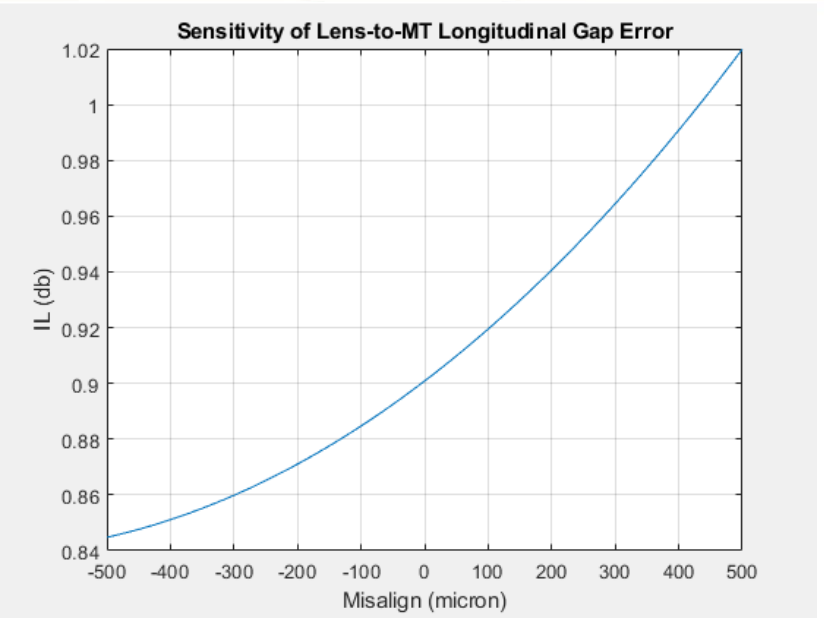
Radius of Curvature=0.192mm

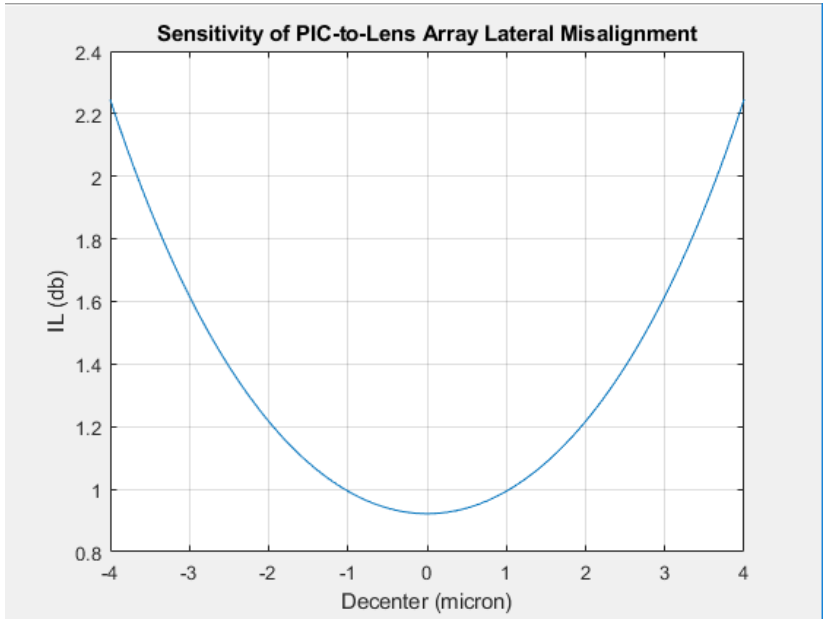
MT Expanded Beam Ferrule

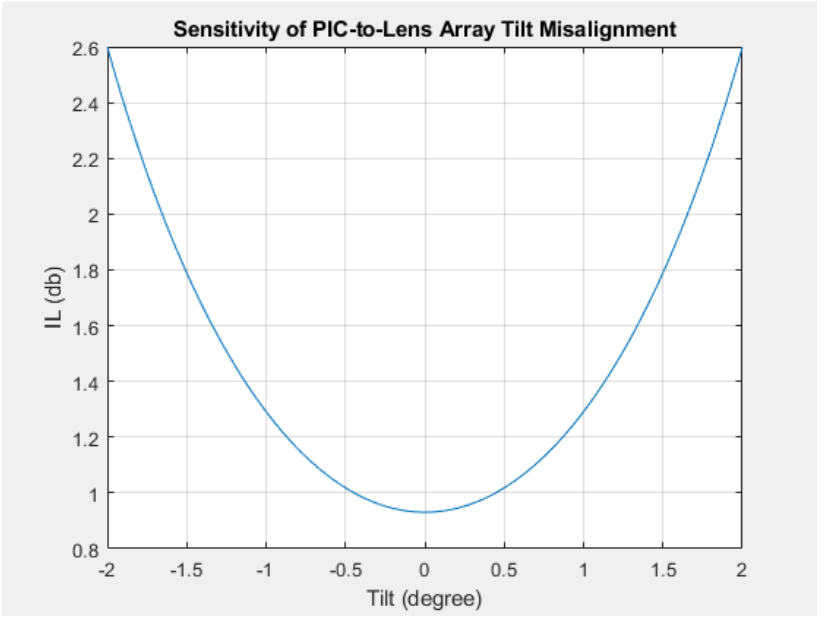
Optical Design Tolerance Analysis



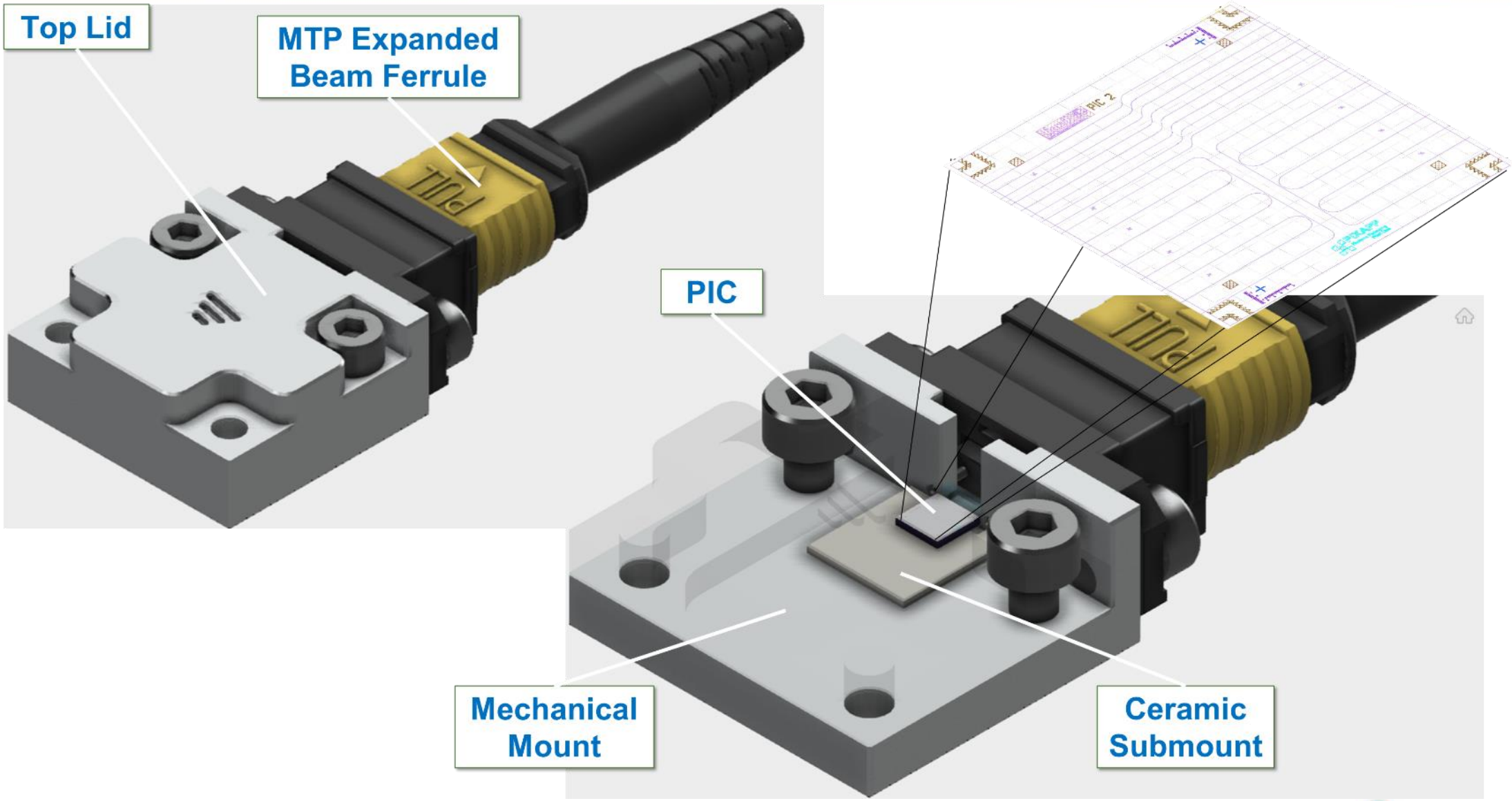








Mechanical Design of the Demonstrator

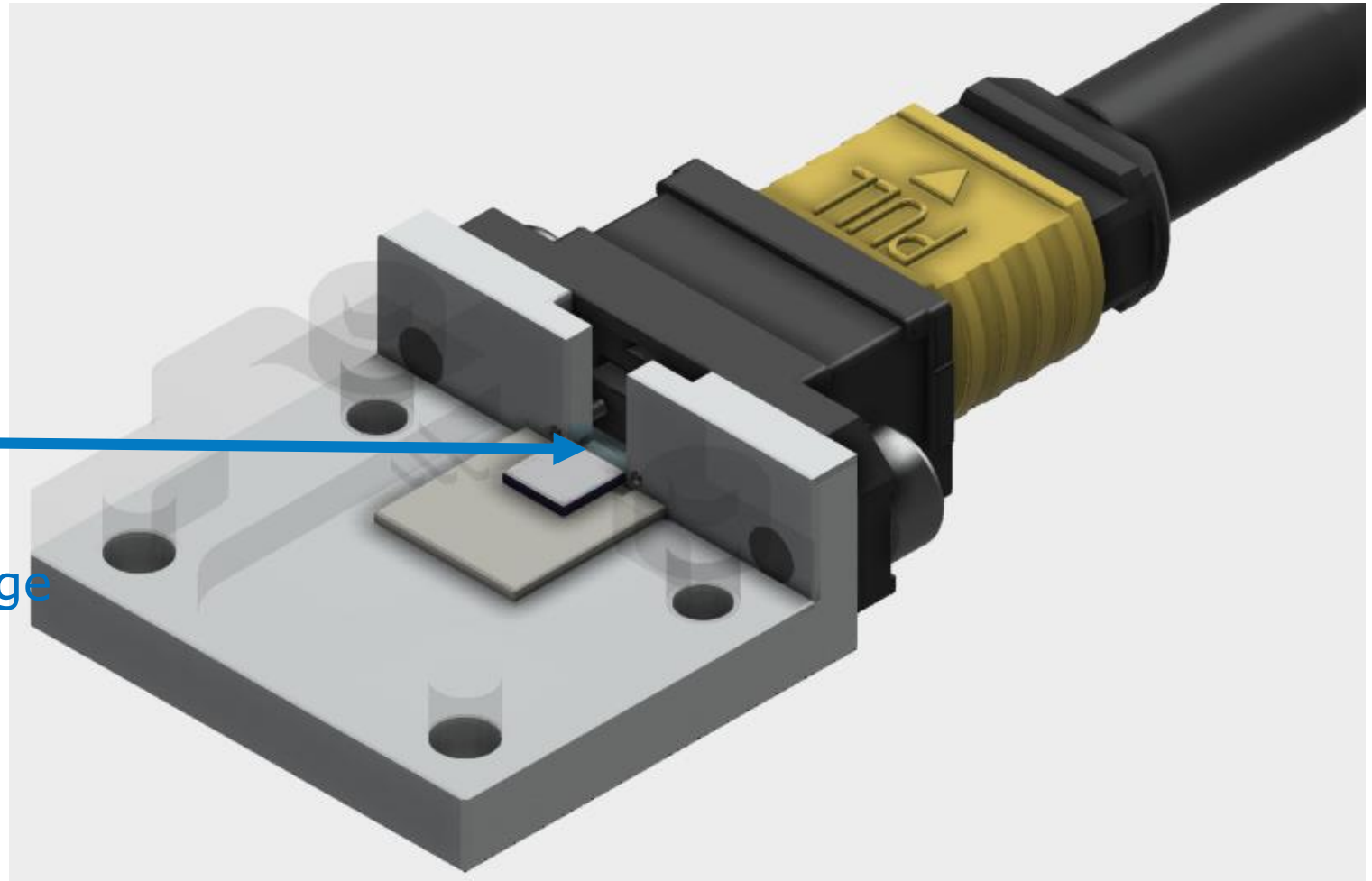


Mechanical Design – Alignment Register

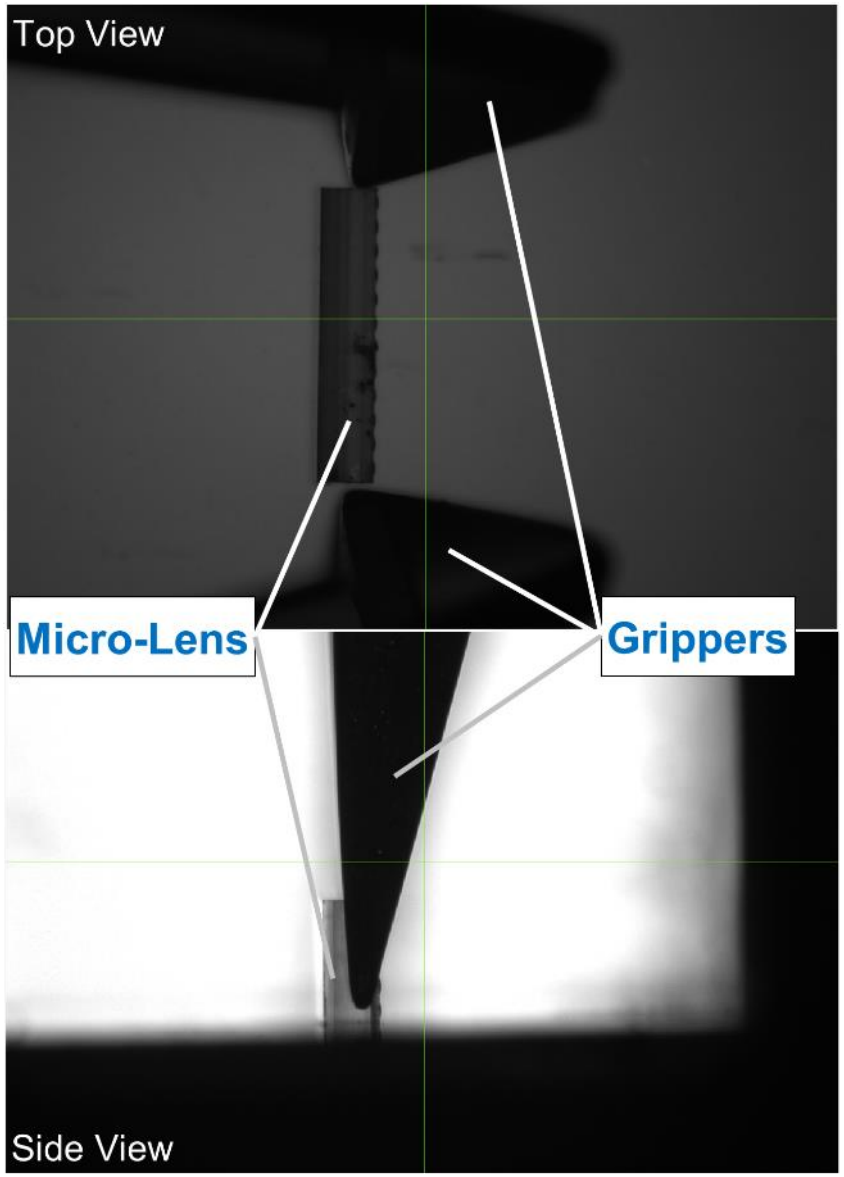
Mechanical Design – Manufacturing Precision

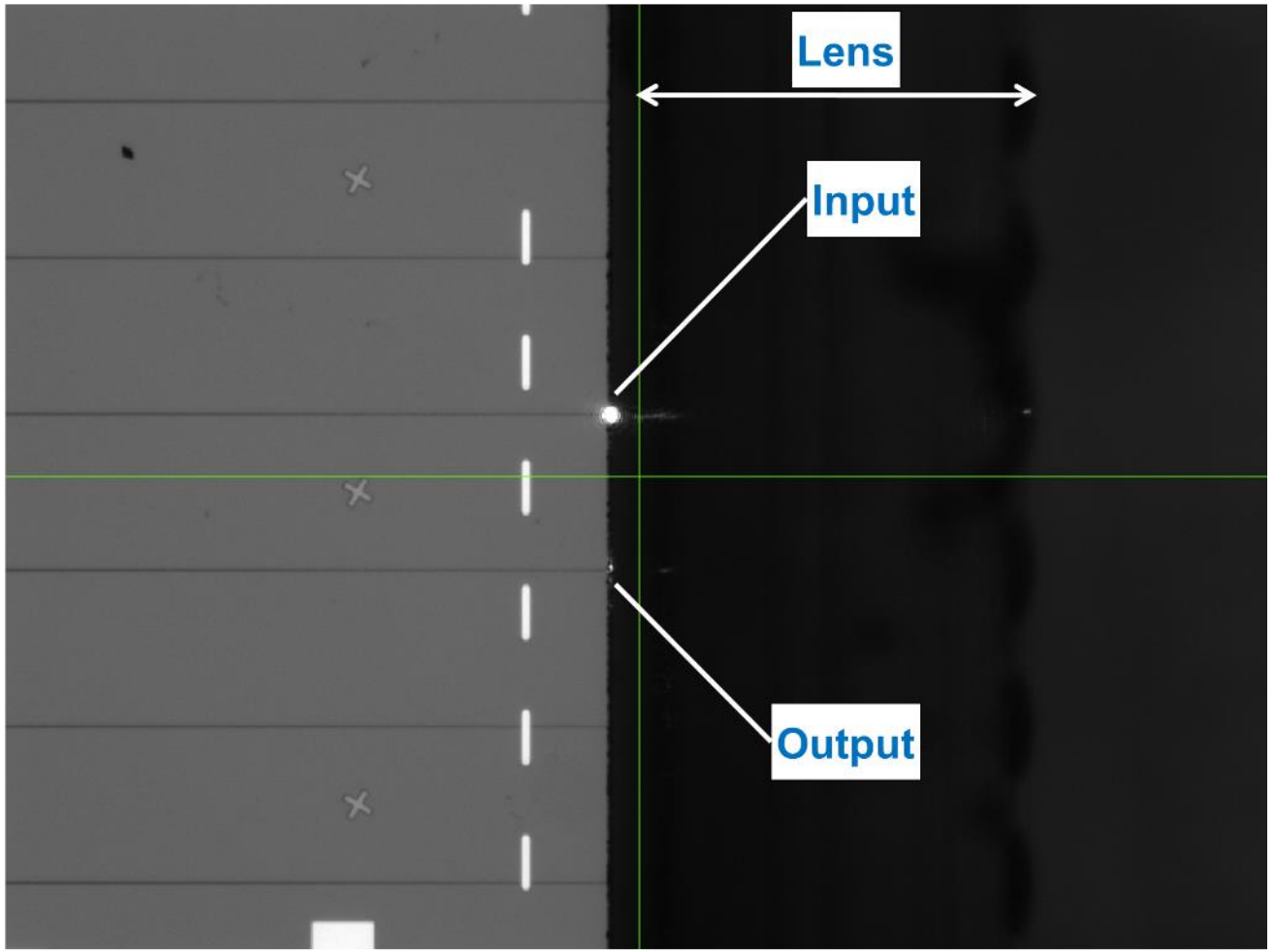
Packaging Process Development

1. Clean the PIC
2. Place PIC on Ceramic Substrate
3. Attach micro-lens to the PIC
4. Attach PIC Assembly to the Package

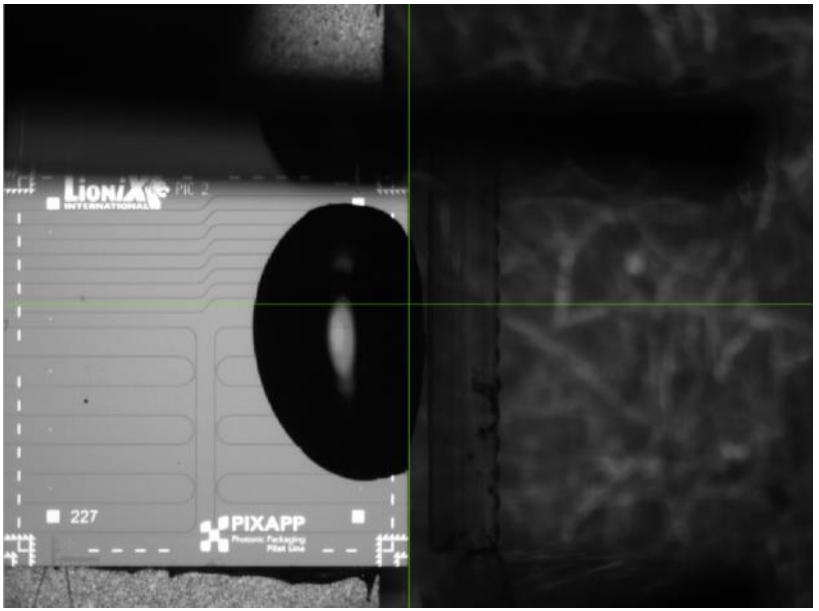


Micro-Lens Attachment – Lens Pickup



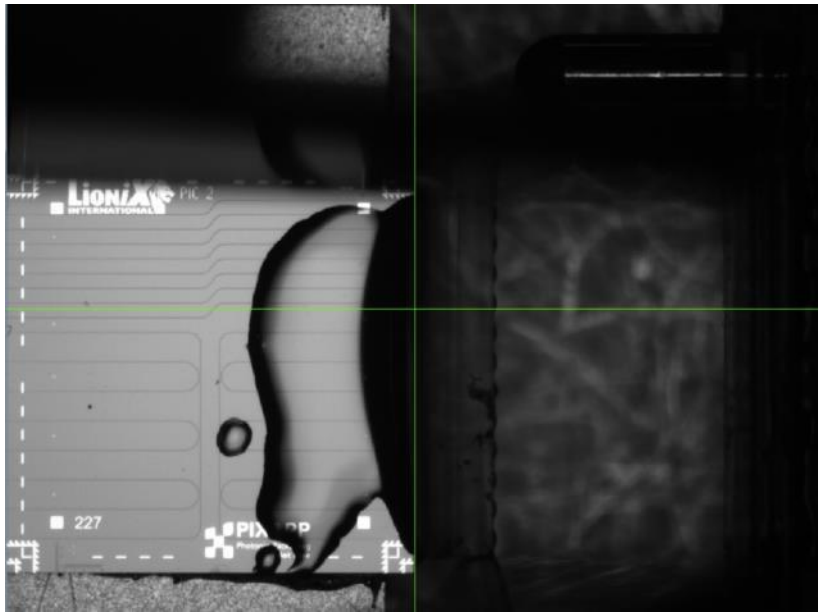


Micro-Lens Attachment



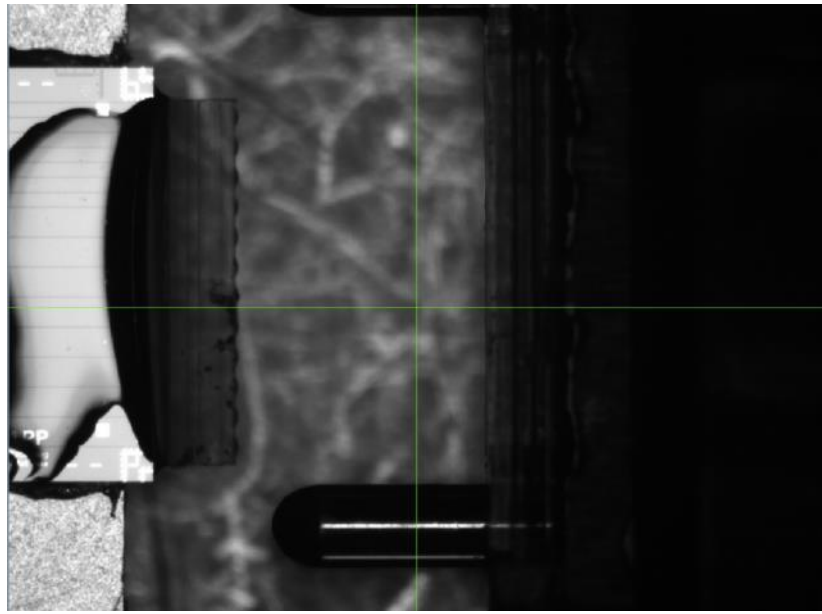
A. Apply the Epoxy

DELO DUALBOND® OB6268



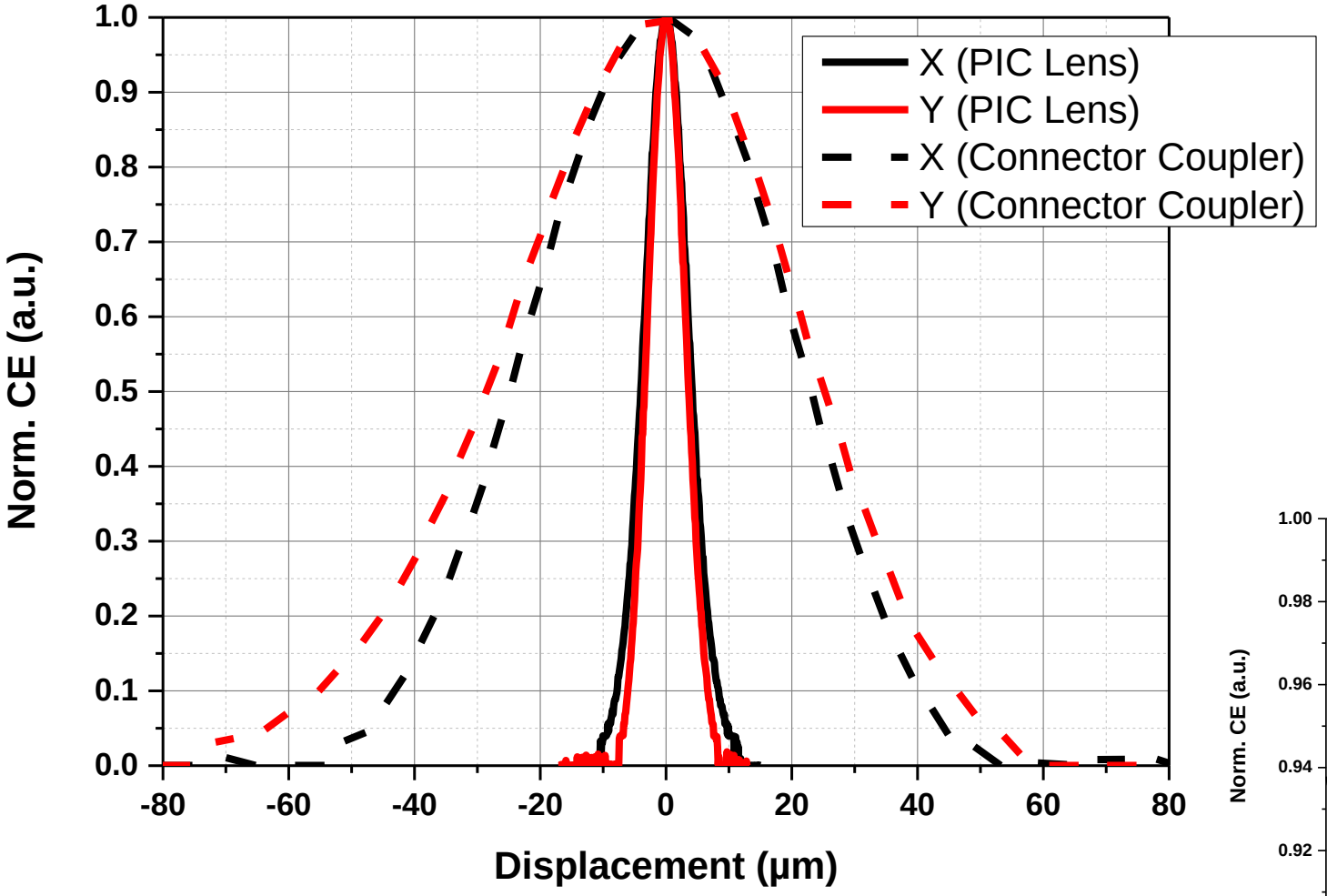
B. UV-Cure the Epoxy

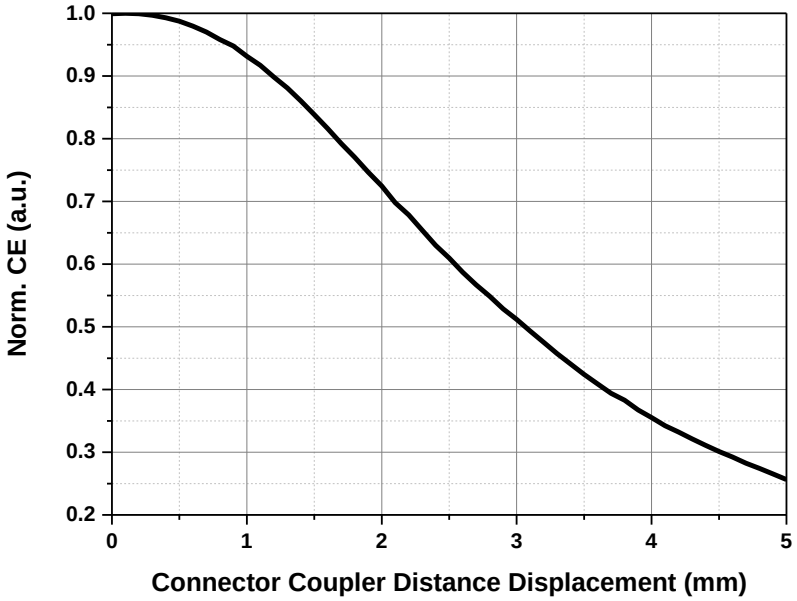
Hg-Lamp, fibre-coupled

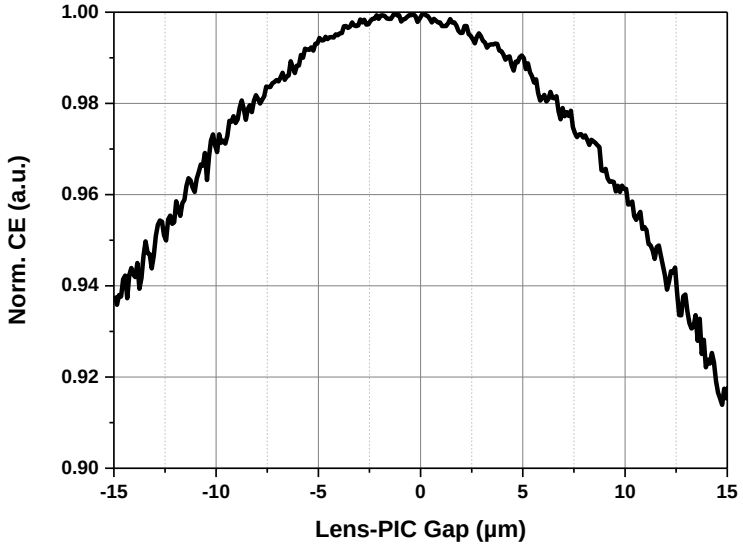


C. Release the Micro-Lens

Micro-Lens Attachment – Alignment Tolerances



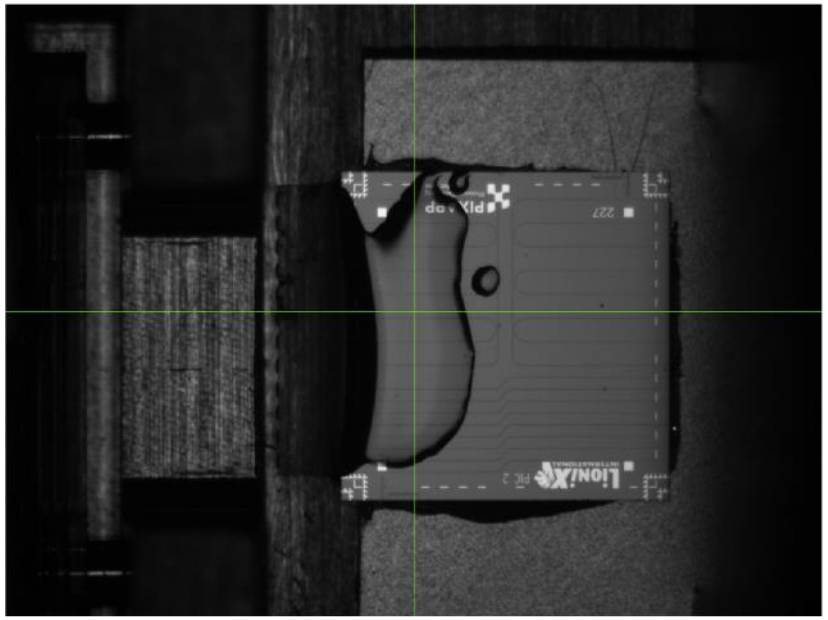


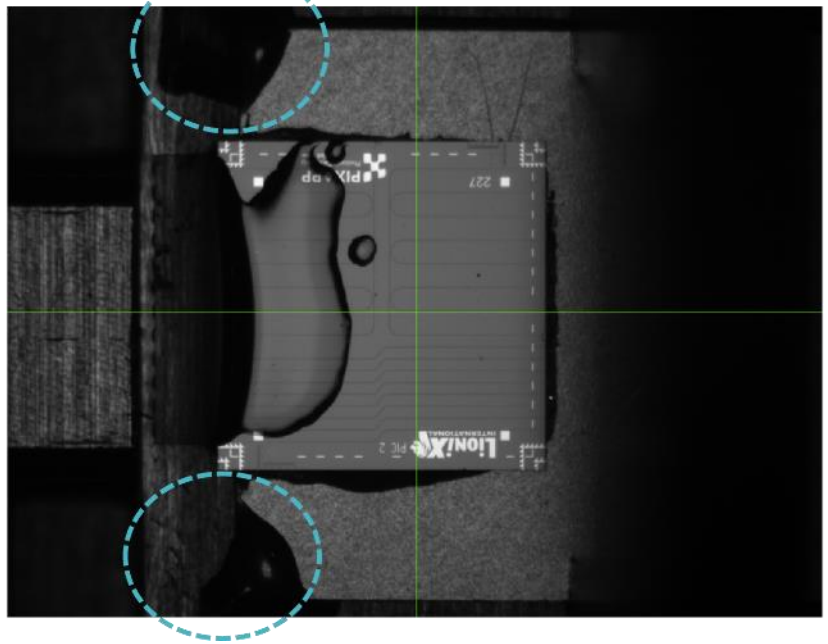


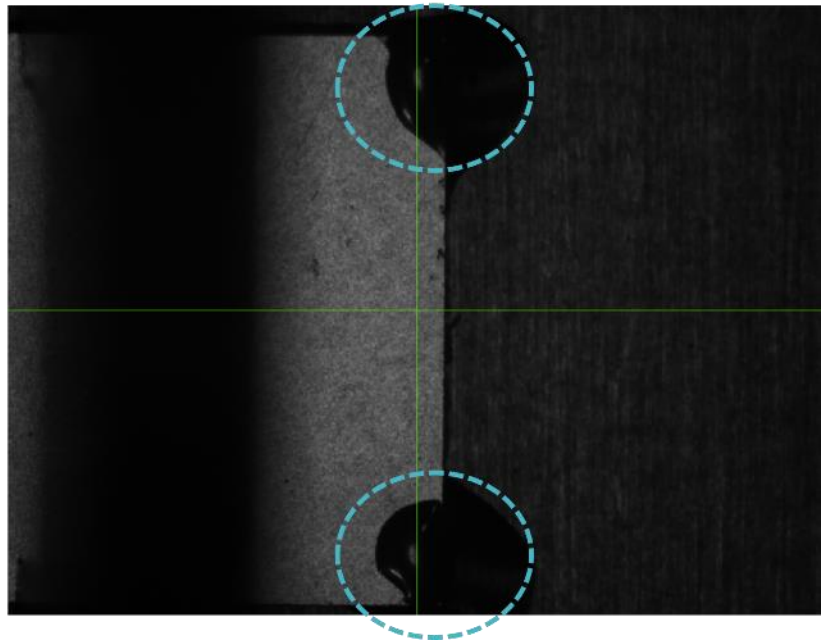
PIC Assembly Attachment

II. Apply & Cure the Epoxy at the front

DELO DUALBOND® OB6268 → Hg-Lamp, fibre-coupled







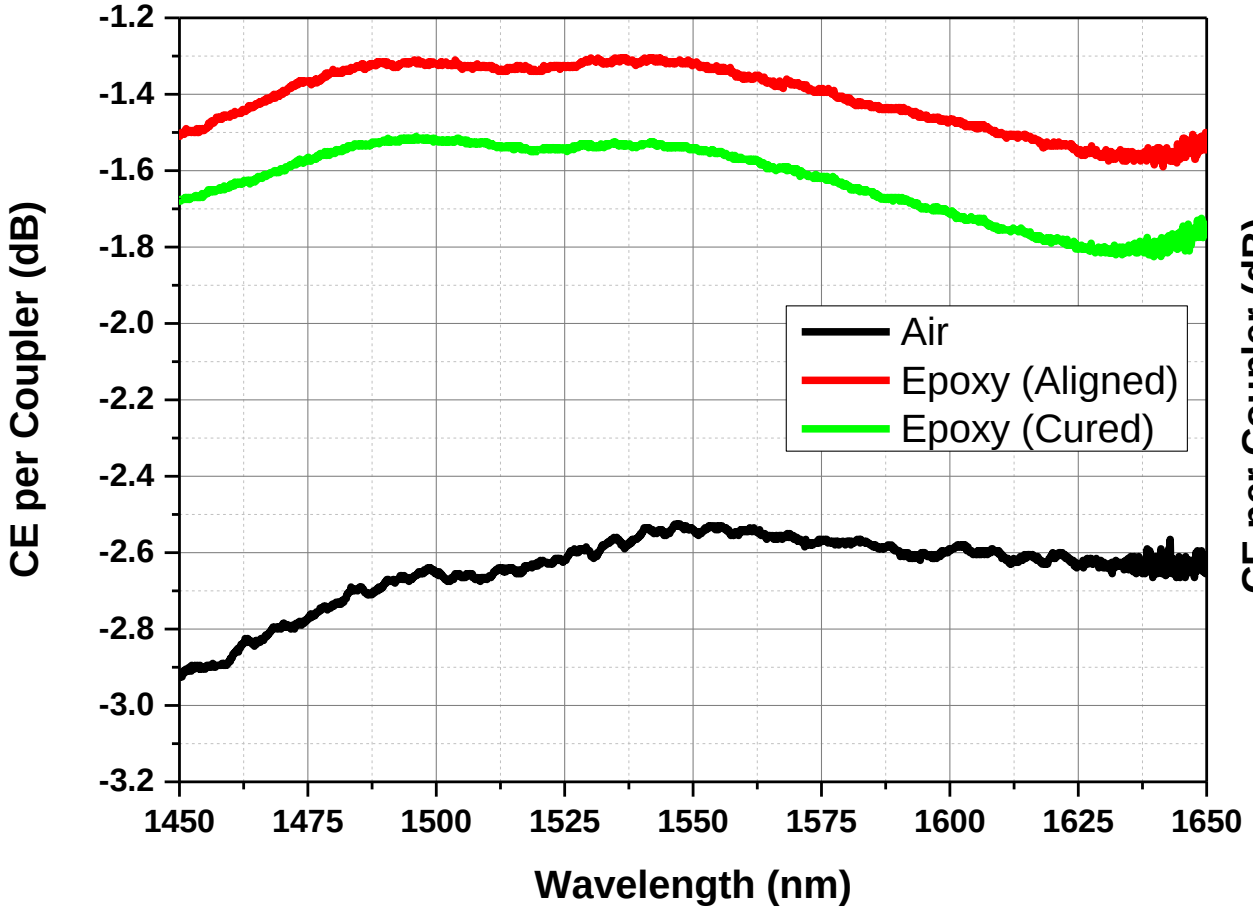
I. Align the PIC Assembly

III. Apply & Cure the Epoxy at the back

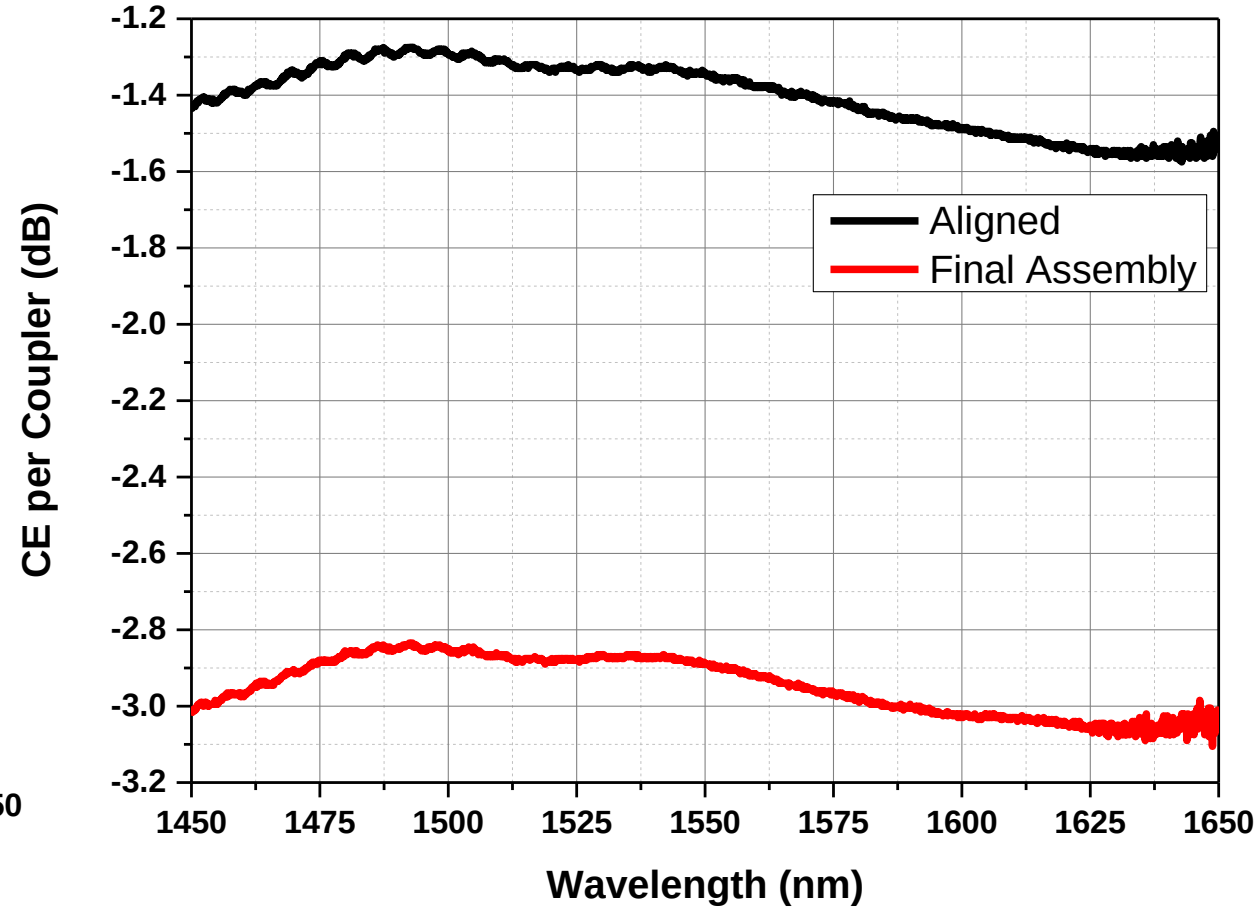
DELO DUALBOND® OB6268 → Hg-Lamp, fibre-coupled

Coupling Efficiency

Lens→PIC



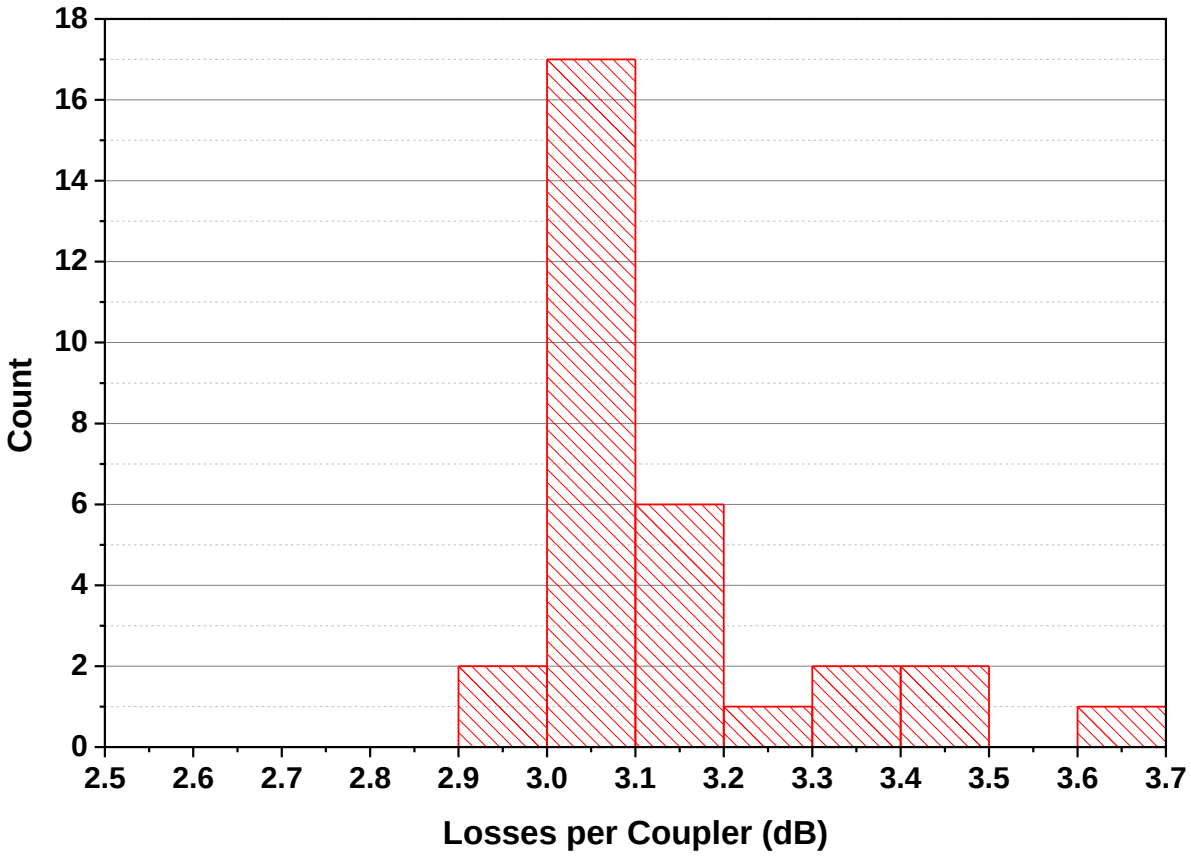
PIC Assembly→Package



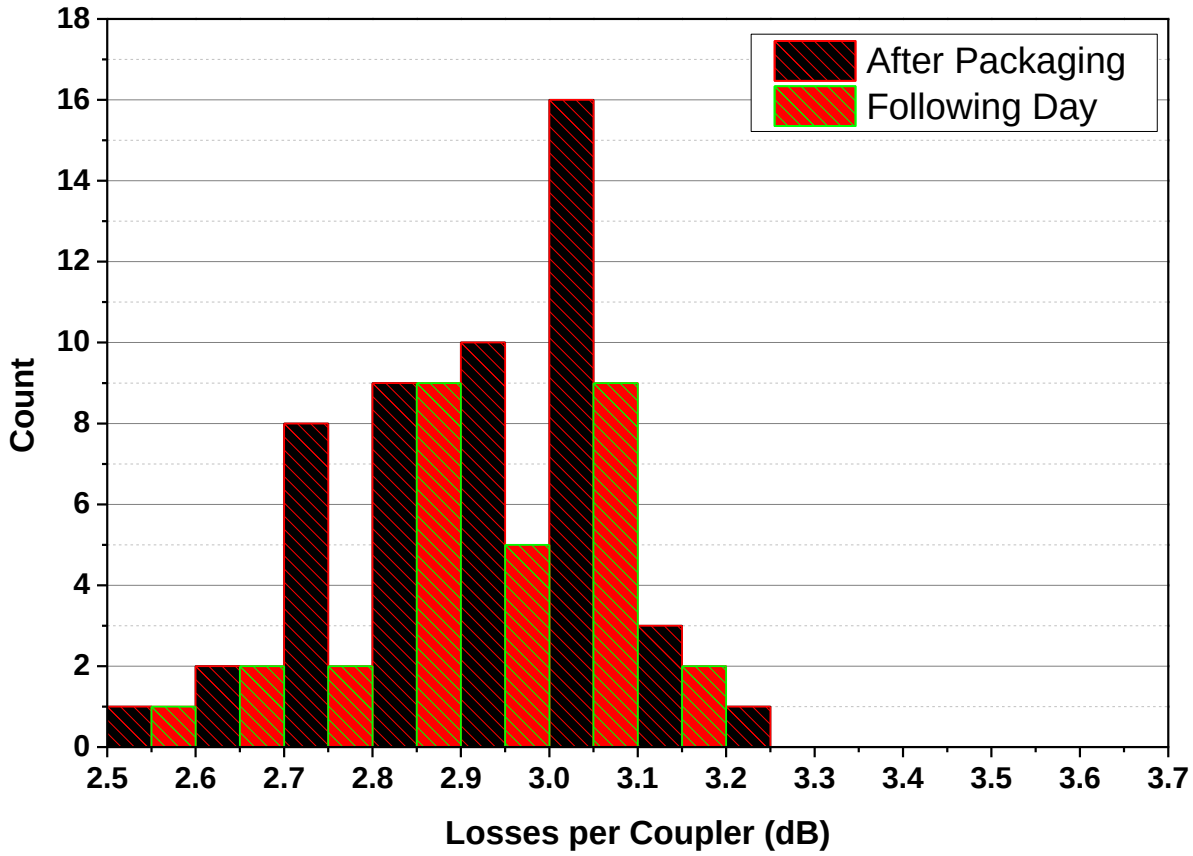
Pluggable Operation

Demonstration of Pluggable Operation – Histogram

Prototype #1



Prototype #2



Special Challenges Encountered

- Project was delayed due to COVID-related delay in PIC supply. Original projection of 9-month duration became 13 months.
  - Project was originally scheduled to be completed by the end of December 2021.
  - PIC samples were available a few months late.
  - Team declared work finished and project goals met at the end of April 2022.

- Agreement between simulated chip coupling efficiency and experimentally measured coupling efficiency is not as good as expected.
  - Kamil Gradkowski (Tyndall) and David Stegall (3M) have continued working on understanding this since April.
  - Team's current suspicion is that values specified for some component characteristics needed in modeling may not correspond to the actual properties of the components.
  - Team has agreed to pursue this issue as part of Phase 2.

Project Presentations, Publications and Publicity

To Date:

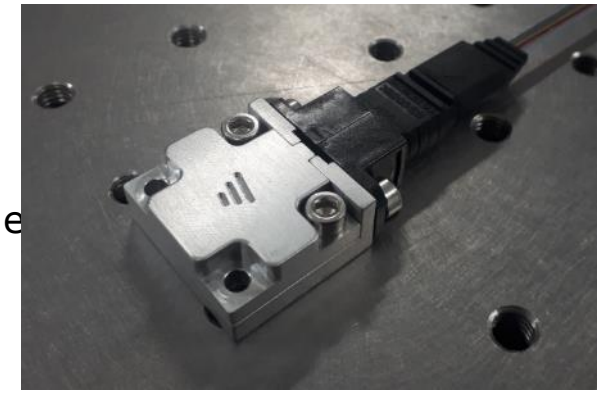
- "Module with Separable Single-Mode Expanded-Beam Optical Interface for Edge-Coupled PIC Optics", IEC SC86C WG4 (Active Devices), March 2022
- "Module with Separable Single-Mode Expanded-Beam Optical Interface for Edge-Coupled PIC Optics", IEC SC86B WG4 (Test and Measurement), May 2022
- "Module with Separable Single-Mode Expanded-Beam Optical Interface for Edge-Coupled PIC Optics", IEC SC86B WG6, WG6 (Connectors), May 2022
- "Demonstration of a Single-Mode Expanded-Beam Connectorized Module for Photonic Integrated Circuits", European Conference on Optical Communication (ECOC 2022), Basil, Switzerland, Sept. 2022.
- "Module with Separable Single-Mode Expanded-Beam Optical Interface for Edge-Coupled PIC Optics", IEC 86B; 86C (Passive and Active Devices) October 2022.
- Demonstration of a Single-Mode Expanded-Beam Connectorized Module for Photonic Integrated Circuits," IEEE/OSA Journal of Lightwave Technology, 24 January 2023, pp 1-9.

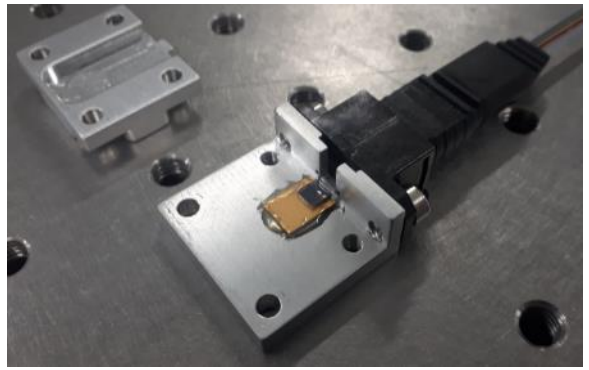
Program Participants

Next Steps - Phase 2

Motivation:

- Expanded beam connectors can provide mechanically robust and contamination-tolerant optical interfaces in fiber-to-fiber connections, but have not yet been adapted to PIC module interfaces.
- Current processes for assembling connectorized-PIC modules are complex and require multiple precision alignments. Development of a simpler process for providing a robust connector interface on a PIC can simplify PIC development and increase market acceptance.





Phase 1 Module

Objective:

- Investigate and optimize the design and assembly considerations for reliable high-volume alignment and assembly of pluggable connectors to show advantages in terms of size, density (no. of channels) and/or optical performance

Strategy/Approach:

- Build on the progress of the Phase 1 Project, utilizing the same PICs, and improving the initial module designs and processes developed.
- Characterize performance improvements resulting from different optical and mechanical designs and assembly processes, especially those related to connectors and optical alignment.

Longer impact:

- Develop design rules for manufacturable pluggable photonic packages (for edge-coupled PICs).
- Regular updates to optic standards committees and publish technical journal articles

Status:

- Refining Phase 2 scope
- New Participation welcome
- Contact gomalley@inemi.org

New project - Characterization of Adhesives for Optical Packaging

Motivation:

- Photonics and co-packaging applications are expanding
- Stable optical and mechanical adhesive systems are needed to ensure reliable optical and mechanical performance
- There is an industry-wide lack of test methods and standards.

Objective:

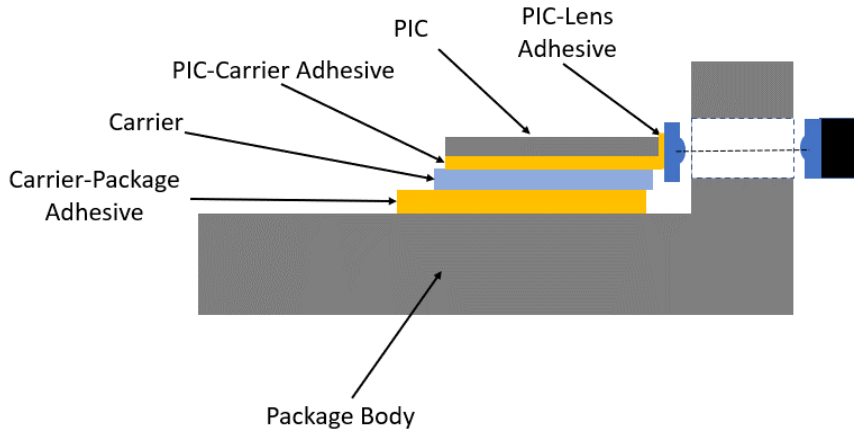
- Investigate adhesive characterization and test methodologies.
- Identify key materials properties to ensure thermal stability and optimize optical and mechanical performance.

Strategy/Approach:

- To validate and recommend methods for testing adhesives at various thicknesses and different temperature ranges (quantum to solder reflow)
- To identify and measure key properties for model development (models today are too simple – need material database)

Leadership/Participants:

- Expected Participants: Materials suppliers, Testing houses, Packaging and Assembly service providers.



Status:

- Led by Delo and Tyndall
- Project in planning phase
- Contact: gomalley@inemi.org

New project - Board-Level Optical Interconnect Performance in Immersion-Cooled Environments

Motivation:

- Immersion cooling is gaining strong traction as a means of energy-efficient and environmentally friendly thermal management in HPCs and data centers.
- On-board optics is gaining importance through co-packaged optics and mid-board optics being used to provide a path to higher interconnect bandwidth.
- There is insufficient understanding of how optical interconnect components will perform in immersion-cooled environments.

Source: Microsoft

Objective:

- To evaluate the compatibility of optical interconnect components (connectors, cables, optical elements, transceivers, etc.) with different immersion cooling environments, including single-phase and dual-phase.
- To understand how interconnect materials and design factors affect performance and reliability of optical interconnect systems in immersion environments

Strategy/Approach:

- Develop an immersion testbed and test protocol for characterizing a representative variety of different on-board/mid-board transceiver, connector and cable solutions in important classes of immersion fluids.
- Evaluate optical interconnect performance under realistic operating conditions.
- Understand degradation mechanisms, develop accelerated testing protocols, and generate guidelines for design and materials choices.

Longer term:

- Report to standards bodies (IEC, ISO, ITU)

Status:

- Of interest to OEM's and all those involved with photonics integration, midboard optics & co-packaged optics
- Chair: Richard Pitwon
- Contact: Grace O'Malley gomalley@inemi.org

Contacts:

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Kamil Gradkowski
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www.Tyndall.ie

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The 21st C – The age of the photonic device

1990 | 2000 | 2010 | 2020 | 2030 → integrated photonics

Age of µ-electronics, growth of photonics, analog downstream	sm fiber comms, birth of the internet, digital downstream	Smartphones, birth of eco-system & interconnectivity	IoT & smart systems, expanding big data	Smart sensors & autonom. mobility connected over 5G	50bn conn. devices, quantum technology optical computing

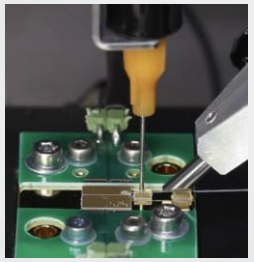
Global presence

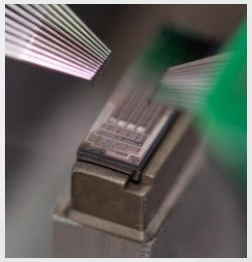
20 years of state-of-the-art photonics assembly & test. 1,000+ systems installed and supported globally for a customer base comprising *the* technology leaders across Europe, Asia and N. America.

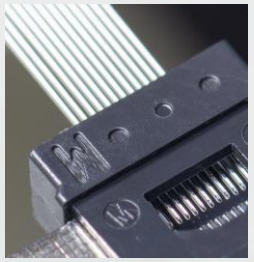
Positioning In Product Development Flow

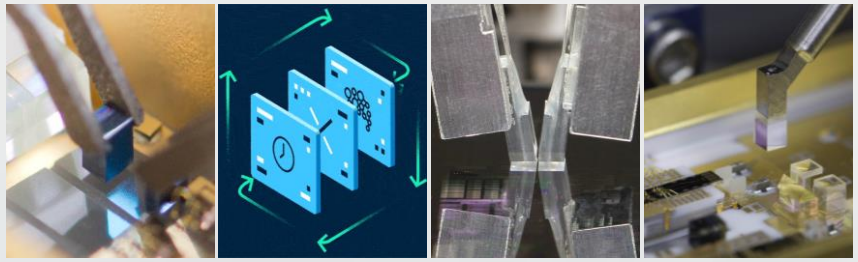
High volume manufacturing

Device Design → R&D / Prototyping → Validation Testing → Process Development → Production → Verification (EoL) Testing → Packaging / Integration → Integration & Test







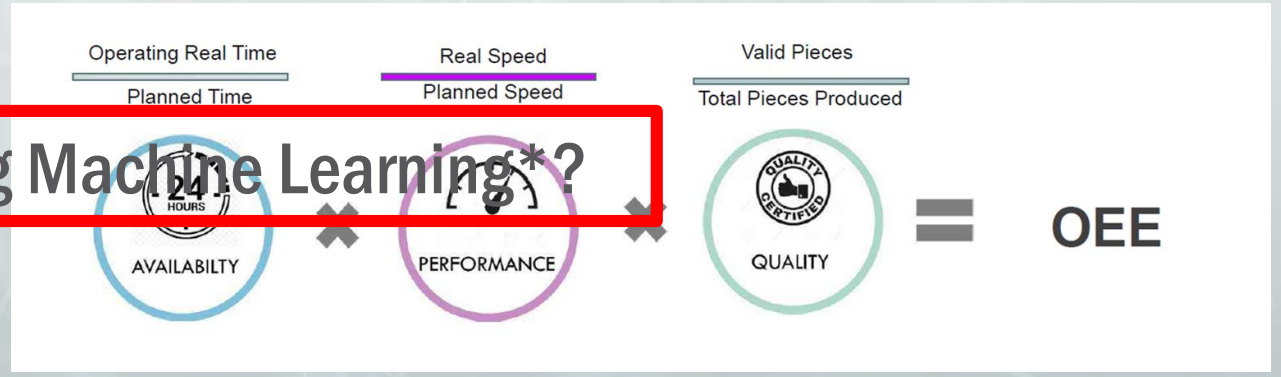


Task / Requirements:	align-&-attach (passive/active) or custom assembly at die or wafer level	test-&-qualify at die or wafer level	process automation & optimization & system design for die or wafer level	low-volume & batch production or high-volume in-line manufacturing with preventative maintenance via ML-based Performance Services at die or wafer level
Product lines:	AssemblyLine BondLine FiberLine CustomLine	TestLine	AssemblyLine BondLine FiberLine CustomLine	AssemblyLine | BondLine | FiberLine TestLine | InspectionLine StackLine | Weld
System platform:	Entry-level Stand-alone	Stand-alone In-line as stand-alone	Stand-alone In-line as stand-alone	Stand-alone (batch production) In-line (HVM)

High Volume Photonics Packaging: A Chance for ML?

Requirements in Production:

- High OEE (Overall Equipment Effectiveness)
- Fast & frequent product ramp-ups
- Complex production processes
  - ➢ Interdependence of parameters
  - ➢ Abundance of data



Can we justify not using Machine Learning*?

*data driven model calculation

Machine Learning in Photonics Packaging: Challenges

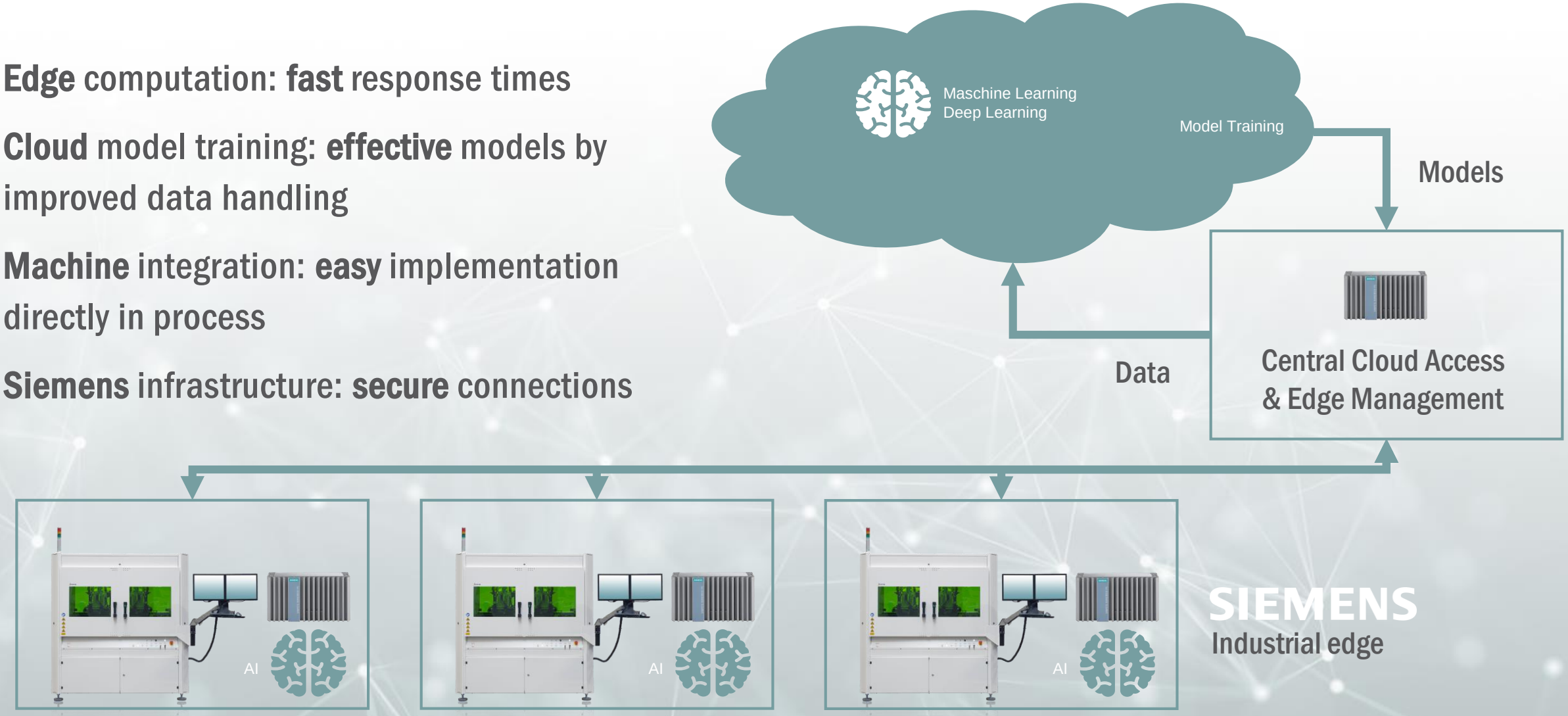
- Short product life cycle
  - ➢ Low model life time
- Lack of unified standards
  - ➢ Model transfer constrained
- Global value chains
  - ➢ No data scientists available on the factory floor

How to make Machine Learning field-proof?

infrastructure, self-adaptive production, self-learning models

Infrastructure: Edge, Cloud & Machine

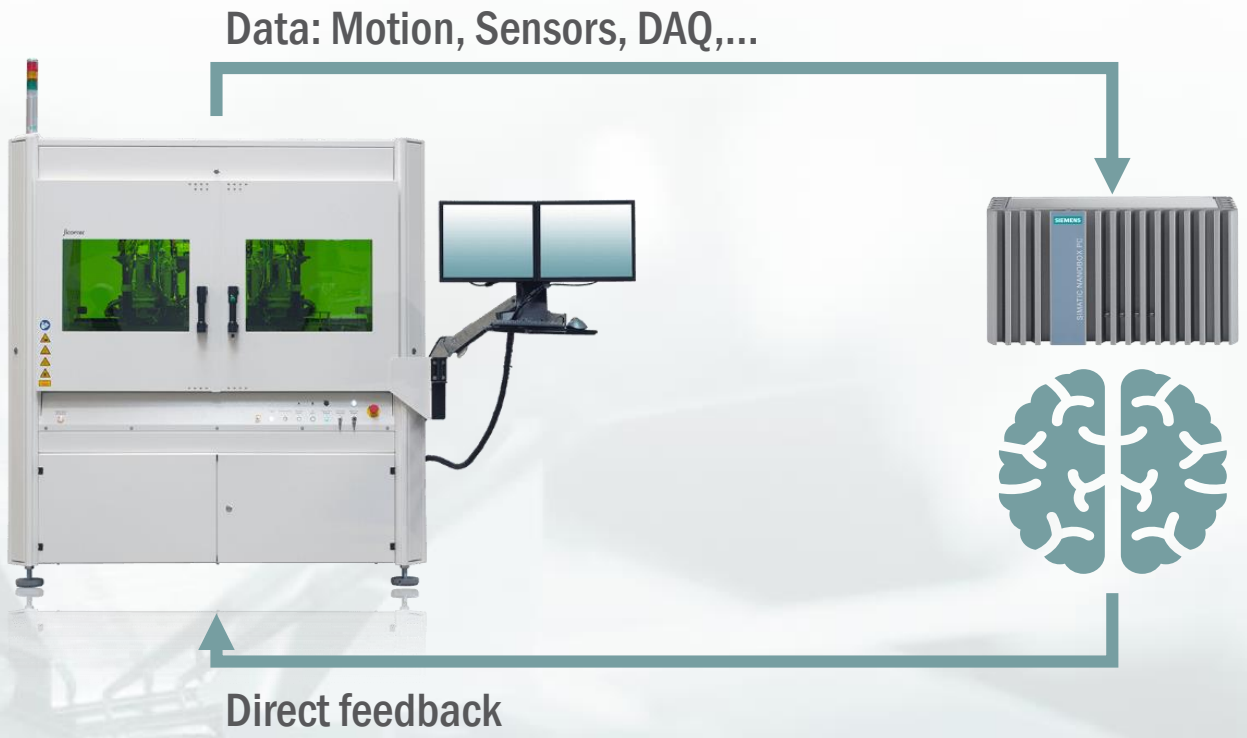
- **Edge** computation: **fast** response times
- **Cloud** model training: **effective** models by improved data handling
- **Machine** integration: **easy** implementation directly in process
- **Siemens** infrastructure: **secure** connections



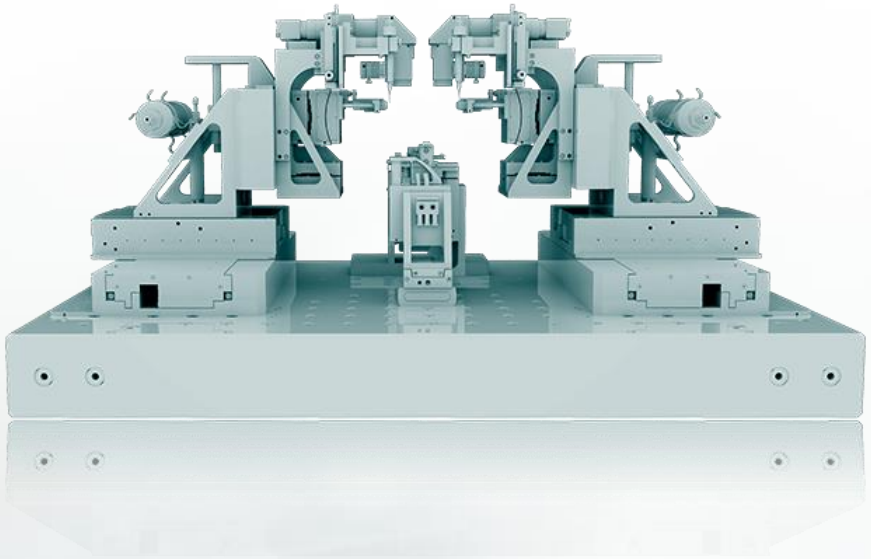
Self-Adaptive Production

Machine Performance improvement by direct feedback to machine

- Machine parameters adapt automatically to changing conditions
- Direct feedback - no human interaction
- Complete automation



Adaptive Motion



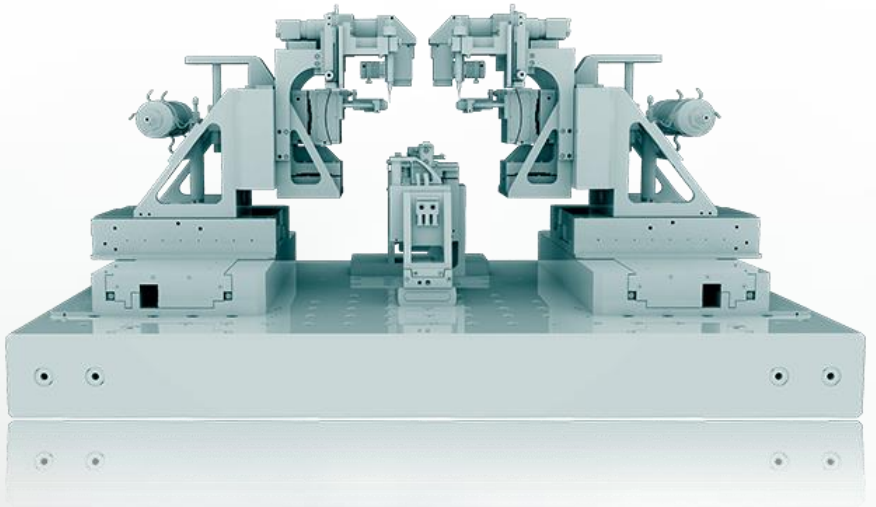
Optimum motion is a trade off:

- High throughput
  - ➢ fast motions
- High yield
  - ➢ accurate motions
  - ➢ Early alerting to prevent part loss
- Field conditions
  - ➢ Performance degradation over time

Ideally we could measure motion accuracy in the field!

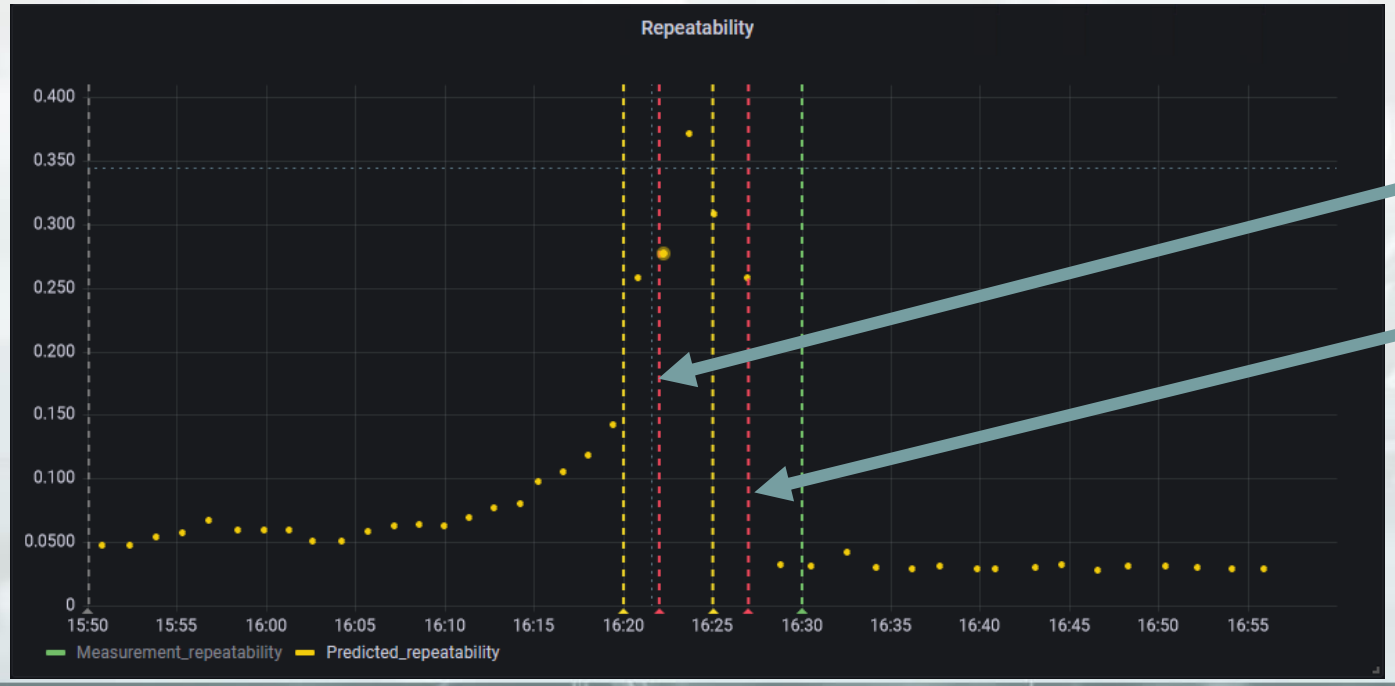
How?

Adaptive Motion



Finding optimum balance between precision & speed

- In real time & during production
- No measurement required in production
- Flexible configuration of response



Repeatability close to max spec, slow down motion

Yield at risk, stop production

Adaptive motion dashboard

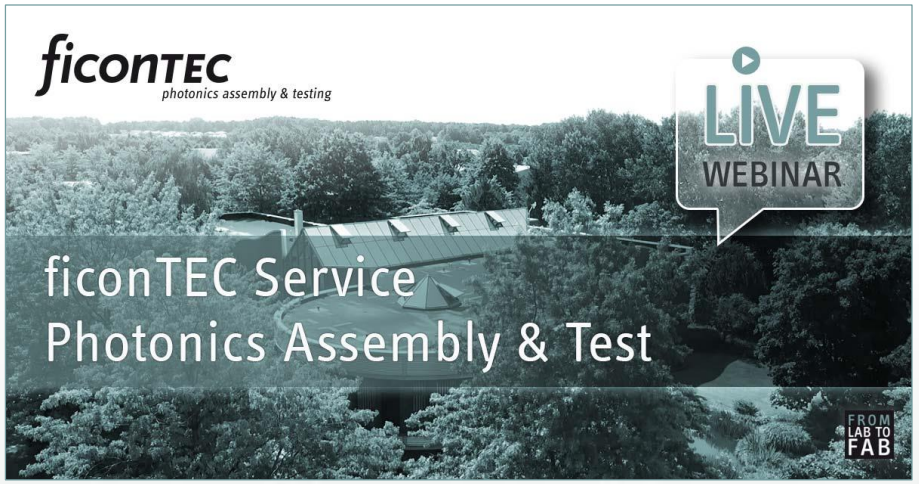
WHERE DOES THAT TAKE US?

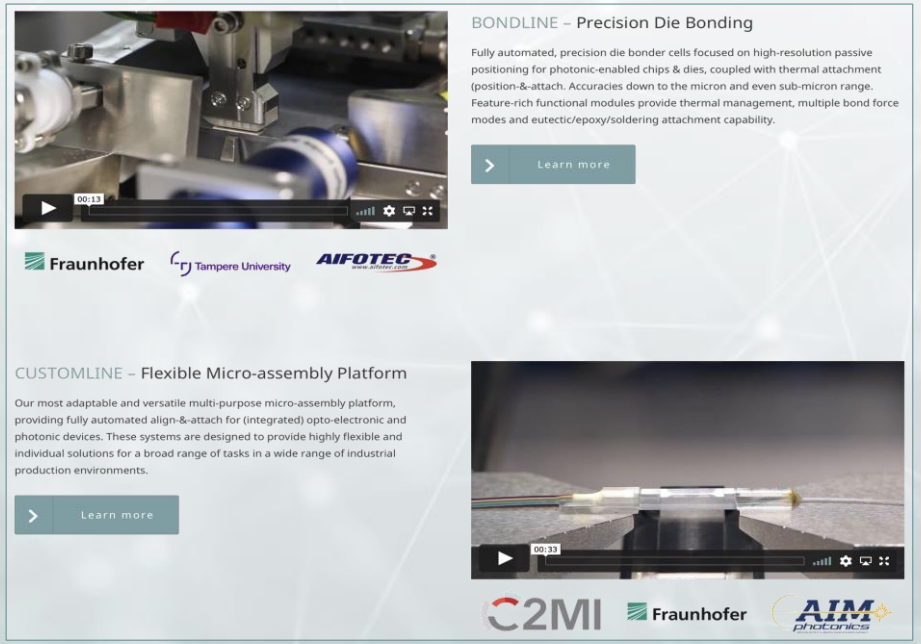
>10% OEE improvement* achieved by

1. **3-10% UPH improvement by self-adaptive production (2 use cases)**
2. **Yield & Process control by automated analysis & alerting**
   - Custom visualization, analysis & alerting for Process Parameters & KPIs
3. **Downtime reduction by Predictive maintenance**
   - Prediction of critical component failure & alerts for preemptive repair

*OEE: Overall Equipment Effectiveness = Availability x relative UPH x Yield

Finding out more …





BLOG

Online:

- Homepage
- ‘ficonTEC Insider’ Blog
- LinkedIN / Twitter
- Vimeo / YouTube
- Locations & Contacts

Thank you!

Process Control & Alerting

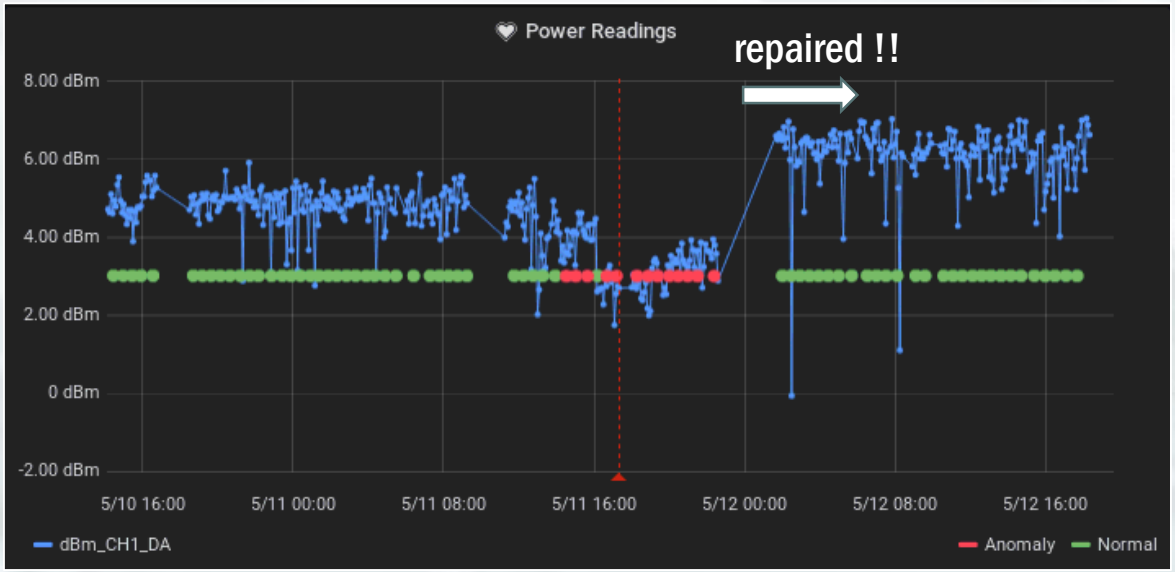
Dashboards & alerting customizable on machine via Open source visualization

- Intuitive interface for customization
- Rollout via ficontec revision control system
- Alerts issued as pop-up in machine process, text message or by email
- Standardized dashboards for KPI analysis included

Predictive Maintenance

Scope

- Monitoring of standardized components: Linear axis systems, Goniometers,...
- Combination with adaptive motion to detect failure before yield is affected
- Leveraging data for reliable ML models: Combination of ficontec data with customer data



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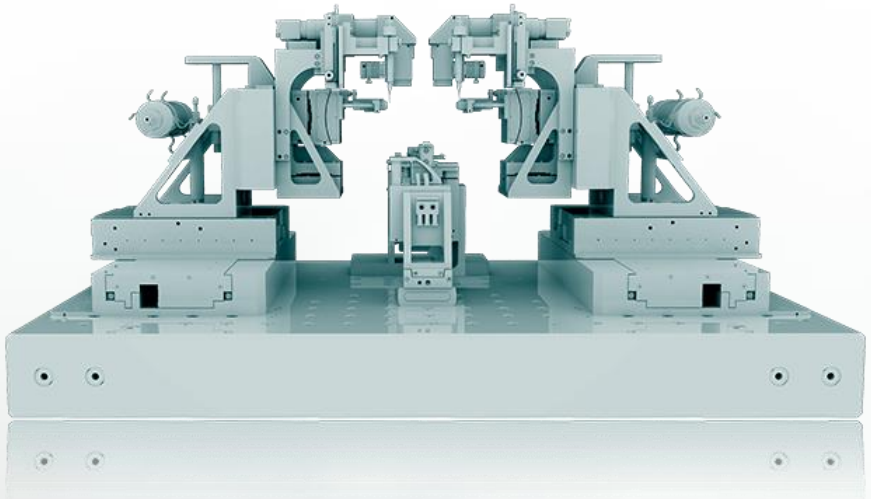

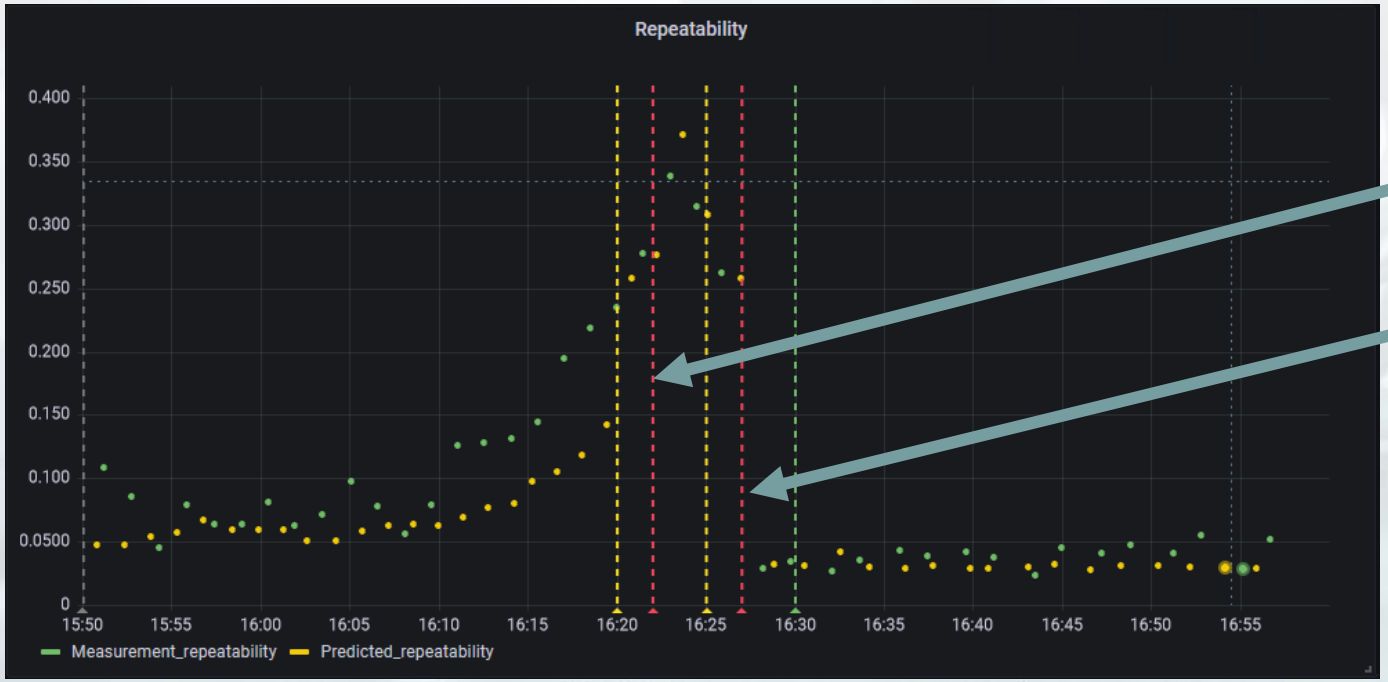

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