The 2023 IEEE 73rd Electronic Components and Technology Conference

May 30 – June 2, 2023

2023 Conference Program & Exhibitor Listings

JW Marriott Orlando, Grande Lakes
Orlando, Florida USA

Sponsored by

Program Supported by

AT&S

For more information visit www.ECTC.net

WELCOME TO THE 73rd ECTC FROM THE GENERAL CHAIR AND PROGRAM CHAIR

On behalf of the Program and Executive Committee, it is my pleasure to invite you to IEEE's 73rd Electronic Components and Technology Conference (ECTC), which will be held at JW Marriott Orlando, Grande Lakes, Orlando, Florida from May 30 to June 2, 2023. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses, foundry and OSAT service providers, substrate makers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1500 people attended ECTC 2022 in what was our first in-person event in three years.

At the 73rd ECTC, around 350+ technical papers are scheduled to be presented in 36 oral sessions and 5 interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as wafer-level and fan-out packaging, 2.5D, 3D and heterogeneous integration, interposers, chiplets, advanced substrates, assembly, materials and thermal modeling, reliability, packaging for harsh conditions, packaging for quantum and AI applications, interconnections, packaging for high speed and high bandwidth, photonics, flexible and printed electronics. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over twenty countries are expected to present their work at the 73rd ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry, such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature seven special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, five special sessions, 90 minutes each, are scheduled. On Tuesday morning, May 30th at 8:30 a.m. Tanja Braun, Fraunhofer IZM, and Przemyslaw Gromala, Robert Bosch GmbH, will chair the session on Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment, followed by Thomas Gregorich, Infinera, and Chaoqi Zhang, Qualcomm chairing a special session at 10:30 a.m. on Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications. On Tuesday afternoon at 1:30 p.m. Stéphane Bernabé, CEA-Leti, and Hiren Thacker, Cisco, will host a special session on the topic of Photonic Integrated Circuit Packaging, followed by a special session on the CHIPS Act, organized by Nancy Stoffel, GE Research, Jan Vardaman, TechSearch International, and William Chen, ASE.

As in previous years, HIR will host a parallel track throughout the day, with four exciting and complementary sessions on AI/ML in Package Co-Design for Chiplets Perspective, Heterogeneous Integration of MEMS & Sensors: Challenges and Opportunities; The CHIPS and Science Act; Additively Manufactured Electronics for Heterogeneous Integration.

On Tuesday evening, the Young Professionals reception will be organized by Yan Liu, Medtronic. Next, Takashi Hisada, IBM, and Yasumitsu Orii, Rapidus, will co-chair the IEEE EPS Seminar on High-Density Substrates.

New this year, the following days (Wednesday-Friday) will kick off with a single-room special session from 8:00 a.m. to 9:15 a.m., which will then be followed by our traditional technical sessions with six parallel tracks. On Wednesday May 31st at 8 a.m., join us early to receive our Welcome message from our General Chair Ibrahim Guven, followed by a captivating presentation and Q&A session by our Keynote speaker Prof. Michael Manfra from Purdue University; the title of the Keynote is "Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging".

At the end of the day, at 6:30 p.m., a special session/reception, co-hosted by ECTC and ITherm, will discuss workforce development for semiconductors and packaging. The panel will be chaired by Kim Yess, Brewer Science, Nancy Stoffel, GE Research, and Christina Amon, University of Toronto. This reception/panel event should not be missed.

On Thursday June 1st at 8 a.m., we will have the pleasure of starting the day with our ECTC Plenary Session, featuring an extensive panel of experts focused on next-generation millimeter-wave packaging. The 75-min session will be chaired by Kevin Gu, Metawave Corporation, and Ivan Ndip, Fraunhofer IZM / Brandenburg Technical University. Kitty Pearsall, Boss Precision, Inc., IEEE EPS President, and David McCann, Lyte, will chair the EPS President's ECTC panel session on Friday morning at 8 a.m. The session will focus on how photonics can enable the bandwidth densities with lower energy per bit in emerging SIP.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and the ECTC Exhibition. Co-located with the IEEE ITherm Conference, the 73rd ECTC will offer 16 CEU-approved PDCs, organized by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 30th and are taught by distinguished experts in their respective fields. The ECTC Exhibition will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than 120 exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 73rd ECTC and to be a part of all the exciting technical and professional opportunities. I also want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 73rd ECTC a success. I look forward to meeting you at the JW Marriott Orlando, Grande Lakes, Orlando, Florida, May 30 – June 2, 2023.

Ibrahim Guven
73rd ECTC General Chair
iguven@vcu.edu

Florian Herrault
73rd ECTC Program Chair
floherrault@gmail.com

WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of the IEEE Electronics Packaging Society, I am delighted to welcome you to the 73rd Electronic Components and Technology Conference – the world's premier event for electronics packaging. Starting 73 years ago, ECTC continues to grow, innovate, and serve our community with an exciting technical program detailing the latest advances in electronics packaging. Building upon the outstanding event from last in-person years and the very positive feedback to our virtual conferences, we expect attendance at ECTC 2023 to well exceed 1400 packaging professionals. This is a fantastic achievement. Our conference portfolio continues to find innovative ways to grow and serve our community. Together with ECTC and our Asia-Pacific flagship conference EPTC, to be held in December, EPS expects to reach similar well attended in-person conferences world-wide in 2023. These achievements would not be possible without the dedication and commitment of our conference organizers and volunteers. I would like to express my sincere thanks to the ECTC Executive and Program Committees, members of the EPS Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their outstanding efforts in bringing you this year's exciting event. We are fortunate to have such an enthusiastic team that keeps finding new ways to serve the electronic packaging community. May I also thank our authors, presenters, and sponsors for their contributions to this year's event. It is very rewarding to see the significant benefits that events such as ECTC have on the Electronics Packaging Society, our industry, and our members. In addition to conferences, EPS has been implementing its exciting plans for membership, chapters, publications, education, and technology to provide a unique service to our members worldwide. You can find more information about these activities at the EPS website. Finally, may I thank you for attending this year's ECTC. Enjoy the conference, and I look forward to meeting you again at one of our future events.

Kitty Pearsall
EPS President 2022-2023

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Conference organizers reserve the right to cancel or change this program without prior notice.

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, seminars, meals, exhibits and IP areas, and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
Please follow hotel policies and signs regarding this. Smoking is also NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, seminars, meals, exhibits and IP areas, and all conference social functions. Thank you for your consideration and cooperation.

REGISTRATION AND GENERAL INFORMATION

REGISTRATION LOCATION AND HOURS

ECTC registration is located at the Grande Registration Desk in the JW Marriott Grande Lakes, across from Mediterranean 3 (lobby level).

Monday, May 29, 2023 – 3:00 p.m. - 6:00 p.m.
Tuesday, May 30, 2023 – 6:45 a.m. - 7:45 p.m.*
(From 6:45 a.m. – 8:15 a.m. registration is for morning session PDC and Special Session Attendees)*
Wednesday, May 31, 2023 – 6:45 a.m. - 4:00 p.m.
Thursday, June 1, 2023 – 7:00 a.m. - 4:00 p.m.
Friday, June 2, 2023 – 7:00 a.m. - 12:00 p.m.

On Tuesday, May 30th light morning refreshments will be provided from 6:45am – 7:30am. Come pick up your registration materials EARLY and grab a bite to eat before our PDC's and Special Sessions start!

****The above schedule for Tuesday will be vigorously enforced to prevent attendees from being late for their courses and sessions. Please make sure to take advantage of the 6:45am start time as registration becomes very congested prior to the start of morning programming.***

DOOR REGISTRATION FEES

Door Registration with Proceedings Download

IEEE Member Pricing

JOINT (full ECTC + ITHERM conference) $1250
IEEE Member Full Registration $950
IEEE Member Speaker / Session Chair $850
IEEE Member One Day $625
IEEE Member Speaker One Day $550

Non-Member Pricing

JOINT (full ECTC + ITHERM conference) $1500
Non-Member Full Registration............................ $1150
Non-Member Speaker / Session Chair $850
Non-Member One Day.................................. $625
Non-Member Speaker One Day $550

Student... $340
Student Speaker $340

Tuesday Professional Development Courses

IEEE Members

Tuesday AM or PM Course with luncheon.................. $440
Tuesday All-Day Courses with luncheon.................... $625

Non-Members

Tuesday AM or PM Course with luncheon.................. $490
Tuesday All-Day Courses with luncheon.................... $675

Tuesday Student All-Day Courses with luncheon $150
Extra Luncheon Tickets for Each Day.................. $75

PROFESSIONAL DEVELOPMENT COURSE INSTRUCTORS BREAKFAST

7:00 a.m. Tuesday
Room Location: Cordova 5 – 6; lower level

PDC Instructors and Proctors are required to attend a briefing breakfast.

SESSION CHAIRS AND SPEAKERS BREAKFAST

7:00 a.m. Wednesday thru Friday
Room Location: Palazzo E

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC.

SPEAKER PREP ROOM

7:00 a.m. – 5:00 p.m., Tuesday – Friday
Room Location: Brava, lower level

Speakers should prepare and review their digital presentations within the allotted times above.

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

GENERAL INFORMATION

Hotel Concierge

The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Press Room

Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eperfecto@gmail.com or (845) 475-1290.

LUNCHEONS

(Room Location: Mediterranean 4 & 5)

This year ECTC will be offering a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. Lunch tickets, found in your registration badge holder, must be presented for entrance into the lunch room. Lost lunch tickets will cost $75 to replace. Please come and enjoy time with other attendees and colleagues in the industry!

Lunch times will vary, see below for specific details for each day.

Tuesday: 12:00 Noon – 1:15 p.m.

Wednesday: 12:45 p.m. – 1:45 p.m.

Thursday: 12:45 p.m. – 1:45 p.m.
Sponsored by: The IEEE Electronics Packaging Society

Friday: 12:45 p.m. – 1:45 p.m.
Don't miss out on this lunch! We will be raffling off several prizes including a hotel stay, free conference registrations, and many other industry gadgets!

General Chair's Speakers Reception

Tuesday, May 30, 2023 • 6:00 p.m. – 7:00 p.m.
(by invitation only)

ECTC Student Reception

Tuesday, May 30, 2023 • 5:00 p.m. – 6:00 p.m.
Location: Outside: Mediterranean 4 & 5 Porte Cochere

Hosted by Texas Instruments, Inc.

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry, and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them succeed in their first job search and reach their current positions. During this reception, you can enjoy good food while networking with industry leaders and achievers. Don't miss your opportunity to interact with people who you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

Exhibition Reception

Wednesday, May 31, 2023 • 5:30 p.m. – 6:30 p.m.
Location: Coquina Ballroom
Open to all conference attendees.

73rd ECTC Gala Reception

Thursday, June 1, 2023 • 6:30 p.m.
Location: Outside: Valencia (lower level)

Sponsored by Koh Young Technologies, Inc.

All registered attendees and their guests are invited to attend.

EPS Worldwide Chapter Officer Meeting

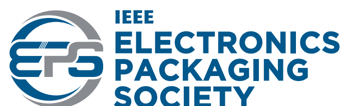
Please attend in person if you are an officer of EPS Chapter or EPS student Chapter.

(Online by invitation)
Thursday June 1, 2023 • 7:00 a.m. – 8:00 a.m.
Room: Cordova 6

Chapter Program Director: Toni Mattila
Reg 1-7 and 9: Annette Teng
Reg 8: Tanja Braun
Reg 10: Andrew Tay

ECTC Mobile App

ECTC is pleased to announce that a free mobile app "Whova" is available again this year. The app provides information on schedules for our technical program and PDCs as well as exhibitors, sponsors, and venue maps. The app also features tools to set your schedule, so you don't miss presentations important to you, social interaction functions, and the ability to provide ratings on presentations that are used in selecting candidates for best paper awards. The app is available for iOS and Android devices from their respective app stores by searching "Whova". After downloading the Whova app please log in using the email address you used to register for ECTC, and the ECTC content will appear automatically. Alternatively, a generic app invitation code will be made available onsite at the conference for attendees.



New This Year

We are proud to announce that a selection of papers will be invited to be published as journal publications in the IEEE Transactions on Components, Packaging, and Manufacturing Technology after the conference. The journal manuscript will have to follow the Transaction guidelines.

73rd ECTC CONFERENCE OVERVIEW

2023 ECTC Special Session on Advanced Packaging for Harsh Environments

Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment – Current Status and Opportunities

Tuesday, May 30, 2023, 8:30 a.m. – 10:00 a.m.

Chairs: Tanja Braun, Fraunhofer IZM, and Przemyslaw Gromala, Robert Bosch GmbH

Palazzo D

Electronic components and systems are among the main contributors to the most innovative ideas and products of today's world. In the automotive industry, electronic components and systems are accountable for more than 80% of all innovation. When we think about highly automated and autonomous systems, advanced packaging is a must. Nowadays, most advanced electronic components such as CPUs or GPUs are being introduced into harsh environments such as automotive, avionics or space applications almost at the same time as in consumer products. Therefore, in our special session, we would like to discuss with the top experts from industry and academia what the current status and opportunities are for advanced packaging for harsh environments.

Ramesh S., General Motors; Giuseppe Barone, Robert Bosch GmbH; Vikas Gupta, ASE US, Inc.; Dae-Woo Kim, Samsung; Shin-Puu Jeng, TSMC; Ram Trichur, Henkel; Kouchi Zhang, TU Delft; Vanessa Smet, Georgia Tech

2023 ECTC Special Session on Hybrid Bonding

Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications

Tuesday, May 30, 2023, 10:30 a.m. – 12:00 p.m.

Chairs: Thomas Gregorich, Infinera, and Chaoqi Zhang, Qualcomm

Palazzo D

This Special Session will explore the applications, requirements, and challenges of Copper Hybrid Bonds (CHB) for Chip-to-Wafer (C2W) applications. Wafer-to-wafer CHB has been in HVM for many years and continues to expand. While C2W is in production, challenges remain. This panel will discuss challenges and solutions for the expanded use of C2W Copper Hybrid Bonds.

The session will include a moderator and speakers, each with a 10-minute presentation followed by a joint 20-minute Q&A session.

Jan Vardaman, TechSearch International; Eric Beyne, IMEC; Xavier Brun, Intel: Kenneth Larsen, Synopsys; Raja Swaminathan, AMD; Thomas Uhrmann, EVG; Chris Scanlan, Besi

2023 ECTC Special Session on Photonics Packaging

Photonic Integrated Circuit Packaging: Challenges, Pathfinding, and Technology Adoption

Tuesday, May 30, 2023, 1:30 p.m. – 3:00 p.m.

Chairs: Stéphane Bernabé, CEA-Leti, and Hiren Thacker, Cisco

Palazzo D

Photonic integrated circuit (PIC) technologies are proliferating into many application spaces; from hyperscale data center, high-performance computing to sensing including LiDAR. Packaging remains the greatest challenge to high-volume manufacturing at high throughput and yield. The main challenges are: Optical coupling, TSV integration for chiplet or photonic interposer approaches, laser integration, thermal management, manufacturability, and reliability. While there are currently only limited standardization activities (OIF, COBO, IEC SC86C/WG4) addressing these challenges, the need for innovative solutions is growing to merge semiconductor 3D packaging technologies and photonics. This session will feature leading practitioners who are actively driving PIC packaging innovation and technology adoption toward high-volume reality.

Gianlorenzo Masini, Cisco; Thierry Mourier, CEA-Leti; Hesham Taha, Teramount; Alexander Janta-Polczynski, IBM; Peter O'Brien, Tyndall Institute; Colin Dankwart, Ficontec Service GmbH

2023 ECTC Special Session on CHIPS Act

Advanced Packaging Manufacturing in North America: Building the Ecosystem

Tuesday, May 30, 2023, 3:30 p.m. – 5:00 p.m.

Chairs: Nancy Stoffel, GE Research, Jan Vardaman, TechSearch International, and William Chen, ASE

Palazzo D

North America has companies that excel in design for electronics systems, device, and advanced packaging. However less than 2% of the packaging occurs in the US. This session will discuss the ambitious goals being set through the CHIPS ACT to bring Advanced Packaging to North America. We will review the targets and developing plans of the US government, funded through the CHIPS Act. The panelists will overview major initiatives launched in R&D and Manufacturing. We will also discuss the challenges to meeting the goals.

Joshua Dillon, Marvell Technology Inc.; Frank Gayle NIST, Office of Advanced Manufacturing; Subramanian Iyer, University of California Los Angeles; Carl McCants, DARPA; Dick Otte, Promex Industries, Inc.; Hem P. Takiar, Micron Technology Inc.

2023 ECTC Heterogeneous Integration Roadmap (HIR) Workshop

Tuesday, May 30, 2023, 8:00 a.m. – 4:30 p.m.

Chairs: William Chen – ASE, Bill Bottoms – 3MTS and Ravi Mahajan – Intel

Palazzo E

Heterogeneous Integration uses packaging technology to integrate dissimilar chips, devices or components with different materials and functions, and from different fabless design houses, foundries, wafer materials, feature sizes and companies into a system or subsystem. 23 Technical working groups will present on their areas of expertise. This workshop is a full-day event with the following schedule.

8:00 a.m. – 8:30 a.m. Welcome & Agenda Review

8:30 a.m. – 10:00 a.m. AI/ML in Package Co-Design for Chiplets Perspective

10:15 a.m. – 11:45 a.m. Heterogeneous Integration of MEMS & Sensors: Challenges and Opportunities

Lunch Break

1:15 p.m. – 2:45 p.m. The CHIPS and Science Act

3:00 p.m. – 4:30 p.m. Additively Manufactured Electronics for Heterogeneous Integration

2023 Young Professionals Networking Panel

Tuesday, May 30, 2023, 7:00 p.m. – 7:45 p.m.

Chair: Yan Liu, Medtronic

Palazzo D

This event is designed just for you – young professionals (including current graduate students). In this active event, we will pair you with senior EPS members and professionals through a series of active and engaging activities. You will have opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

2023 IEEE EPS Seminar on High-Density Substrates

The Future of High-density Substrates – Towards Submicron Technology

Tuesday, May 30, 2023, 7:45 p.m. – 9:15 p.m.

Chairs: Takashi Hisada, IBM, and Yasumitsu Orii, Rapidus

Palazzo E

Chiplets and Heterogeneous Integration (HI) technologies are expected to drive performance and efficiency enhancement of semiconductor modules while Si scaling is slowing down. One of the key attributes of chiplets and HI technologies is the bandwidth of interconnection between chips within the same package. A very short-distance and high-density interconnection from one chip to another enables high-speed data transmission with low energy loss. High-density chip carrier substrate is the core technology driving the evolution of chiplets and HI technologies.

The EPS Seminar organized by TC6 (High-Density Substrate and Board) will discuss ultra-fine-pitch substrate technologies towards submicron ground rule for Chiplets and Heterogeneous Integration. We will have 5 panelists, and each panelist will give a short talk presenting insights on technology trends, technical challenges, application requirements, recent technical updates, and more covering advanced interposer technologies, followed by a panel discussion.

Yasushi Araki, Shinko; Yu-Hua Chen, Unimicron ; Satoru Kuramochi, Dai Nippon Printing (DNP; Madhavan Swaminathan, Penn State University; Griselda Bonilla, IBM

2023 Keynote Speaker

Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging

Wednesday, May 31, 2023, 8:00 a.m. – 9:15 a.m.

Prof. Michael J. Manfra, Purdue University

Mediterranean 4 & 5

Quantum computing will revolutionize the way we tackle certain societally relevant but currently intractable problems. To reach this promise, significant advances in quantum hardware on multiple scales are required. This keynote address will explore the challenges and opportunities in quantum computing hardware ranging from basic choice of qubit platform, through scalable control and readout, to system architecture. Technology advancement will require innovations in material science and device physics to tackle challenges on the quantum plane. Progress will also hinge on innovations in interconnect technology and advanced packaging for an integrated quantum-classical hardware system. As in classical digital computing, thermal management and reliability concerns will impact quantum system performance and must be addressed directly. In this presentation, some exemplars that demonstrate the opportunities for contributions to quantum technology from the community focused electron devices, interconnects and advanced packaging will be discussed. Development of a full-stack quantum computer necessitates industrial programs stimulated and informed by innovation generated in government labs and academic research groups.

2023 ECTC/ITherm Diversity and Career Growth Panel and Reception

Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative

Wednesday, May 31, 2023, 6:30 p.m. – 7:30 p.m.

Chairs: Kim Yess, Brewer Science / ECTC, Nancy Stoffel, GE Research / ECTC, and Cristina Amon, University of Toronto / ITherm

Mediterranean 4 & 5

The electronic industry has an urgent need to increase the technical workforce and address challenges related to recruitment, inclusion and retention of diverse talents. The panelists will discuss the development of initiatives, policies and programs to increase and diversify the workforce, along with metrics to assess progress. Discussions will include the benefits of diversity in high-performing workplaces (improve productivity, innovation), strategies to build a diverse workforce, and tools for inclusion and engagement – sharing both successes and challenges associated with achieving these goals.

Dereje Agonafer, University of Texas Arlington; Courtney Power, NextFlex; Jennifer Edwards, GE Foundation / NEXT Engineer; NIST CHIPS Representative

2023 ECTC Plenary Session on mm-Wave Phased Array Packaging

Millimeter-Wave Phased Array Front-End Integration and Packaging for Next-Generation Communication and Radar Systems

Thursday, June 1, 2023, 8:00 a.m. – 9:15 a.m.

Chairs: Kevin Gu, Metawave Corporation, and Ivan Ndip, Fraunhofer IZM / Brandenburg University of Technology

Mediterranean 4 & 5

Phased arrays are critical components in next generation communication and radar sensing systems. Current state-of-the-art and rapidly emerging research and development on millimeter-wave front-end implementations have created tremendous opportunities for innovation in packaging technologies. In this plenary panel session, we invite six leading domain experts to present their pioneering works in this area. The panel discussion will be focused on major challenges and the latest advancements in packaging and integration technologies for designing and implementing phased array front-end modules, including different substrates, interconnects, antennas, hetero-integration of silicon and III-V chips, co-design with RFICs, thermal management, system demos/prototypes, and so on.

Jonathan Hacker, Teledyne Scientific; Augusto Gutierrez-Aitken, Northrop Grumman Space Systems; Hasan Sharifi, HRL Laboratories, LLC; Madhavan Swaminathan, Pennsylvania State University; Shahriar Shahramian, Nokia Bell Labs; Alberto Valdes-Garcia, IBM Research

2023 IEEE EPS President Panel on Photonics

How Can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP

Friday, June 2, 2023, 8:00 a.m. – 9:15 a.m.

Chairs: Kitty Pearsall, Boss Precision, Inc., and David McCann, Lyte

Mediterranean 4 & 5

This panel will discuss the tools, technologies, and approaches that will enable the industry to enhance the bandwidth density of interconnections in SiP enabled by photonics. To be adopted, such capabilities must be provided with energy per bit that meets the roadmaps and standards targets for the interconnection protocols within the package and on the chip.

Amr S. Helmy, University of Toronto; Ritesh Jain, Lightmatter; Ajey Jacob, University of Southern California; Stefano Oggioni, ATS

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 30, 2023

Morning Courses 8:00 a.m. – 12:00 Noon	Afternoon Courses 1:30 p.m. – 5:30 p.m.
Palazzo B **1. High Reliability of Lead-Free Solder Joints – Materials Considerations** *Course Leader: Ning-Cheng Lee – ShinePure Hi-Tech*	Palazzo B **9. Additive Flexible Hybrid Electronics – Manufacturing and Reliability** *Course Leader: Pradeep Lall – Auburn University*
Palazzo A **2. Wafer-Level Chip-Scale Packaging (WCSP) Fundamentals** *Course Leader: Patrick Thompson – Texas Instruments, Inc.*	Palazzo A **10. Fan-Out Packaging and Chiplet Heterogeneous Integration** *Course Leader: John Lau - Unimicron*
Mediterranean 3 **3. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Level and Advanced RF Packages** *Course Leaders: Ivan Ndip – Fraunhofer IZM/ Brandenburg University of Technology and Markus Wöhrmann – Fraunhofer IZM*	Mediterranean 3 **11. Photonic Technologies for Communication, Sensing, and Displays** *Course Leader: Torsten Wipiejewski – Huawei Technologies*
Mediterranean 2 **4. Eliminating Failure Mechanisms in Advanced Packages** *Course Leader: Darvin Edwards – Edwards Enterprises*	Mediterranean 2 **12. Flip Chip Technologies** *Course Leaders: Shengmin Wen – HaiSemi and Eric Perfecto – IBM Research*
– PDC 5 Canceled –	**– PDC 13 Canceled –**
Mediterranean 6 **6. Reliability Physics and Failure Mechanisms in Electronics Packaging** *Course Leader: Xuejun Fan – Lamar University*	Mediterranean 6 **14. Analysis of Fracture and Delamination in Microelectronic Packages** *Course Leader: Andrew Tay - National University of Singapore*
Mediterranean 7 **7. Reliable Integrated Thermal Packaging for Power Electronics** Course Leader: Patrick McCluskey – University of Maryland	Mediterranean 7 **15. Polymers in Wafer Level Packaging** *Course Leader: Jeffrey Gotro – InnoCentrix, LLC*
Mediterranean 8 **8. Introduction to PWB Thermal Analyses** *Course Leader: Patrick Loney - Northrop Grumman*	**– PDC 16 Canceled –**

Refreshment Breaks
10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Mediterranean & Palazzo Foyers

COMMITTEE MEETINGS

ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday May 30, 2023

8:00 a.m. – 4:30 p.m.
EPS HIR Workshop
Palazzo E

9:00 p.m. – 10:30 p.m.
ECTC OPTO Committee
Cordova 1 (lower level)

9:00 p.m. – 10:30 p.m.
ECTC Interconnect Committee
Cordova 2 (lower level)

Wednesday May 31, 2023

7:00 a.m. – 8:00 a.m.
EPS Power & Energy TC
Cordova 6 (lower level)

7:00 a.m. – 8:00 a.m.
EPS Reliability TC
Cordova 1 (lower level)

7:00 a.m. – 8:00 a.m.
EPS 3D / TSV TC
Cordova 4 (lower level)

4:30 p.m. – 5:30 p.m.
EPS Technical Committee Chairs
Cordova 6 (lower level)

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
(by invitation only)

Thursday, June 1, 2023

7:00 a.m. – 8:00 a.m.
EPS Chapter Chairs Meeting
Cordova 6 (lower level)

7:00 a.m. – 8:00 a.m.
EPS Nanotechnology TC
Cordova 5 (lower level)

7:00 a.m. – 8:00 a.m.
EPS High Density Substrates & Boards TC
Cordova 1 (lower level)

7:00 a.m. – 8:00 a.m.
EPS EDMS TC
Cordova 2 (lower level)

7:00 a.m. – 8:00 a.m.
EPS Thermal & Mechanical TC
Cordova 3 (lower level)

5:30 p.m. – 6:30 p.m.
ECTC 2024 Program Committee Meeting
Mediterranean 2-3

9:00 p.m.
73rd ECTC Governing/ Executive Committee Reception
(by invitation only)

Friday June 2, 2023

7:00 a.m. – 8:00 a.m.
EPS RF & THz Tech. TC
Cordova 6 (lower level)

7:00 a.m. – 8:00 a.m.
EPS Materials & Process TC
Cordova 2 (lower level)

7:00 a.m. – 8:00 a.m.
EPS Photonics TC
Cordova 1 (lower level)

7:00 a.m. – 8:00 a.m.
EPS Emerging Tech TC
Cordova 4 (lower level)

9:00 a.m. – 10:00 a.m.
EPS T-CPMT SAE / AE's
Cordova 5 (lower level)

2:15 p.m. – 5:15 p.m.
ECTC Executive Committee
Cordova 5-6 (lower level)

5:30 p.m. – 6:30 p.m.
ECTC / EPS Steering Committee
Cordova 5-6 (lower level)

ECTC BEST PAPER AWARDS

BEST OF CONFERENCE PAPERS – 2022

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 72nd ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500, and the authors of the Best Interactive Presentation share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

Advanced Fan-Out Packaging Technology for Hybrid Substrate Integration

Lihong Cao, Teck Chong Lee, Rick Chen, Yung-Shun Chang, Hsingfu Lu, Nicholas Chao, Yen-Liang Huang, Chen-Chao Wang, and Chih-Yi Huang – ASE Group

Best Interactive Presentation Paper

Novel Zero Side-Etch Process for <1µm Package Redistribution Layers

Pratik Nimbalkar, Pragna Bhaskar, Christopher Blancher, Mohanalingam Kathaperumal, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology

INTEL BEST STUDENT PAPER – 2022

The winning student receives a personalized plaque and a check for US $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 72nd ECTC.

Co-Design of Thermal Management with System Architecture and Power Management for 3D ICs

Rishav Roy – Purdue University; Shidhartha Das, Benoit Labbe, Rahul Mathur, and Supreet Jeloka – ARM

OUTSTANDING PAPERS – 2022

The winning authors for the Conference Outstanding Session Paper and Interactive Presentation selected from the 72nd ECTC proceedings receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

Organic Interposer CoWoS-R+ (plus) Technology

M. L. Lin, M. S. Liu, H. W. Chen, S. M. Chen, M. C. Yew, C. S. Chen, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company

Outstanding Interactive Presentation Paper

Scalable through Mold Interconnection Realization for Advanced Fan Out Wafer Level Packaging Applications

Aurélia Plihon, Edouard Déschaseaux, Rémi Franiatte, Jérome Dechamp, Simon Vaudaine, Jennifer Guillaume, Catherine Brunet-Manquat, Stéphane Moreau, and Perceval Coudrain – CEA-LETI

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To sign-up for sponsorship or to get more details, please contact Alan Huffman at alan.huffman@ieee.org or +1-336-380-5124.

PROGRAM SESSIONS: WEDNESDAY, MAY 31, 9:30 A.M. -12:35 P.M.

Session 1: Heterogeneous Chiplet Integration	Session 2: High-Performance Packaging Materials	Session 3: Advancements in Copper/Silicon-Oxide Hybrid Bonding
Committee: **Packaging Technologies**	**Committee:** **Materials & Processing**	**Committee:** **Interconnections**
Palazzo D	**Palazzo A & B**	**Mediterranean 2 & 3**
Session Co-Chairs: **Andrew Kim – Apple, Inc.** **Email: hkim34@apple.com** **Mike Gallagher – Dupont Electronics and Imaging** **Email: michael.gallagher@dupont.com**	**Session Co-Chairs:** **Yoichi Taira – Keio University** **Email: taira@appi.keio.ac.jp** **Yi Li – Intel Corporation** **Email: yi.li@intel.com**	**Session Co-Chairs:** **Katsuyuki Sakuma – IBM Corporation** **Email: ksakuma@us.ibm.com** **Matthew Yao – GE Aviation** **Email: matthew.yao@ge.com**
1. 9:30 AM – Ultra High Density Low Temperature SoIC with Sub-0.5 µm Bond Pitch Han-Jong Chia, Shih-Peng Tai, Ji James Cui, Chuei-Tang Wang, Chih-Hang Tung, Kuo-Chung Yee, Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM – High Modulus Photosensitive Permanent Film Utilizing Novel Polymerization System for Advanced MEMS Structure Fabrication*** Ken-ichi Yamagata, Shiori Yuge, Ryosuke Nakamura, HIrofumi Imai – Tokyo Ohka Kogyo Co., Ltd.	***1. 9:30 AM – A Study on the Surface Activation of Cu and Oxide for Hybrid Bonding Joint Interface*** Bohee Hwang, Soohwan Lee, Youngkun Jee, Sangcheon Park, Gyeongjae Jo, Kwangbae Kim, Sungjin Han, Ilhwan Kim, Jumyong Park, Hyunchul Jung, Dongwoo Kang, Un-Byoung Kang – Samsung Electronics Co., Ltd.-Test and System Package
2. 9:50 AM – Process Integration of Photonic Interposer for Chiplet-Based 3D Systems Damien Saint-Patrice, Stephane Malhouitre, Myriam Assous, Thierry Pellerin, Remi Velard, Leopold Virot, Edouard Deschaseaux, Maria-Luisa Calvo-Munoz, Karim Hassan, Stephane Bernabe, Yvain Thonnart, Jean Charbonnier – CEA-LETI	***2. 9:50 AM – Lithographic Performance and Insulation Reliability of a Novel i-Line Photosensitive Dielectric Material*** Go Inoue, Daiki Yukimori, Kaho Shibasaki, Ayano Okuda, Nobuhiro Ishikawa, Toshiyuki Ogata – TAIYO HOLDINGS Co., Ltd.; Young-Gun Han, Taka Kanayama, Tadashi Suetsugu – Fukuoka University	***2. 9:50 AM – Fine Pitch Die-to-Wafer Hybrid Bonding*** Thomas Workman, Jeremy Theil, Gill Fountain, Dominik Suwito, Cyprian Uzoh, Guilian Gao, K. M. Bang, Bongsub Lee, Laura Mirkarimi – Adeia
3. 10:10 AM – Aggressive Pitch Scaling (sub-0.5 µm) of W2W Hybrid Bonding Through Process Innovations Tyler Sherwood, Raghav Sreenivasan, Jason Appell, Raghuveer Patlolla, Kun Li, Ki Cheol Ahn, Joe Salfelder, Ryan Ley – Applied Materials, Inc.; Thomas Kasbauer, Gernot Probst, Jurgen Burggraf, Thomas Uhrmann – EV Group, Inc.	***3. 10:10 AM – Effect of Surface Roughness of Polymer Dielectric Materials on Resolution of Fine Line Features*** Pragna Bhaskar, Mohanalingam Kathaperumal, Christopher Blancher, Mark Losego, Madhavan Swaminathan – Georgia Institute of Technology	***3. 10:10 AM – Direct Die to Wafer Cu Hybrid Bonding for Volume Production*** Chun Ho Fan, Hoi Ping Ng, Siu Cheung So, Ming Li, Siu Wing Lau, Thomas Uhrmann, Juergen Burggraf, Mariana Pires – ASMPT Hong Kong, Ltd.
Refreshment Break: 10:30 a.m.-11:15 a.m. – Coquina Ballroom		
4. 11:15 AM – Design Space Exploration (DSE) for over-136 GB/s IO Bandwidth with LPDDR5X SDRAM Packages on SOC Package in 200 mm^3 Heeseok Lee, Jun So Pak, James Jung, Jisoo Hwang – Samsung Electronics Co., Ltd.	***4. 11:15 AM – Novel High Reliability and Low Dk/Df Dielectric RDL Material for High Frequency 5G Applications*** Kaori Hamada, Hiroshi Ozaki, Toshiyuki Sato, Shin Teraki, Fumikazu Komatsu, Masaki Yoshida, Hirotatsu Ikarashi – NAMICS Corporation	***4. 11:15 AM – Demonstration of a Wafer Level Face-To-Back (F2B) Fine Pitch Cu-Cu Hybrid Bonding with High Density TSV for 3D Integration Applications*** Jerzy Javier Suarez Berru, Stephane Nicolas, Nicolas Bresson, Myriam Assous, Stephan Borel – CEA-LETI
5. 11:35 AM – 3D Stacking of Heterogeneous Chiplets on Modified FOWLP Platform with Thru-Silicon Redistribution Layer Tai Chong Chai, Boon Long Lau, Lim Pei Siang Sharon, David Ho Soon Wee – Institute of Microelectronics A*STAR; Rob Van Kampen, Paul Castillou, lance barron, Mickael Renault, jay ko, Jonathan Hammond – Qorvo, Inc.	***5. 11:35 AM – Single-Layer Release Material Having Laser Lift-Off and Chip Fixing Property for FO-WLP Chip First Process*** Okuno Takahisa, Shinjo Tetsuya, Usui Yuki, Fukuda Takuya, Yanai Masaki, Yagyu Masafumi – Nissan Chemical Industries	***5. 11:35 AM – Cu-Cu Wiring: The Novel Structure of Cu-Cu Hybrid Bonding*** Yoshihisa Kagawa, Takumi Kamibayashi, Nobutoshi Fujii, Shunsuke Furuse, Taichi Yamada, Tomoyuki Hirano, Hayato Iwamoto – Sony Semiconductor Solutions Corporation
6. 11:55 AM – Same Size Mold Chase Technology for Effective Stack Die Architectures Nabankur Deb, Xavier Brun, Yoshihiro Tomita – Intel Corporation; Chris Masuyama, Naoki Hamada, Yoshikazu Hirano – Towa Corporation	***6. 11:55 AM – Novel Photosensitive Polyimides Compositions with Low Dielectric Property and Good Flexibility Corresponding to Redistribution Layers for High Speed Transmission Applications*** Takashi Tazaki, Takashi Yamaguchi, Taiyo Nakamura, Madoka Yamashita – Arakawa Chemical Industries, Ltd.	***6. 11:55 AM – New Cu "Bulge-Out" Mechanism Supporting Sub-Micron Scaling of Hybrid Wafer-to-Wafer Bonding*** Jo De Messemaeker, Liesbeth Witters, Boyao Zhang, Ferenc Fodor, Joeri De Vos, Gerald Beyer, Kristof Croes, Eric Beyne – imec; Yan Wen Tsau – KU Leuven
7. 12:15 PM – A Novel Chiplet Integration Architecture Employing Pillar-Suspended Bridge with Polymer Fine-Via Interconnect Yasuhiro Morikawa – ULVAC, Inc.; Meiten Koh – Taiyo Ink Mfg. Co., Ltd.; Hiroyuki Hashimoto, Takafumi Fukushima – Tohoku University; Chuantong Chen, Wangyun Li, Katsuaki Suganuma – Osaka University; Ichiro Kono – AOI Electronics; Shinji Wakisaka – Oume Electronics; Ken Ukawa – Sumitomo Bakelite Co., Ltd.; Yoichiro Kurita – Tokyo Institute of Technology	***7. 12:15 PM – High Frequency Characteristics of Fine Copper Lines on High Rigidity Dielectrics*** Masataka Nishida, Hirokazu Noma, Tetsuro Iwakura, Masaki Yamaguchi, Kazuyuki Mitsukura – Resonac Corporation	***7. 12:15 PM – Electrical Analysis of Wafer-to-Wafer Copper Hybrid Bonding at Sub-Micron Pitches*** Kevin Ryan, Christopher Netzband, Adam Gildea, Yuji Mimura, Satohiko Hoshino, Ilseok Son, Hirokazu Aizawa, Kaoru Maekawa – TEL Technology Center, America, LLC

PROGRAM SESSIONS: WEDNESDAY, MAY 31, 9:30 A.M. -12:35 P.M.

Session 4: Assembly and Manufacturing Process Enhancement	Session 5: Underfilling and Chip-Package-Interaction	Session 6: Co-packaged Optical Assembly
Committee: Assembly and Manufacturing Technology	**Committee: Thermal/Mechanical Simulation & Characterization**	**Committee: Photonics**
Mediterranean 1	**Mediterranean 6**	**Mediterranean 7 & 8**
Session Co-Chairs: Rameen Hadizadeh – Cirrus Email: rameen.hadizadeh@gmail.com Christo Bojkov – Qorvo, Inc. Email: cbojkov.ectc@gmail.com	**Session Co-Chairs: Xuejun Fan – Lamar University Email: xuejun.fan@lamar.edu Yong Liu – ON Semiconductor Email: Yong.Liu@onsemi.com**	**Session Co-Chairs: Ajey Jacob – University of Southern California Email: ajey@isi.edu Takaaki Ishigure – Keio University Email: ishigure@appi.keio.ac.jp**
1. 9:30 AM – Heterogeneous Integration of Diamond Heat Spreaders for Power Electronics Application Henry Antony Martin – Chip Integration Technology Center/Delft University of Technology; Marcia Reintjes, Xiao Tang – Mintres BV; Dave Reijs, Sander Dorrestein, Martien Kengen, Sebastien Libon, Edsger Smits, Marco Koelink – Chip Integration Technology Center; Rene Poelma, Willem Van Driel, GuoQi Zhang – Delft University of Technology	***1. 9:30 AM – Comparative Study of Process-Reliability Interaction of Additive Circuits with Low-Temperature Solders ECAs and Magnetically Oriented ACAs*** Pradeep Lall, Jinesh Narangaparambil, Ved Soni – Auburn University; Scott Miller – NextFlex	***1. 9:30 AM – A Heterogeneously Integrated Wafer-Level Processed Co-Packaged Optical Engine for Hyper-Scale Data Centres*** Sajay Bhuvanendran Nair Gourikutty, Boon Long Lau, Wen Wei Seit, Ming Chinq Jong, David Ho Soon Wee, Jiaqi Wu, Teck Guan Lim, Rathin Mandal, Ser Choong Chong, Lai Yee Chia, Surya Bhattacharya – Institute of Microelectronics A*STAR; Li Xin, Tsung-Yang Liow – Rain Tree Photonics Pte. Ltd.
2. 9:50 AM – Optimum Rc Control and Productivity Boost in Wafer-Level Packaging Enabled by High-Throughput UBM/RDL Technology Carl Drechsel, Patrik Carazzetti, Juergen Weichart, Ewald Strolz – Evatec AG; Carl Wang – Evatec AG, Taiwan; Kay Viehweger – Fraunhofer IZM	***2. 9:50 AM – Addressing sub-Micron Thermal Warpage: Industrial Application on Semiconductor Devices*** Safia Benkoula – STMicroelectronics; Rodolfo Cruz, Pierre Vernhes – INSIDIX	***2. 9:50 AM – High Density Integration Technologies for SiPh Based Optical I/Os*** Karlheinz Muth, Hari Potluri, Sukesh Kannan – Broadcom, Inc.
3. 10:10 AM – Assembly Challenges and Approaches for 2.5D Chiplet Based System Sharon Pei Siang Lim, Mihai Dragos Rotaru, Wen Wei Seit, Hsiao Hsiang Yao – Institute of Microelectronics A*STAR	***3. 10:10 AM – Optimization of 2.2D Underfill Process by Novel Methodology and Direct Observation of Capillary Underfill Process*** Chia-Peng Sun, Yu-En Liang – CoreTech System (Moldex3D); Dyi-Chung Hu, Er-Hao Chen – SiPlus Co., Ltd.; Jeffrey ChangBing Lee – iST-Integrated Service Technology, Inc.; Srikar Vallury – Moldex3D Northern America, Inc.	***3. 10:10 AM – Photonic System Integration by Applying Microelectronic Packaging Approaches Using Glass Substrates*** Henning Schroeder, Oliver Kirsch – Fraunhofer IZM; Daniel Weber – Technical University Berlin; Hendrick Thiem – TOPTICA eagleyard
Refreshment Break: 10:30 a.m.-11:15 a.m. – Coquina Ballroom		
4. 11:15 AM – A Methodology to Optimize Laser Dicing Parameters to Maximize Dicing Quality Through Machine Learning Sathya Raghavan, Aakrati Jain, Prabudhya Roy Chowdhury, Katsuyuki Sakuma – IBM Research; Roman Doll, Kees Biesheuvel, Faysal Boughorbel, Jeroen Van Borkulo, Mark Mueller – ASMPT ALSI B.V.	***4. 11:15 AM – Strain-Relief Patterns for Flexible Substrate-Supported Optimized Serpentine Configurations*** Rui Chen, Chong Ye, Colin Stewart, Suresh Sitaraman – Georgia Institute of Technology	***4. 11:15 AM – Co-Packaged Optics on Glass Substrates for 102.4 Tb/s Data Center Switches*** Lucas Yeary, Lars Brusberg, Seong-ho Seok, Jung-Hyun Noh, Alon Rozenvax, Cheolbok Kim – Corning, Inc. 5. 11:35 AM – Innovative Fan-Out Embedded Bridge Structure for Co-Packaged Optics Jay Li, Sam Lin, Teny Shih, Nicholas Kao, Yu-Po Wang – Siliconware Precision Industries Co., Ltd.
5. 11:35 AM – Maskless Lithography for High-Density Package Redistribution Layers Prahalad Murali, Pratik Nimbalkar, Mohanalingam Kathaperumal, Mark D. Losego, Rao Tummala, Madhavan Swaminathan – Georgia Institute of Technology	***5. 11:35 AM – Filler Particle Distribution Impact for Interfacial Delamination of Underfill*** Yutaka Suzuki, Jaimal Williamson, Li Jiang, Rajen Murugan – Texas Instruments, Inc.	***5. 11:35 AM – Innovative Fan-Out Embedded Bridge Structure for Co-Packaged Optics*** Jay Li, Sam Lin, Teny Shih, Nicholas Kao, Yu-Po Wang – Siliconware Precision Industries Co., Ltd.
6. 11:55 AM – An Additive Approach to Embed Chips in a Metallic Matrix Infused PCB Roberto Aga, Fahima Ouchen – KBR, Inc./U.S. Air Force Research Laboratory; Rachel Aga – Wright State University; Carrie Batsch, Emily Heckman – AFRL	***6. 11:55 AM – A Time and Cost-Efficient Design Methodology to Estimate Effective Thermal Conductivities in System-on-Chips with Composite Materials*** Ki Wook Jung, Eunju Hwang, Jun Seomun, Sangyun Kim – Samsung Electronics Co., Ltd.-Foundry Business	***6. 11:55 AM – AIM Photonics Demonstration of a 300 mm Si Photonics Interposer*** Colin McDonough, Seth Kruger, Tat Ngai, Sarah Baranowski, David L. Harame – SUNY Research Foundation/SUNY Polytechnic Institute/AIM Photonics; Hao Yang, Skylar Deckoff-Jones, Christopher V. Poulton, Michael R. Watts – Analog Photonics
7. 12:15 PM – Micro Transfer Printing Various Thickness Components Directly from Dicing Tape Kevin Oswalt, David Gomez, Tanya Moore, Prasanna Ramaswamy, Alin Fecioru – X-Celeprint Ltd.	***7. 12:15 PM – On the Effect of Partial Underfilling on the Fatigue Life of Flip-Chip Micro-Solder Bumps in a Heterogeneously Integrated TSI Package Using Finite Element Simulations*** Sasi Kumar Tippabhotla, Ji Lin – Institute of Microelectronics A*STAR	***7. 12:15 PM – Advanced 3D Integration TSV and Flip Chip Technologies Evaluation for the Packaging of a Mobile LiDAR 256 Channels Beam Steering Device Designed for Autonomous Driving Application*** Thierry Mourier, Nadia Miloud-Ali, Natacha Raphoz, Yacoub Sahouane, Patrick Peray, Damien Saint-Patrice, Edouard Deschaseaux – CEA-LETI; Francois Simoens – Steerlight

PROGRAM SESSIONS: WEDNESDAY, MAY 31, 2:00 P.M. - 5:05 P.M.

Session 7: Large Formfactor Dense System Integration by Fan-Out	Session 8: Novel Reliability Test Methods	Session 9: Innovations in Copper Chip-to-Wafer Bonding
Committee: **Packaging Technologies**	**Committee:** **Applied Reliability**	**Committee:** **Interconnections**
Palazzo D	**Palazzo A & B**	**Mediterranean 2 & 3**
Session Co-Chairs: **Steffen Kroehnert – ESPAT Consulting, Germany** **Email: steffen.kroehnert@espat-consulting.com** **Bora Baloglu – Intel Corporation** **Email: bora.baloglu@intel.com**	**Session Co-Chairs:** **S. B. Park – Binghamton University** **Email: sbpark@binghamton.edu** **Sandy Klengel – Fraunhofer IMWS** **Email: sandy.klengel@imws.fraunhofer.de**	**Session Co-Chairs:** **Wei-Chung Lo – Industrial Technology Research Institute** **Email: lo@itri.org.tw** **Ou Li – Advanced Semiconductor Engineering, Inc.** **Email: ou.li@aseus.com**
1. 2:00 PM – 3D Freeform Antenna-in-Package Approach for FOWLP Tanja Braun, Tina Thomas, Karl-Friedrich Becker, Thi Huyen Le, Christian Tschoban, Rolf Aschenbrenner – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University Berlin	***1. 2:00 PM – A New Vibration Test Method for Automotive and Consumer Electronic Devices: Calibration and Fatigue Test*** Dongji Xie, Joe Hai – Nvidia Corporation; Andy Zhang – Texas Instruments, Inc.; Jeffrey Lee – iST-Integrated Service Technology, Inc.; Romuald Roucou – NXP Semiconductor, Inc.; Xue Shi – Bosch Automotive Products Co., Ltd.; Sushil Doranga – Lamar University; Valeriy Khaldarov – ASONIKA, LLC	***1. 2:00 PM – Critical Challenges with Copper Hybrid Bonding for Chip-to-Wafer Memory Stacking*** Wei Zhou, Michael Kwon, Yingta Chiu, Huimin Guo, Bharat Bhushan, Bret Street, Kunal Parekh, Akshay Singh – Micron Technology, Inc.
2. 2:20 PM – Comparable Study for Redistribution Layers in FO POP RDL First and Last (Fan-Out Package on Package) Kuei Hsiao Kuo, Derrick Tai, Sam Peng, Feng Lung Chien – Siliconware Precision Industries Co., Ltd.	***2. 2:20 PM – Magnetic Force-Based Measurement Technique to Investigate the Effect of Lead-Free Solder Intermetallic Compounds (IMC) on Interconnect Reliability*** Rui Chen, Suresh Sitaraman – Georgia Institute of Technology; Nicholas Ginga – University of Alabama in Huntsville	***2. 2:20 PM – Development of Copper Thermal Coefficient for Low Temperature Hybrid Bonding*** Sefa Dag, Ming Liu, Liu Jiang, Amir Kiaee, Gilbert See, Prayudi Lianto, Buvna Ayyagari-Sangamalli, El Mehdi Bazizi – Applied Materials, Inc.
3. 2:40 PM – Extremely Large Area Integrated Circuit (ELAIC): An Advanced Packaging Solution for Chiplets Rabindra Das, Jason Plant, Alex Wynn, Matthew Ricci, Ryan Johnson, Matthew Stamplis, Brian Tyrrell, Kenneth Schultz, Paul Juodawlkis – MIT Lincoln Laboratory	***3. 2:40 PM – Residual Stress Measurement of Build-Up Layer in Silicon Wafers*** Junbo Yang, Chongyang Cai, Yangyang Lai, Jong Hwan Ha, Seungbae Park – Binghamton University; Huayan Wang, Suresh Ramalingam, Gamal Refai-Ahmed – Advanced Micro Devices, Inc.	***3. 2:40 PM – Impact of Plasma Activation on Copper Surface Layer for Low Temperature Hybrid Bonding*** Christopher Netzband, Kandabara Tapily, Dylan Burns, Ilseok Son, Cory Wajda – TEL Technology Center, America, LLC
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Coquina Ballroom		
4. 3:45 PM – Advanced Fan-Out Panel Level Package (FO-PLP) Development for High-End Mobile Application Hyungmin Kim, Jaehoon Choi, Seok Won Lee, Eun Seok Cho, Hwasub Oh, Junho Lee, Seungsu Ha, Wonkyung Choi, Dong Wook Kim – Samsung Electronics Co., Ltd.	***4. 3:45 PM – Chip Level Evaluation of Wafer-to-Wafer Direct Bonding Strength with Bending test*** Juno Kim, Kyungmin Baek, Min-soo Han, Kyeongbin Lim, Minwoo Daniel Rhee – Samsung Electronics Co., Ltd.-Mechatronics Research	***4. 3:45 PM – Investigation of Cu-Cu Direct Bonding Process Utilized by High Porosity and Nanocrystal Structure*** Takuma Nakagawa, Daiki Furuyama, Sho Nakagawa, Yutaro Mori, Kotaro Iwata, Kiyotaka Nakaya, Takuma Katase – Mitsubishi Materials Corporation
5. 4:05 PM – Integrating Chiplets Using Chips First Ultra-High-Density Fan-Out with Maskless Laser Direct Imaging and Adaptive Patterning for High Performance Computing Benedict San Jose, Cliff Sandstrom, Erick Talain, Jan Kellar, Tim Olson – Deca Technologies, Inc.; Mary Maye Melgo, Rizi Gacho, Byung Cheol Kim – Nepes Hayyim Corporation	***5. 4:05 PM – In-Situ Observation of Microscale Crack-Tip Strain Field Evolution in Underfill with Different Toughening Agents via SEM-DIC Coupled Method*** Xuecheng Yu, Gang Li, Yixuan Fan, Rong sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology	***5. 4:05 PM – A High Throughput Two-Stage Die-to-Wafer Thermal Compression Bonding Scheme for Heterogeneous Integration*** Krutikesh Sahoo, Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles
6. 4:25 PM – Reliability Challenges of Large Organic Substrate with High-Density Fan-Out Package Rosa Lin, Laurene Yip, Charles Lai, Cooper Peng – MediaTek, Inc.	***6. 4:25 PM – Experimental Identification of the Failure Modes and Failure Mechanisms of Fiber to Waveguide Couplings Under Cyclic Tensile Loading*** Assane Dione, Jean-Francois Morissette, Julien Sylvestre, Patrick Jacques – University of Sherbrooke; Richard Langlois, Papa Momar Souare – IBM Canada, Ltd.	***6. 4:25 PM – Optimization of Cu Interconnects – SiCN Interfacial Adhesion by Surface Treatments*** Dong Jun Kim, Taek-Soo Kim – Korea Advanced Institute of Science and Technology; Sumin Kang – Korea Institute of Machinery and Materials; Sun Woo Lee, Inhwa Lee, Seungju Park, Jihyun Lee, Joong Jung Kim – Samsung Electronics Co., Ltd.
7. 4:45 PM – Flip Chip Process Enablement in IC Memory Stacked Die Package Chen-Yu Huang, Tsung-Han Chiang, Jungbae Lee, Kohan Lin, Chong-Leong Gan – Micron Memory Taiwan, Co., Ltd.; Travis Jensen – Micron Technology, Inc.	***7. 4:45 PM – A Predictive Metallographic Means to Identify the Relative Risk of Failure for Plated Micro Vias*** Roger Massey, Tobias Bernhard, Kilian Klaeden, Sebastian Zarwell, Edith Steinhaeuser, Sascha Dieter, Stefan Kempa, Frank Bruening – MKS Atotech	***7. 4:45 PM – Towards Selective Cobalt Atomic Layer Deposition for Chip-to-Wafer 3D Heterogeneous Integration*** Madison Manley, Muhannad Bakir – Georgia Institute of Technology; Zachary Deveraux, Nyi Myat Khine Linn, Charles Winter – Wayne State University; Victor Wang, Chenghsuan Kuo, Andrew Kummel – University of California, San Diego

PROGRAM SESSIONS: WEDNESDAY, MAY 31, 2:00 P.M. - 5:05 P.M.

Session 10: Packaging Interconnects	Session 11: Additive Manufacturing and Packaging for Flexible Electronics	Session 12: mm Wave Antenna-in-Package and Arrays
Committee: Thermal/Mechanical Simulation & Characterization	**Committee: Emerging Technologies**	**Committee: RF, High-Speed Components & Systems**
Mediterranean 1	**Mediterranean 6**	**Mediterranean 7 & 8**
Session Co-Chairs: Suresh K. Sitaraman – Georgia Institute of Technology Email: suresh.sitaraman@me.gatech.edu Jiamin Ni – IBM Corporation Email: nijiamin8910@gmail.com	**Session Co-Chairs: Tengfei Jiang – University of Central Florida Email: Tengfei.jiang@ucf.edu Dishit Parekh – Intel Corporation Email: dishit.parekh@intel.com**	**Session Co-Chairs: Jaemin Shin – Qualcomm Technologies, Inc. Email: jaemins@qti.qualcomm.com Yong-Kyu Yoon – University of Florida Email: ykyoon@ece.ufl.edu**
1. 2:00 PM – Finite Element Analysis of Shock & Vibration of a Printed Circuit Board Assembly Using the Beam Elements to Model the Solder Joints Tieyu Zheng – Microsoft Corporation; Babu Aminjikarai – ANSYS, Inc.; Ming-An Yang – Quanta Computer Co.	***1. 2:00 PM – Electromechanical and Thermal Characterization of Printed Liquid Metal Ink on Stretchable Substrate for Soft Robotics Multi-Sensing Applications*** El Mehdi Abbara, Mohammed Alhendi, Riadh Al-haidari, Nathaniel Gee, Mark Poliks – Binghamton University; Emily Boggs, Tan Yewteck, Deepak Trivedi – GE Research; Zachary Farrell, Christopher Tabor – AFRL	***1. 2:00 PM – A Scalable Heterogeneous AiP Module for a 256-Element 5G Phased Array*** Duixian Liu, Xiaoxiong Gu, Christian Baks, Arun Paidimarri, Atom Watanabe, Alberto Valdes-Garcia, Bodhisatwa Sadhu – IBM Corporation; Koichiro Masuko, Yujiro Tojo, Gokul Chandran, Yuta Hasegawa, Xu Lei, Ning Guan – Fujikura, Ltd.
2. 2:20 PM – Modeling and Optimization of Mechanical Performance for Cu Wire Bonding Process Liangbiao Chen, Yong Liu – ON Semiconductor	***2. 2:20 PM – Electrochemical Additive Manufacturing: A Novel Approach to Thermal Management of Electronics*** Madeline Frank, Michael Matthews, Joseph Madril, Ian Winfield – Fabric8Labs	***2. 2:20 PM – Metamaterial Based Compact Patch Antenna Array for Antenna-in-Package Solutions in Frequency Handover Applications*** Payman Pahlavan, Suk-il Choi, Alexander Wilcher, Hae-in Kim, Hanna Jang, Yong-Kyu Yoon – University of Florida
3. 2:40 PM – High-Temperature Creep Properties of a Novel Solder Material and Its Thermal Fatigue Properties Under Potting Material Leiming Du, Guoqi Zhang – Delft University of Technology; Xiujuan Zhao, Willem Van Driel – Signify; Rene Poelma – Nexperia	***3. 2:40 PM – Additively Manufactured Flexible Material Characterization and On-Demand "Smart" Packaging Topologies for 5G/mmWave Wearable Applications*** Kexin Hu, Yi Zhou, Suresh Sitaraman, Manos Tentzeris – Georgia Institute of Technology	***3. 2:40 PM – A Low-Cost Antenna-in-Package (AiP) for D-Band Application*** Hung-Chun Kuo, Po-I Wu, Sheng-Chi Hsieh, Ming-Fong Jhong, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Coquina Ballroom		
4. 3:45 PM – A Novel Stacked-Via Cu/ELK Interconnection Design Configuration to Enhance Advanced Si Packages Reliability Performance Kuo-Chin Chang, Mirng-Ji Lii, Chieh-Hao Hsu, Wei-Hsiang Tu, Tai-Shen Yang – Taiwan Semiconductor Manufacturing Company, Ltd.	***4. 3:45 PM – Advanced Packaging Methods Used for Energy Storage from Intermittent Renewable Sources*** Takafumi Fukushima, Jiayi Shen, Chang Liu – Tohoku University; Tianyu Xiang, Harshit Ranjan, Niharika Tripathi, Randall Irwin, Subramanian S. Iyer – University of California, Los Angeles	***4. 3:45 PM – A New Millimeter-Wave Package Design Based on Pseudo-Cavity Mode Electromagnetic Wave Excitation Using 400-µm Core FCBGA*** Ryuichi Oikawa, Hideki Sasaki, Keita Tsuchiya – Renesas Electronics Corporation
5. 4:05 PM – Sustainable-Ink Process Recipes for the Fabrication of Additively Printed Circuits and Component Attachment Pradeep Lall, Jinesh Narangaparambil, Ved Soni, Shriram Kulkarni, Kartik Goyal – Auburn University; Scott Miller – NextFlex	***5. 4:05 PM – Fabrication of Flexible and Stretchable Highly Conductive Ag-PDMS tri-Layer Interconnect and its Integration Into Li-ion Pouch Cells*** Mayukh Nandy, Siyang Liu, Yanze Wu, Hongbin Yu – Arizona State University	***5. 4:05 PM – 5G mmWave Patch Antenna Array on Extremely Low Loss Alumina Ribbon Ceramic Substrates for Antenna-in-Packaging (AiP)*** Cheolbok Kim, Hoon Kim, Eun Ju Moon, David R. Peters, Heather Vanselous-Barrett – Corning, Inc.; Seong-ho Seok – Corning Technology Center Korea
6. 4:25 PM – New Methodology Assessment of Copper Trace and Solder Joint Fatigue Failures in Board-Level Random Vibrations for Automotive Applications Valeriy Khaldarov, Alexander Shalumov – ASONIKA, LLC; Andy Zhang – Texas Instruments, Inc.; Dongji Xie, Minghong Jian – Nvidia Corporation; Jeffrey Lee – iST-Integrated Service Technology, Inc.; Xue Shi – Bosch Automotive Products Co., Ltd.; Romuald Roucou – NXP Semiconductor, Inc.; Sushil Doranga – Lamar University; Brian Kelly – Advanced Micro Devices, Inc.	***6. 4:25 PM – Adhesion and Reliability Studies of the Heterogeneous Integration of Conductive LSR and Other Components on SiP for Bio-Sensing Applications*** ChihLung (Steven) Lin, PangYuan Lee, Kueihao Tseng, Jenjun Chen, Harrison Chang – Advanced Semiconductor Engineering, Inc.	***6. 4:25 PM – A Novel Approach to Measure and Characterize Radiation Patterns of Antenna-in-Package*** Aditya Jogalekar, Oscar Medina, Andrew Blanchard, Rashaunda Henderson – University of Texas, Dallas; Mahadevan Iyer – Amkor Technology, Inc.; Rajen Murugan, Harshpreet Bakshi, Hassan Ali – Texas Instruments, Inc.
7. 4:45 PM – Physics-Driven Regression Algorithm on Solder Joint Fatigue Life Prediction for Mobile SiP Packages Faxing Che, Yeow Chon Ong, Hong Wan Ng, Ling Pan – Micron Semiconductor Asia Operations Pte. Ltd; Koustav Sinha, Christopher Glancey, Gokul Kumar – Micron Technology, Inc.	***7. 4:45 PM – Evaluation of Screen Printing Process in Fabrication of Small Profile Conductive Ink-Based Contact Force Sensor*** Maria Ramona Ninfa Bautista Damalerio, Rui Qi Lim, James Yap Ven Wee, Ming-Yuan Cheng – Institute of Microelectronics A*STAR; Ran Young Lim – Kalos Medical, Inc.	***7. 4:45 PM – Design and Fabrication of a Sub-THz Co-Reflectively Curved Patch-Reflector Antenna Array for Gain Enhancement and Near Field Focusing*** Ching-Jen Lee, Pin-Cheng Tseng, Wei-Chian Wang, Yun-Hao Liou, Yu-Ting Cheng, Chien-Nan Kuo – National Yang Ming Chiao Tung University

PROGRAM SESSIONS: THURSDAY, JUNE 1, 9:30 A.M. -12:35 P.M.

Session 13: Wafer/Panel-Level and Advanced Substrate Technologies	Session 14: Advances in Heterogeneous Integration Bonding Technology	Session 15: Innovative Interposer and Through-Via Technologies
Committee: **Packaging Technologies**	**Committee:** **Materials & Processing**	**Committee:** **Interconnections**
Palazzo D	**Palazzo A & B**	**Mediterranean 2 & 3**
Session Co-Chairs: **Markus Leitgeb – AT&S AG** **Email: m.leitgeb@ats.net** **Dean Malta – Micross Advanced Interconnect Technology** **Email: Dean.Malta@micross.com**	**Session Co-Chairs:** **Jae Kyu Cho – GlobalFoundries, Inc.** **Email: jaekyu.cho@globalfoundries.com** **Qianwen Chen – IBM Research** **Email: chenq@us.ibm.com**	**Session Co-Chairs:** **C. Key Chung – TongFu Microelectronics Co., Ltd** **Email: chungckey@hotmail.com** **Chuan Seng Tan – Nanyang Technological University** **Email: tancs@alum.mit.edu**
1. 9:30 AM – Supercarrier Redistribution Layers to Realize Ultra Large 2.5D Wafer Scale Packaging by CoWoS S.Y. Hou, Chien Hsun Lee, Tsung Ding Wang, Hao Cheng Hou – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM – Characterization of 300 mm Low Temperature SiCN PVD Films for Hybrid Bonding Application*** Xavier Brun, Md M. Hasan – Intel Corporation; Patrick Carazzetti, Carl Drechsel, Ewald Strolz – Evatec AG	***1. 9:30 AM – Assembly-Based Through-X Via (TXV) Integration Technology by Advanced Fan-Out Wafer-Level Packaging*** Atsushi Shinoda, Chang Liu, Tadaaki Hoshi, Jiayi Shen, Yuki Susumago, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima – Tohoku University
2. 9:50 AM – Development of Fine Pitch Backside Redistribution Layer (BRDL) Process in Fan-Out Panel Level Packaging (FOPLP) Hyunju Lee, Sung Keun Park, Jaemok Jung, Kwangok Jung, Ju-il Choi, Un-Byoung Kang, Dongwoo Kang – Samsung Electronics Co., Ltd.	***2. 9:50 AM – Inorganic Temporary Direct Bonding for Collective Die to Wafer Hybrid Bonding*** Fumihiro Inoue, Tomoya Iwata, Koki Onishi – Yokohama National University; Shunsuke Teranishi, Naoko Yamamoto, Akihito Kawai – DISCO Corporation; Shimpei Aoki, Takashi Hare – Toray Engineering Co., Ltd.; Akira Uedono – University of Tsukuba	***2. 9:50 AM – 3D Flexible Fan-Out Wafer-Level Packaging for Wearable Devices*** Guangqi Ouyang, Fukushima Takafumi, Subramanian S. Iyer – University of California, Los Angeles
3. 10:10 AM – Fabrication of Two-Types Panel-Level Interposers with Fine Cu Wirings and Outstanding Electrical Reliability Masashi Minami, Daisuke Yamanaka, Masaya Toba, Shan Ho Tsai, Sadaaki Katoh, Kazuyuki Mitsukura – Resonac Corporation	***3. 10:10 AM – Cu Damascene Process on Temporary Bonded Wafers for Thin Chip Stacking Using Cu-Cu Hybrid Bonding*** Nagendra Sekhar Vasarla, Dileep Kumar Mishra, Ser Choong Chong, Srinivasa Rao Vempati – Institute of Microelectronics A*STAR; Prayudi Lianto – Applied Materials Singapore	***3. 10:10 AM – Low-Stress TSVs for High-Density 3D Integration*** Jingping Qiao, Binbin Jiao, Shiqi Jia, Ruiwen Liu, Shichang Yun, Yanmei Kong, Yuxin Ye, Xiangbin Du, Lihang Yu, Dichen Lu, Ziyu Liu – Chinese Academy of Science-Institute of Microelectronics; Jie Wang – Institute of Microelectronics, Chinese Academy of Science, Beijing, China
Refreshment Break: 10:30 a.m.-11:15 a.m. – Coquina Ballroom		
4. 11:15 AM – Warpage Modulation Study on Panel-Level Compression Molding Technology for Heterogeneous Integration Applications Liang He, Jason Xie, Shishir Deshpande, Andrew Jimenez, Jung Kyu Han, Gang Duan, Rahul Manepalli – Intel Corporation	***4. 11:15 AM – A New Adhesive for CoW Cu-Cu Hybrid Bonding with High Throughput and Room Temperature Pre-Bonding*** Yasuhisa Kayaba, Yuzo Nakamura, Wataru Okada, Takuo Shikama, Kahori Tamura, Satoshi Inada – Mitsui Chemicals, Inc.	***4. 11:15 AM – Integrated Optical Interconnect Systems (iOIS) for Silicon Photonics Applications in HPC*** Harry Hsia, C.W. Tseng, Chih-Chieh Chang, Jiun Yi Wu, Shih-Peng Tai, S. W. Lu, Jason Wu, Chih-Hang Tung, C. S. Liu, Yutong Wu, K. C. Yee, Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.
5. 11:35 AM – Signal Integrity of 2-µm-Pitch RDL Interposer for High-Performance Signal Processing in Chiplet-Based System Takamasa Takano, Hiroshi Kudo, Masaya Tanaka, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.; Tomoya Sasagawa – DNP America, LLC	***5. 11:35 AM – Low-Temperature and Pressureless Cu-to-Cu Bonding by Electroless Pd Plating Using Microfluidic System*** Po-Shao Shih, Jeng-Hau Huang, Chang-Hsien Shen, Yu-Chun Lin, Simon Johannes Graefner, Vengudusamy Renganathan, C. Robert Kao – National Taiwan University; Chin-Li Kao, Yung-Sheng Lin, Yun-Ching Hung, Chun-Wei Chiang – Advanced Semiconductor Engineering, Inc.	***5. 11:35 AM – Demonstration of a CMOS-Compatible Superconducting Cryogenic Interposer for Advanced Quantum Processors*** King Jien Chui, Yong Chyn Ng, Ya-Ching Tseng, Hongyu Li – Institute of Microelectronics A*STAR
6. 11:55 AM – Thermal and Mechanical Characterization of Embedded PTCQ Packaging Test Chip Die Gerald Weis, Timo Schwarz, Johannes Stahr, Andreas Zluc – AT&S AG; Vladimir Cherman, Geert Van der Plas – imec	***6. 11:55 AM – Volume-Controllable Solder Bumping Technology to Package Substrate Using Injection Molded Solder for Fine-Pitch Flip Chip*** Toyohiro Aoki, Hiroyuki Mori, Koki Nakamura, Takashi Hisada – IBM Research, Tokyo; Katsuyuki Sakuma – IBM Research	***6. 11:55 AM – Process Design Kit and Initial Demonstration of Digital Metal-Embedded Chip Assembly for High Density IO Fan-Out Packaging*** Souheil Nadri, Bor-An Clayton Tu, Hasan Sharifi, Daniel Kuzmenko, Joel Wong, Vu Phan, Courtney Wilt – HRL Laboratories, LLC; Florian Herrault – PseudolithIC, Inc.; Abdullah Khan, David Schwan, David Botticello, Sanjana Das – Cadence
7. 12:15 PM – Reliability of Heterogeneous Integration on Hybrid Substrate With Ajinomoto Build-Up Film Channing Yang, John Lau, Gary Chen, Jones Huang, YH Chen, T. J. Tseng – Unimicron Technology Corp.; Ming Li – ASM Pacific Technology, Ltd.	***7. 12:15 PM – Micro-Structure Analysis of Solder Joint Using Room Temperature Laser-Assisted Bonding (LAB) Process*** Yoon Hwan Moon, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ki-Seok Jang, Jin-Hyuk Oh, In-Seok Kye, Yong-Sung Eom, Kwang-Seong Choi – Electronics Telecommunications Research Institute; Yong-Jun Oh – Hanbat National University	***7. 12:15 PM – 1.65 µm L/S High Density Interconnect on Organic Substrate by Advanced Semi-Additive Process for HPC Applications*** Hussein Hamieh, Juliano Borges, Etienne Paradis, Yann Beilliard, Serge Ecoffey, Dominique Drouin – University of Sherbrooke; Isabel De Sousa, Martin Laliberte – IBM Canada, Ltd.

PROGRAM SESSIONS: THURSDAY, JUNE 1, 9:30 A.M. -12:35 P.M.

Session 16: Sintering and Soldering for High-Power, High-Reliability, and RF Devices	Session 17: Advanced Reliability Modelling and Characterization	Session 18: Advanced Photonic Packaging and Interconnect
Committees: Assembly and Manufacturing Technology and Materials & Processing	**Committees: Thermal/Mechanical Simulation & Characterization and Applied Reliability**	**Committee: Photonics**
Mediterranean 1	**Mediterranean 6**	**Mediterranean 7 & 8**
Session Co-Chairs: **Mark Poliks – Binghamton University** **Email: mpoliks@binghamton.edu** **Omkar Gupte – Advanced Micro Devices, Inc.** **Email: Omkar.Gupte@amd.com**	**Session Co-Chairs:** **Wei Wang – Qualcomm Technologies, Inc.** **Email: wwang@g.clemson.edu** **Tz-Cheng Chiu – National Cheng-Kung University** **Email: tcchiu@mail.ncku.edu.tw**	**Session Co-Chairs:** **Richard Pitwon – Resolute Photonics, Ltd.** **Email: richard.pitwon@resolutephotonics.com** **Soon Jang – ficonTEC USA** **Email: soon.jang@ficontec.com**
1. 9:30 AM – Understanding the Influence of Copper Substrate Oxidation on Silver Pressure Sintering Performance Tamira Stegmann, Andre Schwoebel, Wolfgang Schmitt, Stefan Gunst – Heraeus Germany GmbH & Co. KG; Karsten Durst – Technical University Darmstadt; Nils Neugebauer, Peter Klar – Justus Liebig University of Giessen	***1. 9:30 AM – Fully Coupled Electromigration Modeling Using Peridynamics*** Yanan Zhang, Sundaram Vinod Anicode, Erdogan Madenci – University of Arizona; Xuejun Fan – Lamar University	***1. 9:30 AM – Backside Optical Coupler: A Novel I/O for Mechanically Stable High Efficiency Fiber Coupling*** Sugeet Sunder, Akhilesh Jaiswal, Ajey Jacob – University of Southern California
2. 9:30 AM – Forming of Advanced THT-Interconnects Using SB² Laser Solder Jetting Process Matthias Fettke, Anne Fisch, Georg Friedrich, Moshir Nasser, Thorsten Teutsch – Pac Tech GmbH	***2. 9:50 AM – Predicting Reliability Behavior in HBM Packages Through Numerical Simulation*** Sangkun O, Jongpa Hong, Sangmin Lee, Seoeun Kyung, Junho Lee, Kilsoo Kim, Jihyun Park, Dan Oh – Samsung Electronics Co., Ltd.	***2. 9:50 AM – QPSK Transmitter Photonics Integrated Circuit (PIC) with Integrated Micro-Transfer-Printed EAMs and Custom Driver Compatible with 3D Integration*** Roshanak Shafiiha, Aaron Zilkie – Rockley Photonics; Clint Schow, Xinhong Du, Viviana Arrunategui-Norvick, Yujie Xia – University of California, Santa Barbara
3. 10:10 AM – High Reliability Design of Ag Sinter Joining on a Softened Crack-Less Ni-P / Pt/Ag Metallization AMB Substrate during Aging and Harsh Thermal Cycling Chuantong Chen, Yang Liu, Hupeng Huo, Katsuaki Suganuma – Osaka University; Minoru Ueshima, Takeshi Sakamoto – Daicel Corporation; Yukinori Oda – C. Uyemura & Co., Ltd.	***3. 10:10 AM – Distortion Simulation for Direct Wafer-to-Wafer Bonding Process*** Nathan Ip, Nima Nejadsadeghi – Tokyo Electron America, Inc.; Norifumi Kohama, Hayato Tanoue, Kimio Motoda – Tokyo Electron Kyushu, Ltd.	***3. 10:10 AM – Low-Cost, HVM Singulation of Silicon Photonic ICs for Low-Loss Waveguide-to-Fiber Array Edge Coupling*** Hiren Thacker, Tong Wang, Steve Moyer, Mary Nadeau, Sandeep Razdan, Ginni Chadha – Cisco Systems, Inc.
Refreshment Break: 10:30 a.m.-11:15 a.m. – Coquina Ballroom		
4. 11:15 AM – Risk Assessment of Hybrid Low Temperature Solder on Surface Mount Technology and Board Level Reliability for BGA Packages Jihyun Lee, Yongsung Park, Junho Lee, Hansung Ryu, JeeHyun Jung, Kangjoon Lee, Kilsoo Kim – Samsung Electronics Co., Ltd.	***4. 11:15 AM – Substrate Copper Trace Crack Characterization and Simulation*** Wei Yu, Faxing Che, Yeow Chon Ong, Hong Wan Ng – Micron Semiconductor Asia Operations Pte. Ltd; Vance Liu, Milly Lin, Jay Lin – Micron Memory Taiwan Co., Ltd.; Brad Rumsey, Christopher Glancey – Micron Technology, Inc.	***4. 11:15 AM – Packaging of Ultra-Dynamic Photonic Switches and Transceivers for Integration into 5G Radio Access Network and Datacenter Sub-Systems*** Geert Van Steenberge, Gunther Roelkens, Peter Ossieur, Jeroen Missinne – imec/Ghent University; Joris Van Campenhout – imec; Milan M. Milosevic – PHIX Photonics Assembly; Paraskevas Bakopoulos – NVIDIA; Igor Krestnikov – Innolume; Stefano Stracca – Ericsson Research; Tanja Joerg – AT&S AG; Tanja Braun – Fraunhofer IZM; Qixiang Cheng – Cambridge University
5. 11:35 AM – A Bismuth-Free In-Containing Lower-Temperature Lead-Free Solder Paste for Wafer-Level Package Application that Outperforms SAC305 Hongwen Zhang, Tyler Richmond, Huaguang Wang – Indium Corporation	***5. 11:35 AM – Design-for-Manufacturing and Design-for-Reliability Strategies for Large 80mm+ 2.5D Devices*** Peng Su, Omar Ahmed, Leif Hutchinson, Bernard Glasauer, Gautam Ganguly – Juniper Networks	***5. 11:35 AM – Scalable Fiber-Array-to-Chip Interconnections with Sub-Micron Alignment Accuracy*** Shengtao Yu, Muhannad S. Bakir, Thomas Gaylord – Georgia Institute of Technology
6. 11:55 AM – Planar SiC Power Module Packaging and Interconnections Using Direct Ink Writing Riadh Al-Haidari, Mohammed Alhendi, Dylan Richmond, El Mehdi Abbara, Abdullah Obeidat, Mark Poliks, Mark Schadt – Binghamton University; Arun Gowda, Jeffrey Erlbaum, Han Xiong, Collin Hitchcock – GE Research	***6. 11:55 AM – A Continuum Damage Mechanics Approach for the Reliability of Lead-Free Solders Subjected to Cyclic Loading*** Golam Rakib Mazumder, Mohammad Ashraful Haq, Jeffrey Suhling, Pradeep Lall – Auburn University; Yaxiong Chen, Torsten Hauck, Abdullah Fahim – NXP Semiconductor, Inc.	***6. 11:55 AM – Realization, Multi-Field Coupled Simulation and Characterization of a Thermo-Mechanically Robust LiDAR Front End on a Copper Coated Glass Substrate*** Marcel Kettelgerdes, Amit Pandey, Gordon Elger – Technical University of Applied Science Ingolstadt; Peter Meszmer, Majid Tavakolibasti, Bernhard Wunderle – Chemnitz University of Technology; Michael J. Haeussler, Gunnar Bottger – Fraunhofer IZM; Huseyin Erdogan – Continental AG; Ralph Schacht – Brandenburg University of Technology
7. 12:15 PM – Influence of Microscale Tin Particles on Mechanical Properties of Silver Sintering Joints with Reduced Processing Parameters Steffen Hadeler, Yangyang Long, Rico Ottermann, Folke Dencker, Jens Twiefel, Marc Christopher Wurz – Leibniz University	***7. 12:15 PM – A Quantitative Evaluation of the Inelastic Energy Absorptions in Cu-Polyimide Interconnect and the Effect on Interface Debond Driving Force*** Chien-Yu Wang, Tz-Cheng Chiu – National Cheng-Kung University; Wei-Jie Yin, Dao-Long Chen, Tang-Yuan Chen, Chin-Li Kao – Advanced Semiconductor Engineering, Inc.	***7. 12:15 PM – Cavity-Resonator-Integrated Guided-Mode-Resonance Mirrors for Hybrid Integration of Wavelength-Multiplexed Light Source*** Akari Watanabe, Shunsuke Teranishi, Keisuke Ozawa, Aika Taniguchi, Junichi Inoue, Shogo Ura – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology

PROGRAM SESSIONS: THURSDAY, JUNE 1, 2:00 P.M. - 5:05 P.M.

Session 19: Advances in 3D Integration and Hybrid Bonding	Session 20: Automotive/Board-Level Reliability	Session 21: Fine-Pitch and Intermetallic Considerations in Advanced Solder Interconnections
Committee: **Packaging Technologies**	**Committee:** **Applied Reliability**	**Committee:** **Interconnections**
Palazzo D	**Palazzo A & B**	**Mediterranean 2 & 3**
Session Co-Chairs: **Peng Su – Juniper Networks** **Email: pensu@juniper.net** **Jaesik Lee – Meta Platforms, Inc.** **Email: jaesiklee@fb.com**	**Session Co-Chairs:** **Paul Tiner – Texas Instruments, Inc.** **Email: p-tiner@ti.com** **Varughese Mathew – NXP Semiconductor, Inc.** **Email: varughese.mathew@nxp.com**	**Session Co-Chairs:** **Nathan Lower – Consultant** **Email: nplower@hotmail.com** **Jian Cai – Tsinghua University** **Email: jamescai@tsinghua.edu.cn**
1. 2:00 PM – Thermal Improvement of HBM with Joint Thermal Resistance Reduction for Scaling 12 Stacks and Beyond Taehwan Kim, Youngdeuk Kim, Heejung Hwang, Hwanjoo Park, Jaechoon Kim, Dan (Kyung Suk) Oh – Samsung Electronics Co., Ltd.	***1. 2:00 PM – Impact of Temperature Cycling Conditions on Board Level Vibration for Automotive Applications*** Varun Thukral, Irene Bacquet, Michiel Soestbergen, Jeroen Zaal, Romuald Roucou, Rene Rongen – NXP Semiconductor, Inc.; Willem Driel, G.Q. Zhang – Delft University of Technology	***1. 2:00 PM – Copper Pillar Voids in a Flip Chip Package During High Temperature Application*** Miao Wang, Amar Mavinkurve, Romuald Roucou, Amirul Afripin, CS Foong, Trent Uehling, Nishant Lakhera – NXP Semiconductor, Inc.
2. 2:20 PM – Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing Norio Chujo – Hitachi Research & Development Group/Tokyo Institute of Technology; Hiroyuki Ryoson, Tomoji Nakamura, Koji Sakui, Shinji Sugatani, Takayuki Ohba – Tokyo Institute of Technology	***2. 2:20 PM – Thermal Aging Study of Encapsulated Power Devices Under Autonomous Driving Condition and its Effect on Board Level Reliability*** Yu-Hsiang Yang, Bongtae Han – University of Maryland; Przemek Gromala – Robert Bosch GmbH	***2. 2:20 PM – Solder Joint Reliability of Fully Homogenised SAC-SnBi Low Temperature BGA Interconnections Using Solid Liquid Inter-Diffusion (SLID)*** Hafiz Waqas Ali, David Danovitch, Dominique Drouin – University of Sherbrooke; Richard Langlois, Robert Martel – IBM Corporation
3. 2:40 PM – 2.5D MCM (Multi-Chip Module) Technology Development for Advanced Package Laurene Yip, James Tsai, Rosa Lin, Ian Hsu – MediaTek, Inc.	***3. 2:40 PM – Evolution of Fracture Resistance of the FCBGA Interfaces Under Monotonic and Fatigue Loads in Presence of Sustained Automotive High Temperatures*** Pradeep Lall, Aathi Pandurangan, Padmanava Choudhury, Jeffrey Suhling – Auburn University	***3. 2:40 PM – Intermetallic Growth Study of Ultra-Thin Copper and Tin Bilayer for Hybrid Bonding Applications*** Gaurav Khurana – TU Dresden; Iuliana Panchenko – TU Dresden/Fraunhofer IZM
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Coquina Ballroom		
4. 3:45 PM – Reliability Performance on Fine-Pitch SoIC™ Bond Shih-Wei Liang, Y. R. Liang, Gene C. Y. Wu, K. C. Yee, C. T. Wang, Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***4. 3:45 PM – System-Level Reliability Case Studies of High-Performance Automotive and Medical IC Packages*** Li Jiang, Guangxu Li, Kejun Zeng, Jaimal Williamson, Rajen Murugan – Texas Instruments, Inc.	***4. 3:45 PM – Heterogeneous Integration on Organic Interposer Substrate with Fine-Pitch RDL and 40 Micron Pitch Micro-Bumps*** Katsuyuki Sakuma, Griselda Bonilla – IBM Research; Russell Kastberg – IBM Systems; Toyohiro Aoki – IBM Japan, Ltd.
5. 4:05 PM – Development of 4 Die Stack Module Using Hybrid Bonding Approach Ser Choong Chong, Au Keng Yuen, Jason, Nagendra Sekhar Vasarla, Ismael Daniel Cereno, Srinivasa Rao Vempati – Institute of Microelectronics A*STAR	***5. 4:05 PM – Reliability Challenges and Mitigation Measures of Small Body-Sized Components on Complex and High-Layer Count PCBs*** Peng Su, Omar Ahmed, Arman Ahari, Leif Hutchinson, Bernard Glasauer – Juniper Networks	***5. 4:05 PM – A Study on the Advanced Chip to Wafer Stack for Better Thermal Dissipation of High Bandwidth Memory*** Sangyong Lee, Jinwoo Park, Jong-Kyu Moon, Minsuk Kim, Gyujei Lee, Kangwook Lee – SK hynix, Inc.
6. 4:25 PM – Impact of Dielectric and Copper Via Design on Wafer-to-Wafer Hybrid Bonding Vikas Dubey, Dirk Wuensch, Knut Gottfried, Tobias Fischer, Maik Wiemer, Harald Kuhn – Fraunhofer ENAS	***6. 4:25 PM – Investigation on Fatigue Life of Non-Symmetric Solder Joints in Chip Resistors*** Jonghwan Ha, Junbo Yang, Pengcheng Yin, Karthic Arun Deo, Chongyang Cai, Seungbae Park – Binghamton University	***6. 4:25 PM – Seed Layer Etching, Thermal Reflow and Bonding of Cu-Sn Micro Bumps with 5 µm Diameters*** Yunfan Shi, Zilin Wang, Zheyao Wang – Tsinghua University
7. 4:45 PM – Voids-Free Die-Level Cu/ILD Hybrid Bonding Katsuyuki Sakuma – IBM Research; Roy Yu, John Knickerbocker, Dale McHerron, Ming Li, Siu Cheung So, So Ying Kwok, Chun Ho Fan, Siu Wing Lau – ASM Pacific Technology, Ltd.	***7. 4:45 PM – Investigation of Acceleration Factors for SnAgCu-Bi Solder Joints Under Various Temperature Cycling Test Conditions*** Choongpyo Jeon, Youngsung Choi, Kwangwon Seo, Keunho Rhew, Jinsoo Bae, Yuchul Hwang – Samsung Electronics Co., Ltd.; Hyunsik Jeong – Hanyang University	***7. 4:45 PM – Development of Fluxless Micro-Bonding and Narrow Gap Filling Process*** Sadaaki Katoh, Dongchul Kan, Keiko Ueno, Kazuyuki Mitsukura – Resonac Corporation

PROGRAM SESSIONS: THURSDAY, JUNE 1, 2:00 P.M. - 5:05 P.M.

Session 22: Large Substrate Process Integration Challenges	Session 23: Next Generation Quantum, AI, and Secure System Design	Session 24: High-Speed Signal and Power Integrity
Committee: **Assembly and Manufacturing Technology**	**Committee:** **Emerging Technologies**	**Committee:** **RF, High-Speed Components & Systems**
Mediterranean 1	**Mediterranean 6**	**Mediterranean 7 & 8**
Session Co-Chairs: **Valerie Oberson – IBM Canada, Ltd.** **Email: voberson@ca.ibm.com** **Jobert Van Eisden – MKS Instruments, Inc.** **Email: Jobert.van-Eisden@atotech.com**	**Session Co-Chairs:** **Rohit Sharma – Indian Institute of Technology Ropar** **Email: rohit@iitrpr.ac.in** **Santosh Kudtarkar – Analog Devices, Inc.** **Email: santosh.kudtarkar@analog.com**	**Session Co-Chairs:** **Rockwell Hsu – Cisco Systems, Inc.** **Email: rohsu@cisco.com** **Chuei-Tang Wang – Taiwan Semiconductor Manufacturing Company, Ltd.** **Email: ctwang10492@hotmail.com**
1. 2:00 PM – Extremely Large 3.5D Heterogeneous Integration for the Next-Generation Packaging Technology Ilbok Lee, Soohyun Nam, Sungeun Kim, Sangho Shin, Younglyong Kim, Sunkyung Seo, Hae Jung Yu, Dae-Woo Kim – Samsung Electronics Co., Ltd.	***1. 2:00 PM – Thermal-Aware SoC Macro Placement and Multi-Chip Module Design Optimization with Bayesian Optimization*** Michael Molter, Elyse Rosenbaum – University of Illinois; Rahul Kumar, Osama Waqar Bhatti, Madhavan Swaminathan – Georgia Institute of Technology; Sonja Koller – Intel Corporation	***1. 2:00 PM – Comprehensive PDN/PSIJ Analysis of Silicon Capacitor Use for 8.533 GT/s LPDDR5X Application*** Scott Powers, Jonathan Casanova, Arun Kundu, Varin Sriboonlue, Srivatsan Thiruvengadam, Jaemin Shin – Qualcomm Technologies, Inc.; Xiao Ma – Meta Platforms, Inc.
2. 2:20 PM – Study of Fabrication and Reliability for the Extremely Large 2.5D Advanced Package Kosuke Murai, Hitoshi Onozeki, Dongchul Kang, Kazue Hirano, Mitsukura Kazuyuki – Resonac Corporation	***2. 2:20 PM – 3D Defect Detection and Metrology of HBMs Using Semi-Supervised Deep Learning*** Ramanpreet Pahwa, Richard Chang, Jie Wang, Ziyuan Zhao, Chuan Sheng Foo, Xun Xu, Lile Cai, Kangkang Lu – Institute for Infocomm Research A*STAR; Sharon Lim, Ser Choong Chong, Vempati Srinivasa Rao – Institute of Microelectronics A*STAR	***2. 2:20 PM – Design Considerations for Power Delivery Network and Metal-Insulator-Metal Capacitor Integration in Bridge-Chips for 2.5-D Heterogeneous Integration*** Ankit Kaul, Madison Manley, Muhannad S. Bakir – Georgia Institute of Technology
3. 2:40 PM – A Technical Review on State of the Art In-Plane and Out-of-Plane Deformation Measurement Techniques for Microelectronic Packages Karthik Arun Deo, Yangyang Lai, Junbo Yang, Jong Hwan Ha, Pengcheng Yin, Seungbae Park – Binghamton University	***3. 2:40 PM – A Si-Interposer with Buried Cu Metal Stripes and Bonded to Si-Substrate Backside for Security IC Chips*** Takuya Wadatsumi, Rikuu Hasegawa, Kazuki Monta, Takuji Miki, Makoto Nagata – Kobe University; Takaaki Okidono – SCU Co., Ltd.	***3. 2:40 PM – Statistical Analysis of Off-Chip Power-Integrity for Multicore Systems*** Sodam Han, Sungwook Moon, Jungil Son, Seungki Nam – Samsung Electronics Co., Ltd.-Foundry Business
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Coquina Ballroom		
4. 3:45 PM – Lead Frame vs. Mold Via Rathin Mandal – Institute of Microelectronics A*STAR	***4. 3:45 PM – Physical Authentication of Electronic Devices Using Synthetically Generated 3D Material Signatures*** Tejas Ravindra Kulkarni, Nikhilesh Chawla, Ganesh Subbarayan – Purdue University	***4. 3:45 PM – HBM3 Modules on Latest High Density Organic Laminate—Signal Integrity Design and Analysis with Interconnect Budget Results*** Frank Libsch – IBM Research; Hiroyuki Mori – IBM Research, Tokyo
5. 4:05 PM – A Novel Low-Temperature Connection and High-Temperature Curing Process for Reducing the Warpage of Bonding Pair in Fan-Out Wafer Level Packaging Yun Bai, Kang Li, Cheng Zhong, Qiang Liu, Jinhui Li, Guoping Zhang, Rong Sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology	***5. 4:05 PM – Modeling and Analysis of CMOS-Based Folded Memristive Crossbar Array for 3D Neuromorphic Integrated Circuits*** Sherin A. Thomas, Sahibia Kaur Vohra, Suyash Kushwaha, Rohit Sharma, Devarshi Mrinal Das – Indian Institute of Technology Ropar	***5. 4:05 PM – Signal and Power Integrity Design and Analysis for Bunch-of-Wires (BoW) Interface for Chiplet Integration on Advanced Packaging*** Ram Krishna, Elyse Rosenbaum – University of Illinois; Atom Watanabe, John Golz, Ravi Bonam, Frank Libsch, Arvind Kumar – IBM Corporation
6. 4:25 PM – Package Warpage of Whole Strip Evaluation with Interface Analysis in the Flip-Chip Die Bonding Process Ian Ho, Po-Yu Liao, Teny Shih, Andrew Kang, Yu-Po Wang – Siliconware Precision Industries Co., Ltd.	***6. 4:25 PM – Cryogenic Integration for Quantum Computer Using Diamond Color Center Spin Qubits*** Toshiki Iwai, Kenichi Kawaguchi, Tetsuya Miyatake, Tetsuro Ishiguro, Shoichi Miyahara, Shintaro Sato – Fujitsu, Ltd.; Salahuddin Nur, Ryoichi Ishihara – Delft University of Technology	***6. 4:25 PM – Metaconductor-Based High Signal Integrity Interconnects for 112 Gbps SerDes Interface with Channel Analysis*** Hae-In Kim, Alexander Wilcher, Saeyeong Jeon, Yong-Kyu Yoon – University of Florida; Brice Achkir, Rockwell Hsu – Cisco Systems, Inc.
7. 4:45 PM – Thermal Solutions for Large Die and Package Choong Kooi Chee, Sean Hsu, Janak Patel, Alaba Bamido – Marvell Semiconductor, Inc.	***7. 4:45 PM – Characterizations of Indium Interconnects for 3D Quantum Assemblies*** Celine Feautrier, Edouard Deschaseaux, Alain Gueugnot, Jean Charbonnier, Aurelia Plihon, Ludovic Dupre, Franck Henry, Frederic Berger, Antoine Pagot, Sebastien Renet, Olivier Mailliart, Candice Thomas – CEA-LETI	***7. 4:45 PM – Signal Integrity Co-Design of a High-Speed (20 Gbps) Analog Passive CMOS Switch*** Srikanth Manian, S. Shanmuganarayanan, Rajen Murugan, Sylvester Ankamah-Kusi – Texas Instruments, Inc.

PROGRAM SESSIONS: FRIDAY, JUNE 2, 9:30 A.M. -12:35 P.M.

Session 25: Next Generation High-Performance Computing Architectures	Session 26: Materials Reliability	Session 27: Next Generation Wafer-to-Wafer Copper Bonding
Committee: Packaging Technologies	**Committee: Applied Reliability**	**Committee: Interconnections**
Palazzo D	**Palazzo A & B**	**Mediterranean 2 & 3**
Session Co-Chairs: **Eric Tremble – Marvell** **Email: etremble@marvell.com** **Subhash L. Shinde – Notre Dame University** **Email: sshinde@nd.edu**	**Session Co-Chairs:** **Tae-Kyu Lee – Cisco Systems, Inc.** **Email: taeklee@cisco.com** **Darvin R. Edwards – Edwards Enterprise Consulting, LLC** **Email: darvin.edwards1@gmail.com**	**Session Co-Chairs:** **Li Li – Infinera Corporation** **Email: packaging@yahoo.com** **Dingyou Zhang – Broadcom, Inc.** **Email: dingyouzhang.brcm@gmail.com**
1. 9:30 AM – CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package Yu-Min Liang, Hsieh-Pin Hu, Yu-Chen Hu, Chia-Yen Tan, Chih-Ta Shen, S. Y. Hou – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 9:30 AM – Control of Solder Microstructure Stimulated by Interface Condition of the UBM/Solder and Enhancement of Electromigration Reliability*** Hariram Mohanram, Yi-Ram Kim, Geng Ni, Choongun Kim – University of Texas, Arlington; Sylvester Ankamah-Kusi, Qiao Chen, Patrick Thompson – Texas Instruments, Inc.	***1. 9:30 AM – 0.5 µm Pitch Next Generation Hybrid Bonding with High Alignment Accuracy for 3D Integration*** Christopher Netzband, Kevin Ryan, Ilseok Son, Hirokazu Aizawa – TEL Technology Center, America, LLC; Nathan Ip, Yuji Mimura, Xuemei Chen – Tokyo Electron America, Inc.
2. 9:50 AM – Reliability Performance of S-Connect Module (Bridge Technology) for Heterogeneous Integration Packaging HeeJun Jang, Kyun Ahn, Gamhan Yong, WonHo Choi, JiHyun Kim, Dave Hiner, TaeKyeong Hwang, Mike Kelly, WonChul Do, JinYoung Khim – Amkor Technology, Inc.	***2. 9:50 AM – Al2O3-Coated Bond Wire with Adhesion Promoter & Electrical Insulation*** Soojae Park, Soohyun Jo – OxWires Co., Ltd.; Sichun Seo, Chulhyung Cho – Samsung Electronics Co., Ltd.; Eulgi Min, Kyujung Choi – NCD Co., Ltd.	***2. 9:50 AM – Low Temperature and Fine Pitch Nanocrystalline Cu/SiCN Wafer-to-Wafer Hybrid Bonding*** Wei-Lan Chiu, Ou-Hsiang Lee, Tzu-Ying Kuo, Hsiang-Hung Chang – Industrial Technology Research Institute; James Yi-Jen Lo, Chiang-Lin Shih, Hsih-Yang Chiu – Nanya Technology Corporation
3. 10:10 AM – Advanced Packaging Design Platform for Chiplets and Heterogeneous Integration Lihong Cao – Advanced Semiconductor Engineering, Inc.; Chen-Chao Wang, Chih-Yi Huang – ASE Corporate R&D Center	***3. 10:10 AM – Evolution of Propensity for High Strain-Rate Damage Accrual in Doped and Undoped SnAgCu Lead-Free Solders in Temperature Range of -65 °C to +200 °C After 1-Year Sustained High Temperatures Exposure*** Pradeep Lall, Vishal Mehta, Vikas Yadav, Mrinmoy Saha, Jeffrey Suhling – Auburn University	***3. 10:10 AM – 0.5 µm Pitch Wafer-to-Wafer Hybrid Bonding with SiCN Bonding Interface for Advanced Memory*** Kai Ma, Nikos Bekiaris, Sesh Ramaswami – Applied Materials, Inc.; Taotao Ding, Juergen Burggraf, Gernot Probst, Thomas Uhrmann – EV Group, Inc.
Refreshment Break: 10:30 a.m.-11:15 a.m. – Mediterranean & Palazzo Foyers		
4. 11:15 AM – FO-EB-T Package Solution for High Performance Computing Po Yuan (James) Su, David Ho, Jacy Pu, Yu Po Wang – Siliconware Precision Industries Co., Ltd.	***4. 11:15 AM – Reliability Investigations of Polymer Based Redistribution Layers (RDL) Protected by a Mold Layer*** Ji-Youn Kwak – University of Ulsan; Emmanuel Chery, John Slabbekoorn, Julien Bertheau, Joke De Messemaeker, Eric Beyne – imec	***4. 11:15 AM – Fine-Pitch 30 µm Cu-Cu Bonding Using Electroless Nano-Ag*** Hsiang-Wei Tsai, Yung-Sheng Lin, Chun-Wei Chiang, Yun-Ching Hung, Chin-Li Kao, Ping-Hung Hsieh, I-Ting Lin, Chih-Yuan Hsu – Advanced Semiconductor Engineering, Inc.
5. 11:35 AM – Die to Wafer Hybrid Cu Bonding for Fine Pitch 3D-IC Applications Yeongseon Kim, Juhyeon Kim, Hyoeun Kim, Dohyun Kim, Seonkyung Seo, Chajea Jo, Dae-Woo Kim – Samsung Electronics Co., Ltd.	***5. 11:35 AM – Ionic Sensor Package Design for the Survivability in a Drop/Impact During Deployment*** Pengcheng Yin, Jong Hwan Ha, Junbo Yang, Yangyang Lai, Seungbae Park – Binghamton University; Biju Jacob, Arun Gowda – GE Research	***5. 11:35 AM – Influence of H2O in Bonding Interfaces on Bonding Strength of Plasma-Activated Bonded Silicon Oxide*** Hirotaka Yoshioka, Nobutoshi Fujii, Takushi Shigetoshi, Takahiro Kamei, Kengo Kotoo, Naoki Ogawa, Tatsuya Horikiri, Shunsuke Furuse, Sotetsu Saito, Suguru Saito, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation
6. 11:55 AM – C2W Hybrid Bonding Interconnect Technology for Higher Density and Better Thermal Dissipation of High Bandwidth Memory Kibum Kim – SK hynix, Inc.	***6. 11:55 AM – Effects of Twin Boundary and Precipitates on Board Level Reliability in Sn-Ag-Cu (SAC) Solder Joints Through EBSD Analysis*** DalJin Yoon, Byoungdo Lee, Jihye Kim, Sungho Hyun, Gyujei Lee, Kangwook Lee – SK hynix, Inc.	***6. 11:55 AM – All Nanograined Copper Is Not Created Equal*** Yun Zhang, Peipei Dong, Jing Wang, Xingxing Zhang – Shinhao Materials LLC; Klaus Leyendecker, Tsvetina Dobrovolska, Michael Herkommer, Volker Wohlfarth, Josh Liang – Umicore Galvanotechnik GmbH
7. 12:15 PM – Direct Bonded Heterogeneous Integration (DBHi): Surface Bridge Approach for Die Tiling Claudia Cristina Barrera Pulido, Divya Taneja, Philip McInnes, Isabel De Sousa – IBM Canada, Ltd.; Sayuri Kohara, Akihiro Horibe – IBM Japan, Ltd.; Aakrati Jain, Thomas Wassick – IBM Corporation	***7. 12:15 PM – Copper Wire Degradation Under the Effect of Different Humidity Levels*** Michael Joo Zhong Lim, Zhong Chen, Chuan Seng Tan – Nanyang Technological University; Hai Guan Loh – Infineon Technologies Asia Pacific Pte. Ltd.; Michael Goroll – Infineon Technologies AG	***7. 12:15 PM – A Study on Multi-Chip Stacking Process by Novel Dielectric Polymer Adhesive for Cu-Cu Hybrid Bonding*** Yuzo Nakamura, Kahori Tamura, Yasuhisa Kayaba, Wataru Okada, Takuo Shikama, Satoshi Inada – Mitsui Chemicals, Inc.

PROGRAM SESSIONS: FRIDAY, JUNE 2, 9:30 A.M. -12:35 P.M.

Session 28: Process Enhancements in 3D, FOWLP, and TSV Technologies	Session 29: AI-based Prediction for Heterogeneous Integration and Advanced Packaging	Session 30: Trends in Encapsulants and Low Dk/Df Dielectrics
Committee: Materials & Processing	**Committee: Thermal/Mechanical Simulation & Characterization**	**Committee: Materials & Processing**
Mediterranean 1	**Mediterranean 6**	**Mediterranean 7 & 8**
Session Co-Chairs: **Vidya Jayaram – Intel Corporation** **Email: vidya.jayaram@intel.com** **Dwayne Shirley – Marvell Semiconductor, Inc.** **Email: shirley@ieee.org**	**Session Co-Chairs:** **Patrick McCluskey – University of Maryland** **Email: mcclupa@umd.edu** **Rui Chen – Georgia Institute of Technology** **Email: chenrui@gatech.edu**	**Session Co-Chairs:** **Tanja Braun – Fraunhofer IZM** **Email: tanja.braun@izm.fraunhofer.de** **Kimberly Yess – Brewer Science, Inc.** **Email: kyess@brewerscience.com**
1. 9:30 AM – Magneto-Assisted Graphene Reinforcement: A New Method to Enhance Nanostructure and Properties of Electrodeposited Copper Nithin Nedumthakady, Pragna Bhaskar, Vanessa Smet – Georgia Institute of Technology	***1. 9:30 AM – Feasibility Investigation of Machine Learning for Electronic Reliability Analysis Using FEA*** Robert David Johannes Hoehne, Yichen Qi, Oliver Albrecht, Karsten Meier, Karlheinz Bock – TU Dresden	***1. 9:30 AM – Liquid Compression Mold Underfill Optimization with Low Warpage and Narrow Gap Flow*** Tsuyoshi Kamimura, Shinichi Sato, Yuto Shigeno – NAMICS Corporation; Brian Schmaltz – NAMICS Technologies, Inc.
2. 9:50 AM – Exploring Capabilities of Maskless Lithography for Dual–Image Exposure in FO WLP Ksenija Varga, Thomas Uhrmann, Roman Holly, Tobias Zenger – EV Group, Inc.; Chris Milasincic, Mel Zussman, Ron Legario, Michael Knaus – HD MicroSystems L.L.C.	***2. 9:50 AM – ARTSim: A Robust Thermal Simulator for Heterogeneous Integration Platforms*** Yousef Safari, Adam Corbier, Dima Al Saleh, Boris Vaisband – McGill University	***2. 9:50 AM – Effects of High-Temperature Exposure on the Thermo-Mechanical Behavior of Epoxy Molding Compound and Warpage of Molded Wafers*** Junmo Kim, Myoung Song, Chang-Yeon Gu, Min Sang Ju, Taek-Soo Kim – Korea Advanced Institute of Science and Technology; Sung Woo Ma, Jin Hee Lee, Woong-Sun Lee – SK hynix, Inc.
3. 10:10 AM – Alignment Through Thick Si Layer for High Resolution Patterning on Bonded Wafers with Tight Overlay Margin Using Immersion Lithography Arvind Sundaram, Chin Khang Tew, Guo Wei Tan, Hongyu Li, Nandini Venkataraman, Yuan-Hsing Fu, Chandra Rao Bhesetti, Navab Singh – Institute of Microelectronics A*STAR	***3. 10:10 AM – Reduced-Order Models of Digital Twin Applications for Design Platform of Flexible Hybrid Electronics*** Chang-Chun Lee – National Tsing Hua University; Jui-Chang Chuang, Chen-Tsai Yang, Chung-I Li – Industrial Technology Research Institute	***3. 10:10 AM – Low Temperature Fine Pitch All-Copper Interconnects Combining Photopatternable Underfill Films*** Xinrui Ji, Henk Van Zeijl, Weiping Jiao, Shan He, Leiming Du, Guoqi Zhang – Delft University of Technology
Refreshment Break: 10:30 a.m.-11:15 a.m. – Mediterranean & Palazzo Foyers		
4. 11:15 AM – Recent Progress in the Development of High-Density TSV for 3-Layers CMOS Image Sensors Stephan Borel, Myriam Assous, Stephane Moreau, Steve Pellerin – CEA-LETI	***4. 11:15 AM – Methodology of Artificial Intelligence Aided Hybrid Modeling for Predicting Solder Joint Reliability of BGA Package*** Ling Pan, Faxing Che, Yeow Chon Ong, Hong Wan Ng – Micron Semiconductor Asia Operations Pte. Ltd; Christopher Glancey, Gokul Kumar – Micron Technology, Inc.	***4. 11:15 AM – Novel Low Dk/Df Photoimageable Dielectric for Redistribution Layer*** Guillermo Fernandez Zapico, Fumihiko Kawauchi, Shinya Kawashita, Manabu Hirasawa, Kitaru Sato, Tetsuya Imai, Hidekazu Kondo, Tatsuya Makino – Resonac Corporation
5. 11:35 AM – The Advantages of Low Temperature (<400 °C) Carbon Nano-Tubes (CNTs) as Through Silicon Vias (TSVs) in Multi-Layers Stacking and Backside Power-Via Applications Nilabh Basu, H.-Y. Lin, T.-W. Chen, Y.-C. Chan, Y.-T. Tsai, H.-C. Guo, T.-H. Wu, P.-C. Lin, Y.-C. Lin, Ming-Han Liao – National Taiwan University	***5. 11:35 AM – Effect of Li-Ion Battery Form Factor on the SoH Degradation Under Randomized Charge-Discharge Cycles and C-Rates*** Pradeep Lall, Ved Soni – Auburn University	***5. 11:35 AM – Novel Photo-Definable Low Dk & Df Polyimide for Advanced Package of High Frequency Application*** Hitoshi Araki, Akira Shimada, Hisashi Ogasawara, Masaya Jukei, Masao Tomikawa – Toray Industries, Inc.
6. 11:55 AM – A Precise Wafer Thinning Integration Process for Nano-TSV Formation Ya-Ching Tseng, Nandini Venkataraman, King Jien Chui – Institute of Microelectronics A*STAR	***6. 11:55 AM – AI-Based Design Framework for Warpage Control of Fan-Out Panel-Level Package*** Peilun Yao, Yonglin Zhang, Jinglei Yang – Hong Kong University of Science and Technology; Haibin CHEN, Jingshen Wu – Hong Kong University of Science and Technology (Guangzhou); Haibo Fan, Anthony Cheung – Nexperia HK, Ltd.	***6. 11:55 AM – Novel Low Df Thermosetting Film and Photo Imageable Film*** Meiten Koh, Kazuyoshi Yoneda, Kazutaka Nakada, Yoshitomo Aoyama, Kasumi Hashimoto, Kota Oki – Taiyo Ink Mfg. Co., Ltd.
7. 12:15 PM – Next Generation Infrared (IR) Laser Debonding / Silicon Handle Technology for Precision Chiplet Technology Applications Qianwen Chen, Michael Belyansky, Yasir Sulehria, Akihiro Horibe, Eric Perfecto, Katsuyuki Sakuma, John Knickerbocker – IBM Corporation; Takeshi Tamura, Takayuki Ishii, Panupong Jaipan, Satoshi Nishimura Nishimura, Ilseok Son – Tokyo Electron, Ltd.	***7. 12:15 PM – Thermal Characterization of 3-D Stacked Heterogeneous Integration (HI) Package for High-Power Computing Applications*** Aakrati Jain, Sathya Raghavan, Prabudhya Roy Chowdhury, Mukta Ghate Farooq, Arvind Kumar, Katsuyuki Sakuma – IBM Research; Risa Miyazawa – IBM Research, Tokyo	***7. 12:15 PM – Properties of Low Dielectric Constant Buildup Materials Containing Micron Sized Hollow Silica*** Preeya Kuray – AGC Inc.; Tom McCarthy, Caleb Ancharski, Yoji Nakajima – AGC Multi Material America, Inc.

PROGRAM SESSIONS: FRIDAY, JUNE 2, 2:00 P.M. - 5:05 P.M.

Session 31: MEMS Sensor, Bio, and Advanced Interconnect Reliability	Session 32: Thermo-Mechanical Modelling and Characterization	Session 33: Advances in RDL, Via, and TSV Technologies for Chiplet Integration
Committees: Packaging Technologies and Applied Reliability	**Committee: Thermal/Mechanical Simulation & Characterization**	**Committee: Interconnections**
Palazzo D	**Palazzo A & B**	**Mediterranean 2 & 3**
Session Co-Chairs: **Young-Gon Kim – Renesas Electronics America** **Email: young.kim.jg@renesas.com** **Deepak Goyal – Intel Corporation** **Email: deepak.goyal@intel.com**	**Session Co-Chairs:** **Pradeep Lall – Auburn University** **Email: lall@auburn.edu** **Tieyu Zheng – Microsoft Corporation** **Email: tizheng@microsoft.com**	**Session Co-Chairs:** **Takafumi Fukushima – Tohoku University** **Email: fukushima@lbc.mech.tohoku.ac.jp** **Bernd Ebersberger – Infineon Technologies AG** **Email: bernd.ebersberger@infineon.com**
1. 2:00 PM – Enabling Backside Processing for Perforated Microfluidic Devices Jakob Visker, Yang Han, Evert Visker, Chi Dang Thi Thuy, Mateusz Gocyla, Jan Ackaert, Aurelie Humbert, Serge Vanhaelemeersch, Lan Peng – imec	***1. 2:00 PM – Embedded Microchannel Cooling System Based on Flexible Manifold for High-Performance Computing ICs*** Jie Wang, Yanmei Kong, Binbin Jiao, Ruiwen Liu, Yuxin Ye, Xiangbin Du, Lihang Yu, Yulin Shi, Shichang Yun, Dichen Lu, Ziyu Liu, Jingping Qiao – Chinese Academy of Science-Institute of Microelectronics	***1. 2:00 PM – 3D Silicon Interposer for Terabit/s Transceivers Based on High-Speed TSVs*** Bogdan Sirbu, Kai Zoschke, Tolga Tekin – Fraunhofer IZM; Ukyo Suzuki, Quentin Wilmart – CEA-LETI
2. 2:20 PM – Wafer Level Chip Scale Package Technology Applied to MEMS Pressure Sensor Luca Maggi, Marco Del Sarto, Tiziano Chiarillo, Enri Duqi, Lorenzo Baldo, Adriano Abbisogni – STMicroelectronics	***2. 2:20 PM – Simulation of Device Structure Impacts on Bonding Wave and Strain in Wafer-to-Wafer Cu-Cu Hybrid Bonding*** Takaaki Hirano, Taichi Yamada, Shoji Kobayashi, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation	***2. 2:20 PM – Creative Design and Structure Applied to Chiplets Packaging*** Chen-Chao Wang, Chih-Yi Huang, Chih-Pin Hung, Chung-Hung Lai, Hung-Hsien Huang, Hung-Chun Kuo, Ming-Fong Jhong, Fu-Chen Chu – Advanced Semiconductor Engineering, Inc.
3. 2:40 PM – A Novel FOWLP Method to Integrate Delicate MEMS Components Markus Woehrmann, Tanja Braun, Michael Schiffer, Martin Schneider-Ramelow – Fraunhofer IZM; Marc Dreissigacker – Technical University Berlin	***3. 2:40 PM – Investigation of Cure Kinetics of Advanced Epoxy Molding Compound Using Dynamic Heating Scan: An Overlooked Second Reaction*** Ran Tao, Aaron M. Forster – National Institute of Standards and Technology; Sukrut Prashant Phansalkar, Bongtae Han – University of Maryland	***3. 2:40 PM – TSV-Based Stacked Silicon Capacitor with Embedded Package Platform*** Kyojin Hwang, Heeseok Lee, Junso Pak – Samsung Electronics Co., Ltd.
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Mediterranean & Palazzo Foyers		
4. 3:45 PM – Development of High Reliability 6 µm-Pitch Cu-Cu Connections Using over-400 mm^2-Large Chip on Wafer Bonding Process Takahiro Kamei, Hirotaka Yoshioka, Tatsumasa Hiratsuka, Akihisa Sakamoto, Kan Shimizu, Hayato Iwamoto – Sony Semiconductor Solutions Corporation	***4. 3:45 PM – Effect of Passivation and Mechanical Constraint on Electromigration in Interconnect*** Xuejun Fan – Lamar University; Zhen Cui, Guoqi Zhang – Delft University of Technology	***4. 3:45 PM – Ultra Fine Pitch RDL (UFPRDL) Using Polymer Dual Damascene Processing*** Nelson Pinho, Emmanuel Chery, Nicolas Pantano, John Slabbekoorn, Andy Miller, Eric Beyne – imec
5. 4:05 PM – A Comprehensive Study of Solder Joint Reliability Dependent on Temperature Cycling Profiles and Material Selections with Emphasis on an Improved Solder Fatigue Lifetime Model Bongchan Son, Seung-Hyun Chae, SeungKwon Noh, KilJae Lee, Sangdeok Kim – SK hynix, Inc.	***5. 4:05 PM – Improving Warpage Characterization of Large Wafers in Fan-Out Packaging Technology*** Saskia Gesche Huber, Andreas Stegmaier, Marius van Dijk, Nina Nguyen, Ole Hoelck, Olaf Wittler, Martin Schneider-Ramelow – Fraunhofer IZM	***5. 4:05 PM – Development of a Plasma Etching Process of Copper for the Microfabrication of High-Density Interconnects in Advanced Packaging*** Juliano Borges, Maxime Darnon, Yann Beilliard, Serge Ecoffey, Dominique Drouin – University of Sherbrooke; Isabel De Sousa – IBM Canada, Ltd.
6. 4:25 PM – Electromigration Performance of Fine-Line Cu Redistribution Layer (RDL) for High-Density Fan-Out Packaging JiHye Kwon, JeongMin Ju, EunSook Sohn, JinYoung Khim – Amkor Technology Korea	***6. 4:25 PM – Enhancement of Thermal Transient Prediction Accuracy for Mobile AP Package*** Hwanjoo Park, Jonggyu Lee, Taehwan Kim, Sunggu Kang, Sungho Mun, Jaechoon Kim, Dan Oh – Samsung Electronics Co., Ltd.	***6. 4:25 PM – On the Path to AI Hardware via Chiplet Integration Enabled by High Density Organic Substrates*** Griselda Bonilla – IBM Research; Brian Quinlan, Tom Wassick, Russell Kastberg, Shidong Li, Monali Basutkar – IBM Systems
7. 4:45 PM – Simulation-Assisted Board Level Solder Joint Reliability Optimization for Large 80 mm+ 2.5D Devices Omar Ahmed, Leif Hutchinson, Peng Su, Bernard Glasauer – Juniper Networks; Vishnu Shukla, Tengfei Jiang – University of Central Florida	***7. 4:45 PM – Fan-Out Embedded Bridge with TSV(FO-EB-T) Package Characterization and Evaluation*** Vito Lin, Andrew Kang, Yu-Po Wang – Siliconware Precision Industries Co., Ltd.	***7. 4:45 PM – Fine Pitch Micro Via Interconnection with Reliable Electroless/Electric Cu Plating Layers Combined with High Power DUV Picosecond Laser for Organic Substrates*** Ming-chun Hsieh, Zheng Zhang, Masahiko Nishijima, Aiji Suetake, Chuantong Chen, Hiroyoshi Yoshida, Wanyun Li, Reiko Okumura, Katsuaki Suganuma – Osaka University; Hidekazu Homma, Koji Kita – Okuno Chemical Industries Co., Ltd.; George Okada – Spectronix Corp., Ltd.

PROGRAM SESSIONS: FRIDAY, JUNE 2, 2:00 P.M. - 5:05 P.M.

Session 34: Bonding Assembly - Novel Packaging, Process, and Characterization	Session 35: Packaging and Materials for Flexible Medical Technologies	Session 36: RF, Heterogeneous, and Chiplet Modules
Committee: **Assembly and Manufacturing Technology**	**Committee:** **Emerging Technologies**	**Committee:** **RF, High-Speed Components & Systems**
Mediterranean 1	**Mediterranean 6**	**Mediterranean 7 & 8**
Session Co-Chairs: **Jason Rouse – Taiyo America, Inc.** **Email: jhrouse@taiyo-america.com** **Zia Karim – Yield Engineering Systems** **Email: zkarim@yieldengineering.com**	**Session Co-Chairs:** **Vaidyanathan Chelakara – Acacia Communications** **Email: cvaidyanathan@acacia-inc.com** **Dongming He – Qualcomm Technologies, Inc.** **Email: dhe@qti.qualcomm.com**	**Session Co-Chairs:** **Amit Agrawal – Microchip Technology** **Email: amit.agrawal@microchip.com** **Craig Gaw – NXP Semiconductors, Inc.** **Email: c.a.gaw@ieee.org**
1. 2:00 PM – Laser-Assisted Bonding with Compression (LABC) Based Tiling Bonding Technology, Enabling Technology for Chiplet Integration Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ho-Gyeong Yun, Seok Hwan Moon, Ki-Seok Jang, Jin-Hyuk Moon, Yoon-Hwan Moon, Yong-Sung Eom – Electronics Telecommunications Research Institute	***1. 2:00 PM – Fully Portable Wireless Soft Stethoscope and Machine Learning for Continuous Real-Time Auscultation and Automated Disease Detection*** Sung Hoon Lee, Yun-Soung Kim, Woon-Hong Yeo – Georgia Institute of Technology	***1. 2:00 PM – Heterogeneous Radio Chiplet Module for 5G Millimeter Wave Application*** Agneta Ljungbro, Emil Nylander, Martin Hansson – Ericsson AB; Marcel Wieland, Jungtae (Osbon) Ok, Selaka Bulumulla – GlobalFoundries, Inc.
2. 2:20 PM – Contamination-Free Cu/SiCN Hybrid Bonding Process Development for Sub-µm Pitch Devices with Enhanced Bonding Characteristics Seung Ho Hahn, Wooyoung Kim, Donggap Shin, Yongin Lee, Sumin Kim, Wonyoung Choi, Kyeongbin Lim, Bumki Moon, Minwoo Rhee – Samsung Electronics Co., Ltd.-Mechatronics Research	***2. 2:20 PM – Patch-Type Flex SiP Platform for Healthcare Application*** Ming-Hung Chen, Wei-Hao Chang, Hui-Ping Jian, Chao-Wei Liu, Shang-Lin Wu, Yi-Chun Chou, Sung-Hung Chiang, Jung-Kai Chang, Tun-Ching Pi, Wei-Chun Lee, Jen-Chieh Kao, Yung-I Yeh – ASE Corporate R&D Center	***2. 2:20 PM – Design and Analysis of 3D Heterogeneous Chiplet Stack for RF Front-End Module Miniaturization*** Mihai Rotaru, Chai Tai Chong, Chui King Jien – Institute of Microelectronics A*STAR; Shashank Tiwari – GlobalFoundries, Inc.; Paul Castillou – Qorvo, Inc.
3. 2:40 PM – Integration and Process Challenges of Self Assembly Applied to Die-to-Wafer Hybrid Bonding Emilie Bourjot, Alice Bond, Noura Nadi, Thierry Enot, Loic Sanchez, Pierre Montmeat, Benoit Martin, Alain Campo, Frank Fournel – CEA-LETI; Feras Eid, Johanna Swan – Intel Corporation	***3. 2:40 PM – Development of PMUT Array Packaging from Characterisation Prototypes to Customer Samples*** Mark Andrew Shaw, Domenico Giusti, Fabio Quaglia, Alex Gritti – STMicroelectronics; Gerald Klug, Hitoshi Hoshino – DISCO HiTec Europe; Vempati Srinivasa Rao, Dutta Rahul, David Ho Soon Wee – Institute of Microelectronics A*STAR; Hideyuki Sandoh, Masatoshi Wakahara – DISCO Corporation; Alessandro Savoia – Roma Tre University	***3. 2:40 PM – Embedded mm-Wave Chiplet Based Module Using Fused-Silica Stitch-Chip Technology: RF Characterization and Thermal Evaluation*** Ting Zheng, Madison Manley, Muhannad S. Bakir – Georgia Institute of Technology
Refreshment Break: 3:00 p.m. - 3:45 p.m. – Mediterranean & Palazzo Foyers		
4. 3:45 PM – Critical Dimension Scatterometry as a Scalable Solution for Hybrid Bonding Pad Recess Metrology Haris K. Niazi, Botao Zhang, Xavier F. Brun, Xavier F. Brun – Intel Corporation; Krishnan Shankar – KLA Corporation	***4. 3:45 PM – Multi-Cell Array of Nanogap Electrodes for Labelfree Detection of Biomolecules*** Musafargani Sikkandhar, Yu Chen, Ming-Yuan Cheng – Institute of Microelectronics A*STAR 5. 4:05 PM – Electrospray Printing of Polymeric and Metallic Coatings for Electronics Packaging Emma Pawliczak, Bryce Kingsley, Paul Chiarot – Binghamton University	***4. 3:45 PM – Surface Micromachined Integrable High Efficiency Ridge Gap Waveguide Bandpass Filter for G-Band 6G Applications*** Alexander Wilcher, Hae-in Kim, Ziqi Jia, David Arnold, Yong-Kyu Yoon – University of Florida; Jia Chieh, Alex Phipps – Naval Information Warfare Center Pacific
5. 4:05 PM – A Study of SiCN Wafer-to-Wafer Bonding and Impact of Wafer Warpage Serena Iacovo, Oguzhan Orkut Okudur, Koen D'Have, Johan Meersschaut, Liesbeth Witters, Thierry Conard, Alain Phommahaxay, Steven Brems, Gerald Beyer, Eric Beyne – imec; Thomas Uhrmann, Thomas Plach – EV Group, Inc.	***5. 4:05 PM – Electrospray Printing of Polymeric and Metallic Coatings for Electronics Packaging*** Emma Pawliczak, Bryce Kingsley, Paul Chiarot – Binghamton University	***5. 4:05 PM – Amplified and Filtered x2 Multiplier Chip*** Elizabeth Kunkee, Dah-Weih Duan, Ricardo Medina, Nancy Lin, R. Yogi, Chunbo Zhang, Robert Mendoza, Kevin Leong, Alex Zamora, Scott Sing, David Miller – Northrop Grumman Corp.
6. 4:25 PM – Modeling of the Temperature Profile and Residual Stress During Thermal Compression Bonding in 3D Packages Prabudhya Roy Chowdhury, Sathya Raghavan, Luke Darling, Aakrati Jain, Promod R. Chowdhury, Mukta Ghate Farooq, Katsuyuki Sakuma – IBM Research	***6. 4:25 PM – 3D Printed Electronics with Multi Jet Fusion for Flexible Hybrid Electronics*** Jarrid A. Wittkopf, Sanil Jhaveri, Fan Fei, Manjarik Mrinal, Eric Luna-Ramirez, Lihua Zhao – HP Inc.; Dylan Richmond, Dayue Jiang, Fuda Ning, Mohamed Alhendi, Detlef Smilgies, Mark Poliks – Binghamton University	***6. 4:25 PM – Optimal Channel Design for Die-to-Die Interface in Multi-Die Integration Applications*** Jiyoung Park, Seungki Nam, Sungwook Moon, Jinho Kim – Samsung Electronics Co., Ltd.
7. 4:45 PM – Impact of Thermal Annealing and Other Process Parameters on Hybrid Bonding Performance for 3D Advanced Assembly Technology Taiwo Ajayi, Alvin Gatimu, Chris Woods, Xavier F. Brun – Intel Corporation; Abhishek Bhat, Kay Song, Zia Karim, Charudatta Galande, Phillip Le – Yield Engineering Systems	***7. 4:45 PM – Performance Evaluation of RF Novel Microstrip Lines Printed on Flexible Substrates*** Abdullah Obeidat, Mohammed Alhendi, Mohamed Abdelatty, Ashraf Umar, Emuobosan Enakerakpo, Riadh Al-Haidari, Mark Poliks – Binghamton University	***7. 4:25 PM – Highly Energy Efficient and Electromagnetic Interference Immune Coaxial Through-Substrate-Vias (cx-TSVs) for Millimeter Wave Applications*** Saeyeong Jeon, Hae-In Kim, Yong-Kyu Yoon – University of Florida

Wednesday May 31

Session 37: Interactive Presentations 1
Time: 10:00 a.m. – 12:00 p.m.

Committee: Interactive Presentations

Palazzo Foyer

Session Co-Chairs:
Mark Poliks – Binghamton University
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Kristina Young – GlobalFoundries, Inc.
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Jae Kyu Cho – GlobalFoundries, Inc.
Email: jaekyu.cho@globalfoundries.com

1. Investigation of Cu-to-Cu and Oxide-to-Oxide Bonding
Sangmin Lee, Gwangsik Oh, Junyoung Choi, Yoonho Kim, Sangwoo Park, Sarah Kim – Seoul National University of Science and Technology

2. Doping-Selective Etching of Silicon for Wafer Thinning in the Fabrication of Backside-Illuminated Stacked CMOS Image Sensors
Nandini Venkataraman, Navab Singh, Darshini Senthilkumar – Institute of Microelectronics A*STAR; Benedikt Risse – Nexgen Wafer Systems GmbH; Gregorio Decierdo – Nexgen Wafer Systems Pte. Ltd.; Deepthi Kandasamy, Eng Huat Toh, Louis Lim – GlobalFoundries Singapore

3. Study of Solder Resist Crack Resistance for Flip Chip Ball Grid Array Substrate
Eric Chen, Rick Ye, Wen-Yu Teng, Yu-Cheng Pei, Yu Po Wang – Siliconware Precision Industries Co., Ltd.

4. Reliability Analysis on Ag and Cu Nanoparticles Sintered Discrete Power Devices with Various Frontside and Backside Interconnects
Dong Hu, Xu Liu, Sten Vollebregt, Jiajie Fan, Guoqi Zhang – Delft University of Technology; Ali Roshanghias – Silicon Austria Labs GmbH; Xing Liu, Thomas Basler – Chemnitz University of Technology; Emiel De Bruin – Boschman Advanced Packaging Technology B.V.

5. Impact of Process Parameters on Vacuum Fluxless Solder Reflow Performance in Backend Applications with Bump Pitch of 15 µm and Below
Lei Jing, Vladimir Kudriavtsev, Taylor Nguyen, Jed Hsu, Tapani Laaksonen, Alvin Lin, Xinxuan Tan, Kay Song, Alex Chow, Chris Lane, Zia Karim – Yield Engineering Systems

6. Surface Modification on Hydrophilicity Enhancement Using NH_4OH, NaOH and KOH on Fine-Pitch Low Temperature Cu/SiO_2 Hybrid Bonding
Jia-Juen Ong, Dinh-Phuc Tran, Yu-An Chen, Chih Chen – National Chiao Tung University; Wei-Lan Chiu, Ou-Hsiang Lee, Hsiang-Hung Chang – Industrial Technology Research Institute

7. Development and Demonstration of a Novel Immersion Two Phase Cooling High Power SiC Power Module
Gongyue Tang, Leong Ching Wai, Huicheng Feng, Haoran Chen – Institute of Microelectronics A*STAR

8. Electrochemical Deposition of Indium Bumps on Superconducting Interconnect and Thermo-Compression Bonding for Cryogenic and Quantum Computing
Kumin Kang – Hanyang University; Jaber Derakhshandeh – imec

9. 6-Sided Die Protection for Chiplet Package with Multi-Layer RDL
ByungCheol Kim, Mary Maye Melgo, Rizi Gacho, Jacinta Aman Lim, Hee Yeoul Yoo, Kwan Sun Oh – nepes Corporation; Cliff Sandstrom, Benedict San Jose – Deca Technologies, Inc.

10. Wafer Level Capping Technology for Vacuum Packaging of Microbolometers
Kai Zoschke, Charles-Alix Manier, Hermann Oppermann – Fraunhofer IZM; Dirk Meier, Nishant Malik – Integrated Detector Electronic AS; Elahe Zakizade, Marvin Daniel Michel – Fraunhofer IMS; Avisek Roy, Hoang-Vu Nguyen, Hexin Xia – University of South-Eastern Norway

11. Artificial Intelligence (AI) Based Methodology to Minimize Asymmetric Bare Substrate Warpage
Sathya Raghavan, Griselda Bonilla, Katsuyuki Sakuma – IBM Research; Hiroyuki Mori – IBM Research, Tokyo

12. Scaling of Redistribution Layer for Heterogeneous Packaging in a Panel Level
Yoonyoung Jeon, Youngmin Kim, Hyundong Lee, Minji Kim, Woongkeon Lee, Joonseok Oh – Samsung Electronics Co., Ltd.

13. Process Challenges During CVD Oxide Deposition on the Backside of 20 µm Thin 300-mm Wafers Temporarily Bonded to Glass Carriers
Koen Kennes, Abdellah Salahouelhadj, Samuel Suhard, Jaber Derakhshandeh, Alain Phommahaxay, Steven Brems, Gerald Beyer, Eric Beyne – imec; Alice Guerrero, Xiao Liu – Brewer Science, Inc.

14. Electrical Characterization and Modeling of 2-µm and 1.5-µm Line-and-Space High-Density Signal Wiring in Organic Interposer
Atom Watanabe, Hiroyuki Mori, Xiaoxiong Gu, Frank Libsch, Griselda Bonilla – IBM Corporation

15. Package Integrated Vapor Chamber Heat Spreaders
Cameron Nelson – Amkor Technology, Inc.; SangHyuk Kim – Amkor Technology Korea

16. Analysis of Package-to-System Interaction on Thermal Performance of Large 2.5D Packages Using 3DFabric® Platform
Po-Yao Lin, Kathy Yan, Jun He – Taiwan Semiconductor Manufacturing Company, Ltd.

17. Evaluation of Parylene-HT as Dielectric for Application in Advanced Package Substrates
Pratik Nimbalkar, Mohanalingam Kathaperumal, Madhavan Swaminathan, Rao Tummala – Georgia Institute of Technology

18. Bottom Side Cooling for Glass Interposer with Chip Embedding Using Double-Sided Release Process for 6G Wireless Applications
Joon Woo Kim, Xingchen Li, Xiaofan Jia, Kyoung-Sik Moon, Madhavan Swaminathan – Georgia Institute of Technology

19. Demonstration of a Power-Efficient and Cost-Effective Power Delivery Architecture for Heterogeneously Integrated Wafer-Scale Systems
Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

20. Metal Additively Microfabricated SiPs with Embedded Microfluidic Cooling Towards Heterogeneous Integration with SoCs
Bhushan Lohani, Sheikh Dobir Hossain, Robert C. Roberts – University of Texas, El Paso

21. Large Wafer GaN on Silicon Reconstitution with Gold-to-Gold Thermocompression Bonding
Ankit Kuchhangi, Krutikesh Sahoo, Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

Wednesday May 31

Session 38: Interactive Presentations 2
Time: 2:30 p.m. – 4:30 p.m.

Committee: Interactive Presentations

Palazzo Foyer

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Saikat Mondal – Intel Corporation
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Donna M. Noctor – Nokia Corporation
Email: donna.noctor@nokia.com

1. Advanced Overlay Metrology for CIS Bonding Applications
Florent Dettoni, Emilie Deloffre – STMicroelectronics; Yoav Grauer, Shlomo Eisenbach, Motti Penia, Arkadi Simkin, Dror Elka, Avner Safrani, Marco Polli, Francesco De Paola – KLA Corporation

2. Implementation of New Robustness Assessment Methodology for Crack Stop Constructions
Maria Heidenblut, Michael Goroll – Infineon Technologies AG

3. Hybrid Bonding Utilizing Molding Compound and Dielectric Systems
Yuki Imazu, Kazuyuki Mitsukura – Resonac Corporation

4. A Short Time and N2-Sinterable Cu Sinter Paste with Highly Dispersed Submicron Cu Particles
Takaaki Eyama, Shuichi Inaya, Ukyo Suzuki, Masafumi Takesue – Kao Corporation

5. A Novel and Simple Method of Low Temperature, Low Process Time, Pressureless Interconnection for 3D Packaging
Jeng-Hau Huang, Po-Shao Shih, Chang-Hsien Shen, Vengudusamy Renganathan, Simon Johannes Graefner, Yu-Chun Lin, C. Robert Kao – National Taiwan University; Chin-Li Kao, Yung-Sheng Lin, Yun-Ching Hung, Chun-Wei Chiang – Advanced Semiconductor Engineering, Inc.

6. 50 nm Overlay Accuracy for Wafer-to-Wafer Bonding by High-Precision Alignment Technologies
Hajime Mitsuishi, Hiroshi Mori, Hidehiro Maeda, Mikio Ushijima, Atsushi Kamashita, Masashi Okada, Masanori Aramata, Takashi Shiomi, Shinya Sakamoto, Kishou Takahata, Tomohiro Chiba, Minoru Fukuda, Masahiro Kanbayashi, Toshimasa Shimoda, Isao Sugaya – Nikon Corporation

7. Multi-Stack Hybrid Cu Bonding Technology Development Using Ultra-Thin Chips
Min-Ki Kim, Hyuekjae Lee, Aeni Jang, Seungduk Baek, Ilhwan Kim, Youngkun Jee, Hyun-Chul Jung, Un-Byoung Kang, Dae-Woo Kim – Samsung Electronics Co., Ltd.-Test and System Package

8. An Investigation on Particle Embedding Capability of Wafer Level Spin-on Polymer Underfill Enabling Low Temperature Bonding of Hybrid Bonding System
Hiroto Noda, Akito Hiro, Naoki Nishiguchi – JSR Corporation; Jaber Derakhshandeh, John Slabbekoorn, Eric Beyne – imec

Wednesday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Coquina Ballroom

9. Effect of Chip Metallization and Process Parameters on the Die Attach Properties of Direct Bonded Power Devices
Michael Curkin, Marius Koehler, Nicolas Heuck – Hamm-Lippstadt University of Applied Sciences; Silke Kraft, Jens Mueller, Kurt-Georg Besendoerfer – SEMIKRON Elektronik GmbH & Co. KG

10. The Full-IMCs Interconnects Through Transient Liquid Phase Bonding of Ga/Cu System for Advanced Electronic Packaging
Yi Chen, Zhaoxia Zhou, Changqing Liu – Loughborough University

11. Selective Self-Assembled Monolayer for Copper Surface Protection During Plasma Activation of Hybrid-Bonded Wafers
Jack Rogers – TEL Technology Center, America, LLC

12. Development of a Heterogeneous Integration of GaN Power Device on Si-LSI
Shinei Miyasaka, Yusuke Norihide, Ayano Furue, Satoko Shinkai, Satoshi Matsumoto – Kyushu Institute of Technology

13. Integrated pH and Strain Sensors Development for Nasogastric Tube Placement Application
Ruiqi Lim, Yu Chen, James Ven Wee Yap, Musafargani Sikkandhar, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

14. Portable Multiple-Channel Ion-Selective Sensor
Yu Chen, Musafargani Sikkandhar, James Ven Wee Yap, Ming-Yuan Cheng – Institute of Microelectronics A*STAR

15. Chip-to-Chip Hybrid Bonding with Larger-Oriented Cu Grains for µ-Joints Beyond 100 K
Murugesan Mariappan, Takamichi Miyazaki, Takafumi Fukushima – Tohoku University; Masahiro Sawa, Eriko Sone – JCU Corporation; Mitsumasa Koyanagi – T-Micro

16. Application of Nickel Micro-Plating Bonding (NMPB) Technology to Crystalline Silicon Solar Cell Interconnection
Xinguang Yu, Zhi Fu, Isamu Morisako, Keiko Koshiba, Tomonori Iizuka, Kohei Tatsumi – Waseda University

17. CMOS-Compatible Fine Pitch Al-Al Bonding
Hemanth Kumar Cheemalamarri, Binni Varghese, Sharma Jaibir, Hongyu Li, B. S. S. Chandra Rao, Navab Singh, Srinivasa Rao Vempati, King-Jien Chui – Institute of Microelectronics A*STAR

18. Enhancement of Ga - 21.5 In – 10 Sn Eutectic Alloy Based Thermal Interface Material Incorporating Cu Flake
Jang Baeg Kim, Dong Gil Kang, Tae Joon Noh, Sea Hwan Kim, Seung-Boo Jung – Sungkyunkwan University

19. Board Level FEA Reliability and Stress Modeling for Chip-to-Wafer Bonded Chiplet Package
Rathin Mandal, Chai Tai Chong – Institute of Microelectronics A*STAR

20. High Density VR Solutions Using Immersion Cooling
Jesus G. Ruelas Flores, Arturo Sanchez Hernandez, Ernesto A Padilla Ramirez, Oscar A Del Rio Gonzalez, Carlos E Mora Flores, Andres Ramirez Macias – Intel Corporation

21. Demonstration of Eight Metal Layer Redistribution on Glass Substrate with Fine Features and Microvia
Christopher Blancher, Mohanalingam Kathaperumal, Fuhan Liu, Madhavan Swaminathan – Georgia Institute of Technology

22. Novel IR Laser Cleaving for Ultra-Thin Layer Transfer and 3D Stacked Devices
Thomas Uhrmann, Peter Urban, Boris Povazay, Michael Josef Gruber, Julian Bravin, Daniel Burgstaller, Markus Wimplinger, Bernd Thallner – EV Group, Inc.

23. Robust Edge Coupling Probe Applied in Wafer-Level Optical Testing
Sheng-Ho Huang, Chen-Yu Lin, Yi-Keng Fu – Industrial Technology Research Institute; Sin-Yuan Mu, Mei-Ju Lu, Chia-Sheng Cheng, Jihan Chen – ASE Corporate R&D Center

24. An Intensive Study of Effects of Orientations of Cu Bumps on Cu–Cu Direct Bonding for 3D Integration by Molecular Dynamics Simulation
Deng-Wu Zheng, Min-Bo Zhou, Shuai Liu, Chang-Bo Ke, Xin-Ping Zhang – South China University of Technology

25. Reconstituted-SiO_2 Tier with Integrated Copper Heat Spreader
Ashita Victor, Madison Manley, Shane Oh, Muhannad S. Bakir – Georgia Institute of Technology

26. Reflow Oven Zone Temperature Advisor Using the AI-Driven Smart Recipe Generator
Yangyang Lai, Junbo Yang, Jong Hwan Ha, Pengcheng Yin, Karthik A. Deo, Seungbae Park – Binghamton University

27. A Novel Polymer-Based Ultra-High Density Bonding Interconnection
Yu-Min Lin, Tsung-Yu Ou Yang, Ou-Hsiang Lee, Ching-Kuan Lee, Wei-Lan Chiu, Tao-Chih Chang, Hsiang-Hung Chang – Industrial Technology Research Institute; Michael Gallagher, Po-Yao Chuang, Po-Hao Tsai, Po-Chun Huang – DuPont Electronics and Industrial; Chang-Chun Lee – National Tsing Hua University

28. Comparison of Sintering Methodologies for 3D Printed High-Density Interconnects (2.3 µm L/S) on Organic Substrates for High-Performance Computing Applications
Shrivani Pandiya, Serge Ecoffey, Yann Beilliard, Dominique Drouin – University of Sherbrooke; Christophe Sansregret – Centre de Collaboration MiQroInnovation (C2MI); Isabel De Sousa – IBM Canada, Ltd.

29. Formation and 3D Stacking Process of CMOS Chips with Backside Buried Metal Power Distribution Networks
Naoya Watanabe, Yuuki Araga, Haruo Shimamoto, Katsuya Kikuchi – National Institute of Advanced Industrial Science and Technology; Makoto Nagata – Kobe University

30. Reliability and Failure Analysis of Chip-to-Substrate Cu-Pillar Interconnections with Nanoporous-Cu Caps
Ramon A. Sosa, Vanessa Smet, Antonia Antoniou – Georgia Institute of Technology

Thursday June 1

Session 39: Interactive Presentations 3
Time: 10:00 a.m. – 12:00 p.m.

Committee: Interactive Presentations

Palazzo Foyer

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Frank Libsch – IBM Corporation
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Yoichi Taira – Keio University
Email: taira@appi.keio.ac.jp

1. Voltage Controlled Nanoscale Magnetic Devices for Non-Volatile Memory and Scalable Quantum Computing
Jayasimha Atulasimha, Md Mahadi Rajib – Virginia Commonwealth University

2. Polymer Optical Waveguide Type 3-D MUX Device for Mode Division Multiplexing Links
Ryoto Ichinose, Takumi Kowatari, Takaaki Ishigure – Keio University

3. Extracting Anisotropic Permittivity of PCB Substrate from VNA Measurement on a Rectangular Stripline Resonator Loaded with a Via Array
Zhaoqing Chen, Hung Nguyen, Matteo Cocchini – IBM Corporation

4. Silicon Photonic Co-Packaging: Adhesive Dispense Challenge and Control
Paul Gond-Charton, Sebastien Gouin, Steve Pellerin, Richard Langlois, Patrick Jacques, Denis Blanchard, Eric Turcotte, Steve Whitehead, Elaine Cyr – IBM Corporation

5. Design of Single Miniaturized Dielectric Resonant Antenna for Millimeter Wave 5G Application
Chia-Chu Lai, Sam Lin, Teny Shih, Yu-Po Wang, Tom Tang, Mike Tsai, Ryan Chiu, Kevin Chang, Yu-Chang Dong – Siliconware Precision Industries Co., Ltd.

6. Inverse Prediction of Capacitor Multiphysics Dynamic Parameters Using Deep Generative Model
Kart Leong Lim, Rahul Dutta, Mihai Rotaru – Institute of Microelectronics A*STAR

7. New Interconnection Technologies Based on Ni Nano-Particle and Ni Micro-Plating Bonding with Stress Relaxation Effect for high-Temperature Resistant Power Device Packaging
Kohei Tatsumi, Keiko Koshiba, Yasunori Tanaka, Mayu Miyagawa, Xinguan Yu, Shun Furuya, Tomonori Iizuka – Waseda University

8. High-Performance Amplifier Package Design for Heterogeneous Integration on Si-Interposer
Teck Guan Lim, Lin Zhou, Haoran Chen, Eva Leong Ching Wai, Sasi Kumar Tippabhotla, Lin Ji, Gongyue Tang – Institute of Microelectronics A*STAR; Wei Jia Lu, Chee Heng Goh, Jun Wei Agnes Loh – DSO National Laboratories

9. Through-Silicon-Via Architecture of 3D Integration for Superconducting Quantum Computing Application
Jiexun Yu, Qian Wang, Yao Zheng, Changming Song, Junpeng Fang, Zheyao Wang, Jian Cai – Tsinghua University; Tiefu Li – Tsinghua University/Beijing Academy of Quantum Information Sciences; Haihua Wu – Beijing Academy of Quantum Information Sciences

10. Additive Manufacturing of Millimeter Wave Passive Circuits on Thin Alumina Substrates
Ethan Kepros, Yihang Chu, Bhargav Avireni, Brian Wright, Premjeet Chahal – Michigan State University

11. Frequency Selective Surface (FSS) Based Antenna Array Design for Satellites Capable of All Four Polarizations
Lih-Tyng Hwang, Ming-Yuan Huang, Hung-Chih Lin – National Sun Yat-Sen University

12. Novel Low-Loss Resin Coated Copper and Core Material for Advanced IC Packages
Tomo Mugurma, Andy Behr, Tom Shin – Panasonic Industrial Devices Sales Company of America; Umehara Hiroaki, Saeki Yuya, Kishino Koji – Panasonic Industry Co., Ltd.

13. Deep Learning Based Refinement for Package Substrate Routing
Peng-Tai Huang, Tsubasa Koyama, Tsung-Yi Ho – National Tsing Hua University; Keng-Tuan Chang, Chih-Yi Huang, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

14. Laser Integration on a Photonic Integrated Circuit with High Alignment Accuracy for Data Transmission
Ting Ta Chi, Zhenyu Li, Nanxi Li, Hong Cai, Y. M. Tobing Landobasa, Haitao Yu, Senthilkumar Darshini, Jae Ok Yoo, Hwang Gilho, Jeroen Van Borkulo, Lennon Y. T. Lee, Wen Lee – Institute of Microelectronics A*STAR

Wednesday & Thursday Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. – Coquina Ballroom

15. High Density Photonic Reservoir Computing Using Optical Fiber and Polymer Waveguide
Hidetoshi Numata, Toshiyuki Yamane, Daiju Nakano – IBM Research, Tokyo/IBM Corp., Japan; Jean Heroux – IBM Systems/IBM Corp., Canada

16. Machine Learning Based PCB/Package Stack-Up Optimization for Signal Integrity
Wenchang Huang, Jiahuan Huang, Chulsoon Hwang – Missouri University of Science and Technology; Minseok Kim, Bumhee Bae, Subin Kim – Samsung Electronics Co., Ltd.

17. Self-Aligned Optical Connector Assembly on Polymer Waveguide Integrated Package Substrate for Co-Packaged Optics
Akihiro Noriki, Takeru Amano – National Institute of Advanced Industrial Science and Technology

18. 2.5D Silicon Photonics Interposer Flip Chip Attach
Pushkraj Tumne, Hsiu-Che Wang, Dwayne Shirley, Roberto Coccioli – Marvell Semiconductor, Inc.

19. A Study of the Design and Parameter Effects on System Level Characteristics of Advanced Fan-Out Wafer Level Package (FOWLP)
Kyoungdon Mun, Kyoung-Lim Suk, Dongwook Kim, Suchang Lee, Jihwang Kim, Wonkyung Choi, Jaechoon Kim – Samsung Electronics Co., Ltd.

20. Development of Electronic-Photonic 3D System in Package: Architecture, Integration, and Scaling
Jugal Kishore Bhandari, Divya Sri Rajeswari, Pamidighantam V. Ramana, Rohin Kumar Yeluripati, Mohammed Ubed, Jinin K. Jose, Anusha Veerandi, Sandhya Dharavath – LightSpeed Photonics Pte Ltd

21. Direct Paste Deposition of Inorganic Materials for Sensors Applications
Nicolas Delavault, Tanguy Lacondemine, Remy Kalmar, Manuel Fendler – CEA Tech Grand Est; Sofiane Achache, Frederic Sanchette – UTT LASMIS

22. Highly Compact and High Gain 2 x 2 Patch Array Antenna with Slotted Meanderline Loading
Hanna Jang, Payman Pahlavan, Yong-Kyu Yoon – University of Florida

23. Design of a Compact Size Bridge Connected Multiband MIMO Antenna for Automotive 5G and DSRC Communications System
Mohammad Pervez, Amanpreet Kaur – Oakland University

24. A Fully Additive Fabrication Approach for sub-10-Micrometer Microvia Suitable for 3-D System-in-Package Integration
Roghayeh Imani, Shailesh Chouhan, Jerker Delsing – Lulea University of Technology; Jussi Putaala, Olli Nousiainen, Juha Hagberg, Sami Myllymaki, Sarthak Acharya, Heli Jantunen – University of Oulu

25. The Performance and Reliability of Screen-Printed Flexible Multilayer Leads for Wearable Vital Sign Monitoring Devices
Udara S. Somarathna, Behnam Garakani, Mohammed Alhendi, Riadh A. Al-Haidari, Mark Poliks – Binghamton University; Darshana L. Weerawarne – University of Colombo; Matthew J. Misner, Andrew Burns, Gurvinder S. Khinda, Azar Alizadeh – GE Global Research

26. First Demonstration of Die-Embedded Alumina Ribbon Ceramic (ARC) Packaging for 6G Wireless Applications
Joon Woo Kim, Nahid Aslani-Amoli, Fuhan Liu, Madhavan Swaminathan – Georgia Institute of Technology; Rajesh Vaddi, Garima Nagar – Corning, Inc.

27. Security Robustness of Buried Power Rail Interconnect Technology: Modeling, Analysis and Countermeasures
Sirish Oruganti, Nishant Gupta, Sai Subrahmanya Teja Nibhanupudi, Meizhi Wang, Jaydeep Kulkarni – University of Texas, Austin

28. Intelligent Multi-Physics Design of 3-D Leadframe-Based SiC Power Module with Die Stacking for Transportation Electrification
Emanuel Torres-Surillo, Christian Molina-Mangual, Vanessa Smet – Georgia Institute of Technology

Thursday June 1

Session 40: Interactive Presentations 4
Time: 2:30 p.m. – 4:30 p.m.

Committee: Interactive Presentations

Palazzo Foyer

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Kuo-Ning Chiang – National Tsing Hua University
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Jeffrey Lee – iST-Integrated Service Technology, Inc.
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Karan Bhangaonkar – Intel Corporation
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1. Simulation of Solder Crack Phenomenon in Molding Process
Tzu Chieh Chien, Shih Kun Lo, Zong Yuan Li, Yen Hua Kuo, Ming Shaw Shy, Hui Chung Liu, Lu Ming Lai, Kuang Hsiung Chen – Advanced Semiconductor Engineering, Inc.

2. Embedded Micro-Pin Fin Heat Sink of Two-Phase Liquid Cooling for High Heat Flux 3D ICs
Huicheng Feng, Gongyue Tang, Xiaowu Zhang, Boon Long Lau, Ming Chinq Jong, Keng Yuen Jason Au, King Jien Chui – Institute of Microelectronics A*STAR; Jing Lou, Hongying Li, Duc Vinh Le – Institute of High Performance Computing A*STAR

3. Warpage Estimation of Panel-Level Package from Panel to Strip by Using Multi-Scaling Sub-Modeling Technique
Chang-Chun Lee, Chi-Wei Wang, Che-Pei Chang, Jui-Chang Chuang – National Tsing Hua University

4. A Thermally Friendly Bonding Scheme for 3D System Integration
Gordon Kuo, J. Y. Chen, C. C. Hsieh, C. J. Lee, Jason Wu, James Cui, Y. L. Kuo, C. H. Tung, KC Yee, Doug Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

5. Reliability in Selective Thinning Technology of Solder Resist for New IC Substrate Architecture
Yuya Suzuki – Taiyo Ink Mfg. Co., Ltd.; Yuji Toyoda – Mitsubishi Paper Mills Ltd.

6. Simulation, Prediction, and Verification of the Corrosion Behavior of Cu-Ag Composite Sintered Paste for Power Semiconductor Die-Attach Applications
Xinyue Wang, Zhoudong Yang, Pan Liu – Fudan University; Guoqi Zhang – Delft University of Technology; Jing Zhang – Heraeus Materials Technology Shanghai Ltd.

7. Thermal Characterization and Management of GaN-on-SiC High Power Amplifier MMIC
Yong Han, Gongyue Tang, Boon Long Lau – Institute of Microelectronics A*STAR

8. A Thin-Film Reconfigurable SiC Thermal Test Chip for Reliability Monitoring in Harsh Environments
Romina Sattari, Henk van Zeijl, GuoQi Zhang – Delft University of Technology

9. Life-Prediction of SAC305/Bi-Based Hybrid Solder Joint Considering Bi-Diffused Layers with Gradual Bi Concentrations
Yongrae Jang, Bongtae Han – University of Maryland; Hak-Sung Kim – Hanyang University

10. Thermal-Mechanical-Electrical Co-Design of Fan-Out Panel-Level SiC MOSFET Packaging with a Multi-Objective Optimization Algorithm
Wei Chen, Xuyang Yan, Jiajie Fan – Fudan University; Mesfin S. Ibrahim – Hong Kong Polytechnic University; Jing Jiang – Sky Chip Interconnection Technology Co., Ltd.; Xuejun Fan – Lamar University; Guoqi Zhang – Delft University of Technology

11. Su8 Out-of-Plane Stress Reduction Via Design of Experiment and Machine Learning
Ziqi Jia, Shuyu Shi, Yong-Kyu Yoon – University of Florida

12. Assessment Methods for the Characterization of Flux Material Systems Toward Water Absorption
Quang-Duc Pham, Norbert Holle – Robert Bosch GmbH; Juergen Wilde – University of Freiburg

13. Optimization of the Cu Microstructure to Improve Copper-to-Copper Direct Bonding for 3D Integration
Ralf Schmidt, Christian Schwarz – Atotech (MKS Instruments)

14. Effect of Ceramic Filler in Epoxy Mold Compound on Thermomechanical Property of FOWLP
Taejoon Noh, Haksan Jeong, Seung-boo Jung – Sungkyunkwan University

15. Atomistic Simulation Analysis of Plasma Surface Activation in Wafer-to-Wafer Oxide Fusion Bonding
Hojin Kim, Yu-Hao Tsai, Satohiko Hoshino, Ilseok Son, Kaoru Maekawa, Peter Biolsi, Sitaram Arkalgud – TEL Technology Center, America, LLC

16. Inorganic Capping Layers in Advanced Photosensitive Polymer Based RDL Processes: Processing and Reliability
Nelson Pinho, Emmanuel Chery, John Slabbekoorn, Mikhail Krishtab, Andy Miller, Eric Beyne – imec; Ritwik Bhatia, Ganesh Sundaram – Veeco

17. A Combined Simulation and Experimental Study on Cracking and Delamination Behavior at the Cu/Polyimide Interface of RDLs in Chiplet Package Subjected to Thermo-Mechanical Loads
Bin Chen, Guang-Chao Lyu, Hong-Guang Wang, Long Zheng, Yun-Kai Deng, Xin-Ping Zhang – South China University of Technology

18. Evolution of the Creep Response of SAC+Bi Lead-Free Solders Subjected to Various Thermal Exposures
Mohammad Al Ahsan, S. M. Kamrul Hasan, Jeffrey Suhling, Pradeep Lall – Auburn University

19. Modeling Grain Size Effects on Deformation Behavior of SAC Solder Joints
Debabrata Mondal, Jeffrey Suhling, Pradeep Lall – Auburn University

20. Reliability Study on High Performance Photo Imageable Dielectric for Advanced Package
Okseon Yoon, Jinyoung Kim, Kiseok Kim, Seonghyun Yoo, Jihye Shim, Suchang Lee, Hyoeun Lee, Sueryeon Kim – Samsung Electronics Co., Ltd.

21. A Novel Indium Metal Thermal Interface Material and Package Design Configuration to Enhance High-Power Advanced Si Packages Thermal Performance
Kuo-Chin Chang, Mirng-Ji Lii, Kuan-Min Wang, Chien-Chang Wang, Bang-Li Wu – Taiwan Semiconductor Manufacturing Company, Ltd.

22. High Temperature Storage of Cu-Cu Joints Fabricated by Highly (111)-Oriented Nanotwinned Cu
Shih-Chi Yang, Chih Chen – National Yang Ming Chiao Tung University

Refreshment Breaks: 10:30 a.m. - 11:15 a.m. and 3:00 p.m. - 3:45 p.m. for Thursday in Coquina Ballroom and Friday in Mediterranean & Palazzo Foyers

23. Time-Dependent Bulk Behavior of Cured Epoxy Molding Compound
Sukrut Prashant Phansalkar, Bongtae Han – University of Maryland, College Park

24. High-Performance, Multilayer Copper-Graphene Micro-Foam Wicks for Vapor Chambers
James Moss, Vanessa Smet, Antonia Antoniou – Georgia Institute of Technology

25. Module, Antenna, and Package Design Considerations for mm-Scale IoT Devices
Arun Paidimarri, Duixian Liu, Christian Baks, Bodhisatwa Sadhu, Alberto Valdes-Garcia – IBM Research

26. 9W/cm²/K Heat Transfer Coefficient Vapor Chamber for HPC Server Cooling Applications
Takashi Funakoshi, Katsunori Komehana – Fujikin, Inc.; Hiroyoki Ryoson, Kosuke Suzuki, Tomoji Nakamura, Takayuki Ohba – Tokyo Institute of Technology

Friday June 2

Session 41: Student Interactive Presentations
Time: 10:00 a.m. – 12:00 p.m.

Committee: Interactive Presentations

Palazzo Foyer

Session Co-Chairs:
Alan Huffman – SkyWater Technology
Email: alan.huffman@ieee.org

Biao Cai – IBM Corporation
Email: biaocai@us.ibm.com

Pavel Roy Paladhi – IBM Corporation
Email: rpaladhi01@gmail.com

Jin Yang – Intel Corporation
Email: jin1.yang@ieee.org

1. An Ultra-Fine Wiring Method for Polymer-Based Embedded Silicon Fan-Out Packaging (P-eSiFO)
Lang Chen, Bo Wen, Xiao Han, JinWen Zhang, Wei Wang, Chenxi Lin – Peking University-Institute of Microelectronics

2. Grain Orientation and Prediction of Thermal Shock Fatigue of Sn-3Ag-0.5Cu Solder Joints for Fan-Out Wafer Level Packaging
Shuye Zhang, Xinyi Jing, Peng He – Harbin Institute of Technology; Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

3. Warpage Modeling and Optimization for Polymer-Based Embedded Silicon Fan-Out Packaging (P-eSiFO) During Thermal Process Loadings
Jianyu Du, Lang Chen, Han Xu, jinwen Zhang, Wei Wang – Peking University

4. Copper-to-Copper Direct Bonding Process Using Current-Induced Enhancement Method
Byungkwan Kwak, Jinhyun Lee, Sanghwa Yoon, Bongyoung Yoo – Hanyang University

5. Secure and Scalable Key Management for Waferscale Heterogeneous Integration
Yousef Safari – McGill University/University of California, Los Angeles; Pooya Aghanoury, Subramanian S. Iyer, Nader Sehatbakhsh – University of California, Los Angeles

6. A Method to Improve 3D Interconnections Resource Utilization and Reliability in Hybrid Bonding Process Considering the Effects on Signal Integrity
Ang Li, Jianfei Jiang, Qin Wang, Zizheng Dong, Shuya Ji, Xiulan Cheng, Yuhang Zhao – Shanghai Jiao Tong University

7. Wafer-Level Integration of Atomic Vapor Cell Chip with Thermal and RF Modules
Ziji Wang, Jintang Shang – Southeast University

8. Optimization of Embedded Manifold Cooling Characteristic Parameters for GaN HEMT
Dichen Lu, Yuxin Ye, Mei Wu, Ruiwen Liu, Xiangbin Du, Lihang Yu, jie Wang, Jingping Qiao, Ziyu Liu, Yulin Shi, Binbin Jiao, Yanmei Kong – Chinese Academy of Science-Institute of Microelectronics

9. Low Dk/Df Thermosetting Siloxane Hybrid Material for Microwave Communication Printed Circuit Board
Seung-Mo Kang, Byeong-Soo Bae – Korea Advanced Institute of Science and Technology

10. Optimization of Si PnC MEMS Nanowires for Ultra-Low Thermal Conductivity
Sunghyun Hwang, James D. Overmeyer, S. M. Enamul Hoque Yousuf, Philip X.-L. Feng, Yong-Kyu Yoon – University of Florida; William N. Carr – Phononic MEMS, Inc.

11. Rapid Formation of High-Strength Sintered Silver Joints with High Reliability
Xu Zhang, Pengli Zhu, Tao Zhao, Liang Xu, Rong Sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology

12. Reference Thermal Chips for 2D and 3D Co-Packaging Process Development
Parnika Gupta, Robert Bernson, Noreen Nudds, Sean Collins, Kamil Gradkowski, Padraic E. Morrissey, Peter O' Brien – Tyndall National Institute-Photonic Packaging

13. Wideband Circularly Polarized FOWLP Antenna in Package for Satellite Communications
KaiBo Zheng, Mei Sun – Institute of Microelectronics A*STAR; Yongxin Guo – National University of Singapore

14. A High Precision Analysis Method Based on Thermal Test Chip for Thermal Characteristics of Thermal Interface Materials
Yulin Shi, Binbin Jiao, Qixing Hao, Yanmei Kong, Ruiwen Liu, Shichang Yun, Yuxin Ye, Lihang Yu, Xiangbin Du, Jie Wang, jingping Qiao, Dichen Lu – Chinese Academy of Science-Institute of Microelectronics

15. A Bionic Sweating Cooling Method for High Power Chip Based on Evaporation and Convection
Lihang Yu, Binbin Jiao, Yuxin Ye, Xiangbin Du, Yanmei Kong, Ruiwen Liu, Shichang Yun, Yulin Shi, Jie Wang, Dichen Lu, Ziyu Liu, Jingping Qiao – Chinese Academy of Science-Institute of Microelectronics

16. Generative Adversarial Network Based Adaptive Transmitter Modeling
Priyank Kashyap, Prasanth Prabu Ravichandiran, Dror Baron, Chau-Wai Wong, Tianfu Wu, Paul Franzon – North Carolina State University

17. FISHI: Fault Injection Detection in Secure Heterogeneous Integration via Power Noise Variation
Tao Zhang, Md Latifur Rahman, Hadi Mardani Kamali, Kimia Zamiri Azar, Mark Tehranipoor, Farimah Farahmandi – University of Florida

18. Preparation of Bubble-in-Bubble Structures for Atomic Sensors
Wenqi Li, Ziji Wang, Jintang Shang – Southeast University

19. Design and Fabrication of Embedded Silicon Fan-Out Manifold Microchannels Cooling (eSiFO-MMC)
Yuchi Yang, Zhou Yang, Peijue Lyu, Jianyu Du, Lang Chen, Wei Wang – Peking University; Jin Kang, Weihai Bu, Kai Zheng, Yikang Zhou, Chi Zhang – Semiconductor Technology Innovation Center (Beijing) Corporation

20. RFID Based Vehicular Positioning System for Safe Driving Under Adverse Weather Conditions
Bhargav Avireni, Yihang Chu, Ethan Kepros, Mauro Ettorre, Premjeet Chahal – Michigan State University

21. Fingerprint Extrication with Near-Field Terahertz Time-Domain Spectroscopy (THz-TDS) for IC Hardware Assurance
Chengjie Xi, John True, William Henry Mitchell, Aslam Khan, Navid Asadizanjani – University of Florida

22. Additively Manufactured Near Chip Scale Interposers for DC and RF Applications
Emily Lamport, Andrew M. Luce, Yuri Piro, Alkim Akyurtlu – UMass Lowell; Susan Trulli – Raytheon Technologies

23. Evaluation of Electromechanical Performance of a Flexible Hybrid Electronics Temperature Monitor
Zhi Dou, Dylan Richmond, Mark Schadt, Mohammed Alhendi, Mark Poliks – Binghamton University; Rafael Tudela – Tapecon, Inc.

24. Comparative Mechanical Behavior of Sn-Bi Based Low Temperature Solder Alloys Under Different Pretest Aging Conditions
Sukshitha Achar P L, Colin Greene, Sean Lai, Radu Radulescu, Hannah Fowler, John Blendell, Corol Handwerker, Ganesh Subbarayan – Purdue University; Nilesh Badwe – Indian Institute of Technology Roorkee

25. New Triple-Junction Solar Cell Assembly Process for Concentrator Photovoltaic Applications
Konan Kouame, Maxime Darnon, Gwenaelle Hamon – University of Sherbrooke

26. Characterization of Packaging, Electronic, and Photonic Materials at Cryogenic Temperatures Using a Multi-Angle Backscattering Mueller-Matrix Ellipsometer
Christopher Lewis, Jacob Marchio, Drew Sellers, Michael Hamilton – Auburn University

27. A Comparison of Wearable Metasurfaces
Adria Kajenski, Guinevere Strack, Alkim Akyurtlu – University of Massachusetts, Lowell; Shahriar Khushrushahi – Notch, Inc.

28. TrueAdapt™ - AI Based Maskless Patterning to Compensate for Die-Shift in Fan-Out Wafer Level Packaging
Golam Sabbir, Subramanian S. Iyer, Lenny Wu, Henry Sun, Krutikesh Sahoo, Guangqi Ouyang – University of California, Los Angeles

29. Die Embedded Glass Interposer with Minimum Warpage for 5G/6G Applications
Xingchen Li, Xiaofan Jia, Joon Woo Kim, Kyoung-Sik Moon, Madhavan Swaminathan – Georgia Institute of Technology; Matthew Jordan – Sandia National Laboratories

Friday Refreshment Break: 9:15 a.m. - 10:00 a.m. in Mediterranean & Palazzo Foyers

Exhibition

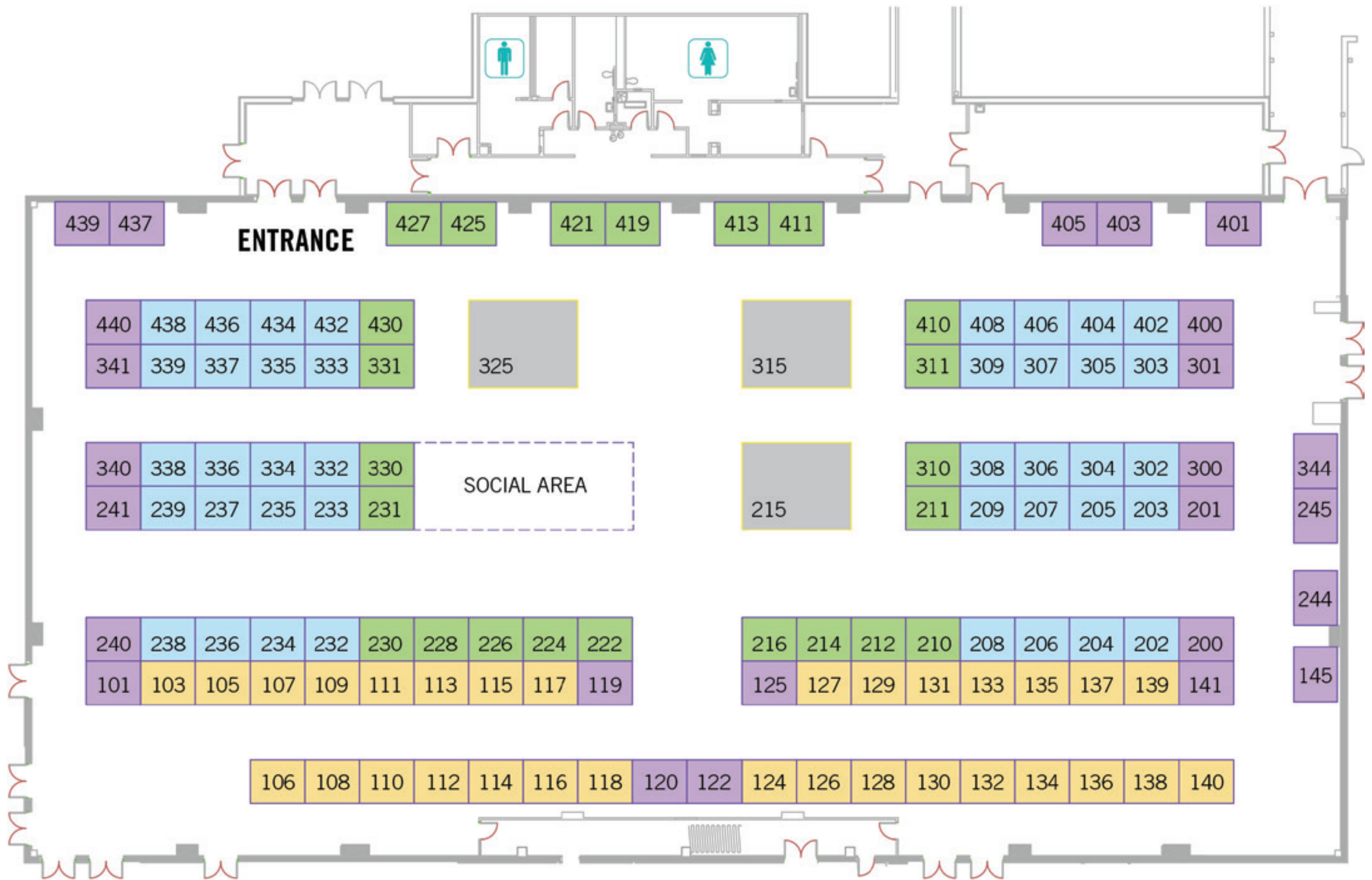
Wednesday, May 31

9:00 a.m. - 12:30 p.m. / 2:00 p.m. - 6:30 p.m.

Thursday, June 1

9:00 a.m. - 12:30 p.m. / 2:00 p.m. - 4:00 p.m.

Coquina Ballroom



2023 ECTC EXHIBITORS

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The 3D Systems Packaging Research Center (PRC) at Georgia Tech is a graduated NSF Engineering Research Center focusing on advanced packaging and system integration leading to System on Package (SoP) technologies. The center conducts research and education in all aspects of packaging that includes design, materials, process, assembly, thermal management, and integration driven by applications, which include broad areas such as high-performance computing, artificial intelligence, automotive, broadband wireless and space. The center team consists of 29 faculty from five schools, 11 research/administrative staff, 50+ graduate/ undergraduate students and several visiting engineers. This is enabled through collaboration with over 40 industry/govt. organizations and 14 universities.

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Akrometrix, over the last 25 years, has established itself as the worldwide leader of Warpage Measurement Systems and Testing Services. Our solutions determine the actual warpage characteristics of electronic assemblies/ components down to the sub-micron level, from extreme sub-freezing to high temperature conditions. Whether it be sample testing in a Q.C. lab, developing new products in engineering or room-temperature testing on the manufacturing floor, Akrometrix metrology solutions provide our customers critical data that leads to repeatable and reliable electronic assemblies utilized in consumer products up to mission critical military applications.

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Amazing Cool Technology is committed to the research and development of graphene-modified materials, using unique graphene pre-dispersion technology, which can quickly and successfully introduce various applications.

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AOI Electronics is the No.1 sales ranking OSAT in Japan, and its business focuses on the assembly and testing of electronic products. We have over 50 years of semiconductor packaging and testing experiences, and serve customers around the world. AOI Electronics provides a variety of packaging technologies, FOLP® (Fan-Out PLP), WLP, FC-QFN, Cu-Pillar, SiP, Sensor, MEMS etc. We offer advanced packaging technologies of 5G, RF, Power IC (Built-in passive, Embedded Multi-Chip, SiP) and test solutions for communications applications including mobile and infrastructure markets.

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S3IP brings the capabilities and technical resources of Binghamton University, a leading research institution, at the disposal of electronics and energy systems manufacturers and similar manufacturing industries. Our 6 research centers address pressing real-world challenges in microelectronics manufacturing, flexible hybrid electronics, and heterogeneous integration of electronics, and thin film electronic devices for energy harvest and storage. Advanced battery research is directed by Dr. Stan Whittingham, 2019 Nobel Laureate for invention of the Li-ion battery. Our professional staff, backed by the deep expertise of faculty, assists companies in problem solving and use of our 7 laboratories addressing manufacturing methods and materials, thermal management, failure analysis, and reliability improvement.

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Brewer Science is a global leader in developing and manufacturing next-generation materials and processes that foster the technology needed for tomorrow. Since 1981, we've expanded our technology portfolio within advanced lithography, advanced packaging, smart devices, and printed electronics to enable cutting-edge microdevices and unique monitoring systems for industrial, environmental, and air applications. Our relationship-focused approach provides outcomes that facilitate and deliver critical information. Our headquarters are in Rolla, Missouri, with customer support throughout the world. We invite you to learn more about Brewer Science at www.brewerscience.com.

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Cadence is a pivotal leader in electronic systems design, building upon more than 30 years of computational software expertise. The company applies its underlying Intelligent System Design strategy to deliver software, hardware and IP that turn design concepts into reality. Cadence customers are the world's most innovative companies, delivering extraordinary electronic products from chips to boards to complete systems for the most dynamic market applications, including hyperscale computing, 5G communications, automotive, mobile, aerospace, consumer, industrial and healthcare. For eight years in a row, Fortune magazine has named Cadence one of the 100 Best Companies to Work For.

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Canon U.S.A., Inc. (www.usa.canon.com) is a leader in Office Products, Imaging Systems, Medical Systems and Industrial Products. The Canon Industrial Products Division provides advanced wafer and panel process equipment for a wide range of applications and advanced compound semiconductor fabrication processes including power, automotive and 5G applications. Canon Industrial Products also enable advanced FEOL semiconductor processes to More-Than-Moore applications including 3D-IC, Interposer, FOWLP and FOPLP Advanced Packaging processes.

Canon U.S.A. offers cost-effective wafer and panel processing solutions including i-line & KrF optical lithography systems, nanoimprint lithography systems, flat-panel lithography systems, a variety of PVD systems designed for several applications, and room temperature permanent wafer bonding equipment.

Based in San Jose, California, Canon USA Industrial Products Division enables a world of innovation for customers seeking to expand More-than-Moore markets. Please contact semi-info@cusa.canon.com or visit usa.canon.com/industrial for more information on Canon Industrial Products.

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CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 1,900, a portfolio of 3,100 patents, 11,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble, France, and has offices in Silicon Valley and Tokyo. CEA-Leti has launched 70 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

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Corning offers advanced glass carriers in a wide range of CTEs in both wafer and panel formats. A CTE-matched carrier substrate helps customers minimize their problem of in-process warp. We offer quick sampling in small quantities in minimal turnaround time.

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CPS is the world leader in developing and manufacturing advanced materials solutions and products, particularly metal matrix composites (MMC) to improve performance and reliability of applications across power electronics, aerospace, and defense markets.

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premier manufacturer of hermetic packages, machined modules and housings in Kovar, Aluminum, and our MMC materials. CPS manufactures a complete line of SMP connectors for integration to packages at CPS or on your production floor.
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Deca was born of a passion to transform the way the world builds advanced electronic devices. In our first decade, our 10X thinking brought to life exciting breakthroughs with M-Series™ and Adaptive Patterning®.

Our flagship M-Series is a fully encapsulated wafer & panel-level fan-out technology which provides an ideal structure for single & multi-die packaging, chiplet integration, 3D PoP and embedded die interposers. M-Series is delivering exceptional quality and reliability for leading Smartphone manufacturers around the globe with shipment volumes exceeding one billion units per year.

Deca's Adaptive Patterning technology compensates for natural variation in embedded die structures without costly processes or design limitations. After high-speed optical measurement, Adaptive Patterning generates a bespoke and optimized layout which is precisely aligned to each device.

As a pure-play technology development, transfer and licensing company, Deca is the leading independent provider of advanced packaging technology in the semiconductor industry.

Our world class investors, including Infineon, Qualcomm, ASE, nepes and SunPower provide Deca with a strong foundation for continuing innovation and growth.

Contact us at ThinkDeca.com

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For 54 years, DISCO Hi-Tec America, Inc. has been a leader in the semiconductor industry in cutting (Kiru), grinding (Kezuru), and polishing (Migaku) technologies. DISCO's focus has expanded beyond mechanical dicing to include laser and plasma singulation. DISCO continues to be the leader in wafer thinning and polishing/stress relief with technologies such as SDBG enabling thinning of die to 20um or less. To support the increasing complexity in today's packages, DISCO has also released equipment capable of laser via drilling in non-silicon transparent materials, silicon carbide ingot slicing (KABRA), and laser lift off. In order to support research and development efforts, joint development initiatives, and next generation product prototyping, DISCO Hi-Tec America's new larger KKM Services lab in San Jose offers capability to process materials with our latest advanced cutting, grinding, and polishing technologies.

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DuPont Electronics & Industrial is a global supplier of new technologies and performance materials serving the semiconductor, circuit board, display, digital and flexographic printing, healthcare, aerospace, industrial and transportation industries. From advanced technology centers worldwide, teams of talented research scientists and application experts work closely with customers, providing solutions, products, and technical service to enable next-generation technologies.

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Ebinax provides advanced plating services. Our mission is to pursue new surface finishing possibilities to contribute to the future of manufacturing. Ebinax provides surface finishing that helps to solve the heat problems that occur with increased of circuit density and amount of information in communication devices. We have been providing ceramic (Al2O3, AlN, SiC, Si3N4, etc.) circuit boards for 40 years as heat dissipation substrates for Peltier modules and Submounts. In addition, we have developed a new technology that can coat micron-sized fins onto the surface, further improving the cooling capacity of metal heat sinks. Ebinax also provides new TGV (Through-Glass Via) substrates by combining high-density and smooth through-hole processing technology and our surface finishing technology.

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ERS electronic GmbH, based in Germering close to Munich, has been providing innovative thermal management solutions to the semiconductor industry for more than 50 years.

The company has gained an outstanding reputation, notably with its fast and accurate air cooling-based thermal chuck systems for test temperatures ranging from -65°C to +550°C for analytical, parameter-related and manufacturing probing.

ERS also supplies the Advanced Packaging market with its fully automatic and manual debonding and warpage adjust tools used for Fan-Out Wafer-Level-Packaging (FOWLP) and Panel-Level-Packaging (FOPLP) technologies up to 650 x 650 mm format.

Our headquarters, sales department, engineering center and production facilities are in the Munich suburb of Germering, and we also have sales and support offices worldwide.

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EV Group (EVG) is a leading supplier of high-volume production equipment and process solutions for the manufacture of semiconductors, MEMS, compound semiconductors, power devices and nanotechnology devices.

A recognized market and technology leader in wafer-level bonding and lithography for advanced packaging and nanotechnology, EVG's key products include wafer bonding, thin-wafer processing and lithography/nanoimprint lithography (NIL) equipment, photoresist coaters, as well as cleaning and inspection/metrology systems.

With state-of-the-art application labs and cleanrooms at its headquarters in Austria, as well as in North America and Asia, EVG is focused on delivering superior process expertise to its global R&D and production customer and partner base – from the initial development through to the final integration at the customer's site.

Founded in 1980, EVG services and supports an elaborate network of global customers and partners all over the world, with more than 1100 employees worldwide and fully-owned subsidiaries in the U.S., Japan, South Korea, China and Taiwan.

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Evatec provides PVD solutions tailored to the packaging platforms in the Advanced Packaging market. They combine best in class cost of ownership with unique technology innovations to meet today's and future requirements. Our "wafer" platforms process up to 300mm formats designed for highest levels of throughput support the use of long life targets and are equipped with a unique degassing technology that achieves best in class contact resistance and layer uniformity performance required in WLCSP, FOWLP and 2.5D/3D devices. FOPLP applications and next generation IC substrate technologies are supported by Evatec`s CLUSTERLINE® 600 equipment platforms capable of processing substrate sizes up to 650 x 650 mm, deliver highest levels in outgassing performance, layer adhesion and stack uniformity. In EMI shielding of chips on a package level, Evatec offers production solutions with the step coverage, film adhesion and low process temperatures required to protect the chip effectively at high throughput.

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F & K DELVOTEC is an interconnect solution company. We offer ultrasonic wire bonding and laser bonding process for different applications. We support our customers by offering equipment, consultation, feasibility testing, and small volume production services. Please contact Terry Chen for further information.

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ficonTEC provides device micro-assembly and testing solutions for the photonics industry. These solutions are realized as cutting-edge, high-precision production systems utilizing advanced automation approaches, regardless of the device material and target application. Our modular system architecture is additionally scalable, so that exploratory, proof-of-process development as well as high-volume manufacturing requirements are addressable – and anything in between.

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Finetech's high-accuracy die bonding equipment supports the most precise and complex applications in advanced packaging, die attach and micro assembly. Sub-micron placement is possible with an extensive range of bonding technologies including thermo-compression, ultrasonic, eutectic, epoxy, sintering, ACF/ACP, Indium and precision vacuum die bonding. Manual, motorized and automated models provide an equipment migration pathway from R&D and prototyping to production, with a unique capability to run the automated models in manual mode for true flexibility. Quality optics and highly stable machine design provide the accuracy and repeatability that today's applications demand.

The deep process knowledge we have gained through decades of experience adds value to our equipment. Our engineers work with customers to create effective solutions for specific applications - they understand that "one size" does not necessarily fit all.

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Fraunhofer IMWS' core competencies lie in the area of the characterization of materials down to the atomic scale and in material development.

Our Business Unit "Electronic Materials and Components" investigates components, systems and materials of electronics and microsystem engineering, like integrated semiconductor circuits, sensors, electronic components and assemblies. These are analyzed and tested comprehensively, in order to understand the relationship between technological process and application conditions with microstructure and material properties as well as with the affected functional performance in detail. For the benefit of our customers, we master complex, powerful methods that include non-destructive analytics, high-resolution methods of electron microscopy and solid-state spectroscopy, surface and trace analysis methods, and mechanical material characterization that includes modeling and numerical simulation.

Major areas of our work are the process characterization on a microstructural level complementing the introduction of innovative technologies as well as the fast and client-focused root cause analysis of faults and of defect formation. The results are incorporated into the clients' manufacturing processes and thus help to increase the quality and reliability of these systems.

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As part of the Fraunhofer-Gesellschaft, Fraunhofer IZM specializes in applied and industrial contract research. Fraunhofer IZM's focus is on packaging technology and the integration of multifunctional electronics into systems.

Fraunhofer IZM has two sites in Germany. Apart from its headquarters near Berlin Mitte, the institute is also represented in Dresden and Cottbus, strategically important centers for electronic development and manufacturing.

The four Fraunhofer IZM departments promote internationally cutting-edge technology development. The departments jointly work on application areas and key development topics, ensuring the research is advanced across technologies. In key development topics, the Fraunhofer IZM researchers monitor and develop highly promising research questions, paving the way for future projects with industry.

Here, Fraunhofer IZM benefits from its close cooperation with the Technischen Universität Berlin and other scientific institutes. Fraunhofer IZM has cooperated on highly productive preliminary research with the TU Berlin since its establishment, and the close relationship between the institute and university is best illustrated by the current practice of appointing a joint IZM institute head and TU university professorship.

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FUJIFILM Electronic Materials is a leading supplier of advanced materials to the electronics industry. We offer a full complement of advanced photoimageable and non-photoimageable polyimide and PBO materials designed to meet current and future advanced packaging challenges. We have a unique dry film photoimageable dielectric material available in film thickness range of <5mm to 200mm. Fujifilm has demonstrated an innovative magnetic material technology drawn from our proprietary photoresist and magnetic materials expertise.

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HD MicroSystems L.L.C. (HDM) is the leading manufacturer of liquid polyimide (PI) and polybenzoxazole (PBO) dielectric coatings. HDM is introducing new High-Reliability, Low Temp Cure PI's, including NMP-Free. HDM polymeric materials are the process-of-record (POR) in many front-end wafer applications for interlayer dielectrics (ILD) and stress buffer coatings (SB), as well as back-end advanced packaging technologies such as Flip Chip, WL-CSP, redistribution dielectrics layers (RDL) and bonding adhesives, both temporary and permanent for 3D/TSV, wafer thinning and Flexible Hybrid applications. HDM is developing materials for low loss, high frequency RF applications. In addition to conventional spin coating, HDM is enabling coating methods such as slot die, ink jet, ultrasonic spray, gravure and 3D printing.

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Heller Industries was founded in 1960 and pioneered convection reflow soldering in the 1980s. Over the years, Heller has partnered with its customers to continually refine systems to satisfy advanced applications requirements. By embracing challenge and change, Heller has earned the position as the global leader in thermal process solutions for the SMT, electronics assembly, power device assembly, and semiconductor advanced packaging industries.

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IBM Bromont is a world leader in semiconductor packaging technology, products and services. Available to customers worldwide, we invite you to take advantage of our experience, system level mindset and skilled engineers to execute your most advanced packaging and test solutions. Tap into our deep competencies as the industry continues to shift to custom SoCs and SiPs. IBM is known for its multi-chip packaging and heterogeneous integration.

We offer full turnkey solutions from modeling and characterization through Burn-in and test. Our test capability spans digital, analog, mixed signal, RF as well as multi-site programming, test pattern conversion, and load board design. We provide high quality mechanical, thermal and electrical design (including high speed/SERDES, signal integrity and power integrity), ensuring effective execution of new and updated platforms. Services include materials and process characterization, optimized substrate design, and failure analysis while package platforms range from large organic substrates to 2.3D, Silicon Photonics technologies and Si-bridge for chiplet interconnection with our DBHI packaging solution.

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Since the company's founding in 1934, Indium Corporation® has been driven by its curiosity to look at materials from a different perspective – transforming the ordinary into the unexpected. Indium Corporation® is a premier materials refiner, smelter, manufacturer, and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic

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TDM by Insidix is a topography & deformation measurement machine using Projection Moiré for temperature-dependent warpage measurement. We designed our technology for the 3D measurements of complex objects under thermal stress. TDM exerts thermal profiles and cycles on electronics components in the same way as they are imposed on devices during production processes or operations.

TDM has an internal heating/cooling sequence with an optical set-up for 3D topography analysis under thermal stress for all materials, components, and sub-systems. We measure the 3D deformation related to the imposed thermal stress throughout the thermal cycle and reveal the device's faults.

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Integra Technologies is a global leader in the sourcing, packaging, testing and characterization of highly specialized, mission-critical semiconductor components and related value-added services for high-reliability ("Hi-Rel") applications where dependability and failure-free performance are of paramount importance. Integra provides a span of in-house services and capabilities to support a broad variety of Hi-Rel components throughout the entire value-added life-cycle - from prototyping, through testing, and ultimately to volume production. More specifically, Integra specializes in semiconductor die prep, packaging, assembly, test, reliability qualification, DPA and FA service for high-reliability applications.

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Intekplus is a visual inspection equipment specialist with 3D/2D measurement and inspection technology. We apply our technology in various applications including 2D, 2.5D, 3D, SiP, FCBGA, FOWLP, FOPLP, heterogeneous packages, and substrates. Intekplus equipment can identify bump height, coplanarity, warpage, scratch, chipping, crack, misalignment, shift, missing, stain, FM, and other defects. Other than advanced packaging, we serve other products like CIS(CMOS Image Sensor), Memory, Medical, LED, OLED, and MEMS. We have advanced 2D and 3D sensor technology and develop image processing software. A single qualified recipe can be transferred to other systems in the same or in other locations for hassle-free recipe management and quality control.

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INVENTEC PERFORMANCE CHEMICALS, a company of the French Dehon group, is a global provider of SOLDERING, CLEANING & COATING materials for Electronic, Semiconductor and Industrial applications.

For almost 60 years, we have shown leadership in innovation by putting ENVIRONMENT & HEALTH IMPACT, SUSTAINABILITY and RELIABILITY at the core of our product development. Besides great technical performance of our products, we also make sure our TECHNICAL EXPERTS are close where you are, offering responsive and added value support.

With ISO 9001 & 14001 production sites in France, Switzerland, USA, Mexico, Malaysia and China we can guarantee a smooth and cost-effective supply chain. On top of this, all our production facilities are equipped with a CLEANING APPLICATION CENTER, where customers are invited to test our proposed cleaning solutions.

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JCET Group is the world's leading integrated-circuit manufacturing and technology services provider, offering a full range of turnkey services that include semiconductor package integration design and characterization, R&D, wafer probe, wafer bumping, package assembly, final test, and drop shipment to vendors around the world.

Our comprehensive portfolio covers a wide spectrum of semiconductor applications such as mobile, communication, compute, consumer, automotive and industry, etc., through advanced wafer-level packaging, 2.5D/3D, System-in-Packaging, and reliable flip chip and wire bonding technologies. JCET Group has two R&D centers in China and Korea, six manufacturing locations in China, Korea, and Singapore, and sales centers around the world, providing close technology collaboration and efficient supply-chain manufacturing to customers in China and around the world.

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JSR's THB series of thick film photoresists, along with WPR series of dielectric coatings and LP series of lift-off photoresists, offer advanced packaging technology portfolios to enable manufacturing of WL-CSP, Flip Chip, TSV, LED and MEMS devices with fine-pitched and cost effective micro-bump, Cu-pillar, RDL, and lift-off processes.

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Shibuya supplies innovative back-end semiconductor manufacturing tools such as sub-micron accuracy flip-chip bonders, micro solder ball placers, and high-speed turret handlers. Shibuya is now offering a newly developed "Fluxless LATCB" solution to the advanced HPC (High-Performance Computing) packaging industry. LATCB stands for Laser-Assisted Thermo-Compression Bonding and Shibuya

combines this cutting-edge technology with its fluxless bonding technology. Fluxless LATCB's 3600mm2 large die bonding capability with its super high-speed laser heating and simple and flexible fluxless bonding technology can bring industry-leading ultra-high solder interconnection density with the highest productivity and no corrosive residues.

Booth 205
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SHIKOKU CHEMICALS Co. has synthesized a number of unique resin crosslinking agents using our organic synthesis technology. Among them, we have discovered that the isocyanuric acid skeleton has excellent electrical properties, and are developing a new crosslinking agent with this skeleton as its core structure.

Also, GliCAP is a new interface chemical developed based on our organic synthesis technology. Unique organic coating formed on copper surface directly improves adhesion between copper and resin effectively.

SHIKOKU CHEMICALS Co. will continue to design and create materials that can balance the characteristics that have become issues in the market."

Booth 434
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Founded in 1984 as a subsidiary of the General Electric Company, Shin-Etsu MicroSi is a driving force in both the semiconductor and microelectronics industries worldwide. By infusing science and chemistry with innovation and collaboration, we create leading-edge solutions that turn possibilities into realities–while providing the proven quality and time-tested dependability on which our customers rely.

From computers to cell phones, 5G, automobiles, coatings, and more, our products are used by companies throughout the world to make the integrated circuits and semiconductor devices that power everyday living.

Booth 139
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Shinko develops and produces various "Semiconductor Packages" adapting for the miniaturization, acceleration, and performance enhancement of semiconductors.

We aim to enrich and contribute to the lives of people all over the world by providing our cutting-edge packaging technologies, for markets including IoT and AI, anticipated to become more widely used in the future, and the automotive market, in which technology development is accelerating for applications such as autonomous driving and electric vehicles (EV). Shinko also develops leading package technologies for high performance computing and data networking solutions."

Booth 238
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SHT Smart High-Tech AB is a company focusing on producing new heat-dissipating materials reinforced with graphene with a focus on cooling electronics, processors, graphics cards, LEDs, and other heat-sensitive and heat-intensive products. This is something that is essential to be able to develop high-performance electronics that are smaller, faster and lighter with more functionality-in a sustainable way. We offer high-performance graphene-reinforced materials and associated process know-how. One example of our unique and innovative developments is our graphene-reinforced interface material "Thermal Interface Material", called TIM, for electronics and power module cooling, which conducts heat efficiently both vertically and horizontally. TIM is found in our GT product series, which is available in different versions with different performances.

Booth 403
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Sigray is a San Francisco Bay Area based company, specializing in the development & integration of high-resolution, high-throughput X-ray analytical equipment.

Sigray Apex XCT is a 3D X-ray tomography platform designed for full wafers and large PCBs, capable of producing resolution down to the sub-micron regime while providing 3D imaging times on the order of a few minutes. The technique is completely non-destructive and suitable for a variety of FA, R&D, and production applications. Further to Apex XCT, Sigray produces other disruptive X-ray technologies, such as: AttoMap Micro-XRF, the flexible PrismaXRM 3D X-ray microscope, and QuantumLeap laboratory XAS.

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Silitronics offers Chip package design & assembly services from concept to NPI to volume production. We have expertise to propose, develop & implement cost effective solutions from concepts to finished products. We are located in the heart of Silicon Valley in a 10,000+ sq. ft. state of art automated facility with 10K & 1K clean rooms.

We have fully automated: Flip Chip with +/- 0.5um, Auto Dispensing and Pick/Place within +/- 3um, Auto Wire Bonders for 45um pitch, 200um wire length & 50um loop height, Auto Eutectic, Hermetic Sealing, PCBA, 3D Laser Scope, Die Shear, X-ray & Wire Pull Tester for Quality Control.

Silitronics' regularly do process development which are so advanced that there is no precedence & does not fit in a standard assembly template. Often design rules have to be pushed beyond their limits. This requires development of test vehicles, identification of right material, careful process control, monitoring of assembly parameters, DOE & investments in new equipment. Our team is ready to discuss your next project in design, process development or Chip assembly.

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SkyWater (NASDAQ: SKYT) is a U.S. investor-owned semiconductor manufacturer and a DMEA-accredited Category 1A Trusted Foundry. SkyWater's Technology as a Service model streamlines the path to production for customers with development services, volume production and heterogeneous integration solutions in its world-class U.S. facilities. This pioneering model enables innovators to co-create the next wave of technology with diverse categories including mixed-signal CMOS, ROICs, rad-hard ICs, power management, MEMS, superconducting ICs, photonics, carbon nanotubes and interposers. SkyWater serves growing markets including aerospace & defense, automotive, biomedical, cloud & computing, consumer, industrial and IoT. For more information, visit: www.skywatertechnology.com.

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Sono-Tek's ultrasonic coating technology is currently being used at the package level for EMI shielding coatings. Tested and approved using market-available EMI materials, our unique non-clogging spray coating systems, followed by low temperature heat cure, offer a more cost effective and faster alternative to costly sputtering equipment. Our FlexiCoat EMI system was designed to run continuously in production at a higher throughput than sputtering, at roughly 1/10th the cost.

Sono-Tek's ultrasonic coating technology also is well known for thin, repeatable, and low waste coatings. Other applications include: Photoresist deposition, polyimide, flux dispensing for flip chip applications, and nano suspensions (CNT, graphene, nano-wires, etc). Visit www.sono-tek.com for more information.

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STAr Technologies, Inc. was established on August 29, 2000 and headquartered in Hsinchu City, Taiwan and has branch offices in the United States of America, Japan, Singapore, South Korea, China and India. To further its reach and support, we also engage distributors in North America, Europe, South Asia Pacific, Greater China and Japan to serve regional customers directly. STAr is the acronym for "Semiconductor Test Architect" and as in the name - we are the architects with leading technologies for semiconductor test solutions.

STAr Technologies provides intellectual property, software, hardware, consumables, service and expertise to meet the requirements and challenges within the semiconductor and optical device industries. Our expertise extends across parametric electrical tests (E-test), wafer-level and package-level reliability (WLR & PLR), mixed signal tests, assembly and packaging services, probe cards, load boards, test interfaces and sockets.

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Founded in 1999, Surfx Technologies has developed and brought to market a true low-temperature, variable chemistry, atmospheric pressure plasma. Our products incorporate the most advanced plasma technology and are covered by multiple U.S. patents. Surfx's mission is to be the worldwide leader in the surface treatment of materials for the semiconductor, electronics assembly, aerospace, and medical device industries. We are driven by a total commitment to our customers. We take pride in our products and service. Our promise is to deliver to you the highest quality product for your manufacturing needs.

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SUSS MicroTec is a leading supplier of equipment and process solutions for microstructuring in the semiconductor industry and related markets.

Our portfolio covers a comprehensive range of products and solutions for backend lithography, wafer bonding and photomask processing, complemented by micro-optical components. In close cooperation with research institutes and industry partners SUSS MicroTec contributes to the advancement of next-generation technologies such as 3D Integration and Imprint Lithography as well as key processes for Wafer-Level Packaging, MEMS and LED manufacturing. With its global infrastructure for applications and service, SUSS MicroTec supports more than 8,000 installed systems worldwide.

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High performance and high reliability materials showcased by TAIYO INK are beneficial for advanced IC packaging, as well as conventional packaging applications. Consequently, Taiyo Ink has more than 90% market share of solder resist products for the IC packaging industry. One of the latest materials from TAIYO is a photo-imageable dry film with 10 µm resolution, PVI-3 HR100S, which has low curing temperature of 180°C, and can be applied as high-density RDL dielectrics for advanced packaging substrates & PLP/WLP. Taiyo also develops a variety of new dielectric materials with additional performance, such as magnetic, optical, or electrical performances. We look forward to talking with you at our booth.

Booth 405
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TATSUTA Electric Wire & Cable Co., Ltd is a leading manufacturer of innovative advanced paste for high performance electronics. By using our electrically and thermally conductive paste, higher density interconnect(HDI), longer product life and outstanding reliability are achievable. With our knowledge of metal-resin formulation technology, our materials support your development cycles/process time shorten and process temperature lower as well, which enables lower carbon emission and eco-friendly process. For more information, please visit the website and you will see our latest developments related with carbon neutrality, low temperature curing, thermal management and EMI shielding.

Booth 133
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Tazmo is a semiconductor manufacturing equipment company listed in the prime section of Tokyo Stock Market. Our main products are as follows.

(1) Semiconductor manufacturing systems for the temporary bonding and de-bonding of Silicon wafers and support glass for back grinding process.

(2) Coater/Developer for semiconductor manufacturing processes.

Equipment for resist coat/develop and other chemical solutions using our accumulated technologies. Coating with highly viscous materials and other materials that are difficult to work with while achieving good coating uniformity.

(3) Cleaning tools and surface treatment for semiconductor manufacturing processes.

Cleaning machines for manufacturing of semiconductor, slurry supply units, chemical supply units and phosphoric acid recycling.

(4) Flat Panel Display Manufacturing Equipment

Equipment used for manufacturing various types of flat panels. Tazmo has the largest share for LCD color filter resist coaters.

(5) Clean wafer transfer system

Tazmo provides various wafer transfer systems to other semiconductor manufacturing equipment suppliers. These products include robots, aligners and EFEM.

For more information, please visit our website: / www.tazmo.co.jp/en/product

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475 Half Day Rd., Suite 300
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Contact: Jose Perez
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TDK is a leader in factory automation systems. Our products include TDK precision AFM 15 Thermosonic and AFM 15 Thermal Compression flip chip die bonders. TDK flip chip die bonder's uses a micro scrub process to lower heat required for die attach process. TDK micro scrub process eliminates flux and supports 5~10 mm line width and 3mm spacing.

Additionally, TDK load ports feature high-performance that meet your needs for particle-free operation, high throughput and high durability of continual motion. In addition to the TAS300 load port, we also offer the TAS300 J1 and the TAS450.

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TechSearch International, Inc. has a 31-year history of market and technology trend analysis focused on semiconductor packaging, materials, and assembly. Research topics include WLP, FO-WLP and panel-level processing, Flip Chip, CSPs, BGAs, 3DICs, Si Interposers, System-in-Package (SiP) and Heterogeneous Integration, embedded components, ADAS and automotive electronics, and power devices. In conjunction with SavanSys Solutions, wire bond, flip chip, WLP, and 3D IC cost models are offered. Multi-client and single client consulting services are offered. TechSearch International professionals have an extensive network of more than 19,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.

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Manufacturer of tape lamination, tape removal, wafer/substrate mounting to film frame, and UV irradiation equipment for back-grinding, dicing, dry film resist and other taping applications.

Booth 233
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TOK's state-of-the-art micro processing technology produces groundbreaking and innovative products. We have pioneered the development of polymer-containing functional photoresists based on photolithography technologies that are essential for the formation of semiconductor circuits.

Along with advancement in the micro-fabrication of an electronic circuit, our sophisticated technologies provide solutions to enhance the functionality of semiconductors, such as miniaturization, high-integration, multi-functionality, and high-speed. We offer various new materials necessary for many device manufacturers, including advanced immersion photoresists enabling the formation of several tens nanometer scale features.

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Toray Industries, Inc. has devoted itself to developing new fields and materials as a basic materials manufacturer.
We have supplied both film-type and coating-type materials in the semiconductor market over decades.

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Toray's unique polyimide and film processing technologies provide excellent reliability and performance, already proven in the market.

We also offer newly developed materials specifically designed to be implemented for the low dielectric loss 5G/mmWave applications (B-stage and liquid products available).

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Booth 336
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TOWA is a leading company in the semiconductor molding equipment market. We offer equipment using our high quality / flow free compression molding method and our proven transfer molding method. We also manufacture ultra-precision molds that have been highly acclaimed by customers. Together with our molding equipment, our singulation system was developed from both aspects of the dicer and product handler to provide the optimal method of singulation for each product type. The result is high quality cutting whilst improving customers' productivity with high throughput.

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Toyota Tsusho America, Inc is the trading arm of Toyota Motor Group and we are developing the business in seven divisions such as Electronics & Chemical, Automotive, and the supporting administrative division. We have 35 locations in North America, in addition to 43 affiliate and subsidiary locations to provide valuable products and services for enterprise-level industries such as automotive, electronics, and more. As the Electronics & Chemical division, we are providing and developing services and cutting-edge products for semiconductor production such as Photoresist, CMP Slurry, High-frequency CCL, and Encapsulants to contribute to the growth of the electronics industries.

Booth 137
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Established in 1964, USHIO INC. (TOKYO: 6925) is a leading manufacturer of light sources such as lamps, lasers, and LEDs, in a broad range from ultraviolet to visible to infrared rays, as well as optical equipment and cinema-related products that incorporate these light sources. It also makes products in the electronics field (such as semiconductors, flat panel displays and electronic components) and in the visual imaging field (including digital projectors and lighting). Many of these products enjoy dominant market shares. In recent years, USHIO has undertaken business in the life science area, such as the medical and the environmental fields. See www.ushio.co.jp/en.

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VALID Co., LTD is an integrated solution provider which has the following business areas not confined to: Development and mass production of parts for medical ultrasound diagnostic devices, medical instruments for surgical robots and orthopedic implants, automobile power-train and metal 3D printers as well as industrial measurement equipment. Its specialty consists of design, verification, prototyping and production stage with robust engineering and production capabilities. The company is located in Pyeongtaek-si within 1 hour driving distance from Seoul, S. Korea.

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With over 20 years of experience, we have established our name as the technology leader in bond testing throughout the world. With 100% of our focus on bond testing, Xyztec teams with customers to offer innovative solutions that address their specific bond test needs. Our mission is to take on the challenges of many different industries by offering customers products that improve their quality and increase their bottom line. We offer full automation solutions for both wire pull and shear operations. We also revolutionized the sensor exchange by mounting up to 6 sensors on a rotational measurement unit (similar to a software selected turret). Changing between tests is a matter of only a few seconds!

Among others, we support Military, Medical, industrial, automotive and microelectronic applications.

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Yamaha Robotics Holdings Integrates Back-end Semiconductor process and Creates Value-added Process technology.

Integration and Streamlining Back End Semiconductor Assembly One stop solution for Intelligent Factory.

Equipment Product line includes: Flip Chip, Die bonder, wire bonder, molding, inspection and SMT.

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Yole Group is an international company recognized for its expertise in the analysis of markets, technological developments, and supply chains, as well as the strategy of key players in the semiconductor, photonics, and electronics sectors.

With Yole Intelligence, Yole SystemPlus and Piséo, the group publishes market, technology, reverse engineering and costing analyses and provides consulting services in strategic marketing and technology analysis. The Yole Group Finance division also offers due diligence assistance and supports companies with mergers and acquisitions.

Yole Group benefits from an international sales network. The company now employs more than 180+ people. More information on www.yolegroup.com.

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Zuken is a global provider of leading-edge software and consulting services for system-level electrical and electronic design and manufacturing. Founded in 1976, Zuken has the longest track record of technological innovation and financial stability in the electronic design automation (EDA) software industry for advanced packaging, printed circuit board design, and multi-domain co-design. The company's extensive experience, technological expertise and agility, combine to create world-class software solutions. Zuken's transparent working practices and integrity in all aspects of business produce long-lasting and successful customer partnerships that make Zuken a reliable long-term business partner. Zuken is focused on being a long-term innovation and growth partner. The security of choosing Zuken is further reinforced by the company's people— the foundation of Zuken's success. Coming from a wide range of industry sectors, specializing in many different disciplines and advanced technologies, Zuken's people relate to and understand each company's unique requirements.

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Zymet manufactures Adhesives & Encapsulates and has been serving the electronics industry for over 30 years. Products include rewardable undersells and edge bond adhesives for high reliability and harsh environment applications. Other products include ultra-low stress adhesives, electronically conductive adhesives, thermally conductive adhesives, and non-conductive pastes.

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FIRST CALL FOR PAPERS

IEEE 74th Electronic Components and Technology Conference • www.ectc.net
May 28 - May 31, 2024 at the Gaylord Rockies Resort & Convention Center, Denver, Colorado, USA

The Electronic Components and Technology Conference (ECTC) is the premier international conference that brings together the best in electronics packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Electronics Packaging Society (EPS) of the IEEE. You are invited to submit abstracts that provide non commercial information on new developments, technology and knowledge in the areas including, but not limited to the topics in what follows for each technical program subcommittee of ECTC.

Applied Reliability: Reliability of 2D, 2.5D, Si-bridge, 3D, chiplets, SiP, WLCSP, FOWLP, FOPLP & heterogeneous integration; Interconnect reliability in micro-bump, micro-pillar, Cu- pillar, TSV, TGV, RDL, HDI, stacked-die, hybrid-bond, flip chip & wire bonded packages; Novel reliability test methods, life models, FA techniques & materials characterization; Component and board level reliability in computing, HPC, mobile, networking, automotive, power electronics, harsh/hi-temp environments, IoT, sensors, AI, autonomous vehicles, medical, wearable electronics, LEDs, displays & memory.

Assembly and Manufacturing Technology: Assembly and manufacturing challenges for new markets; Die bonding methods and processes; embedded packaging and modules; Wafer level process/materials technologies; Die and package singulation manufacturing; New & next generation substrates; Smart factory/manufacturing; Design for Manufacturing; Assembly related test/yield hardware development; Integrating advanced thermal solutions in manufacturing: Design/performance, integrating solutions, thermal materials, low stress/ high thermal; Process advancements/yield enhancements: Cost of inspection, sampling, metrology, new processes for fine RDL, small via fabrication, transfer/ compression/injection mold; Heterogeneous integration and process: chiplets, 3D stacking, bridge technology, large body, warpage management; Shielding/ protection technologies and manufacturing.

Emerging Technologies: Emerging, novel and unique packaging and material technologies for: Soft and intelligent packaging; Flexible/stretchable hybrid electronics; Implantable biosensors and bioelectronics; Bio-resorbable packaging; Extreme harsh environment; Nanomanufacturing; Paper sensors/electronics pop-up/origami; MEMS & NEMS; Close-To-Motor high-voltage power electronics; Packaging for wide band gap devices; Anti-tamper, cryptography; Additive manufacturing; Packaging for quantum computing and electro-optical integration; Recyclable and sustainable electronics packaging; AI, ML and computer vision for packaging; Point-of-care diagnostic packaging; Space hardened packaging; Green and sustainable electronics; Net zero strategy/technology.

Interconnections: Interconnection Technology and Processing: Hybrid/direct Cu bonding, fan-out, panel-level, chiplets, SiP, flip-chip, 2.5D/3D, Si/glass/organic interposers, TSV, micro- bump, Cu pillar, wire bonding, thermo-compression bonding, fine-pitch/multi-layer RDL, printable interconnects, flexible substrates, photonic interconnects, quantum interconnects; Interconnection material, characterization and reliability; Conductive/non-conductive adhesives, low temperature solder, underfill, molding compounds, thermal interface materials, thermal/ mechanical/electrical tests and reliability; Interconnection physical co-design and architectures for emerging applications- HPC, mobile, 5G, IoT, power and rugged electronics, medical and health, automotive, aerospace, flexible hybrid electronics, micro-LED display.

Materials & Processing: Wafer & panel level packaging materials; Materials for harsh environments; Packaging substrates; Flexible, stretchable, & wearable electronics; Wafer bond/debond materials; TSV; Emerging electronic materials & processes; Novel solder metallurgies; Dielectrics and underfills; Molding compounds; Thermal interface materials; Advanced wire bonding and conductive adhesives.

Packaging Technologies: Architectures, chiplets, and applications for 2.5 & 3D, TSV & interposer; Advanced flip-chip, SiP, CSP, PoP, MEMS, sensors & IoT; Automotive & power electronics; bio, medical, flexible & wearable packaging; Embedded & advanced substrates; Fan-out, wafer & panel level processes; Heterogeneous integration.

Photonics: Assembly and packaging for all applications that leverage photonics components and circuits. Packaging of Photonics Integrated Circuits (PICs) for telecom, datacom, and 5G; Co- packaged and near-packaged optics; Heterogeneous integration; Artificial intelligence; quantum systems such as processors, sensors, and networks; Medical devices; Automotive/LIDAR; Aerospace, defense, and cryogenic/harsh environment; RF/MW photonics; Free-space optics; AR/VR; WDM, and high power lasers; Micro-LEDs and 3D light-field displays; Imaging and environmental sensors; New materials, connectors; EDA tools, and test methods/equipment.

RF, High-Speed Components & Systems: 5G/6G, IoT, cloud computing, autonomous vehicles, AI/machine learning; Antennas, radars, sensors, power transfer, EM shielding, wired/ wireless communications, RF to THz; Electrical and multi-physics modeling, simulation and characterization of interconnects, components, modules, and heterogeneous integration; Signal/power integrity, and chip/package/board co-design.

Thermal/Mechanical Simulation & Characterization: Thermal/ mechanical simulation and characterization at component, board, and system levels for all packaging technologies: Reliability-related modeling including fracture mechanics, fatigue, electromigration, warpage, delamination, moisture, drop, shock and vibration, and modeling for harsh environments (thermal, chemical, etc.); Material constitutive relations; Chip-package interaction for heterogeneous integration, wafer fabrication and package assembly process related modeling; Novel modeling techniques including multi-scale physics, co-design approaches; Quantum computing; Measurement methodologies, characterization and correlations, model order reduction, sensitivity analysis, optimization, statistical analysis; Application of artificial intelligence on modeling, characterization, digital twin; Simulations for virtual release.

Interactive Presentations: Abstracts may be submitted related to any of the already listed topics. Highly encouraged at ECTC, interactive presentations allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to visit ECTC's website to submit an abstract in which you describe the novelty, scope, content, and key points of your proposed manuscript. You can also submit an optional supporting figure or data table. Abstracts cannot contain more than 700 words and must be received by October 9, 2023, together with a 50 words (or less) description of its novelty. All abstracts must be submitted electronically at www.ectc.net together with the affiliation, mailing address, business telephone number, and email address of all co-authors with your submission. The authors are notified about the abstract selection outcome by December 15, 2023.

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Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on a subset of the listed topics. From proposals received, 16 PDCs are selected for offering at the 74th ECTC on Tuesday, May 28, 2024.

Each selected course is given a minimum honorarium of $1,500. In addition, instructors of the selected courses are offered the speaker discount rate for the conference. Attendees of the PDCs are offered Continuing Education Units (CEUs). These CEUs can be recognized by employers as a formal measure of participation and attendance in "noncredit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals can be submitted via the ECTC website at www.ectc.net by October 22, 2023. Authors are notified of course acceptance with instructions by December 15, 2023.

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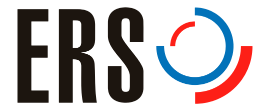
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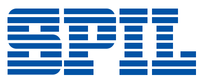
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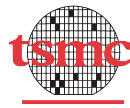
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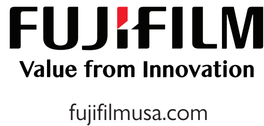
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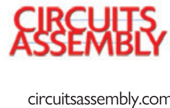
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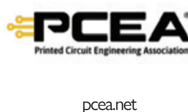
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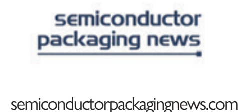
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JW MARRIOTT ORLANDO GRANDE LAKES, ORLANDO, FLORIDA, USA

JW MARRIOTT

ORLANDO GRANDE LAKES®

North
South
Coquina Ballroom
Load-In Door
Coquina Office
Pre-function
Salon 8
Salon 7
Salon 6
Salon 5
Mediterranean Ballroom
Salon 4
Salon 3
Salon 2
Salon 1
Pre-function
Mediterranean Porte-Cochere

JW MARRIOTT
LOBBY LEVEL

Salon H
Salon G
Salon F
Salon E
Salon D
Palazzo Ballroom
Salon C
Salon B
Salon A
Pre-function
Breezeway
Grande Registration Desk
Registration Desk
Escalators Up/Down
Rotunda
Business Center
Meeting Planner Office
Entrance from Hotel Lobby

JW MARRIOTT
LOWER LEVEL

Segura 4
Segura 3
Segura 2
Segura 1
Segura 6
Segura 5
Del Lago 4
Del Lago 3
Del Lago 2
Del Lago 1
Marbella 4
Marbella 3
Marbella 2
Marbella 1
Amarante 3
Amarante 2
Amarante 1
Cordova 6
Cordova 5
Cordova 4
Cordova 3
Cordova 2
Cordova 1
Milagro Boardroom
Dorada
Brava
Cataluna II
Cataluna I
Pre-function
Breezeway
To Spa
Valencia &
Valencia Terrace
Barcelona
Escalators Up/Down
Madrid
Petra
Palma
Sevilla 1
Sevilla 2
The JW Studio
Additional Lower Level Spaces

ADDITIONAL JW MARRIOTT
LOWER LEVEL SPACES

Almeria III
Almeria II
Almeria I
Family Bathroom
Stairs to Lobby
Citron Restaurant
Monterey
Primo Garden
Citrus B
Citrus A

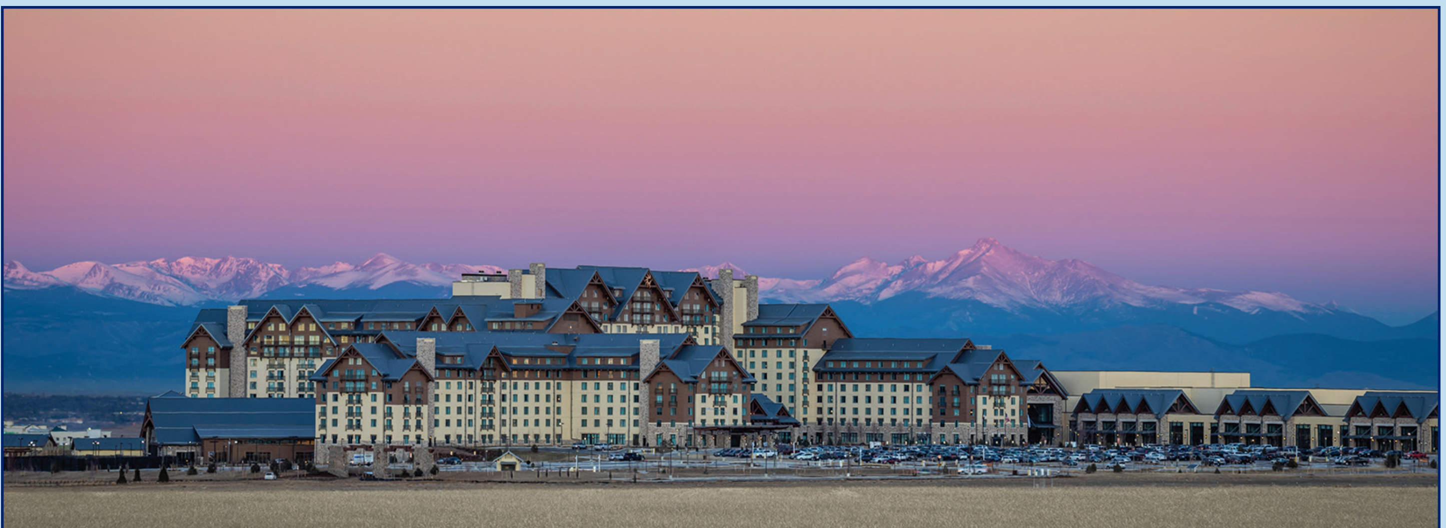
JW MARRIOTT ORLANDO, GRANDE LAKES

4040 Central Florida Parkway, Orlando, Florida 32837

407.206.2300 jwgrandelakes.com

Gaylord Rockies Resort & Convention Center
Denver, Colorado, USA
May 28 – May 31, 2024

Standing at the edge of the Front Range, Gaylord Rockies Resort & Convention Center showcases the state's alpine charm and offers guests a welcome reprieve from the typical mountain resort stay. From our thrilling Arapahoe Springs Water Park, to an exciting lineup of family-friendly activities and entertainment, there's something for the entire family to enjoy. Guests can explore the beautiful Grand Lodge and its stunning mountain views, five delicious restaurants, bars, the world-class Relâche Spa, and a state-of-the-art fitness center. For those planning or attending their next meeting or event, the resort features over 500,000 sq ft of flexible meeting space, 1,387 modern guest rooms, and 114 spectacular suites. With a fantastic water park, seasonal events, entertainment, and close proximity to local attractions, Gaylord Rockies Resort is the place where you can enjoy more of everything you love.



CONFERENCE AT A GLANCE

REGISTRATION

Monday, May 29, 2023
3:00 p.m. - 6:00 p.m.

Tuesday, May 30, 2023
6:45 a.m. - 7:45 p.m.*
*(AM PD Courses & Special Session Only)

Wednesday, May 31, 2023
6:45 a.m. - 4:00 p.m.

Thursday, June 1, 2023
7:00 a.m. - 4:00 p.m.

Friday, June 2, 2023
7:00 a.m. - 12:00 Noon

ECTC Registration Desk located across from Mediterranean 3 (lobby level)

ECTC EXHIBITION

Wednesday
9:00 a.m. - 12:30 p.m.
2:00 p.m. - 6:30 p.m.
Reception - 5:30 p.m. - 6:30 p.m.

Thursday
9:00 a.m. - 12:30 p.m.
2:00 p.m. - 4:00 p.m.
Coquina Ballroom

SPEAKER PREPARATION ROOM

Tuesday – Friday
7:00 a.m. – 5:00 p.m.
Brava, lower level

TUESDAY

PDC Instructors and Proctors Briefing & Breakfast
7:00 a.m. – 8:00 a.m.
Cordova 5 & 6

Professional Development Courses (PDCs)
8:00 a.m. – 12:00 p.m.
1:30 p.m. - 5:30 p.m.
See page 8 for locations

IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop
8:00 a.m. – 4:30 p.m.
Palazzo E

Special Sessions:
ECTC Special Session 1
8:30 a.m. – 10:00 a.m.
Palazzo D

ECTC Special Session 2
10:30 a.m. – 12:00 p.m.
Palazzo D

ECTC Special Session 3
1:30 p.m. – 3:00 p.m.
Palazzo D

ECTC Special Session 4
3:30 p.m. – 5:00 p.m.
Palazzo D

Refreshment Breaks
10:00 a.m. – 10:20 a.m.
3:00 p.m. – 3:20 p.m.
Mediterranean & Palazzo Foyers

Lunch
12 Noon – 1:15 p.m.
Mediterranean 4 & 5

ECTC Exhibition Setup
1:00 p.m. – 5:00 p.m.
Coquina Ballroom

ECTC Student Reception
5:00 p.m. – 6:00 p.m.
Outside: Mediterranean 4 & 5 Porte-Cochere

General Chair's Speakers Reception
6:00 p.m. – 7:00 p.m.
Mediterranean 4 & 5
By invitation only

Young Professionals Networking Panel
7:00 p.m. – 7:45 p.m.
Palazzo D

IEEE EPS Seminar
7:45 p.m. – 9:15 p.m.
Palazzo E

WEDNESDAY – FRIDAY

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Palazzo E

Sessions
9:30 a.m. – 12:35 p.m. or
2:00 p.m. – 5:05 p.m.
see pages 10-21 for specifics

Sessions 1, 7, 13, 19, 25, 31
Palazzo D

Sessions 2, 8, 14, 20, 26, 32
Palazzo A & B

Sessions 3, 9, 15, 21, 27, 33
Mediterranean 2 & 3

Sessions 4, 10, 16, 22, 28, 34
Mediterranean 1

Sessions 5, 11, 17, 23, 29, 35
Mediterranean 6

Sessions 6, 12, 18, 24, 30, 36
Mediterranean 7 & 8

Interactive Presentations
10:00 a.m. - 12:00 p.m. or
2:30 p.m. - 4:30 p.m.
see pages 22 - 23 for specifics

Sessions 37 - 41
Palazzo Foyer

Lunch
12:45 p.m. - 1:45 p.m.
Mediterranean 4 & 5

Refreshment Breaks
10:30 a.m. – 11:15 a.m.
3:00 p.m. – 3:45 p.m.
Wednesday & Thursday
Coquina Ballroom

Friday
Mediterranean and Palazzo Foyers

73RD ECTC GALA RECEPTION

Thursday at 6:30 p.m.
Valencia, lower level outside (Backup Location: Mediterranean 4 & 5)

DAILY MAINSTAGE

ECTC Keynote
Wednesday
8:00 a.m. – 9:15 a.m.
Mediterranean 4 & 5

Diversity and Career Growth Panel Session
Wednesday
6:30 p.m. – 7:30 p.m.
Mediterranean 4 & 5

EPS Plenary Session
Thursday
8:00 a.m. – 9:15 a.m.
Mediterranean 4 & 5

IEEE EPS President Panel
Friday
8:00 a.m. – 9:15 a.m.
Mediterranean 4 & 5

The 2024 IEEE 74th Electronic Components and Technology Conference

May 28 – May 31, 2024

Mark Your Calendars Now!

Gaylord Rockies Resort & Convention Center
Denver, Colorado, USA

Sponsored by

For more information visit www.ECTC.net