

**Professional Development  
Courses  
Tuesday, June 1, 2010**

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**MORNING COURSES  
8:00 AM - 12:00 PM**

**1. Achieving High Reliability of Lead-Free  
Soldering - Materials Consideration  
Course Leader: Ning-Cheng Lee – Indium  
Corporation**

Ning-Cheng Lee is the Vice President of Technology of Indium Corporation. He has been with Indium since 1986. Prior to joining Indium, he was with Morton Chemical and SCM. He has more than 20 years of experience in the development of fluxes and solder materials for SMT industries. He received his PhD in polymer science from University of Akron in 1981, and a BS in chemistry from National Taiwan University in 1973. Ning-Cheng is the author of "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies", and co-author of "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials". He received 1991 award from SMT Magazine and 1993 and 2001 awards from SMTA for best proceedings papers of SMI and SMTA international conferences, and 2008 award from IPC for Honorable Mention Paper – USA Award of APEX conference. He was honored as 2002 SMTA Member of Distinction, and received 2003 Lead Free Co-Operation Award from Soldertec, and received 2006 Exceptional Technical Achievement Award from CPMT. He serves on the SMTA board of directors.

**2. UltraHigh-Thermal-Conductivity  
Packaging Materials**

***Course Leader: Carl Zweben – Thermal  
Materials Consultant***

Dr. Zweben, now an independent consultant, has directed development and application of advanced electronic packaging and thermal management materials for over 35 years. He was the first to use silicon carbide particle-reinforced aluminum (Al/SiC) and other advanced thermal materials in electronic packaging. He was formerly Advanced Technology Manager and Division Fellow at GE Astro Space. Other affiliations have included Du Pont, Jet Propulsion Laboratory, Materials Sciences Corporation, and the Georgia Tech NSF Packaging Research Center.

Dr. Zweben was the first, and one of only two winners of both the GE One-in-a-Thousand and Engineer-of-the-Year awards. He is a Life Fellow of ASME, a Fellow of ASM and SAMPE, an Associate Fellow of AIAA. He was a Distinguished Lecturer for AIAA and ASME. He has published and lectured widely on advanced thermal materials, and is Co-Editor-in-Chief of the six-volume Comprehensive Composite Materials.

Dr. Zweben has directed and lectured at over 200 short courses for many organizations, including ECTC, SemiTherm, ASME, Nokia, Delphi Electronics, Coherent Laser, Rogers Corporation, BAE Systems, Boeing, Lockheed Martin, Northrop Grumman, ITT, Reynolds, Princeton University High Energy Physics Group, the Electro-Optics Center, the US Air Force, and others. He received the UCLA Certificate of Appreciation for Excellence in Teaching.

***3. Wafer Level-Chip Scale Packaging  
Course Leader: Luu Nguyen – National  
Semiconductor Corporation***

L. T. Nguyen is a Senior Engineering Manager in the Packaging Research Group at National Semiconductor Corp., working on various aspects of wafer-level packaging, lead-free and halogen-free, thermal measurement and modeling, design-for-manufacturability, design-for-reliability, precision analog, printed electronics, and MEMS. He received his Ph.D in Mechanical

Engineering from MIT, and has worked at IBM Research and Philips Research.

He co-edited two books on packaging, and has close to 200 publications. He has over 70 patents and invention disclosures. He is a Fellow of IEEE and ASME, and a Fulbright Scholar (Finland 2002). He is currently an Associate Editor for the IEEE Transactions on Advanced Packaging, IEEE Transactions on Components and Packaging Technologies, and IEEE Transactions on Electronics Packaging Manufacturing. He was a Guest Editor for the T-EPM for a special issue on Drop Testing, and the T-ADvP for two issues on Wafer Level Packaging. He received two Best of Conference Awards (27th IEMT 2002 and InterPack 2005) and eight IMAPS and IEMT Best of Session Conference Awards. Other awards include the 2003 Mahboob Khan Outstanding Mentor Award from the Semiconductor Research Corporation in recognition of contributions to student mentoring, research collaboration, and technology transfer, and the 2004 IEEE CPMT Outstanding Sustained Technical Contributions Award.

He has also been involved with an Engineering Council since 2002 to develop a comprehensive program to foster professional development, practical training, best practices sharing, mentoring, cross-training, and e-learning among more than 2,500 National Semiconductor engineers worldwide. These efforts were recognized with the IEEE Educational Activities Board Employer Professional Development Award (2005), the IEEE Region 6 Outstanding Corporate Engineering Community Service Award (2006), and the European Electronics Industry Elektra "Investing in People" Award (2006).

***4. 3D IC Integration - An Emerging  
System Level Architecture  
Course Leader: Philip Garrou –  
Microelectronic Consultants of NC***

Dr. Garrou currently consults in the areas of thin film technology, IC packaging, microelectronic materials and 3D IC integration. From 2002 – 2004 he was Director of Technology for Dow Chemicals

Advanced Electronic Materials business. From 1997 – 2002 he was General Manager of Dows BCB dielectric business.

Dr. Garrou is a fellow of IEEE & IMAPS and has served as President of the IEEE CPMT (2003-2005) and IMAPS (1998). Dr. Garrou has been Associate Editor of IEEE Transactions on Components and Packaging. He is currently a contributing editor and 3D IC blogger for Semiconductor International. He has authored > 100 technical publications. He edited and authored the McGraw Hill Multichip Module Handbook (1998) and Wiley-VCH Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits (2008).

Awards: 2000 - IMAPS Ashman award for "...technical achievement in Microelectronics Packaging". 2002 - Fraunhofer IZM International Adv Packaging Award for "...pioneering achievement in the introduction of new thin film polymeric packaging materials." 2007 - IEEE CPMT Sustained Technical Achievement Award for "...for 25 years of technical contributions and leadership in thin film dielectric materials and microelectronic applications including multichip modules, bumping and wafer level packaging, integrated passives and 3D integration"

### ***5. Nanopackaging Applications and Modelling***

***Course Leaders: Chris Bailey – University of Greenwich; James Morris – Portland State University***

Chris is Professor of Computational Mechanics and Reliability at the University of Greenwich, London, United Kingdom. He received his PhD in Computational Modeling in 1988, and an MBA in Technology Management in 1996. He has published over 200 papers on Design and Simulation of micro/nano-technology based processes and products and has managed many UK and International projects and worked closely with over 100 companies with regards their design, simulation and modelling requirements. Chris is a member of the NAFEMS Multi-Physics/Scale

Modelling working group, a senior member of IEEE-CPMT, and a UK Committee member of IMAPS. In 2003 he was the Royal Society visiting Professor to Hong Kong. In 2007 he was and Programme Chair for High Density Packaging Conference in Shanghai, China, and also the local organizer of the IEEE sponsored EuroSime conference in London. In 2008 he was the General Chair for the Electronics System-integration Technology Conference (ESTC-2008) in Greenwich, London.

James E. Morris is a Professor of Electrical & Computer Engineering at Portland State University, Oregon, and an IEEE Fellow. Professor Morris is an IEEE-CPMT Distinguished Lecturer, and won the 2005 CPMT David Feldman Outstanding Contribution Award. He is an Associate-Editor of the IEEE Transactions on Components & Packaging Technology, and has edited four books on electronics packaging, with “Nanopackaging: Nanotechnologies and Electronics Packaging” from Springer the most recent. Recently appointed as the CPMT Society representative on the IEEE Nanotechnology Council, he has established a NTC Nanopackaging technical committee to act as a Nanopackaging program committee for the annual IEEE NANO conference, and has instituted a regular Nanopackaging column in the IEEE Nanotechnology magazine. His research activities have been focused recently on electrically conductive adhesives and the electrical conduction mechanisms in discontinuous thin metal films, with applications to nanopackaging and single-electron transistor nanoelectronics, but with continuing projects in device modeling and sensors too. Over the past year, he has held the Nokia-Fulbright Fellowship at Helsinki University of Technology, following an Erskine Fellowship at the University of Canterbury, N.Z., and research appointments at the University of Greenwich, Dresden University of Technology, and Chalmers University of Technology.

**6. Moisture Related Reliability in  
Electronic Packaging**  
**Course Leader: Xuejun Fan – Lamar  
University**

Dr Xuejun Fan is currently at Lamar University. Prior to that he was in Chandler, Arizona, from 2004 to 2007, a Senior Member Research Staff with Philips Research Lab at Briarcliff Manor, New York from 2001 to 2004, and a Member Technical Staff and Group Leader at the Institute of Microelectronics (IME), Singapore from 1997 to 2000. Dr. Fan has been active in instructing short courses in the area of reliability mechanics of IC packaging and microsystems. In 2008, he is elected as CPMT Distinguished Lecturer. In 2009 he received 2008 the 2008 Best Paper Award of IEEE Transactions on Components and Packaging Technologies. Dr. Fan's interests and expertise lie in the areas of design, modeling, material characterization, and reliability in micro-/nano- electronic packaging and microsystems. He has published more than 100 scientific papers and filed 5 patents in world-wide patent offices. In his earlier career as a university faculty in China from 1989 to 1997, he received the Young Scientist Fellowship from Japan Society of Promotion of Science to spend a year at the University of Tokyo in 1993. He was a visiting professor at the University of British Columbia, Vancouver, Canada from 1996 to 1997. Dr. Fan was promoted to a full professor at Taiyuan University of Technology, Taiyuan, Shanxi in 1991, and became one of the youngest professors in China when he was 27. He was a nominee for the title of "1991 Ten Outstanding Youth of China", and received Young Faculty Award in 1994 from Fok Ying-Tung Education Foundation.

***7. Fundamentals and Applications of  
Package Reliability Predictions  
Course Leader: Shubhada Sahasrabudhe,  
Alan Lucero – Intel Corporation***

Shubhada Sahasrabudhe received a Bachelor's degree in Mechanical Engineering from University of Pune, India and a M.S. degree in Mechanical Engineering from University of Maryland, College Park. She is a Senior Reliability Engineer with the Assembly Technology Development Quality and Reliability Division at Intel Corporation since 2001. Over the

past 9 years, she has played a key role in driving knowledge based reliability methods. She holds a patent and has published many technical papers in the field of electronic package reliability. She teaches Package Quality and Reliability Methods within Intel and also at Arizona State University.

Alan Lucero currently manages a reliability methods development group in TD Q&R. As an undergraduate Alan's studies and work centered on the physics of electronic materials where he worked 2 yrs as an assistant at New Mexico Inst. Of Mining & technology. As a graduate student at Univ. of Illinois – Urbana-Champaign Alan designed, modeled, synthesized and characterized self organizing polymers for use in mechanical and biological systems. Professional work at Intel over the past 14 yrs. has centered on package reliability engineering and moving from standards based methods to align knowledge based physics of failure reliability assessment and analysis methods. Alan holds patents and papers related to many aspects of package reliability.

***8. Packaging of High Brightness (HB)  
LED for Solid State Lighting  
Course Leaders: Ricky Lee – HKUST;  
Sheng Liu – Huazhong University of  
Science and Technology***

Ricky Lee received his PhD degree from Purdue University. Currently he is Professor of Mechanical Engineering and Director of Center for Advanced Microsystems Packaging (CAMP) at the Hong Kong University of Science & Technology (HKUST). His research activities cover flip chip technologies and wafer level packaging, through silicon vias and 3D packaging, LED and optoelectronics packaging, lead-free soldering and solder joint reliability. Ricky has substantial publications in international journals/conference proceedings and received several best paper awards. He also co-authored three books and owns three technical patents. Ricky is Fellow of IEEE and ASME, and Institute of Physics (UK). In addition, he is elected IEEE CPMT Distinguished Lecturer and receives CPMT Electronics Manufacturing Technology

Award. Furthermore, he serves as Editor-in-Chief of IEEE Transactions on Components & Packaging Technologies and Associate Editor of IEEE Transactions on Advanced Packaging. Ricky is the project leader to implement HB-LED SSL on Hong Kong subway trains.

Sheng Liu is a Changjiang scholar professor of Mechanical Engineering at Huazhong University of Science and Technology and he has a dual appointment at Wuhan National Laboratory for Optoelectronics. He once was a tenured faculty at Wayne State University. He has over 17 years experience in LED/MEMS/IC packaging. He has extensive experience in consulting with many leading multinational and Chinese companies. He once won prestigious White House/NSF Presidential Faculty Fellow Award in 1995, ASME Young Engineer Award in 1996, NSFC Overseas Young Scientist Award in 1999 in China, IEEE CPMT Exceptional Technical Achievement Award in 2009, and Chinese Electronic Manufacturing and Packaging Technology Society Special Achievement Award in 2009. He has been an associate editor of IEEE Transaction on Electronic Packaging Manufacturing since 1999 and an associate editor of Journal of Frontiers of Optoelectronics in China since 2007. He is currently one of 11 National Committee Members in LED under Ministry of Science and Technology of China from 2006-2011. He obtained his Ph.D. from Stanford University in 1992. He is ASME Fellow. He has filed and owed more than 80 patents in China and USA, and has published more than 300 technical articles, edited more than 9 proceedings in English for ASME and IEEE, he has co-authored the first book in LED packaging for lighting applications, which will appear at the end of 2009.

## **AFTERNOON COURSES**

**1:15 - 5:15 PM**

***9. Finite Element Simulation and Life Prediction for Solder Joint Reliability***  
***Course Leader: Ahmer Syed – Amkor Technology***

Mr. Ahmer Syed is Vice President of Mechanical & Thermal Engineering at Amkor Technology, USA heading the mechanical and thermal test and simulation group.

Mr. Ahmer Syed has been involved in solder joint reliability predictions for almost 20 years and has published various technical papers dealing with solder joint reliability, finite element simulations, life prediction, and acceleration factors. He also chaired JEDEC task group to develop board level drop test method (JESD22-B111) and cyclic bend test method (JESD22-B113). He has strong background in solder damage mechanisms for thermal and mechanical loading conditions and has led Amkor technical group in Pb free solder alloy selection. He has also represented Amkor in various industry consortia and groups on package and board level reliability and Pb free solder.

#### ***10. Thermal Management of Hot Spots and 3D Chip Stacks***

***Course Leaders: Avram Bar-Cohen – University of Maryland; Karl Geisler – General Dynamics Advanced Information Systems***

Avram Bar Cohen is Distinguished University Professor and Chair of Mechanical Engineering at the University of Maryland, where he continues his research in the thermal management of micro/nano electronic and photonic systems. He is the co-author (with A.D. Kraus) of "Design and Analysis of Heat Sinks" (1995) and "Thermal Analysis and Control of Electronic Equipment" (1983) and has co-edited 13 books in this field. He has authored and co-authored some 250 Journal papers, Refereed Proceedings papers, and Chapters in books, and has delivered more than 50 Keynote, Plenary, and Invited Lectures at major technical Conferences and Institutions. He is currently the Editor-in-Chief of Transactions and a member of the Board of Governors of the IEEE CPMT Society. Bar-Cohen received the 2007 InterPack Achievement Award, the 2001 IEEE CPMT Society Outstanding Sustained Technical Contributions Award, the 2000 ASME Worcester Reed Warner Medal, and

was earlier recognized with the ASME Heat Transfer Memorial Award and the ASME Curriculum Innovation Award in 1999 (with S. Bhavnani and Y. Joshi), the ASME/IEEE IThERM Achievement Award in 1998, ASME Edwin F. Church Medal in 1994, and the THERMI Award from the IEEE/Semi-Therm Conference in 1997. He is a Fellow of ASME and of IEEE.

Karl Geisler is a Lead Mechanical Engineer at General Dynamics Advanced Information Systems in Bloomington, MN. Activities include product development, thermal packaging, and thermo mechanical reliability of terrestrial, airborne, and space electronics. He has taught Heat Transfer in Electronic Equipment at the University of Minnesota, Twin Cities. Geisler has co-authored 2 archival journal papers, 13 conference papers, and 4 book chapters related to thermal analysis and design of electronics and boiling heat transfer. He received the PhD degree in Mechanical Engineering from the University of Minnesota in February of 2007 and is a member of ASME and the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society.

**11. Three-Dimensional (3D)  
Hyper-integration and Packaging of  
Micro-Nano-Systems  
Course Leader: James Jian-Qiang Lu –  
Rensselaer Polytechnic Institute**

James Jian-Qiang Lu received his Dr. rer. nat. (Ph.D.) degree from Technical University of Munich in December 1995, and is currently an Associate Professor in Electrical Engineering at Rensselaer Polytechnic Institute (RPI), Troy, NY. At RPI, he worked with the Interconnect Focus Center (IFC) research program of 3D hyper-integration technology from 1999, and several other programs with focus on hyper-integration and micro-nano-bio interfaces for future chips. Prior to 1999, he held research and faculty positions at a number of universities in China, Germany and the United States. Dr. Lu has broad research experiences from micro-nano-electronics theory and design to materials, processing, devices, integration and packaging (e.g., GaAs, GaN and Si devices, novel FETs,

terahertz electronics, carbon-nanotubes, and Si IC interconnects). He has authored/co-authored more than 200 publications in refereed journals, conferences or books, and given a number of invited presentations, seminars and short courses. Dr. Lu also served as technical chair, workshop chair, session chair, panelist and panel moderator, and conference committee members for many conferences. He is a senior member of IEEE (CPMT & EDS), a member of APS, MRS, ECS, and a member of IMAPS National Technical Committee (Chair of 3D Packaging). He received the 2008 IEEE CPMT Exceptional Technical Achievement Award in May 2008 “for his pioneering contributions to and leadership in 3D integration/packaging”.

## ***12. Key Enabling Technologies for 3D IC Integration and WLP***

***Course Leader: John Lau – Industrial Technology Research Institute***

John Lau has been an ITRI Fellow of Industrial Technology Research Institute (ITRI) since January 2010. Prior to that, he was a visiting professor at HKUST for 1 year, the Director of Microsystems, Modules & Components Laboratory with IME for 2 years and a Senior Scientist/MTS at HP/Agilent in California, US for more than 25 years. With more than 30 years of R&D and manufacturing experience, he has authored or co-authored more than 300 peer-reviewed technical publications and more than 100 book chapters, and given more than 250 presentations. He has authored and co-authored 16 textbooks on advanced packaging, solder joint reliability, and lead-free soldering and manufacturing. John earned his Ph.D. degree in theoretical and applied mechanics (University of Illinois) and three M.S. degrees in structural engineering, engineering physics and management science in North America. He is an elected ASME Fellow and has been an IEEE Fellow since 1994.

## ***13. Polymers and Nano-Composites for Electronic and Photonic Packaging : Recent Advances***

**Course Leaders: C.P. Wong – Georgia Tech; Daniel Lu – Henkel Corporation**

Prof. C. P. Wong is a Regents' Professor and the Charles Smithgall Institute Endowed Chair at the School of Materials Science and Engineering at Georgia Institute of Technology (GT). He received his B.S. degree from Purdue University, and his Ph.D. degree (with Prof. Bill Horrocks) from the Pennsylvania State University. After his doctoral study, he was awarded a two-year postdoctoral fellowship with Nobel Laureate Professor Henry Taube at Stanford University. Prior to joining GT in 1996, he was with AT&T Bell Laboratories for many years and became an AT&T Bell Laboratories Fellow in 1992.

His research interests lie in the fields of polymeric electronic materials, electronic, photonic and MEMS packaging and interconnect, interfacial adhesions, nano-functional material syntheses and characterizations. nano-composites such as well-aligned carbon nanotubes, graphene, lead-free alloys, flip chip underfill, ultra high k capacitor composites and novel lotus effect coating materials.

He received many awards, among those, the AT&T Bell Labs Fellow Award in 1992, the IEEE CPMT Society Outstanding Sustained Technical Contributions Award in 1995, the IEEE Third Millennium Medal in 2000, the IEEE EAB Education Award in 2001, the IEEE CPMT Society Exceptional Technical Contributions Award in 2002, the Georgia Tech Class 1934 Distinguished Professor Award in 2004, named holder of the Charles Smithgall Chair (one of the two GT Institute Chairs) in 2005, the GT Outstanding PhD Thesis Advisor Award, the IEEE Components, Packaging and Manufacturing Technology Field Award in 2006, the Sigma Xi's Monie Ferst Award in 2007, the Society of Manufacturing Engineers' Total Excellence in Electronic Manufacturing Award in 2008 and the IEEE CPMT David Feldman Award in 2009.

He holds over 50 U.S. patents, and has published over 900 technical papers, co-authored and edited 10 books and is a member of the National Academy of Engineering since 2000.

Dr. Daniel Lu is the Technical Director of the R&D department of Electronics Materials Division of Henkel Corporation in Yantai, China. Daniel Lu received his MS and PhD degrees on Polymer Science and Engineering from Georgia Institute of Technology in 1996 and 2000, respectively. Prior to joining Henkel, Dr. Lu worked for the R&D department of Intel Corporation as a Sr. Scientist for 7 years. He also had worked for Lucent Technologies, Amoco's Electronics Materials Division, and the Electronics Materials Group of National Starch and Chemical Company before. Dr. Lu has extensive experience in electronic packaging materials and processing. Dr. Lu received many awards including IEEE/CPMT Outstanding Young Engineer Award in 2004, ECTC best poster paper in 2007, Intel's most patent filing in 2003-2007, Intel Divisional Recognition Awards in 2002, 2003, and 2007, Intel most patent granting of the year for 2006 and 2007, Best Graduate Student of the Year of Georgia Tech Packaging Research Center in 2000, and Best Paper of the Session of International Symposium and Exhibition on Advanced Packaging Materials in 2000. Dr. Lu published more than 40 technical papers, wrote chapters for four books, holds 52 US patents, and has more than 30 pending patent applications. Dr. Lu is a senior member of IEEE and an associate editor of IEEE Transactions on Advanced Packaging.

***14. Flip Chip Fabrication and Interconnection***  
***Course Leader: Eric Perfecto – IBM Corporation***

Eric Perfecto is a Senior Technical Staff Member at IBM, with 27 years of experience in the development of advanced packages at IBM Microelectronics. He holds an M.S. in Chemical Engineering from the University of Illinois and an M.S. in Operations Research from Union College.

Eric developed and implemented multi-level thin films on top of ceramic substrates for high end servers. He is currently responsible for the UBM and Pb-free solder selection, implementation and yield improvements at

IBM. His technical interests include chip joining, chip package interaction, electromigration, 3D, and design for manufacturing.

Eric has published over 50 external papers, including two best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds over 30 US patents, and has been honored with two IBM Outstanding Technical Achievement Awards.

Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. He has achieved senior member status from IEEE, IMAPS and Society of Plastic Engineers, and is a member of the Society of Hispanic Engineers. He is currently an elected member of the Board of Governors of the CPMT society of IEEE.

***15. Package Failure Analysis - Failure Mechanisms and Analytical Tools***  
***Course Leaders: Rajen Dias and Deepak Goyal – Intel Corporation***

Dr Rajen Dias graduated with a MS and Ph.D in Materials Science from Lehigh University and joined Intel in 1984. He is currently a Principal Engineer in the Assembly Technology Development Quality & Reliability Group. His main areas of responsibility are in understanding failure modes and mechanisms of new package technologies and in developing next generation analytical tools and techniques for the failure analysis. He is currently the Vice General Chair of ECTC and a member of IEEE

Deepak Goyal graduated (Ph.D in Materials Science) from State University of New York, Stony Brook in 1990 and joined Intel as Failure analysis engineer. He is currently the Manager of the Assembly Technology Development Quality and Reliability Labs at Intel. His group supports the reliability stressing, materials and failure analysis for the Assembly Technology Development at Intel and next generation of analytical and

reliability stress tools and techniques. He is a senior member of the IEEE

### ***16. Digital Memory Design for Packaging Engineers***

#### ***Course Leader: Moises Cases – The Cases Group, LLC***

Moises Cases has over 39 years of progressive experience in very-large scale integration (VLSI) chip and package designs, in system level electrical and package designs, and in complex project and people management. He retired as a Distinguished Engineer and Master Inventor from the IBM Corporation, System and Technology Group (STG). Mr. Cases was the team leader for system electrical design and integration of modular and blade servers, responsible for signal and power distribution integrity, and system level timings for complex multiple board system designs. Presently, Mr. Cases is the President and CEO of The Cases Group, LLC; a Texas Limited Liability Company dedicated to design and consulting services for electronic systems. He obtained his Master of Science in Computer Engineering from Syracuse University, NY in 1979, Master of Science in Electronic Engineering from New York University, NY in 1973, and a Bachelor of Science in Electrical Engineering from City College of New York, NY in 1969. He is a Fellow member of IEEE society and a member of Tau Beta Pi and Eta Kappa Nu honor societies.

Mr. Cases was awarded IEEE Fellow grade in 2008 for contributions to design and noise control for power and signal distribution in digital systems. He was the general co-chairman (representing the industry) of the IEEE Electrical Performance of Electronic Packaging (EPEP) workshop for 2005 through 2006, and he was the general chairman of the 1999 IEEE Systems Packaging Workshop. Moises is also an Associate Editor for IEEE CPMT Transactions on Advanced Packaging since 2002. He chaired the electromechanical working group (EWG) for the Infiniband Trade Association (IBTA) from 2003 to 2008. Mr. Cases has received the Hispanic in Technology Corporate Award from the Society of Hispanic Professional Engineers

(SHPE) in 2006, the Business/Community Representative of the Year Award from Austin Independent School District (AISD) in 2007, the Albert V. Baez Award from HENAAC in 2007, the Teacher-Engineer Partnership Award from IEEE in 2008, and the Outstanding Sustained Technical Contribution Award from IEEE and CPMT societies in 2009. He was elected to the IBM Academy of Technology in 2008 and he is presently a member emeritus of the Academy. He received numerous awards and recognitions over the 39 years of services with the IBM Corporation including 22 Invention Achievement Awards and 5 Outstanding Technical Achievement Awards in appreciation and recognition for creative contributions to IBM progress.