Professional Development Course Offerings for the 2012 Electronic Components and Technology Conference (ECTC)

1. LEAD-FREE SOLDER JOINT RELIABILITY - MATERIAL CONSIDERATION
Course Leader: Ning Cheng Lee – Indium Corporation

Course Objectives:

This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail, and novel alloys with reduced fragility will be presented. Electromigration, corrosion, and tin whisker growth will also be discussed. Furthermore, the reliability of through-hole solder joints will be reviewed, and recommendations will be provided, particularly for thick boards. The emphasis of this course is placed on the understanding of how the various factors contribute to the failure modes, and how to select proper solder alloys and surface finishes for achieving high reliability. Also presented are the desirable future alloys and fluxes in order to meet the challenge of miniaturization.

2. MULTI-PHYSICS MODELING IN IC PACKAGING AND MICROSYSTEMS
Course Leader: Xuejun Fan – Lamar University

Course Objectives:

Modeling and simulation has become indispensable to the development of new technologies and reliability evaluations in microelectronics packaging and microsystems. This course aims to give a state-of-the-art and in-depth coverage of the advances and applications in a broad range of modeling and simulation in IC packaging and microsystems: 1) diffusion type modeling, including heat conduction, moisture diffusion, chemical etching process, static electrical current flow, and mass diffusion in electromigration; 2) coupled and integrated multi-physics modeling techniques in temperature/humidity (such as reflow process and HAST condition), and thermal-electrical-mechanical and mass diffusion in electromigration. 3) fracture mechanics and delamination modeling including damage mechanics approach; 4) fatigue/creep modeling with various creep model options; and 5) dynamic modeling under drop/impact loading at component and system levels. The physics of modeling, the fundamental principles, and mathematical formulations are discussed, with the numerical implementation techniques using commercial finite element analysis code. Numerous practical skills and approaches for performing multi-physics modeling, non-linear modeling, dynamic modeling, and fracture mechanics modeling will be described. The course uses many real case studies to demonstrate the applications of modeling together with experimental validations.

3. WAFER LEVEL CHIP SCALE PACKAGING (WL-CSP)
Course Leader: Luu Nguyen – Texas Instruments

Course Objectives:

Wafer Level Chip Scale Packaging (WL-CSP) has gained so much success as a packaging form factor in the consumer arena in the past few years that it is almost considered as a technology commodity. It has been driven by needs for cost reduction, size shrinkage, and enhanced performance. This course will provide an overview of the WL-CSP technology. The market drivers, benefits, and challenges facing industry-wide adoption will be discussed. The current WL-CSP configurations will be reviewed in terms of their construction, manufacturing process, and published electrical and thermal performance, together with package and board level reliability. Since the technology marks the convergence of fab, assembly, and test, the course will also address some fundamental issues such as: 1. Does it fit best with front-end or back-end processing? 2. Will it be applicable and cost effective for memory and other complex devices such as ASICs and microprocessors? 3. Are the current standards for design rules, outline, and reliability applicable? 4. What is the impact of extensions to higher pin count packages (>100) and other arenas such as RF, imaging, sensors, and MEMS will be reviewed.

4. 3D INTEGRATION: ALTERNATIVE TO CONTINUED SCALING

Course Leader: Philip Garrou – Microelectronic Consultants of NC

Course Objectives:

This course is based on the authors activity in 3D integration over the past 7 years with leading companies in the industry, his weekly 3D blog insights From the Leading Edge in Solid State Technology, the 2 volume Wiley-VCH book "Handbook of 3D IC Integration: Technology and Applications of 3D IC Circuits" which the author authored and edited and the authors articles in Yokes i-Micronews entitled "A Closer Look". The course will begin by defining and contrasting 3D Integration (thinning, bonding and TSV) to 3D packaging (thinning stacking and wire bonding to the BGA base). The various drivers for 3D integration including the electrical performance and economic issues will be examined. We will examine the various process sequences being proposed for 3D integration and the process unit operations necessary to fabricate a 3D stack. The processes sequences proposed by IDMs, Universities, and Institutes will be compared and contrasted. We will look at the first products going commercial in 2012. We will then examine the applications being commercialized by early and later adopters and the evolving infrastructure that will be necessary to accomplish this. The course examines the current state of 3D design and test and will end by looking the remaining technical and market barriers.

5. POLYMERS/NANO-COMPOSITES – ELECTRONIC & PHOTONIC PACKAGING RECENT ADVANCES

Course Leaders: C.P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation

Course Objectives:

Polymers and nanocomposites are widely used in electronic and photonic packaging as adhesives, encapsulants, insulators, dielectrics, molding compounds and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high performance novel No Flow Underfills, Reworkable Underfills for Ball Grid Array (BGA), Chip Scale Packaging (CSP), System in a Package (SIP), Direct Chip Attach (DCA), Flip-Chip (FC), Paper-thin IC and 3D Packaging, Conductive Adhesives (both ICA and ACA), Embedded Passives (high K polymer composites), nano particles and nanofunctional materials such as CNTs, graphenes. It is imperative that both material suppliers, formulators and their users have a thorough understanding of polymeric materials and the recent advances on nano materials and their importance in the advances of the electronic packaging and interconnect technologies.

6. Analog and Power Electronics Packaging

Course Leader: Yong Liu – Fairchild Semiconductor Corporation

Course Objectives:

Analog and power electronic packaging are the fastest growing segments and wide applications in the electronic industry due to the rapid advances in integrated circuit (IC) fabrication and the demands of a growing market in almost all areas of electronic application such as consumer electronics, home electronics, computing electronics, automotive, railway and high/ power industry. However, due to the intrinsic structural nature, the requirement for analog and power product and its reliability is extremely high. This course will present a state-of-art and in-depth overview of recent advances in analog and power electronic packaging. A review of recent advances in analog and power electronic packaging and modeling is presented based on the development of analog IC and power device integration. The short course will cover in more detail how advances in both semiconductor analog and power advanced package design and materials have co-enabled significant advances in analog and power device capability during recent years. Along with new packaging development, the role of modeling is a key to assure successful package design. An overview of the analog and power package modeling is also presented. Challenges of analog and power semiconductor packaging in both next generation design and modeling are presented and discussed.

7. FUNDAMENTAL CONCEPTS IN RELIABILITY & MECHANICS OF ELECTRONIC PACKAGING

Course Leaders: Shubhada Sahasrabudhe & Sandeep Sane – Intel Corporation

Course Objectives:

The objective of this course is to provide an overview of the fundamentals of mechanics and reliability and how they can be integrated to perform knowledge-based package risk assessment. This is a methodology that uses the knowledge of the field environment and empirical models to perform quality and reliability assessment and leverages mechanics to proactively assess the impact of geometry and material choices. The course will start with the introduction of the key elements of reliability assessment like Use Conditions, accelerated/life tests, methods of statistical data analysis, acceleration factor models for different failure mechanisms, use of statistics to project rel performance at UC. It will also highlight the main components of mechanics like stress-strain curves, characterization of material behavior, stress analysis methods and fundamentals of fracture mechanics. The course will then introduce the methodology for using mechanics for effective reliability assessment. The concepts of design for reliability and experiment planning supporting the methodology will be discussed. Comprehensive case studies highlighting different package risk areas will be introduced to showcase the application of methodology to real examples. In class reliability statistics/mechanics-based assessment exercises will help students practice skills. Target Audience: Engineers working on packaging, reliability, and materials.

8. METHODS FOR EFFICIENT HIGH-FREQUENCY MODELING AND OPTIMIZATION OF INTERCONNECTIONS IN ELECTRONIC PACKAGING

Course Leaders: Ivan Ndip -- Fraunhofer IZM; Michael Toepper -- Fraunhofer IZM

Course Objectives:

Novel electronic packages and system-integration concepts are continuously being developed to meet the ever-increasing demand for low-cost and high-performance systems. To ensure high-speed signal transmission, all interconnections in these packages must be capable of supporting broadband signals without degrading signal integrity beyond acceptable limits. Furthermore, the choice of the right packaging material for interposers/boards plays a crucial role in the cost and performance of the entire system. The objective of this course is to provide and illustrate methods for efficient high-frequency modeling and optimization of interconnections in electronic packaging, considering signal integrity and electromagnetic interference effects in different packaging materials.

9. PACKAGE FAILURE ANALYSIS - FAILURE ANALYSIS AND ANALYTICAL TOOLS

Course Leader: Rajen Dias – Intel Corp.; Deepak Goyal – Intel Corp.

Course Objectives:

The technical course will provide an overview of the failure modes and mechanisms observed in the plastic packages. A brief introduction to the methodology of failure analysis of these packages will be described. Emphasis will be paid to the tools and techniques currently used and the future direction for the tools and techniques required for successful and timely failure analysis of next generation package technologies. A discussion on the strategies for use of these techniques and a flow chart for failure analysis will be included.

10. NEAR JUNCTION REMEDIATION OF ON-CHIP HOT SPOTS

Course Leaders: Avram Bar-Cohen – University of Maryland; Karl Geisler – General Dynamics Advanced Information Systems

Course Objectives:

The continued miniaturization of high performance solid-state electronics, the emergence of 3D packaging and chip stack technology, and the maturation of wide band gap microwave devices have made near-junction thermal transport a requisite part of any successful thermal packaging strategy. While conventional, remote cooling techniques are incapable of targeting the often-dominant, on-chip temperature rise, high-conductivity substrates, microfluidics, and thermoelectric techniques can be used to suppress the generation of on-chip hot spots. However, successful implementation of near-junction techniques requires the integration of thermal management principles and concepts into the design and development process from the earliest stages of product design. The characterization and remediation of near-junction temperature spikes is the focus of this proposed Professional Development Course. Following a brief review of the silicon and compound semiconductor roadmaps and conventional thermal packaging technology, first-order relations for the analytic prediction of on-chip temperature distributions for logic and power components on silicon will be presented. Attention will then turn to the cooling potential and issues encountered in the use of high thermal conductivity SiC and diamond substrates; miniaturized, thin film, and self-cooling solid state thermoelectric coolers; and liquid as well as evaporative microfluidic cooling.

11. TECHNOLOGY ADVANCES IN 3D-TSV INTEGRATION AND PACKAGING OF MICRO-NANO-SYSTEMS

Course Leader: James J.Q. Lu – Rensselaer Polytechnic Institute

Course Objectives:

Based on the instructor's 3D research activities since late 1990s, this course will discuss the latest development of Through-Strata-Vias (or Through-Si-Vias, TSVs) and other relevant enabling technologies for 3D IC integration and packaging. A comprehensive overview of 3D integration and packaging technologies will be presented, including motivation, key technologies, technology assessment and status towards commercialization. In this course, 3D hyper-integration technologies are divided into 4 categories: 3D packaging, chip-to-wafer (C2W) assembly, transistor build-up, and wafer-to-wafer (W2W) 3D. For 3D packaging, the ICs are packaged vertically in chip-to-chip (C2C), system-in-packaging (SiP) and package-on-package (PoP) fashions. The C2W assembly is similar to SoC approach, but with known-good-dies (KGDs) assembled on an IC wafer, then processed in wafer-level. In transistor build-up 3D, active devices are built-up over an IC wafer. In W2W 3D, different systems are first fabricated independently and then stacked and interconnected vertically. This course will discuss all these technologies, with emphasis on advances of Through-Strata-Vias (TSVs) technologies, 3D platforms and potential applications. A particular focus will be on various TSV fabrication/processing methods and applications, with relevant critical issues addressed, such as TSV processing, alignment, bonding, wafer thinning and handling for C2C, C2W and W2W integration platforms. Sample designs and applications towards commercialization will also be presented. The issues associated with each technology category will be discussed, including integration architecture and design tools, yield and cost, thermal and mechanical constraints, and manufacturing infrastructure. Finally, future directions into micro/nano/electro-opto/bio system hyper-integrations including MEMS will be presented, showing 3D-TSV hyperintegration as a very promising emerging architecture for future computer, network, nanotech, and biotech applications.

12. *3D IC PACKAGING & INTEGRATION AND 3D SI INTEGRATION*

Course Leader: John Lau – Industrial Technology Research Institute

Course Objectives:

3D integration consists of 3D IC packaging, 3D IC integration, and 3D Si integration, which will be discussed. Emphases are placed on the key enabling technologies for 3D IC/Si integrations, such as TSV forming, filling, and CMP, front and back-side metallization, RDL, IPD, temporary bonding and de-bonding, wafer thinning and handling, thin chip/wafer strength measurement and improving, W2W bumpless bonding, lead-free microbumping (d15µm pitch) and assembly, low-temperature wafer bumping and C2C and C2W bonding, and thermal management. Useful characterization and reliability data for 3D IC integration will also be provided. The application of 3D IC integration such as CMOS image sensor, MEMS, LED, memory/logic + logic/microprocessor, active and passive interposers will be presented. More than 15 companies - passive interposes (samples) used as substrates, carriers, stress relief (reliability) buffer, and thermal management tools will be discussed. Furthermore, the critical issues of TSV and 3D integration will be given and some potential solutions or research topics will be recommended. Finally, TSV manufacturing yield and hidden costs will be discussed and several roadmaps of 3D IC/Si integration will be provided. All the materials are based on the technical papers and books published within the past 3 years by the lecturer and others.

13. POLYMERS IN ELECTRONIC PACKAGING

Course Leader: Jeffrey Gotro – InnoCentrix, LLC

Course Objectives:

The course will provide a broad overview of polymers used in semiconductor packaging and the important structure-property-process-performance relationships. We will cover in more depth the chemistries, material properties, and process considerations for adhesives, underfills, coatings and mold compounds. Additionally, we will provide an introduction to common thermal analysis methods (DSC, DMA, TMA, and TGA) used to characterize thermosetting polymers used in semiconductor packaging. Finally, the course will provide an introduction to the rheological performance of polymer-based materials used in packaging semiconductors. In most cases, adhesives, underfills, mold compounds and coatings are applied as a viscous liquid and then cured. The flow properties of these materials are critical to performance in high volume manufacturing. The course will provide an introduction to rheology measurements and examples of rheology issues in semiconductor packaging.

14. FLIP CHIP TECHNOLOGY

Course Leader: Eric Perfecto – IBM Corporation

Course Objectives:

This course will cover all aspects of the flip chip technology. It will detail and compare the various UBM (electroplating, electroless plating and sputtering) and solder (electroplating, ball drop, C4NP, and solder screening) depositions methods, which are used in traditional single chip modules, chip scale packages and 3D applications. It will include process considerations when joining to laminate, ceramic and Si substrates. This course will cover the accelerated reliability tests currently used to qualify the flip chip connections, the failure types and the analytical tools used to identify defect root cause. Finally, it will cover the issues and solutions associated with Pb-free solder implementation, such as barrier consumption, Kirkendall void formation, BEOL dielectric cracking, electromigration, etc. The students are encouraged to bring failed samples analysis for group discussion on root cause.

15. DESIGN FOR PACKAGE RELIABILITY

Course Leaders: Darcin Edwards – Texas International; Yauyu Pang – Texas Instruments

Course Objectives:

This class will highlight the need to design packages up front for highly reliable field performance. It will cover the types of co-design which can make the difference between devices which are successful and those which fail. Major emphasis will be given to the use of modeling to characterize assemblies from the pre-design stage through final system design. These models should include Electrical, Thermal, and Thermomechanical analysis. Models are only as good as the inputs to those models, so a description of the required inputs and methods to characterize the materials properties will be described. Some interactions are best addressed by up-front test die validation. A description of typical electrical, thermal, and thermomechanical test structures will be provided along with guidelines for getting the most from these devices. The influence of shadow moiré testing on determining the accuracy of thermomechanical models will be addressed. Since a majority of field failures result from thermomechanical effects, particular emphasis will be placed on validating thermomechanical models for reliability prediction. Methods for characterizing the adhesion of interfaces and the relationship of the measured results to modeled values will be highlighted. New findings for Pb-free solders will be presented, including aging effects and the rarely considered collapse of solders which can occur when a device is placed under a heat sink load.

16. IC PACKAGE DESIGN SIGNAL & POWER INTEGRITY & EMC

Course Leader: Sam Karikalin – Broadcom Corp.

Course Objectives:

This course will teach the fundamentals of IC Package Electrical Performance metrics such as Signal Integrity, Power Integrity and Electromagnetic Compatibility and how to apply that knowledge to an advanced IC Package design. Conceptual discussions on the basic principles of Interconnect Electromagnetics, such as RLC Parasitics, Transmission Line behavior, and the associated common design challenges such as Signal Reflections, Crosstalk, Simultaneous Switching Noise and Power Delivery Network Resonances will be made at a level that is understandable to common Package

Design engineers. Relationship between these common Signal Integrity and Power Integrity design issues and system level Electromagnetic Compatibility will be introduced, besides the other component level causes for inter-system and intra-system EMC issues. Areas of electrical performance concern in typical wafer level, flip chip and wire bonded packages on laminate / build-up substrates will be discussed and generic electrical design guidelines will be provided.