Integration Embraces Packaging

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Innovation & More Innovations
Smaller, Faster, Cheaper, Less Power

1900  20th Century  2000

For Controlled Release at the ECTC2014 Conference on Component Technology
The Legacy of the Miniaturization Will Continue

Data Warehouse 2014

Power of System Integration in a Package

Data Warehouse 20xx

Indiana University Data Center, Bloomington, Indiana
PCB Trends

System Integration in a Package

- 2.5D/3D
- SiP
- Stacked PoP/PiP
- MCM

Timeline:

- 1950
- 1970
- 1980
- 1990
- 2000
- >2010
Electronic Circuits

2.5D/3D, MCM, PoP, MCP

Microprocessor
DSP
Application-Processors
Graphic Unit Processor
Micro Controller

SiP

Data Gathering
Data Sensing
Data Distributions (Audio, Video, Data)
Power, Power Harvesting, Power Management
Antenna/Switch/Filters Frontend, MEMS, etc.

Interconnection with Software Layers and Security Protocols

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Multichip Module (MCM)

- MCM increases system performance resulting from decreasing the length of wiring needed to provide interconnection between two IC devices
  - Lower parasitic and shorter lines than PCB board
- High end applications:
  - High end networking, gaming & computing
  - Military and aerospace applications
- Low volume with high price tag except for gaming
- Not well suited for consumer products
Multichip Package (MCP)

- Simpler version of MCM
- Lower cost, 2-12 bare die without passives
- Tighter substrate design rules
- Size reduction advantage
- Mature technology with solid infrastructure
- Different packaging structures
  - Stacked die, Package-on-Package (PoP), Package-in-Package (PiP), F2F
  - Flip chip and wirebond
System Level Packaging (SiP)

- Packaging solution for system or sub-system integration
- Extend Moore’s law
- SiP does not compete with SoC
- Emphasis on functional integration
  - Noise reduction, power reduction
  - Controlling EMI radiation
  - System miniaturizations
    - X, Y, Z dimensions
- Comes in different packaging solutions
  - 2.5D/3D, SiP, SiP-in-SiP, SiP-in-PoP, etc.
- System Level Packaging/ System Integrated Packaging
  - CMOS, GaAs, digital, analog, RF, passives components, crystal, MEMS, antenna, shielding, embedded substrates, etc.
Miniaturization: Passive Components

Printed on Substrate
Integrated Passive Devices
Embedded Passives Substrate
Package Shielding for Wireless System

Package Level Shielding

Traditional System Level Shielding
Design Methodology

- Reusable Design
- Design for Cost
- Design for Test and Design for Manufacturability
- Design for Performance Electrical, Thermal & Mechanical
- Size (X,Y,Z) Reductions
- System Evaluation
Module Electrical Design

- Computing, networking and graphic modules are based on high performance “SoC” and high speed & high bandwidth memory such as DDR3 & DDR4
- Module success depend on its superb electrical performances with its targeted system
  - Signal speed and bandwidth (Terabit)
  - Low power and low noise requirement
  - Meeting end system signaling protocols
Current & Voltage Distribution Map
(layer by layer)

Voltage

Current

3D View of Voltage Fluctuations
EMI Map (layer by layer)
Thermal Map (layer by layer)

Package Isotherms
System Integration Constraints

- Component and functional placements
- Component size, thickness, orientation, etc.
- Supply chain restrictions
- Noise and power budgets
- EMI radiation and susceptibility
- Manufacturability
- KGD availability
- Testability
- Cost and cost reduction
- Thermal performance
- Mechanical stability
Thank You

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