APX (Advanced Package X)
- Advanced Organic Technology for 2.5D Interposer
Agenda / Outline / Overview

- Benefits of 2.5D APX Interposer
- Technology Feature of APX
- Cross Section
- Design Rule Comparison
- Material Property
- Design Rule for Impedance Control
- Electrical Performance Study
- Routing Capability/Study
- Reliability Test Status
- Surface Finish Experience
- Technology Roadmap
Benefits of 2.5D APX Interposer

- Fine pitch wiring and Small Size Via to support 2.5D interposer
- Plane pattern can be applied to POWER supply for lower IR Drop
- Z0 matching of Line, Via. and TH to 50Ω
- Smaller Signal transmission loss vs Silicon Interposer
- APX CTE is around 10ppm to strike a balance between 1st and 2nd assembly
- High stiffness by using high Young Modulus and Low CTE core for easy handling and assembly
- Open/short test can be done before APX is shipped
- Lower Cost potential vs Silicon Interposer or Glass interposer
Technology Feature of APX

- **Fine Line/Space**
  - Min. Line Width: 6um
  - Min. Space: 6um

- **Small Build Up VIA**
  - Via Hole dia.: 20um
  - Via Land dia.: 32um
  - 3 Stack

- **Micro bump pitch**
  - Min. 40um (experienced)
  - Min. 50um (a line escape between vias)

- **Fine Line/Space on Core (FC1/BC1)**
  - Min. Line Width: 20um
  - Min. Space: 20um

- **Advanced Build-up Material**
  - Ultra-Thin: 8um
  - Low Loss Tangent: 0.0066

- **Low CTE Organic Interposer**
  - 10~11 ppm (total)

- **Max. Stack Up:** 5-2-5

- **Fine Pitch PTH**
  - Pitch: 110um
  - Hole dia.: 60um
  - Land dia.: 80um

- **Ultra-Thin:** 8um
- **Low Loss Tangent:** 0.0066
Cross Section of APX 5-2-5 Structure

FINISHED CARRIER CROSS SECTION
## Design rule Comparison

<table>
<thead>
<tr>
<th></th>
<th>ABF Build Up (most advanced)</th>
<th>APX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. Line Width (um)</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>Min. Space (um)</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>Via Hole Diameter (um)</td>
<td>65</td>
<td>20</td>
</tr>
<tr>
<td>Via Land Diameter (um)</td>
<td>85</td>
<td>32</td>
</tr>
<tr>
<td>Max. number of Via Stack</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td>Build up Layer Thickness (um)</td>
<td>30</td>
<td>8</td>
</tr>
<tr>
<td>(2\textsuperscript{nd} or above B/U Layer)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. build up layer</td>
<td>11</td>
<td>5</td>
</tr>
<tr>
<td>Max. Layer Count</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>(11-2-11)</td>
<td>(5-2-5)</td>
</tr>
<tr>
<td>PTH Pitch (um)</td>
<td>150</td>
<td>110</td>
</tr>
</tbody>
</table>

Cross section for 6 µm Line / 6 µm Space
## Material property

<table>
<thead>
<tr>
<th>Item</th>
<th>ABF</th>
<th>APX</th>
<th>Core (Supplier's Catalogue Value)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GX-13</td>
<td>GZ-41</td>
<td>Build Up (ZS-100) (Measured by KST with 10umt film)</td>
</tr>
<tr>
<td></td>
<td>Build Up (ZS-100) (Measured by KST with 10umt film)</td>
<td>Build Up (ZS-100) (Measured by KST with 10umt film)</td>
<td>Build Up (ZS-100) (Measured by KST with 10umt film)</td>
</tr>
<tr>
<td>Loss tangent</td>
<td>0.016/0.012 (1MHz/1GHz)</td>
<td>0.0057/0.0058 (1MHz/1GHz)</td>
<td>0.0063/0.0066 (2.8GHz/10GHz)</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>3.6/3.35 (1MHz/1GHz)</td>
<td>3.4/3.3 (1MHz/1GHz)</td>
<td>3.1 / 3.1 (2.8GHz/10GHz)</td>
</tr>
<tr>
<td>CTE x-y</td>
<td>TMA 46 (25-150degC)</td>
<td>TMA 20 (25-150degC)</td>
<td>TMA 28 (30-100degC)</td>
</tr>
<tr>
<td>CTE z</td>
<td>TMA 47 (25-150degC)</td>
<td>TMA 20 (25-150degC)</td>
<td>TMA 28 (30-100degC)</td>
</tr>
<tr>
<td>Tg</td>
<td>TMA 156</td>
<td>TMA 171</td>
<td>TMA 150</td>
</tr>
<tr>
<td>Young's Modulus</td>
<td>Gpa 4.0</td>
<td>Gpa 9.0</td>
<td>Gpa 6.4-7.3</td>
</tr>
</tbody>
</table>
Design Rule for Impedance Control by APX

**Micro strip line**

<table>
<thead>
<tr>
<th>Single end</th>
<th>Differential pair</th>
</tr>
</thead>
<tbody>
<tr>
<td>LW = 16.5um, Z0 = 50 ohm</td>
<td>SP = 30.5um, Zdiff = 100 ohm</td>
</tr>
</tbody>
</table>

**Strip line**

<table>
<thead>
<tr>
<th>Single end</th>
<th>Differential pair</th>
</tr>
</thead>
<tbody>
<tr>
<td>LW = 7.5um, Z0 = 50 ohm</td>
<td>SP = 14.5um, Zdiff = 100 ohm</td>
</tr>
</tbody>
</table>

**Strip line**

<table>
<thead>
<tr>
<th>Single end</th>
<th>Differential pair</th>
</tr>
</thead>
<tbody>
<tr>
<td>LW = 10um, SP = 19.5um, Z0 = 50 ohm</td>
<td>LW = 9um, SP1 = 21um, SP2 = 16um, Zdiff = 100 ohm</td>
</tr>
</tbody>
</table>
Electrical Performance Study

Loop Inductance Comparison

Current Build Up

APX

Cross Talk Noise Comparison

Current Build Up

APX

Loop Inductance Simulation Result

Cross talk noise Simulation Result
APX Routing Capability Study for 2.5D Package

120µm pitch FCA
- TSV (15µm)
- FV2 (15µm)
- FV3 (15µm)
- Wiring between Pads:
  - 6 Line between vias
  - Pad dia. 32µm
  - L / S = 6µm / 6µm

50µm pitch FCA (WB-DRAM)
- Via structure (4-2-4, 5-2-5)
- TSV (8µm)
- FV4 (8µm)
- FV3 (8µm)
- FV2 (8µm)
- Wiring between Pads:
  - 1 Line between pads
  - Pad dia. 32µm
  - L / S = 6µm / 6µm
  - 50µm

55µm pitch FCA (HBM)
- Via structure (5-2-5)
- TSV (8µm)
- FV4 (8µm)
- FV3 (8µm)
- FV2 (8µm)
- Wiring between Pads:
  - 1 Line between pads
  - Pad dia. 32µm
  - L / S = 6µm / 6.5µm
  - 55µm
HBM Ballout Map

HBM Overall

I/O Signal Region (24 rows)

Power Supply Region

TEST PORT

I/O Signal Region

HBM Overall

I/O Signal Region

TEST PORT

Power Supply Region - Channels [No. 1st]

Power Supply Region - Channels [No. 2nd]

Depopulated Microbump "NO BUMP" Area 5u eqivalent pitch

MICROSTACK

TEST PORT [DIRECT ACCESS]

TEST PORT [DIRECT ACCESS]

18 channels +MIDSTACK (220 columns)

96um

55um

25um (MicroBump Diameter)

96um

55um

25um (MicroBump Diameter)

VPP

NC

VSS

VDAC

RSVD

DA

DFU, ARFU, MR FU

Test

Temp

RESET

VDDQ

The New Value Diameter

SoC
Signal Fan-out Design Study from HBM

Top (FCA PAD)
- FC5 (Power)
- FC4 (Signal)
- FC3 (GND)
- FC2 (Signal)
- FC1 (Power)

CORE
- BC1 (Power)
- BC2 (Signal)
- BC3 (GND)
- BC4 (Signal)
- BC5 (Power)

BOTTOM (BGA PAD)

PTH

PTH

Signals (24) Signals (24) Signals (24) Signals (24)

330um
Signal Fan-out Design Study Result

All Signals can be fan-out!
Reliability Test Status

Substrate Level Reliability Test Status

Test Vehicle
1. 3 Stacked VIA Chain
2. 6um(Line width / 6um Line-to-Line-Space
3. 6um Line-to VIA_Land Space

Qualification Test Status
WTC (-65/150degC; 400cycles) Passed
DTC (-55/125degC; 1000cycles) Passed
HAST(130degC,85%,3.7V; 288hrs) Passed
THB (85degC,85%,5V; 1000hrs) under Testing

Module Level Reliability Test Status

Test Vehicle
1. Dummy Chip Attached / No FCA Joint on 3 Stacked VIA Chain

Qualification Test Status
WTC (-65/150degC; 400cycles) Passed
DTC (-55/125degC; 1000cycles) Passed
## Surface Finish Experience

<table>
<thead>
<tr>
<th></th>
<th>OSP</th>
<th>NiAu, NiPdAu</th>
<th>SAC (Solder)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad Pitch</td>
<td>&gt; 40um</td>
<td>&gt; 50um</td>
<td>&gt; 150um</td>
</tr>
<tr>
<td>Pad-Pad Space</td>
<td>&gt; 8um</td>
<td>&gt; 18um</td>
<td></td>
</tr>
</tbody>
</table>

![Glicoat-SMD F2(PK) Entek Cu56](reference picture)

*Reference picture*
## APX Technology Roadmap

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Substrate</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTE (ppm)</td>
<td>~3Q</td>
<td>4Q~</td>
<td>10-11</td>
<td>10-11</td>
<td>10-11</td>
</tr>
<tr>
<td><strong>Size (mm)</strong></td>
<td>&lt;93(12/12)</td>
<td>&lt;70(10/10)</td>
<td>&lt;93(12/12)</td>
<td>&lt;70(10/10)</td>
<td>&lt;93(12/12)</td>
</tr>
<tr>
<td>Depend on Build up L/S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Depend on Equipment</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core Layer</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Min Line/ Space (um)</td>
<td>20/20</td>
<td>20/20</td>
<td>20/20</td>
<td>20/20</td>
<td>15/15</td>
</tr>
<tr>
<td>Core Thickness (um)</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>150 or 200</td>
</tr>
<tr>
<td>PTH Hole (um)</td>
<td>&gt;50</td>
<td>&gt;50</td>
<td>&gt;50</td>
<td>T.B.D.</td>
<td>T.B.D.</td>
</tr>
<tr>
<td>PTH Pitch (um)</td>
<td>&gt;150</td>
<td>&gt;110</td>
<td>&gt;100</td>
<td>&gt;100</td>
<td>&gt;80</td>
</tr>
<tr>
<td>PTH Land (um)</td>
<td>80</td>
<td>80</td>
<td>80</td>
<td>80</td>
<td>65</td>
</tr>
<tr>
<td>Build Up</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Build up Material</td>
<td>Polymide</td>
<td>Epoxy</td>
<td>Epoxy</td>
<td>T.B.D.</td>
<td>T.B.D.</td>
</tr>
<tr>
<td>Number of Build up Layer</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Min. Line/ Space (um)</td>
<td>10/10</td>
<td>6/6</td>
<td>5/5</td>
<td>3/3</td>
<td>3/3</td>
</tr>
<tr>
<td>Conformal V1 via</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hole (um)</td>
<td>40/38</td>
<td>40/38</td>
<td>33</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Land (um)</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>Filled Vn via</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hole (um)</td>
<td>20</td>
<td>20</td>
<td>15</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>Land (um)</td>
<td>32</td>
<td>32</td>
<td>25</td>
<td>25</td>
<td>22</td>
</tr>
<tr>
<td>Number of Via stack</td>
<td>0</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

Update: May 2014
The New Value Frontier

KYOCERA

京セラSLCテクノロジー株式会社