Prospect for the memory Packaging technology

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Agenda

1. Electronic Packaging Trend
2. Memory Packaging Roadmap
3. Innovative Packaging Technology
   - Package
   - Process
   - Material
4. Conclusion
Packaging technology is developing to compensate the technology gap between Si and PCB tech.

- Bridging the gap between Si and PCB process capabilities
  - High I/O & speed: PGA → FBGA → Flip Chip → WLP/TSV

- Improvement by the high functionality of IT application
  - High Density & Functionality, High thermal dissipation.
Flip chip and TSV/WLCSP are promising technologies to satisfy faster speed, wider bandwidth and smaller/thinner package

<table>
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<th>Past</th>
<th>Present</th>
<th>Near Future</th>
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<td>PC/Notebook</td>
<td>Smart Phone/Tablet PC /Smart Device</td>
<td>IoT (Wearable Device, Smart Car, Smart Home and so on)</td>
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### Memory Packaging Roadmap

#### Device Market

- **PC/Notebook**
- **Smart Phone/Tablet PC /Smart Device**
- **IoT (Wearable Device, Smart Car, Smart Home and so on)**
- **Cloud(Big Data)**

#### Memory Package

- **DRAM**
  - Past: BOC, TSOP, RDL DDP/QDP, Flip Chip
  - Present: TSV, 2.5D SiP***
  - Near Future: 3D SiP, Optical Interconnection
- **NAND Flash**
  - Past: TSOP, eMCP
  - Present: eMMC (with Controller), UFS, SSD
  - Near Future: BGA SSD, NAND TSV

*EMI: Electro Magnetic Interference
**FOWLP: Fan-out Wafer Level Package
***SiP: System in Package
① Package Stack

AP & Memory package stack is widely being used.

PoP (Package on Package)

- Mobile Application: AP + Memory
- Top/Bottom PKG Warpage Control
② Chip Stack (Planar)

Planar chip stack is driven by low cost and high density requirement
2.5D SiP is a suitable solution to place memory dies near SoC

**Planar Stack Package**

- BOC/Flip chip planar DDP(Dual Die Package)
- Pinwheel package
  - Thin Profile
  - Improve Signal Integrity

**2.5D SiP**

- SoC + 2/4/8 HBMs(High Bandwidth Memory) on interposer
- Various structures: CoCoS, CoWoS (TSMC), EMIB (Intel)

Source: AMD

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Innovative Packaging Technology - Package
② Chip Stack (Vertical)

Conventional chip stack using wiring and TSV chip stack are implemented

**Wire Interconnection**
- MCP (Multi Chip Package)
- UFS (Universal Flash Storage)
- CoC (Chip on Chip)

**TSV Interconnection**
- 3DS
- HBM (High Bandwidth Memory)
③ Fan out package

FOWLP is a promising solution, but cost reduction is needed.

Innovative Packaging Technology - Package

Market Driver for Fan-out

Fan-out Packaging for SiP

- PoP Bottom Package with Logic (Mobile AP)
  - TSMC InFO¹
  - Amkor SLIM² & SWIFT³
  - SPIL SLIT⁴

*Source: http://giglehd.com/zbxe/14078384

¹InFO (Integrated Fan Out Wafer Level PKG), ²SLIM (siliconless integrated module), ³SWIFT (Silicon Wafer Integrated Fan-out Tech.), ⁴SLIT (Silicon-less Interconnect Tech.)
③ Fan out package

FOWLP is a promising solution, but cost reduction is needed.

Cost Reduction Challenges for FOWLP

- High Packaging Cost
- Cost Reduction by Panel Level Packaging

Hurdle of FOPLP

- Yield
  - Warpage Control
  - Die Bonding Accuracy
  - Panel Handling
- Infra Investment
SK hynix is leading new and advanced memory package development against diverse and rapidly changing circumstances of semiconductor industry.
Thanks for Your Time