

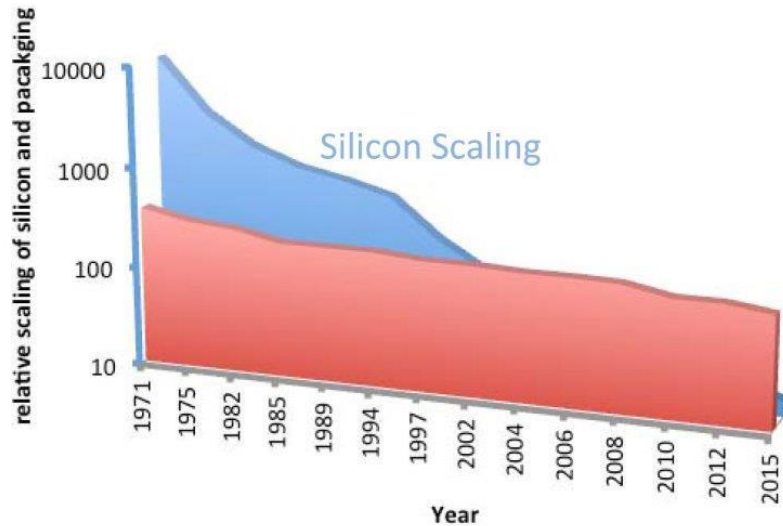
# Panel Fan-Out Manufacturing: Why, When, and How?



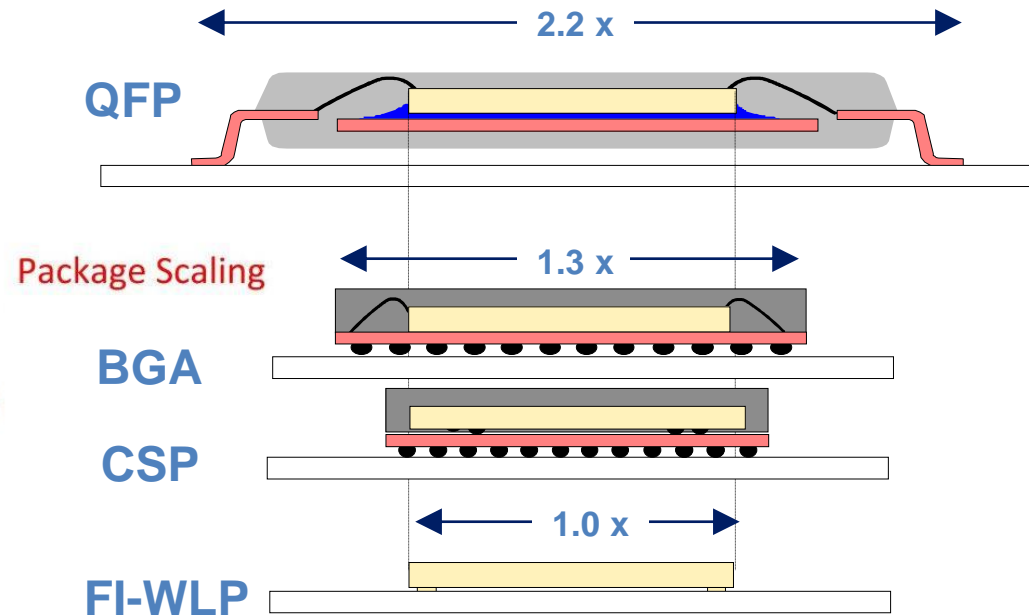
**Rolf Aschenbrenner**  
**Deputy Director**  
**Fraunhofer IZM, Berlin**

# Panel Level Packaging is not a geometrical extension

## Silicon Scaling $\neq$ Package Scaling



S. Iyer (UCLA), IEEE Trans CPMT 2016



Smallest SCP!!  Die = Package

***Solution for SiP???? – Focus on system-level-scaling***

# Heterogeneous integration for SiP using *Embedding*

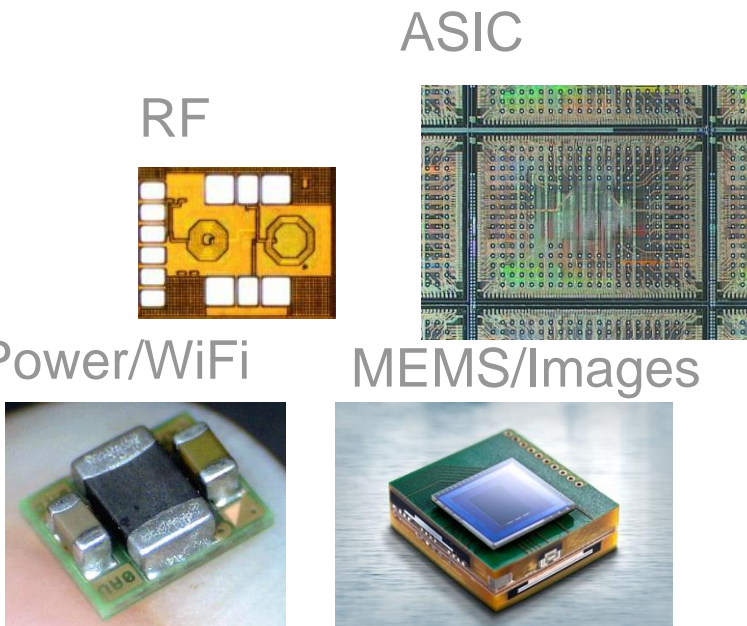
I/O Count

high

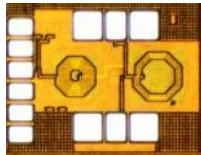


medium

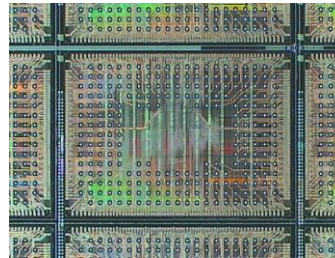
small



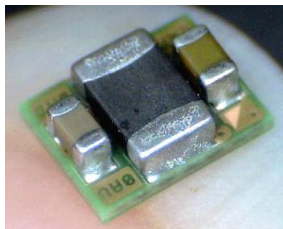
RF



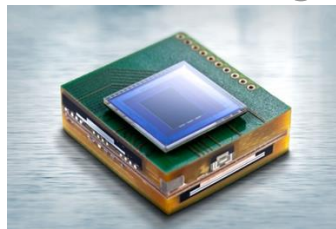
ASIC



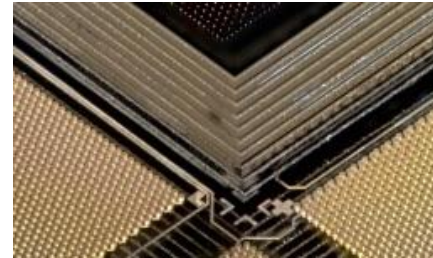
Power/WiFi



MEMS/Images



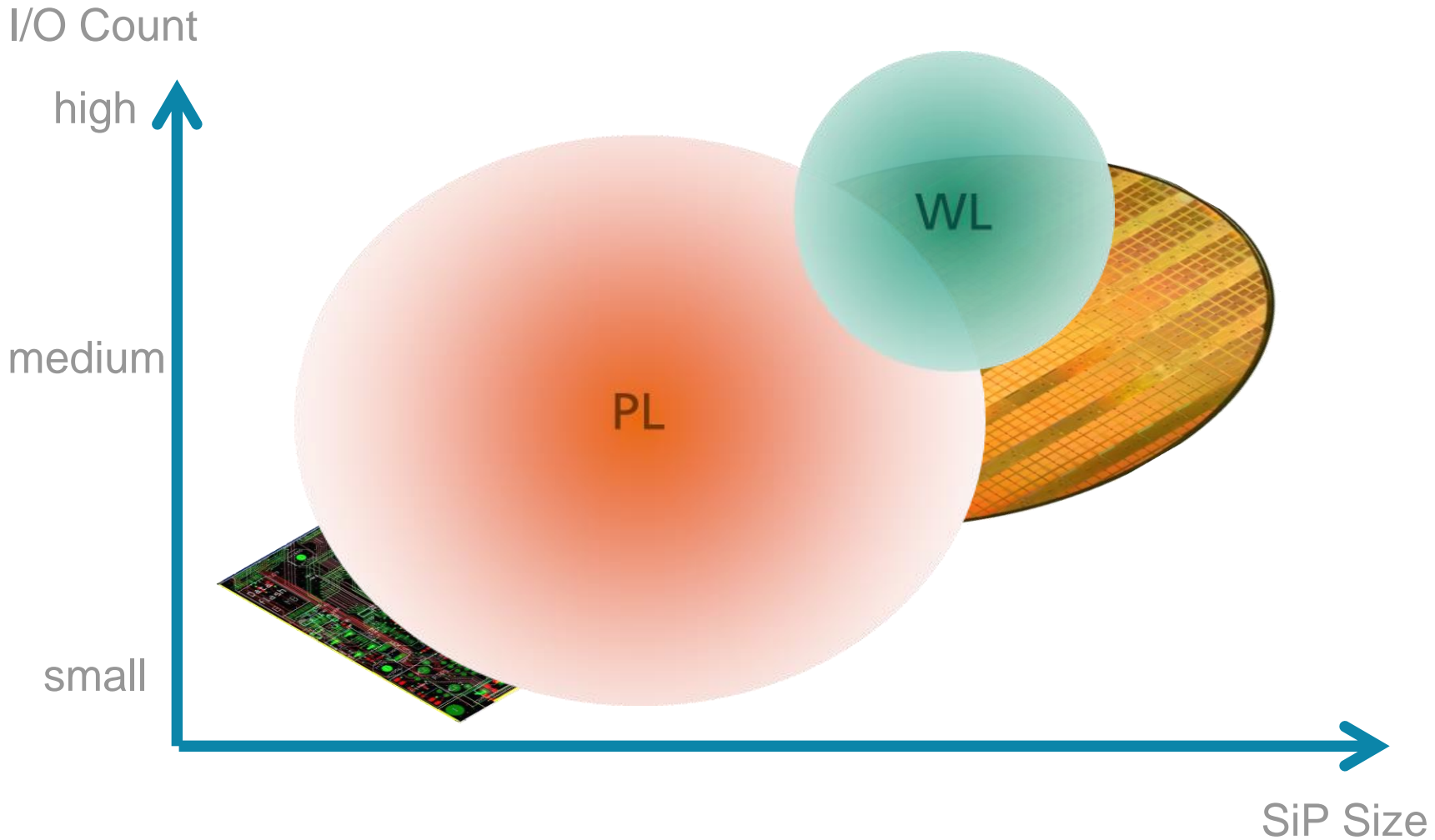
GPU, CPU + Memory, FPGA



SiP Size



# Panel Level is: The intelligent combination of Wafer Level Processing and PCB Processing



# Fraunhofer IZM has formed a consortium for Panel Level Packaging

Goal is to drive Panel Level FO-WLP to a similar performance as WLP but at lower cost



intel  
**Hitachi Chemical**  
*Working On Wonders*

ASM  Pacific Technology Ltd.

**AT&S** **Unimicron**

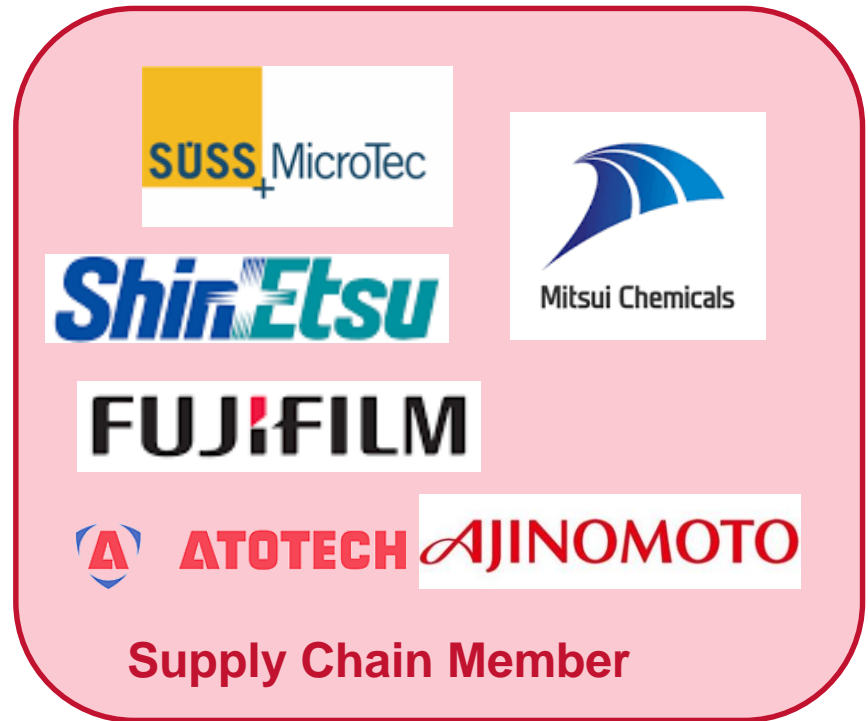
 *evatec*  
process systems The Thin Film Powerhouse


 **SEMSYSCO**


 **nanium**

 **brewer science**

**Full Member**




 **SUS** MicroTec

 Mitsui Chemicals

**ShinEtsu**

**FUJIFILM**

 **ATOTECH** **AJINOMOTO**

**Supply Chain Member**

 **Fraunhofer**  
IZM