Heterogeneous Integration & SiP

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Convergence of Packaging and System Integration

IC Developer Driven

OSAT & EMS Integration & Miniaturization
System-in-Package (SiP)

System OEM Driven

Device Package

System Module
From Single Building to Metropolitan

Financial Center, Business Headquarters

Density (Manhattan)

Hybrid (Taipei)
SiP – Dual Direction of Design Solutions

Component Counts

Hybrid & Module

High I/O Density Design

* System in Package-intelligent design

**RDL**

**Total Chips I/O**

1000

100

10

1

15K

40K

200K
SiP Design Flow: Integrating w/IC & System

**Targeting for High Density**
(FOCoS/2.5D)
Want fast and optimized RDL

**Targeting for Hybrid Integration**
(SiP, DECA, Embedded aEASI/SESUB)
Want to minimize iteration & accurate DRC

* System in Package-intelligent design
Design Challenges

• Tangible Benefit for Integration
  • Performance, Cost, TTM

• System and Component Specs Met when Co-exited in Package
  • Power, PI, Thermo, Wrapage, SI, RF, MEMS, ...

• D4M, Yield

• Test

• Reliability for Applications

• Co-Design Among Designers from IC, Package, and System

• Co-Design with Multi-physics Considerations, Simulations
SiP-id for High Density Design

Advantages of SiP-id for high density package design

- Import chip netlist
- Design operations
- Design rule checking

Before

- Tool loads file for even with 30k I/Os > 1.5 hours
- < 2 mins With new tool

After

- Manual tool module for degassing and theiving > 3 hours
- < 5 mins New tool with flexible functions

- Manual and tool for limited I/O < 30k > 1.5 hours
- < 10 mins New tool for ultra high density > 200k I/Os
SiP-id for Hybrid SiP Design

Design for manufacturability
Auto DRC

Component placement made simple

Reduce back and forth communication

Compatible to OrCAD/Allegro SIP Layout SPB 17.2 and above
Discussion

• What is the state of the art in co-design?
  ✓ Co-design among designers from IC, package, and system
  ✓ Co-design with multi-physics considerations, simulations

• What are the key challenges that need to be overcome?
  ✓ Tangible benefit for integration
    • Performance, Cost, TTM
  ✓ System and component specs met when co-exited in package
    • Power, PI, Thermo, Wrapage, SI, RF, MEMS, ...
  ✓ D4M, yield
  ✓ Test
  ✓ Reliability for applications

• What needs to happen for these challenges to be overcome?
  ✓ An Design Flow that integrates these element, and is agreed across the IC, packaging, and system industries