On behalf of the Program and Executive Committees, it is my pleasure to invite you to IEEE’s 69th Electronic Components and Technology Conference (ECTC), which will be held at The Cosmopolitan, Las Vegas, Nevada, USA from May 28 – 31, 2019. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor companies, foundry and OSAT service providers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1,400 people have attended ECTC in each of the last three years.

At the 69th ECTC, more than 360 technical papers are scheduled to be presented in thirty-six oral sessions and five interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as wafer-level and fan-out packaging, 2.5D, 3D and heterogeneous integration, interposers, advanced substrate, assembly, materials modeling, reliability, packaging for harsh conditions, power packaging, interconnections, packaging for high speed and high bandwidth, photonics, flexible and printed electronics. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over twenty countries are expected to present their work at the 69th ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature six special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, May 28 at 10 a.m., W. Hong Yeo and Mikel Miller will chair a special session covering “Transient Electronics: A Green Revolution for Packaging.” On the same day at 2 p.m., Rena Huang and Soon Jang will chair a session titled “Photonics on the Cutting-Edge of Technology Evolution.” Tuesday evening will also include the ECTC Panel Session at 7:30 p.m. chaired by IEEE EPS President Avi Bar-Cohen and Karlheinz Bock, where young researchers will share their visions of future packaging technologies and participate in discussions with experts in the field.

This conference will feature a Women’s Panel and Reception, jointly organized by ECTC and ITherm, on Wednesday, May 29, 2019 at 6:30pm. This year, panelists will share their perspectives on effective programs and strategies to enhance the participation of women in engineering throughout career progression, from the university to the executive suite. The panel will be chaired by Kristina Young-Fisher and Cristina Amon. On the same day at 7:30 p.m., Tanja Braun will chair the ECTC Plenary Session titled “Sensors and Packaging for Autonomous Driving.” In this plenary session, experts will address the challenges and demands for sensors and packages for autonomous driving along the value chain. On Thursday, May 30 at 8 p.m., the IEEE EPS Seminar entitled “Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements” will be moderated by Yasumitsu Orii and Sheigenori Aoki.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE ITherm Conference this year, the 69th ECTC will offer eighteen PDCs, organized by the PDC Committee chaired by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 28 and are taught by distinguished experts in their respective fields. The Technology Corner exhibits will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 69th ECTC and be a part of all the exciting technical and professional opportunities. I also take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 69th ECTC a success. I look forward to meeting you in Las Vegas, Nevada May 28 –31, 2019.

Nancy Stoffel
69th ECTC Program Chair
General Electric Research
Email: rstoffel194@gmail.com

Index

ECTC Registration .................................................. 3, 32, 33
General Information .................................................. 3
Hotel Information .................................................. 3, 32
Conference Overview .............................................. 4
2019 Photonics Special Session ................................... 5
2019 ECTC Special Session ....................................... 5
2019 ECTC Panel Session ......................................... 5
2019 ECTC Plenary Session ....................................... 5
ECTC/ITherm Young Professionals Panel & Reception .......... 5
ECTC Luncheon Keynote Speaker ................................ 6
2019 IEEE EPS Seminar ............................................. 6
2019 ECTC/ITherm Women’s Panel and Reception .............. 6
ECTC Luncheon Keynote Speaker ................................ 7
Luncheons and Receptions ........................................... 7
Executive and Program Committees ............................. 8-9
Professional Development Courses ............................. 10-15
Area Attractions ..................................................... 15
Program Sessions ..................................................... 16-31
2019 Technology Corner Exhibits ................................ 32
### Advance Registration

**Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions see page 32.**

Register early ... save US$100 or more! All registrations received after May 2, 2019 will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk on the 4th floor in the Belmont Commons.

### On-Site Registration Schedule

Registration will be held on the 4th floor in the Belmont Commons.

<table>
<thead>
<tr>
<th>Day</th>
<th>Time</th>
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</thead>
<tbody>
<tr>
<td>Monday, May 27, 2019</td>
<td>3:00 p.m. – 5:00 p.m.</td>
</tr>
<tr>
<td>Tuesday, May 28, 2019</td>
<td>6:45 a.m. – 5:00 p.m.*</td>
</tr>
<tr>
<td>*6:45 a.m. – 8:00 a.m.: Morning PDCs &amp; Morning ECTC Special Session only</td>
<td></td>
</tr>
<tr>
<td>Wednesday, May 29, 2019</td>
<td>6:45 a.m. – 4:00 p.m.</td>
</tr>
<tr>
<td>Thursday, May 30, 2019</td>
<td>7:30 a.m. – 4:00 p.m.</td>
</tr>
<tr>
<td>Friday, May 31, 2019</td>
<td>7:30 a.m. – 12:00 Noon</td>
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</table>

The above schedule for Tuesday will be rigorously enforced to prevent students from being late for their courses.

### General Information

Conference organizers reserve the right to cancel or change the program without prior notice. The meeting spaces within the Cosmopolitan of Las Vegas, as well as the ECTC, are both smoke-free environments.

### Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual’s belongings is the individual’s responsibility.

### ITherm 2019

ITherm will be co-located with ECTC 2019 at The Cosmopolitan of Las Vegas. For more information on ITherm conference details, please visit their website at: https://www.ieee-itherm.net/itherm/conference/home

### ECTC Sponsors

With 68 years of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 1,500 individuals and organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Program, and several other sponsorship options that can be customized to your company’s interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under “Sponsors.”

To sign-up for sponsorship or to get more details, please contact Wolfgang Sauter at wsauter20@gmail.com or +1-802-922-3083.

### Hotel Accommodations

Rooms for ECTC attendees have been reserved at The Cosmopolitan of Las Vegas. The special conference rate for a single/double occupancy room is:

**US$166.00 per night**

This price includes single or double occupancy in one room. There will be an upcharge of $30 per person if occupancy includes more than two individuals.

Please note these rooms are on a first come, first served basis. If the conference rate is no longer available, attendees will be offered the next best price available.

Room reservations must be made through our website at http://www.ectc.net/location/index.cfm or directly with the hotel. The conference rate of $166.00/night is available until April 26, 2019, or until the room block runs out, whichever comes first. All reservations made after the cutoff date of April 26, 2019 at 5 p.m. Pacific Time, or after the room block is filled, will be accepted on a space and rate availability basis. **If you need to cancel a reservation, please do so AT LEAST 5 days before arrival for a full refund.** Each hotel guest is subject to all hotel rules and regulations. Check-in time: 3 p.m. & check-out time: 12 noon local time.

### Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for ECTC. Be advised that you may receive emails about booking a hotel room for ECTC from third-party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. ECTC’s only authorized site for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that you have personally used in the past to book travel. Please be advised, there are scam artists out there, and if it’s too good to be true, it is likely. Should you have any questions about booking a hotel room, please contact ECTC staff at: lrenzi@renziandco.com

### Transportation Services

There is no complimentary transportation to and from the airport to The Cosmopolitan of Las Vegas. Please check with the service desk at the airport on the various forms of transportation including taxis, buses, and private car services.
May 28, 2019
Morning Professional Development Courses
8:00 a.m. - 12:00 p.m.
1. Achieving High Reliability of Lead-Free Solder Joints - Materials Considerations
2. Introduction to Fan-Out Wafer Level Packaging
3. Fundamentals of Glass Technology and Applications for Advanced Semiconductor Packaging
4. Moore’s Law for Packaging to replace Moore’s Law for ICs
5. Polymers and Nanocomposites for Electronic and Photonic Packaging
6. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel Level Packages and Interposers
7. Solving Package Failure Mechanics for Improved Reliability
8. Characterization of Advanced EMGs for FO-WLP, Heterogeneous Integration, and Automotive Electronics
9. Integrated Thermal Packaging and Reliability of Power Electronics

Afternoon Professional Development Courses
1:15 p.m. - 5:15 p.m.
10. Flip Chip Technologies
11. Wafer-Level Chip-Scale Packaging (WCSP) Fundamentals
12. Flexible Hybrid Technologies - Manufacturing and Reliability
13. Fan-Out Wafer/Panel Level Packaging and 3D IC Heterogeneous Integration
14. Polymers for Wafer Level Packaging
16. Robust Electronics for Automotive Applications Including Autonomous Driving
17. From Wafer to Panel Level Packaging
18. Electronics Cooling Technologies for Handheld Devices, Computing, and High Power Electronics

ECTC Special Session
9:30 a.m. - 11:30 a.m.
“Transistor Electronics: A Green Revolution for Packaging?”

Photonics Special Session
2:00 p.m. - 3:30 p.m.
“Photonics on the Cutting-Edge of Technology Evolution”

ECTC Panel Session
7:45 p.m. - 9:15 p.m.
“Future (Visions) of Electronics Packaging”

May 29, 2019
Technical Sessions
8:00 a.m. - 11:40 a.m.
1. Wafer Level Fan-Out Process Integration
2. Next Generation Wirebonding and Die Attach/Sintering
3. Re-Distribution Layer and Additive Manufacturing
4. Advancements in Automotive and Power Devices
5. Bonding Manufacturing Technologies
6. Emerging Flexible Hybrid Electronics

Interactive Presentation Sessions 37 & 38
9:00 a.m. - 11:00 a.m.
12:00 p.m. - 4:00 p.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.
7. Advances in Flip Chip Technology
8. Material and Process Trends in FOWLP & PLP
9. Wearables and Thin Package Reliability & CPI
10. Dicing and Encapsulation Technologies
11. Automotive and Harsh Environment Reliability
12. Advanced Photonic Devices & Packaging

ECTC Plenary Session
7:30 p.m. - 9:00 p.m.
“Sensors and Packaging for Autonomous Driving”

May 30, 2019
Technical Sessions
8:00 a.m. - 11:40 a.m.
13. Technologies Enabling 3D and Heterogeneous Integration
14. Fine Pitch Solder-Free Bonded Interconnects
15. High-Bandwidth Packaging
16. Advanced Materials for High-Speed Electronics
17. Materials and Design for Reliability of Next Generation Packages
18. Warpage and Material Performance

Interactive Presentation Sessions 39 & 40
9:00 a.m. - 11:00 a.m.
12:00 p.m. - 4:00 p.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.
19. MEMS, Sensors, & IoT
20. Fanout and Heterogeneous Integration
21. 5G, mm-Wave and Antenna-in-Package
22. Advanced Substrates and Interconnect Technology
23. High Bandwidth 3D & Photonics Integration

“Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements”

May 31, 2019
Technical Sessions
8:00 a.m. - 11:40 a.m.
25. Wafer Level Packaging Fan-In-Fan-Out Structure and Materials
26. High-Speed Signaling for HPC and Memory
27. Advanced Biosensors and Bioelectronics
28. Embedded Substrates and Integrated Technologies
29. Electromigration and Innovative Reliability Test Methods
30. Assembly and Process Modeling

Student Interactive Presentations Session 41
8:30 a.m. - 10:30 a.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.
31. Automotive and Power Packaging
32. Power and Panel Assembly
33. Thermal-Mechanical Simulation for Fan-Out, Flip Chip, and WLCSP
34. Emerging Materials and Processing
35. New Interconnects for Package Scaling
36. RF & Power Components and Modules

Session Summary by Interest Area

<table>
<thead>
<tr>
<th>3D/TSV Topics</th>
<th>S13, S23</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fan-Out Topics</td>
<td>S1, S8, S20, S25, S33</td>
</tr>
<tr>
<td>Packaging Technologies</td>
<td>S1, S3, S7, S13, S19, S25, S31</td>
</tr>
<tr>
<td>Applied Reliability</td>
<td>S11, S17, S24, S29, S34</td>
</tr>
<tr>
<td>Assembly &amp; Manufacturing Technology</td>
<td>S5, S10, S28, D32</td>
</tr>
<tr>
<td>Emerging Technologies</td>
<td>S3, S6, S27</td>
</tr>
<tr>
<td>High-Speed, Wireless &amp; Components</td>
<td>S15, S21, S26, S36</td>
</tr>
<tr>
<td>Interconnections</td>
<td>S2, S14, S20, S23, S35</td>
</tr>
<tr>
<td>Materials &amp; Processing</td>
<td>S4, S8, S16, S22, S34</td>
</tr>
<tr>
<td>Thermal/Mechanical Simulation &amp; Characterization</td>
<td>S9, S18, S30, S33</td>
</tr>
<tr>
<td>Photonics</td>
<td>S12, S23</td>
</tr>
<tr>
<td>Interactive Presentations</td>
<td>S37, S38, S39, S40, S41</td>
</tr>
</tbody>
</table>
**2019 Photonics Special Session**

*Photonics on the Cutting-Edge of Technology Evolution*

Tuesday, May 28, 2019, 2:00 p.m. – 4:30 p.m.

Chairs: Rena Huang - Rensselaer Polytechnic Institute and Soon Jang - ficonTEC (USA) Corporation

The special session aims to capture the latest technology advancements in the fast evolving photonics areas that have wide interest to industry, academia and government laboratories worldwide. Invited speakers will discuss topics of optical neuromorphic computing, Si photonics for optical quantum computing, heterogeneous integration, advanced LiDARs for autonomous vehicles, and optical time domain reflectometer (OTDR) integration into fiber optic transceivers. The invited technical leaders will share their visions on impacted applications.

1. Bert Offrein – IBM Research GmbH-Zurich
2. Mark Thompson – PsiQuantum
3. Roy Meade, VP Manufacturing – Ayar Labs

**2019 ECTC Plenary Session**

*Sensors and Packaging for Autonomous Driving*

Wednesday, May 29, 2019, 7:30 p.m. – 9:00 p.m.

Chair: Tanja Braun, Fraunhofer Institute for Reliability and Microintegration (IzM)

The future of individual, safe, and flexible transportation is widely seen as driverless. Already today's sensor systems in combination with intelligent algorithms are providing essential support for human drivers. The rise of AI and a growth of a surrounding infrastructure enhancing car to x communication will enable various scenarios for autonomous driving. During the plenary session key experts from industry will discuss the challenges and demands for sensors and packages for autonomous driving along the value chain.

1. Scott Chen – Advanced Semiconductor Engineering, Inc.
3. Dr. Veer Dhandapani – NXP Semiconductors
4. Dragos Maciuca - Ford

**2019 Young Professional Networking Panel**

*These sessions are open to all conference attendees.*
2019 ECTC/ITherm Women’s Panel and Reception

Unleashing the Power of Diversity in our Workforce
Wednesday, May 29, 2019, 6:30 p.m. – 7:30 p.m.
Chairs: Kristina Young-Fisher - GLOBALFOUNDRIES and Cristina Amon – University of Toronto

IEEE EPS Society President Avi Bar-Cohen and 69th ECTC Junior Past General Chair Sam Karikalan cordially invite all ECTC attendees to attend our fifth Women’s Panel and Reception. The panelists will speak on Unleashing the Power of Diversity in the Workforce. Discussion will include the power of diversity in a high-performing workplace, strategies to build a diverse workforce, and tools for inclusion and engagement. Panelists will discuss the creation of policies and programs to increase representation along with metrics to assess progress throughout career progression. The panelists will share both successes and challenges to achieving these goals.

1. Monica Jackson – GE Aviation
2. Rolf Aschenbrenner – Fraunhofer IZM
3. Dereje Agaonafer- University of Texas at Arlington
4. Jean Trewhella- GLOBALFOUNDRIES

2019 IEEE EPS Seminar
Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements
Thursday, May 30, 2019, 8:00 p.m. – 9:30 p.m.
Chairs: Yasumitsu Orii - Nagase, Japan and Sheigenori Aoki - Fujitsu

This panel will outline the product requirements for the smartphone for 2025-2030 in the era of 5G and 6G. Subsequently, these product requirements will be translated into packaging material challenges and approaches. Representatives of materials companies will share their approaches to meet the projected smartphone system requirements including materials for fan-out wafer-level and panel-level packaging, molding materials, high-speed substrates, and low-loss substrates.

To show the product requirements:
1. Toshihiko Nishio – SBR Technology Company
2. Eiichi Nomura – Nagase Chemtex
3. Koichi Hasegawa – JSR
4. Kenji Nishiguchi – Risho Kogyo
5. Mike Sakaguchi – Tatsuta Electric Wire & Cable

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ECTC Luncheon Keynote

**Soft Electronic and Microfluidic Systems for the Skin**

*Wednesday, May 29, 2019*

**John A. Rogers**

Director of Center for Bio-Integrated Electronics, Northwestern University

Recent advances in materials, mechanics, and manufacturing establish the foundations for high-performance classes of electronics and other microsystems technologies that have physical properties precisely matched those of the human epidermis. The resulting devices can integrate with the skin in a physically imperceptible fashion to provide continuous, clinical-quality information on physiological status. This talk will summarize the key ideas and presents specific examples in wireless monitoring for neonatal intensive care, and in capture, storage, and biomarker analysis of sweat.

**Luncheons**

**Tuesday PDC Luncheon**

All individuals attending a PDC are invited to join us for lunch. Proctors and instructors are welcome, too!

**Wednesday Conference Luncheon**

Please be sure not to miss our Wednesday luncheon with guest speaker Dr. John Rogers, Northwestern University. All conference attendees are welcome!

**Thursday EPS Luncheon**

Our sponsor, the IEEE Electronics Packaging Society, will be sponsoring lunch on Thursday for all conference attendees!

**Friday Program Chair Luncheon**

Please attend Friday’s lunch hosted by the 69th ECTC Program Chair. We will honor conference paper award recipients and raffle off a variety of prizes including a hotel stay, free conference registrations, and many other attractive items!

**General Chair’s Speakers Reception**

*Tuesday, May 28, 2019 • 6:00 p.m. – 7:00 p.m.*  
*(by invitation only)*

**ECTC Student Reception**

*Tuesday, May 28, 2019 • 5:00 p.m. – 6:00 p.m.*  
*Hosted by Texas Instruments, Inc.*

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry, and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them succeed in their first job search and reach their current positions. During this reception, you can enjoy good food while networking with industry leaders and achievers. Don’t miss your opportunity to interact with people who you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

**Exhibitor Reception**

*Wednesday, May 29, 2019 • 5:30 p.m. – 6:30 p.m.*

All badged attendees are invited to attend a reception in the exhibition hall.

**69th ECTC Gala Reception**

*Thursday, May 30, 2019 • 6:30 p.m. – 8:00 p.m.*

All badged attendees and their guests are invited to attend a reception hosted by the Gala Reception sponsors.
PROFESSIONAL DEVELOPMENT COURSES

Tuesday, May 28, 2019

Kitty Pearsall, Chair
Boss Precision, Inc.
kitty.pearssall@gmail.com
+1-512-845-3287

Jeff Suhling, Assistant Chair
Auburn University
jsuhling@auburn.edu
+1-334-844-3332

MORNING COURSES
8:00 a.m. – 12:00 Noon

1. ACHIEVING HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIALS CONSIDERATIONS
Course Leader: Ning-Cheng Lee – Indium Corporation

Course Objective: This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMCs) under a variety of material combinations and aging conditions and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in details, and novel alloys with reduced fragility will be presented. Also presented are crucial parameters for high reliability solder alloys for automotive industry. Electromigration and tin whisker will also be discussed. The emphasis of this course is placed on the understanding of how the various factors contribute to the failure modes, and how to select proper solder alloys and surface finishes for achieving high reliability.

Course Outline:
1. Main Stream Lead-free Soldering Practice
2. Surface Finishes Issues
3. Mechanical Properties
4. Intermetallic Compounds
5. Failure Modes
6. Reliability - Thermal Cycle
7. Reliability - Fragility
8. Reliability - Rigidity & Ductility
9. Reliability - Electromigration
10. Reliability - Tin Whisker

Who Should Attend: Directors, managers, design engineers, process engineers, and reliability engineers who care about achieving high reliability lead-free solder joints and would like to know how to achieve it should take this course.

2. INTRODUCTION TO FAN-OUT WAFER LEVEL PACKAGING
Course Leader: Beth Keser – Intel Corporation

Course Objective: Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high-volume manufacturing for over 10 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wire bond and bump interconnections, substrates, lead frames, and the traditional flip chip or wire bond chip attach and underfill assembly technologies across multiple applications. This course will cover the advantages of FO-WLP, potential application spaces, package structures available in the industry, process flows, material challenges, design rule roadmap, reliability, and benchmarking.

Course Outline:
1. Current Challenges in Packaging
2. Definition and Advantages
3. Applications
4. Package Structures
5. Process
6. Material Challenges
7. Design Rule Roadmap
8. Reliability
9. Benchmarking

Who Should Attend: Engineers and managers responsible for advanced packaging development, package characterization, package quality, package reliability and package design should attend this course. Suppliers who are interested in supporting the materials and equipment supply chain should also attend. Both newcomers and experienced practitioners are welcome.

3. FUNDAMENTALS OF GLASS TECHNOLOGY AND APPLICATIONS FOR ADVANCED SEMICONDUCTOR PACKAGING
Course Leaders: Dr. Indrajit Dutta – Corning, Inc. and Dr. Jay Zhang – Corning, Inc.

Course Objective: This course is intended to guide technologists toward a deeper understanding of how to leverage engineered glass as a material for advanced IC packaging applications. Following a review of the fundamental principles of glass structure, composition, and properties, we will discuss the unique attributes that make glass an enabling material, including strength and reliability, chemical durability, thermal behavior, associated thermal relaxation behavior, and electrical properties. In addition, we will review the “glass toolkit” as a platform alternative for semiconductor packaging development, including various manufacturing (glass melting and forming) approaches, the diversity of compositional options, and a survey of glass processing approaches that can be adapted from adjacent glass technology spaces to advanced semiconductor packaging. Finally, a series of case studies will illustrate how glass is contributing to emerging technologies in the microelectronics space and explore current and potential applications in advanced semiconductor packaging, consumer electronics, and internet of things (IoT) applications. Examples include the role of glass as a carrier for temporary bonding, integrated glass wafers for optical sensors and augmented reality, key components in RF communications, as well as glass interposers for 2.5D and 3D packaging.

Course Outline:
1. Fundamentals of Glass
   - What is Glass?
   - Overview of Glass Attributes
2. Versatility of Glass
   - Glass Composition Review
   - Melting and Forming Process
   - Overview of Major Forming Processes
   - Secondary Processes
   - Options for Enhanced Properties
3. Major Applications and Markets
   - Wafer-Level Optics
   - Semiconductor
   - Case Studies

Who Should Attend: Engineers, technical managers, scientists, buyers, and managers involved in materials, research and development, as well as advanced semiconductor packaging. We welcome individuals or companies with little or no experience in using glass.

4. MOORE’S LAW FOR PACKAGING TO REPLACE MOORE’S LAW FOR ICs
Course Leader: Rao Tummala – Georgia Institute of Technology

Course Objective: This course proposes that Moore’s Law for Packaging replaces Moore’s Law for ICs, as the latter is seen as coming to an end. Moore’s Law for ICs is about scaling transistors to ever smaller sizes, from node-to-node and interconnecting and integrating these to result in more transistors in smaller chips at lower cost from 300 mm wafers. As transistor scaling and integration comes to an end due to physical, material, and electrical limitations, Moore’s Law for Packaging (MLP) can be viewed as interconnecting and integrating smaller chips with the highest transistor density and with the highest performance at the lowest cost. Package or system scaling is proposed to be one and the same, as the end goal of packaging is a system. Just as Moore’s Law has two components – number of transistors and cost of each transistor, MLP is proposed to have two components as well – the number of interconnections or I/Os and the cost of each I/O.

This course lays the ground work for Moore’s Law for Packaging by showing how I/Os have evolved from one package family node to the next, starting with <16 I/Os in the 1960s to the current silicon interposers with about 200,000 I/Os. It proposes a variety of ways to extend Moore’s Law, such as extending Si interposers and beyond using glass in panel embedding.

Just as Moore’s Law has both a doubling of transistors and a halving of cost every 24 months, MLP must do the same. Interconnections have been driven by computing systems and within computing systems, between logic and memory. The new era of artificial intelligence, mimicking human brains, is yet another reason for Moore’s Law for System Interconnections. Currently, the most advanced MLP is with wafer-based silicon packaging. But silicon-based packaging has many limitations at material, substrate or interconnect and system levels. At material level, its electrical loss and its dielectric constant are very high.
At interconnect level, its capacitance and resistance are very high, leading to so-called RC delays. In addition, Si-based packaging doesn’t conform to Moore’s Law for cost. Cost, of course, is the basis for going away from Moore’s Law for ICs. At system levels, Si interposers, while they are perfectly matched to ICs, they are totally mismatched to boards, requiring additional packaging, thus making system level interconnections even longer. So, what are future technologies beyond Si interposers to drive Moore’s Law for packaging. This course will present and discuss a variety of options.

**Course Outline:**
1. Current Approach to Devices and Systems
2. Moore’s Law for ICs, Its Evolution and Its Future
3. Three Eras of Moore’s Law: For ICs, Packaging or Interconnections and for Systems
4. Moore’s Law for Packaging: Observation and Proposal
5. Evolution of Package Interconnections (I/Os) from the 1960s Consistent with Moore’s Law
6. Future of Moore’s Law

**Who Should Attend:**
R&D executives as well as senior technical and marketing managers involved in all aspects of electronics from academic and industry R&D, supply-chain IC, package and systems manufacturing, marketing, investments, and users who deal with strategic directions for their company.

5. **POLYMERS AND NANOCOMPOSITES FOR ELECTRONIC AND PHOTONIC PACKAGING**

**Course Leaders:** C. P. Wong – Georgia Institute of Technology, Daniel Lu – Henkel Corporation

**Course Objective:**
Polymers and nanocomposites are widely used in electronic and photonics packaging as adhesives, encapsulants, insulators, dielectrics, molding compounds, and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high-performance novel no-flow underfills, reworkable underfills for ball grid array (BGA), chip scale packaging (CSP), system in a package (SiP), direct chip attach (DCA), flip-chip (FC), paper-thin IC and 3D packaging, conductive adhesives (both ICA and ACA), embedded passives (high K polymer composites), nano particles and nano functional materials such as CNTs (some with graphene). It is imperative that both material suppliers, formulators, and their users have a thorough understanding of polymeric materials and the recent advances on nano materials and their importance in the advances of the electronic packaging and interconnect technologies.

**Course Outline:**
1. Fundamental of Polymers and Materials Science and Engineering
2. Material Needs for Next-Generation Electronic Packaging
3. Novel Nanocomposites for Flip-Chip Underfill Applications
4. Recent Advances on Nano Lead-Free Alloys for High-Performance Components Interconnects
5. Low-Cost High-Performance Lead-Free Interconnect Materials and Processes
6. Recent Advances on CNTs as Thermal Interface Materials (TIMs)
7. Lotus Effect Coating for Self-Cleaning
8. Fundamentals of Electrically Conductive Adhesives (ECAs)
9. Recent Advances on Conductive Adhesives
10. Recent Advances on Nano Conductive Adhesives

**Who Should Attend:**
Engineers, scientists, researchers, designers, managers, and graduate students interested in the fundamentals of electronic packaging as well as those involved in the process of electrical design, layout, processing, fabrication, and/or system-integration of electronic packages.

6. **SOLVING PACKAGE FAILURE MECHANISMS FOR IMPROVED RELIABILITY**

**Course Leader:** Darvin Edwards – Edwards Enterprises

**Course Objective:**
This course explores past and present reliability failure mechanisms that plague semiconductor packages. Primary reliability challenges and major failure mechanisms will be investigated in emerging and high-volume package types such as TSVs, FOWLPs, WLCSPs, FC-BGAs plastic leaded, and no lead packages. The class will focus on reliability topics including TSV-chip interactions, micro bump mechanical reliability, electromigration performance, stress induced ILD damage under bumps and wire bonds, Cu vs. Au wire bond reliability challenges, complications associated with package delamination, solder joint reliability, system level issues such as drop and bend reliability, and the impact of aging on reliability performance. For each failure mechanism, the resultant failure modes and failure analysis techniques needed to verify the mechanisms will be summarized. Recommended failure analysis fault isolation techniques will be described.

This solutions-focused course concentrates on process parameters, design techniques and material selections that eliminate failures and improve reliability to ensure participants can design-in reliability and design-out failures. Characterization and implementation of design guidelines that enable reliable products will be described and encouraged. A test structure methodology combined with qualification by similarity will be highlighted as a technique for early detection of chip/package reliability risks.

**Course Outline:**
1. Introduction to Package Reliability
2. Failure Modes vs. Failure Mechanisms
3. Failure Analysis Techniques and Fault Isolation Package Failure Mechanisms: WLCSPs
4. FC-BGA Package Failure Mechanisms
5. Molded and Leadless Package Failure Mechanisms
6. WLCSPs Package Failure Mechanisms
7. Embedded Die & Fan-Out WLP Failure Mechanisms
8. TSV Failure Mechanisms
10. Common Test Structures for Failure Mechanism Identification
11. Qualification by Similarity (QBS)
12. Summary

**Who Should Attend:**
This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is needed. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions.
8. CHARACTERIZATION OF ADVANCED EMCS FOR FO-WLP, HETEROGENEOUS INTEGRATION, AND AUTOMOTIVE ELECTRONICS

Course Leaders: Przemysł Gromala – Robert Bosch Gmb; Bongtan Han – University of Maryland

Course Objective:
Epoxy-based molding compounds (EMCs) are widely used in the semiconductor industry as one of the most important encapsulating materials. For the advanced packaging technologies, in particular, FO-WLP technologies and heterogeneous integrations, EMCs play a more significant role than the conventional plastically-encapsulated packages because of thin profiles and complex process conditions required for the advanced packaging technologies. In the automotive industry, where demand for more advanced packaging technologies increases rapidly for autonomous and connected cars, EMCs are often used to protect, not only individual IC components, but also entire electronic control units (ECUs), or power modules.

The stress caused by the mismatch of the coefficient of thermal expansion (CTE) between EMCs and adjacent materials is one of the major causes of reliability problems (e.g., excessive warpage, delamination, BRL, etc.). During assembly or even operating conditions, EMCs are subjected to temperatures beyond the glass transition temperature. Around the glass transition temperature, EMCs exhibit significant volumetric and isochoric viscosity, which leads to nonlinear viscoelastic behavior. In contrast, at low temperatures, EMCs show linear viscoelastic behavior. This complex material characteristic in the full temperature range of interest renders the design of electronic devices a nontrivial task. The mechanical behavior of EMCs has to be understood clearly to offer predictive simulation strategies, which has become an integral part of product development processes.

This training will address details of such strategies, summarize the required material characterization procedure, and close with some representative examples.

Course Outline:
1. Introduction
2. Selection of the Material (Preliminary Qualitative Analysis)
3. Material Characterization
4. Cure Kinetics
5. Curing Shrinkage
6. Coefficient of Thermal Expansion
7. Linear Viscoelastic Properties
   - Master Curve and Shift Factor of Young’s Modulus
   - Master Curve and Shift Factor of Bulk Modulus
8. Viscoelastic Behavior in the Non-linear Domain
   - Moisture Diffusivity and Solubility
   - Coefficient of Hygroscopic Swelling
9. Modeling Strategies
   - Linear Viscoelastic Modeling
   - Nonlinear Viscoelastic Modeling
   - Verification and Validation
10. Summary

Who Should Attend:
Engineers and technical managers who are already involved in the material characterization and modeling, numerical modeling, process engineers and PhD students who need fundamental understanding or broad overview.

9. INTEGRATED THERMAL PACKAGING AND RELIABILITY OF POWER ELECTRONICS

Course Leader: Patrick McCuskey – University of Maryland

Course Objective:
Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation has resulted in significant improvements in efficiency over previous technologies, but it also has made it essential that the reliability of power electronics be characterized and enhanced. Recently, increased power levels, made possible by new compound semiconductor materials combined with increased packaging density have led to higher heat densities in power electronic systems, especially inside the switching module, making thermal management more critical to performance and reliability of power electronics.

This course will emphasize approaches to integrated thermal packaging that address performance limits and reliability concerns associated with increased power levels and power density. Following a quick review of active heat transfer techniques, along with prognostic health management, this short course will present the latest developments in the materials (e.g., organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS, and systems and the techniques used for their reliability assessment.

Course Outline:
1. Motivation for Integrated Thermal Packaging for Reliable Power Electronic Systems
2. Simulation and Assessment of Active Thermal Management Techniques: Air, Single Phase Liquid, Two Phase Heat Pipes, and Thermoelectric
3. Application of Thermal Management Techniques to Commercial Power Systems
4. Durability Assessment: Failure Modeling, Simulation, Testing, and Health Monitoring
5. Reliability and Thermal Packaging of Active Devices: Si, SiC, GaN, and Interconnects
6. Reliability and Thermal Packaging of Switching Modules, including Organic Encapsulates
7. Reliability in Rigid Assembly Packaging: PCB, Solder, and Glass Interposers
9. Reliability of Additively Manufactured and Embedded Power Electronics

Who Should Attend:
This course is intended for practicing engineers, designers, and technical managers who work with high heat flux electronics or power electronics and want to learn more about the design, manufacturing, thermal management, and reliability of these power electronic systems.
10. Flip Chip Solder Deposition Processes  
11. Cu Pillar Technology  
12. Flip Chip Solder Selection and Characterization  
13. Flip Chip Electromigration  
14. Non-Solder Interconnects

Who Should Attend:  
The target audience includes scientists, engineers, and managers currently using flip-chip (with solder or Cu pillar) or those considering moving from wire bonding to flip-chip, as well as reliability, product or applications engineers who need a deeper understanding of flip-chip technologies: the advantages, limitations, and failure mechanisms.

II. WAFER-LEVEL CHIP-SCALE PACKAGING (WLCSP) FUNDAMENTALS

Course Leader: Patrick Thompson – Texas Instruments, Inc.

Course Objective:  
This course will provide an overview of Wafer-Level Chip-Scale Packaging (WLCSP) technology. The market drivers, end applications, benefits, and challenges of using WLCSPs in different applications will be discussed. WLCSP configurations, such as bump-on-pad and bump-on-polymer, as well as fan-in, and fan-out formats, will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other areas such as RF sensors and MEMS will be reviewed. Future trends will be covered, including alternate alloy solder balls, increasing ball count, decreasing ball pitch, wafer-level underfill, decreasing package thickness, stacked WLCSP, fan-out WLCSP modules, embedded components, and the advent of large format (panel) processing. Since the technology marks the convergence of fab, assembly, and test, the course will address questions such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, package outline, reliability, and equipment sufficient? Will WLCSP technology be applicable and cost-effective for memory and other complex devices such as ASICs and microprocessors? What are the benefits and limitations of WLCSP in automotive applications?

Course Outline:  
1. Market Drivers for WLCSPs: Portable Consumer, Medical, Automotive, Industrial, Sensors, MEMS  
2. Key WLCSP Technologies  
3. Equipment and Materials References  
4. Infrastructure Service Providers  
5. Pitch and Height Trends  
6. Cost, Benefits, and Limits of WLPs  
7. Reliability: Thermal Cycling, Drop, Bend, Temperature/Humidity, Electromigration  
8. Fan-Out WLP  
9. Supply Chain  
10. Embedded Die  
11. Single Die Embedding vs. SIP Module  
12. Challenges in Evolution to Large Format Processing

Who Should Attend:  
The course will be useful to the following groups of engineers: Newcomers to the field who would like to obtain a general overview of WLCSP; R&D practitioners who would like to learn new methods for solving CSP problems; and those considering WLCSP as a potential alternative for their packaging solutions.

12. FLEXIBLE HYBRID TECHNOLOGIES - MANUFACTURING AND RELIABILITY

Course Leader: Pradeep Lall – Auburn University

Course Objective:  
In this course, manufacture, design, assembly, and accelerated testing of flexible hybrid electronics for applications in some of the emerging areas will be covered. Flexible hybrid electronics opens the possibilities for the development of stretchable, bendable, foldable form-factors in electronics applications which have not been possible with the use of rigid electronics technologies. Flexible electronics may be subjected to strain magnitudes in the neighborhood of 50-150 percent during normal operation. The integration processes and semiconductor packaging architectures for flexible hybrid electronics may differ immensely in comparison with those used for rigid electronics. The manufacture of thin electronic architectures requires the integration of thin-chips, flexible encapsulation, compliant interconnects, and stretchable inks for metallization traces. A number of additive manufacturing processes for the fabrication and assembly of flexible hybrid electronics have become tractable. Processes for handling, pick-and-place operations of thin silicon and compliant interposers through interconnection processes such as reflow requires an understanding of the deformation and warpage processes for development of robust process parameters which will allow for acceptable levels of yields in high-volume manufacture. Modeling of operational stresses in flexible electronics requires the material behavior under loads including constant exposure to human body temperature, saliva, sweat, ambient temperature, humidity, dust, wear and abrasion. The strains imposed on flexible stretchable electronics may far exceed those experienced in rigid electronics requiring the consideration of finite-strain formulation in development of predictive models. The failure mechanisms, failure modes, acceleration factors in flexible electronics under operational loads of stretch, bend, fold and loads resulting from human body proximity are significantly different than rigid electronics. The testing, qualification, and quality assurance protocols to meaningfully inform manufacturing processes and ensure reliability and survivability under exposure to sustained harsh environmental operating conditions, may differ in flexible electronics as well. A number of product areas for the application of flexible electronics are tractable in the near-term including Internet of Things (IoT), medical wearable electronics, textile woven electronics, robotics, communications, asset monitoring, and automotive electronics.

Course Outline:  
1. Ultra-Thin Chips  
2. Die-Attach Materials for Flexible Semiconductor Packaging  
3. Compliant Interconnects  
4. Flexible Encapsulation Materials  
5. Inkjet and Aerosol-Jet Printing Processes  
6. Dielectric Materials for Large-Area Flexible Electronics  
7. Flexible Substrates  
8. Stretchable Inks for Printed Traces  
9. Pick-and-Place and Material Handling Processes  
10. Additive Technologies in Flexible Electronics  
11. Reflow and Printing Processes  
12. Accelerated Testing Protocols

Who Should Attend:  
The targeted audience includes scientists, engineers, and managers currently using flexible electronics or considering moving from rigid electronics to flexible electronics, as well as reliability, product or applications engineers who need a deeper understanding of flexible electronics: the advantages, limitations, and failure mechanisms.

13. FAN-OUT WAFER/PANEL LEVEL PACKAGING AND 3D IC HETEROGENEOUS INTEGRATION

Course Leader: John Lau – ASM Pacific Technology Ltd.

Course Objective:  
Recent advances in fan-out wafer/panel level packaging (TSMC’s InFO-WLP and Fraunhofer IZM’s FO-PLP), 3D IC packaging (TSMC’s InFO PoP vs. Samsung’s ePoP), 3D IC integration (Hybris/Samsung’s HiBiM for AMD/NVIDIA’s GPU vs. Micron’s HiBiM for Intel’s Knights Landing CPU), 2.5D IC Integration (Xilinx/TSMC’s CoWoS and TSV-less interconnects and interposers), embedded 3D hybrid integration (of VCSEL, driver, serializer, polymer waveguide, etc.), 3D CIS/IC integration, 3D MEMS/IC integration, and Cu-Cu hybrid bonding will be discussed in this presentation. Emphasis is placed on various FOWLP assembly methods such as chip-first with die-up, chip-first with die-down, and chip-last (RDL-first). Because redistribution layers (RDLs) play an integral part of FOWLP, various RDL fabrication methods such as Cu damascene, polymer, and PCB/LDI will be discussed. A few notes and recommendations on wafer vs. panel, dielectric materials, and molding materials will be provided. Also, TSV-less interposers such as those given by Xilinx/SPIL, Amkor/SPIL/Xilinx, STATSchipPac, ASE, MediaTek, Intel, TTI, Shinko, Cisco/ eSilicon, Samsung, and Sony will also be discussed. Furthermore, new trends in semiconductor packaging will be presented.

Course Outline:  
1. Formation of FOWLP: (a) Chip-first (die face-down); (b) Chip-first (die face-up); (c) Chip-last  
2. Fabrication of RDLs: (a) Polymer and ECD Cu + Etching (b) PECVD and Cu Damascene + CMP; (c) Hybrid RDLs  
3. TSMC InFO-WLP, InFO-PoP, InFO_AiP  
4. Formation of FOPLP: (a) PCB + SAP; (b) PCB + LDI; (c) PCB + TFF-LCD; (d) SEMCO PLP  
5. Wafer vs. Panel: (a) Application Ranges; (b) Critical Issues of FOPLP  
6. Embedded Chips Panel-Level Packaging (ECP): (a) Ti/AT&R; (b) TDK; (c) Fujikura; (d) Schweizer  
7. Embedded Chips: (a) in Silicon (Maxim); (b) in Glass (GIT)  
8. System-on-Chip (SoC): (a) A10; (b) A11; (c) A12  
9. Heterogeneous Integration vs. SoC  
10. Heterogeneous Integration on Organic Substrates (SP): (a) Amkor (Automobiles); (b) ASE (Watches); (c) Intel/AMD’s CPU/GPU/ HBM; (d) Cisco/eSilicon (Organic Interposer)
11. Heterogeneous Integration on Silicon Substrates (TSV-Interposer): (a) Leti (SoW); (b) TSMC/ Xilinx (CoWoS); (c) AMD and NVidia’s Graphic Cards; (d) AMD (chiplet)

12. Heterogeneous Integration on RDLs and/or TSV-less Interposers (1): (a) Xilinx/SPIL’s TSV-less SLiT and NTI; (b) Amkor’s TSV-less SLiM and SWIFT with FOWLP; (c) SPIL’s TSV-less FOWLP with Hybrid RDLs

13. Heterogeneous Integration on RDLs and/or TSV-less Interposers (2): (a) STATSChipPac’s FOFC eWLB; (b) ASE’s TSV-less FOCoSs; (c) MediaTek’s TSV-less RDLs by FOWLP

14. Heterogeneous Integration on RDLs and/or TSV-less Interposers (3): (a) Intel’s TSV-less EMIB; (b) Imagination Bridge + FOWLP; (c) 3D IC Heterogeneous Integration for Application Processor Chipset

15. Samsung’s Heterogeneous Integration on RDLs: (a) for Mobile Applications and (b) for High-end Applications

16. Trends in FOWLP, FOPLP, and Heterogeneous Integration

Who Should Attend:
If you (students, engineers, and managers) are involved with any aspect of the electronics and optoelectronic industry, you should attend this course. It is equally suited for R&D professionals and scientists. All the materials are based on the papers and books published in the past three years, and each participant will receive more than 200 pages of the lecture notes.

14. POLYMERS FOR WAFER LEVEL PACKAGING

Course Leader: Jeffrey Gotro – InnoCentrix, LLC

Course Objective:
The course will provide an overview of polymers used in wafer level packaging and the important structure-property-process-performance relationships for polymers used in wafer level packaging. The main learning objectives will be: 1) understand the types of polymers used in wafer level packages, including underfills (pre-applied and wafer applied), mold compounds, and substrate materials; 2) gain insights on how polymers are used in Fan Out Wafer Level Packaging, specifically polymer resin and polymer redistribution layers (RDL); and 3) learn the key polymer and processes challenges in Fan Out Wafer Level Packaging including panel level processing. We will cover in more depth the chemistries, material properties, process considerations, and reliability testing for polymers used in wafer level packaging including epoxy mold compounds and dielectric redistribution layers (RDL) for eWLP. The course has been completely updated to include a detailed discussion of the polymers and polymer-related processing for Fan-Out Wafer Level packaging (such as chip first and chip last (RDL first)).

Course Outline:
1. Overview of Polymers used in Wafer Level Packaging
2. Wafer Level Process Flows (Chip-first versus Chip-last (RDL first))
3. Epoxy Mold Compounds for eWLP
4. Photosensitive Polyimides and Polybenzoxazoles
5. Pre-applied Underfills and Wafer Level Underfills, Chemistry and Process
6. High Density Substrate Materials including Coreless Substrates
7. Polymer Challenges in Fan-out Wafer Level Packaging
8. Reliability Testing for Fan-out Wafer Level Packaging
9. Wafer versus Panel Processing: Polymer Challenges and Solutions

Who Should Attend:
Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used electronic packaging will also find this course valuable.

15. RELIABILITY MECHANICS AND MODELING FOR IC PACKAGING - THEORY, IMPLEMENTATION, AND PRACTICES

Course Leaders: Ricky Lee – HKUST and Xuejun Fan – Lamar University

Course Objective:
This course aims to present a comprehensive coverage of reliability mechanics and modeling under various loading conditions. In addition to the introduction of fundamentals, the course contents are arranged in four modules. Module 1 covers modeling under thermal loading, such as problems related to mismatch of thermal expansion or non-uniform temperature distribution. Module 2 deals with the modeling under mechanical loading, such as mechanical bending and/or drop impact. Module 3 will cover modeling under humidity/moisture loading for moisture related problems, such as failures in soldering reflow as well as under high HAST and high-HAST. Module 4 will introduce multi-physics modeling that involves the combined thermal, moisture, electrical, and mechanical loading. Theoretical foundation, modeling implementation, and the best practices for numerical simulations will be covered. Emerging trends and future perspectives in reliability mechanics and modeling will be discussed.

Course Outline:
1. Fundamentals of Stress Analysis and Computational Modeling for IC Packaging
2. Reliability Issues and Modeling under Thermal Loading
3. Reliability Issues and Modeling under Mechanical Loading
4. Reliability Issues and Modeling under Moisture/Humidity Loading
5. Reliability Issues and Modeling under Combined Loading – Multi-physics Modeling

Who Should Attend:
This course is intended for technical managers and staff members, reliability engineers, scientific researchers, and graduate students who are involved in thermal/mechanical modeling, package design, material selection, qualification and reliability assessment of chip-package interaction, package, and package/board interaction.

16. ROBUST ELECTRONICS FOR AUTOMOTIVE APPLICATIONS INCLUDING AUTONOMOUS DRIVING


Course Objective:
The amount of electronics in vehicles has increased dramatically over the last several years and will increase further in the future. Autonomous driving demands highly robust surround-sensing of the entire vehicle. The demand for alternative, more energy-efficient forms of mobility stimulates the application of electro mobility. Electronics modules integrated in sensors and actuators facing harsh environment and higher temperatures. Smaller packages and higher integration levels are needed through embedded systems in package, multi-die packages and finer pitch packages. New packaging technologies have to be qualified for the reliability and safety of automotive standards. E-mobility increases today’s life time requirements of automotive electronics. Additional to the driving time, the charging operations have to be considered. To meet these new life time requirements, the qualification of electronics module is changing from the detection of defects to robustness validation. This approach to qualification is based on knowledge of physics of failure mechanisms and how they relate to specific mission profiles. Based on broad practical experience with complete supply chain examples of robustness validation will be demonstrated. Finally, an overview of the methods of design for reliability with a focus on modeling and simulation of materials interactions will be given.

Course Outline:
1. Electronics Packages for External Sensing and e-Drive
2. Robustness Validation of Automotive Electronics
3. Damage Mechanism in Automotive Electronics
4. Design for Reliability of Automotive Electronics

Who Should Attend:
This PDC is dedicated to engineers and managers already involved in the field of reliability of electronics packaging especially for automotive electronics and for those who need fundamental understanding on robustness validation and design for reliability.

17. FROM WAFER TO PANEL LEVEL PACKAGING

Course Leaders: Tanja Braun and Michael Töpper – Fraunhofer IZM

Course Objective:
Panel Level Packaging (PLP) is one of the latest trends in microelectronics packaging. Besides technology developments towards heterogeneous integration including multiple die packaging, passive component integration in package and redistribution layer or package-on-package approaches also layer substrates formats are targeted. Manufacturing is currently done on wafer level up to 12”/300 mm and 330 mm respectively. For higher productivity and therewith lower costs, larger form factors are introduced. Instead of following the wafer level roadmaps to 450 mm, PLP might be the next big step. PLP has the opportunity to adapt processes, materials and equipment from other technology areas. Printed Circuit Board (PCB), Liquid Crystal Display (LCD) or solar equipment is manufactured on panel sizes and offer new approaches also for PLP. However, an easy upscaling of technology when
moving from wafer to panel level is not possible. Materials, equipment and processes have to be further developed or at least adapted. The PDC will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging including Fan-out Panel Level Packaging substrate embedding approaches. This will include material discussion, technologies, applications and market trends as well as cost modelling.

**Course Outline:**
1. Introduction Advanced Packaging
2. Trends in Wafer Level Packaging
3. Fan-In and Fan-Out Wafer Level: Material, Processes, Applications
4. Introduction and Definition Level Packaging
5. Fan-Out Panel Level Packaging: Technologies, Challenges and Opportunities
6. Substrate Embedding Technologies
7. Cost Modelling

**Who Should Attend:**
Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level Packaging and the transition to Panel Level Packaging should attend. Engineers and managers are welcome as detailed technology descriptions, as well as market trends, applications, and cost modelling are presented.

18. ELECTRONICS COOLING TECHNOLOGIES FOR HANDHELD DEVICES, COMPUTING, AND HIGH-POWER ELECTRONICS

**Course Leaders:** William Maltz and Guy Wagner – Electronic Cooling Solutions

**Course Objective:**
The objective of this course is to cover the major aspects of thermal design from hand-held consumer electronics devices up through liquid cooling of very high heat density devices. Rather than presenting “heat transfer 101,” the purpose of this course is to present a synopsis of the practical knowledge and best practices we at Electronic Cooling Solutions have gained by working on the thermal design of these devices. The course starts out looking at the thermal limits for natural convection and radiation cooling of hand-held devices. From there, it addresses forced convection of higher power devices including servers and datacom equipment. This will cover the use of various types of fans and blowers including the best position for locating them inside of the chassis. The acoustic challenges of using air movers will also be discussed. Finally, the practical aspects of when and how to implement liquid cooling will be presented. This will include looking at the advantages and disadvantages of liquid cooling as well as a discussion of the limits of single-phase liquid cooling.

**Course Outline:**
1. Cooling of Handheld Devices
   - Cooling Limits Driven by Touch Temperature
   - Convection
   - Radiation
   - Use of Heat Spreaders and Heat Pipes
   - Use of Micro-Blowers
   - Importance of Solar Radiation
2. Cooling of Computers, Servers, Datacom Equipment
   - When to Use Air Movers
   - Axial Flow Fans vs. Centrifugal Blowers
   - Testing and Fan Acoustics
   - Fan Location: Push vs Pull
   - Limits of Air Cooling

**Who Should Attend:**
Engineers and technical managers who are involved in packaging technology development that necessitates an understanding of heat sink design and optimization in the context of the thermal management of electronics should attend.

**AREA ATTRACTIONS**

Touted as The Entertainment Capital of the World, Las Vegas offers something for everyone. Most famous for its gambling, shopping, fine dining, entertainment, and nightlife, Las Vegas is also known as a top three destination in the U.S. for business conventions.

It’s a city that caters to young and old, from those who crave the outdoors and adventure, to those who want to be wined and dined and enjoy the nightlife. While excursions to the Grand Canyon, Hoover Dam, and the American Alpine Institute are all within reach, when you’re ready to relax and unwind, The Cosmopolitan of Las Vegas offers world-class restaurants, luxurious spas, unique entertainment, and sleeping rooms that are more reminiscent of a private urban residence than they are of an actual hotel room.

**IMPORTANT NOTICE**
Morning PD Courses 1 through 9 or afternoon PD Courses 10 through 18 run concurrently. Make sure you indicate which course you plan to attend in the morning and/or in the afternoon. As sessions run concurrent, attendance is only allowed at one session in the morning and one session in the afternoon. See page 32 for registration information.
<table>
<thead>
<tr>
<th>Session 1: Wafer Level Fan-Out Process Integration</th>
<th>Session 2: Next-Generation Wirebonding and Die Attach/Sintering</th>
<th>Session 3: Re-Distribution Layer and Additive Manufacturing</th>
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<tr>
<td><strong>Committee:</strong> Packaging Technologies</td>
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1. **8:00 AM - 3D-MiM Fan-Out for 3D-MiM (MUST-in-MUST) Technology for Advanced System Integration**
   - Ann-Jhih Su, Terry Ku, Chung-Hao Tsai, Kuo-Chung Yee, and Douglas Yu – Taiwan Semiconductor Manufacturing Company

2. **8:25AM - Construction on FO-MCM With C4 Bumps Built First Based on Chip Last Assembly Technology**
   - Chih-Hsun Hsu, C. Key Chung, C.F. Lin, Yi Jenf Jiang, Trista Xie – Siliconware Precision Industries Co., Ltd.

3. **8:50AM - Feasibility Study of Fan-Out Panel-Level Packaging for Heterogeneous Integration**
   - Cheng-Ta Ko, Henry Yang – Unimicron; John Lau, Ming Li - ASM

4. **10:00AM - Development of Ultra-Thin FO Package-on-Package for Mobile Application**
   - Hsiang Yao Haoa, Soon Wee Ho, Lin Siak Boon, Wai Leong Ching, Chong Ser Choong, Lim Pei Siang, Tai Chong Chai – Institute of Microelectronics, A*STAR

   - Shuying Ma, Fengxia Zheng, Daquan Yu, Peng Li, Weidong Lu – Huantian Technology Electronics Co., Ltd.; Jambo Yu, Jason Goodelle – Synaptics Incorporated

   - Jun Kyu Lee, Sang Yong Park, Young Ho Kim, Jae Cheon Lee, Yong Tae Kwon, Jong Heon Kim, Nam Chul Kim, Chang Woo – NEPES Corporation

7. **11:15AM - Ultra-High Density I/O Fan-Out Design Optimization with Signal and Power Integrity**
   - Chih-Yi Huang, Chien-Chao Wang, Hung-Chun Kuo, Ming-Fong, Jhong, Tsun-Lung Hsieh, Mi-Chun Hung, Keng Tuan Chang – Advanced Semiconductor Engineering, Inc.
<table>
<thead>
<tr>
<th>Time</th>
<th>Session Title</th>
<th>Session Co-Chairs</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:00 AM</td>
<td>Comprehensive Study of Copper Nano-Paste for Cu-Cu Bonding</td>
<td>Ser Choong Chong, Pei Sang – Institute of Microelectronics</td>
</tr>
<tr>
<td>8:25 AM</td>
<td>Fluxless Bonding Technique of Diamond to Copper Using Silver-Indium Multilayer Structure</td>
<td>Roobezh Sheiki, Yonggun Hu, Chin C. Lee – University of California, Irvine</td>
</tr>
<tr>
<td>8:50 AM</td>
<td>Formulation and Processing of Conductive Polysulfide Sealants for Automotive and Aerospace Applications</td>
<td>Bo Song, Fan Wu, Kyoung-Sik Moon, C. P. Wong – Georgia Institute of Technology</td>
</tr>
<tr>
<td>10:00 AM</td>
<td>Challenges and Approaches to Developing Automotive FCBGA Grade 1/0 Package Capability</td>
<td>Rajen Dias – Amkor Technology, Inc.; Mike Kelly, Devanjan Balaraman, KwangSeok Oh, JoonYoung Park, Hideaki Shoji, Tomso Shriawa – Amkor Technology, Inc.</td>
</tr>
<tr>
<td>10:25 AM</td>
<td>Advanced Substrates for GaN-Based HEMTs Devices</td>
<td>Anthony Cibi, Julie Wiedz, René Escollier, Denis Blachier, Stéphane Bécu, Perceval Coudrain, William Vandendeale, Jerome Biscarrat, Charlotte Gilot, Matthew Charles – CEA-LETI</td>
</tr>
<tr>
<td>10:50 AM</td>
<td>A New Reliable, Corrosion Resistant Gold-Palladium Coated Copper Wire Material</td>
<td>Sandy Klenegl, Robert Klenegl, Tino Stephan, Jan Schischka,Matthias Petzold – Fraunhofer IMWS, Motoki Eto, Nontoshi Araki, Takashi Yamada – Nippon Micronmetal Corporation</td>
</tr>
<tr>
<td>11:15 AM</td>
<td>Ultrasonic-Accelerated Intermetallic Joint Formation with Composite Solder for High-Temperature Power Device Packaging</td>
<td>Hongjun Ji, Mingyu Li, Weiwel Zhao – Harbin Institute of Technology</td>
</tr>
</tbody>
</table>
## Program Sessions: Wednesday, May 29, 1:30-5:10 p.m.

<table>
<thead>
<tr>
<th>Session 7: Advances in Flip Chip Technology</th>
<th>Session 8: Material and Process Trends in FOWLP &amp; PLP Session</th>
<th>9: Wearables and Thin Package Reliability &amp; CPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Packaging Technologies</td>
<td>Committee: Materials &amp; Processing</td>
<td>Committee: Thermal/Mechanical Simulation &amp; Characterization</td>
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<tr>
<td>Session Co-Chairs:</td>
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<tr>
<td>Dan Baldwin</td>
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<td>H.B. Fuller Company</td>
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<td>Email: <a href="mailto:dan.baldwin@hbfuller.com">dan.baldwin@hbfuller.com</a></td>
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<tr>
<td>Michael Gallagher</td>
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<td>DuPont Electronics and Imaging</td>
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<tr>
<td>Email: <a href="mailto:michael.gallagher@dupont.com">michael.gallagher@dupont.com</a></td>
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<td>Ming-Che Hsieh, Namju Cho – STATS ChipPAC Pte. Ltd.; Ian Hsu, Chi-Yuan Chen, Stanley Lin, Ta-Jen Yu – MediaTek, Inc.</td>
<td>Yongsuk Yang, Kyosung Hwang, Robin Gorrell – 3M</td>
<td>Pradeep Lall, Amrit Abrol – Auburn University; Jason Marsh – NextFlex; Ben Leever – Air Force Research Laboratory</td>
</tr>
<tr>
<td>2. 1:55 PM - Ultra Large Area SIPS and Integrated mmW Antenna Array Module for 5G mmW Outdoor Applications Pouya Talebeydokhti, Sidharth Dalmia, Trang Thai, Sharon Tal, Raanan Sover – Intel Corporation</td>
<td>2. 1:55 PM - Design and Demonstration of 1µm Low Resistance RDL Using Panel Scale Processes for High Performance Computing Applications Bartlet DeProspo, Chandra Nair, Emanuel Torres, Fuhan Liu, Mohan Kathapuranil, Rau Tummalia – Georgia Institute of Technology; Frank Wei, Ye Chen – DISCO Corporation; Aya Momozawa, Atsushi Kubo – Tokyo Ohka Kogyo Co., Ltd.</td>
<td>2. 1:55 PM - Bladder Inflation Stretch Test Method for Reliability Characterization of Wearable Electronics Benjamin Stewart, Suresh Saratram – Georgia Institute of Technology</td>
</tr>
<tr>
<td>4. 3:30 PM - Package-on-Package Micro-BGA Microstructure Interaction with Bond Assembly Parameters Pascale Gagnon, Clement Fortin, Tom Weiss – IBM Corporation</td>
<td>4. 3:30 PM - Development of Novel Low-Temperature Curable Positive-Tone Photosensitive Dielectric Materials with High Reliability Yutaro Koyama, Yuki Masuda, Yu Shoji, Kei Hashimoto, Masao Tomikawa – Toray Industries, Inc.</td>
<td>4. 3:30 PM - A Novel Metal Scheme and Bump Array Design Configuration to Enhance Advanced Si Packages CPI Reliability Performance by Using Finite Element Modeling Technique Kuo-Chin Chang, Ming-Ji Li, Steven Hsu, Hao-Chun Liu, Yen-Kun Li, Sheng-Han Tsai, Chieh-Hao Hsu – Taiwan Semiconductor Manufacturing Company, Ltd.</td>
</tr>
</tbody>
</table>

**Refreshment Break: 2:45-3:30 p.m.**
### Program Sessions: Wednesday, May 29, 1:30-5:10 p.m.

<table>
<thead>
<tr>
<th>Session 10: Dicing and Encapsulation Technologies</th>
<th>Session 11: Automotive and Harsh Environment Reliability</th>
<th>Session 12: Advanced Photonic Devices &amp; Packaging</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Assembly &amp; Manufacturing Technology</td>
<td>Committee: Applied Reliability</td>
<td>Committee: Photonics</td>
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<td>Session Co-Chairs:</td>
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<td>Session Co-Chairs:</td>
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<tr>
<td>Garry Cunningham</td>
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<td>Vikas Gupta</td>
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<td>NGC</td>
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<td>Texas Instruments, Inc.</td>
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<td>Email: <a href="mailto:Garry.Cunningham@ngc.com">Garry.Cunningham@ngc.com</a></td>
<td></td>
<td><a href="mailto:gvikas@iti.com">gvikas@iti.com</a></td>
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<tr>
<td>Paul Tiner</td>
<td></td>
<td>Sandy Klengel</td>
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<tr>
<td>Texas Instruments, Inc.</td>
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<td>Fraunhofer Institute for Microstructure of Materials and Systems</td>
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<tr>
<td>Email: <a href="mailto:p-tiner@iti.com">p-tiner@iti.com</a></td>
<td></td>
<td><a href="mailto:sandy.klengel@imws.fraunhofer.de">sandy.klengel@imws.fraunhofer.de</a></td>
</tr>
<tr>
<td>1. 1:30 PM - A More than Moore Enabling Wafer Dicing Technology</td>
<td>1. 1:30 PM - Improvement on Thermal-Aging Reliability of Ag Sinter Joining on Gold Surface Finished Substrates via a Preheating Treatment</td>
<td>1. 1:30 PM - Micro-Fabricated SERF Atomic Magnetometer for Weak Gradient Magnetic Field Detection</td>
</tr>
<tr>
<td>Jeroen van Borculo, Rogier Eversons, Richard van der Stam – ASM Pacific Technology</td>
<td>Zheng Zhang, Chuan Tong Chen, Katsuaki Suga Numa – Osaka University</td>
<td>Xiang Yue, Jingfeng Shang, Chen Ye – Southeast University</td>
</tr>
<tr>
<td>2. 1:55 PM - Plasma Dicing Integration Schemes for Scribe Lane Layout and the Impact on Die Strength</td>
<td>2. 1:55 PM - Package Material Selection Criteria for High-Temperature Automotive Applications</td>
<td>2. 1:55 PM - Highly Reliable White LED Chip Fabricated by Direct Printing Phosphor Glass Layer on LED Wafer</td>
</tr>
<tr>
<td>4. 3:30 PM - Active Control of NCF Fillet Shape for 3D CoW by Multibeam Laser Bonder</td>
<td>4. 3:30 PM - Reliability Investigation of Extremely Large Ratio Fan-Out Wafer-Level Package with Low Ball Density for Ultra-Short-Range Radar</td>
<td>4. 3:30 PM - Silicon Photonic 4X4 Switch with Flip-Chip Integrated Semiconductor Optical Amplifiers</td>
</tr>
<tr>
<td>6. 4:20 PM - Reliability and Benchmark of 2.5D Non-Molding and Molding Technologies</td>
<td>6. 4:20 PM - Prognostication of Accrued Damage and Impending Failure Under Temperature-Vibration in Automotive Electronics</td>
<td>6. 4:20 PM - Vertically Stacked and Directionally Coupled Cavity-Resonator-Integrated Grating Couplers for Integrated-Optic Beam Steering</td>
</tr>
<tr>
<td>Yu-Hsiang Hsiao, Che-Ming Hsu, Yi-Sheng Lin, Chien-Lin Chang Chien – Advanced Semiconductor Engineering, Inc.</td>
<td>Pradeep Lall, Tony Thomas, Jeff Suhling – Auburn University</td>
<td>Shogo Ura, Junichi Inoue – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology</td>
</tr>
<tr>
<td>7. 4:45 PM - Laser-Induced Trench Design, Optimisation and Validation for Restricting Capillary Underfill Spread in Advanced Packaging Configurations</td>
<td>7. 4:45 PM - Electrochemical Impedance Spectroscopy (EIS) for Monitoring the Water Load on PCBAs to Predict Electrochemical Migration Under DC Loads</td>
<td>7. 4:45 PM - CiB (Chip-in-Board) Optical Engine Module Using Advanced Fan-Out Package Technology</td>
</tr>
<tr>
<td>Gul Zeh; David Danovitch – University of Sherbrooke; Eric Turcotte – IBM Canada, Ltd.</td>
<td>Simone Lauer, Theresa Richter – Robert Bosch GmbH; Rajan Ambat, Vadimas Verdingovas – Technical University of Denmark</td>
<td>Sang Yong Park, Jun Kyu Lee, Young Tae Kwon, Jong Heon, Nam Chul Kim, Chang Woo Lee, Jo Hyun Nam, Ji Ni Shim, Sung Hyuk Lee – NEPES Corporation</td>
</tr>
</tbody>
</table>

### Refreshment Break: 2:45-3:30 p.m.
Session Co-Chairs: 
Tom Gregorich  
Leeds Electric Manufacturing Technology (IMEC)  
Email: tgregorich@imec.com

1. 8:00 AM - Active Interposer Technology for Chiplet-Based Advanced 3D System Architectures  
Gauthier Chabot, Jean-Christophe Langlois, Rémi Vérand, Arnaud Garnier, Didier Lattard, Pascal Vivet, Fabienne Ponthière, Thierry Moreau – CEA-LETI; Andrea Vinci – Inttek; Alexis Farcy – STMicroelectronics

2. 8:25 AM - Process Development of Power Delivery Through Wafer Vias for Silicon Interconnect Fabric  
Meng-Hsiang Liu, Amir Hanna, Yandong Luo, Zhe Wan, Subramanian S. Iyer – University of California, Los Angeles

3. 8:50 AM - Active Through-Silicon Interposer Based 2.5D IC Design, Fabrication, Assembly and Test  
Jayasanker Jayabal, Vivek Chidambaram, Sharun Lim Pe Sang, Wang Xiangyu, Jing Ming Ching, Surya Bhattacharya – Institute of Microelectronics

4. 10:00 AM - System on Integrated Chips (SoC) for Next-Generation Advanced System Integration Technology  

5. 10:25 AM - Die-to-Wafer (D2W) Processing and Reliability for 3D Packaging of Advanced Node Logic  

6. 10:50 AM - Enabling Ultra-Thin Die to Wafer Hybrid Bonding for Future Heterogeneous Integrated Systems  
Alain Phommahaxay, Samuel Suhard, Pieter Bex, Serena Iacovo, John Stuakboon, Fumihito Inoue, Lan Peng, Koen Kennes, Erik Sleekx, Eric Beyne – IMEC

7. 11:15 AM - The Thermal Dissipation Characteristics of the Novel System-in-Package Technology (ICE-SiP) for Mobile Packages and 3D High-End Packages  
Junji Li, Qi Liang, Chen Chen, Tiein Shi, Guanglan Xiao, Zirong Tang – Huazhong University of Science & Technology
### Program Sessions: Thursday, May 30, 8:00-11:40 a.m.

<table>
<thead>
<tr>
<th>Session 16: Advanced Materials for High-Speed Electronics</th>
<th>Session 17: Materials and Design for Reliability of Next Generation Packages</th>
<th>Session 18: Warpage and Material Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Committee:</strong> Materials &amp; Processing</td>
<td><strong>Committee:</strong> Applied Reliability</td>
<td><strong>Committee:</strong> Thermal/Mechanical Simulation &amp; Characterization</td>
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<td>Session Co-Chairs:</td>
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<tr>
<td>Yoichi Taira</td>
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<td>Keio University</td>
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<tr>
<td>Yu-Hua Chen</td>
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<td>Unimicron Technology Corporation</td>
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<tr>
<td>1. 8:00 AM - Low-Loss Glass Substrates Formulated with a Variety of Dielectric Characteristics for mm Wave Applications</td>
<td>1. 8:00 AM - Highly (1 1 1) Oriented Nanowtinced Cu for High Fatigue Resistance in Fan-Out Wafer-Level Packaging</td>
<td>1. 8:00 AM - Improved Finite Element Modeling of Moisture Diffusion Considering Discontinuity at Material Interfaces in Electronic Packages</td>
</tr>
<tr>
<td>Kazutaka Hayashi, Nobutaka Kidera, Yoichiro Sato – AGC Inc.</td>
<td>Yu-Jin Li, Chin-Han Tseng, J-Hain Tseng – National Chiao Tung University; Benson Lin, Cia-Cheng Chang – MedaTek, Inc.</td>
<td>Leila Saveri, Xuejun Fan – Lamar University; Rahul Joshi, Keith Newman – Advanced Micro Devices, Inc.</td>
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<tr>
<td>2. 8:25 AM - Evaluation of Fine-Pitch Routing Capabilities of Advanced Dielectric Materials for High-Speed Panel-RDL in 2.5D Interposer and Fan-Out Packages</td>
<td>2. 8:25 AM - WL CSP Package/PCB Design for Board Level Reliability Improvement</td>
<td>2. 8:25 AM - Study of Thermal Aging Behavior of Epoxy Molding Compound for Applications in Harsh Environments</td>
</tr>
<tr>
<td>Shriya Dwarkanath, Fujiu Han, Pukurtha Markandeya Raj, Mohanadigan Kathaperumal, Rao P. Tummala – Georgia Institute of Technology; Asushi Kubo – Tokyo Ohka Kogyo Co; Dashi Okamato – Taya Inr, Milk Co.</td>
<td>Jason Chiu, Kuo-Chiu Chang, Pei-Haw Tsao, Steve Hsu, Ming-Ji Lii – Taiwan Semiconductor Manufacturing Company, Ltd.</td>
<td>Adwait Inamdar, Alexandru Prisacaru, Martin Fleischman – Robert Bosch GmbH; Agnes Veres – Robert Bosch Kft; Bongtae Han – University of Maryland</td>
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<tr>
<td>4. 10:00 AM - The Highly Effective EMI Shielding Materials for Magnetic and Electric Wave Over the Wide Range of Frequency in Near Field</td>
<td>4. 10:00 AM - The How and Why of Biased Humidity Tests with Copper Wire</td>
<td>4. 10:00 AM - Peridynamics for Predicting Thermal Expansion Coefficient of Graphene</td>
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<tr>
<td>5. 10:25 AM - Low-Loss NCF Material for High-Frequency Device</td>
<td>5. 10:25 AM - In-Situ Photoelastic Measurement of Temperature Dependent Stresses in Copper Through-Glass Via (TG Via) Substrate</td>
<td>5. 10:25 AM - Machine Learning to Improve Accuracy of Warpage Simulations in Ultra-Thin Packages</td>
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<tr>
<td>6. 10:50 AM - In-Situ Redox Nanowelding of Copper Nanowires with Surficial Oxide Layer as Solder for Flexible Transparent Electromagnetic Interference Shielding</td>
<td>6. 10:50 AM - Mechanical Properties and Microstructural Fatigue Damage Evolution in Cyclically Loaded Lead-Free Solder Joints</td>
<td>6. 10:50 AM - Study on Warpage of Fan-Out Panel Level Packaging (FO-PLP) Using Gen-3 Panel</td>
</tr>
<tr>
<td>Xianwen Liang, Jianwen Zhou, Gang Li, Tao Zhao, Pengli Zhu, Rong Sun – Shenzhen Institutes of Advanced Technology; Ching-Ping Wong – Georgia Institute of Technology</td>
<td>Sinan Su, Md Mahmudur Chowdhury, Mohd Aminul Hoque, S’a’d Hamasha, Jeffrey C. Suhling, John Evans, Pradeep Lall – Auburn University</td>
<td>Faxing Che, Kaz Yamamoto, Srinivas Rao Vempati, Nagendra Sekhar Varasala – Institute of Microelectronics</td>
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<tr>
<td>7. 11:15 AM - High Conductive Compartment EMI Shielding Material with Jet-Dispensing Technology</td>
<td>7. 11:15 AM - Improving Reliability of SI Fabric (Si-IF)</td>
<td>7. 11:15 AM - Mechanical Properties of Intermetallic Compounds at Elevated Temperature by Nanoindentation</td>
</tr>
<tr>
<td>Xuan Hong, Qizhuo Zhao, Xinpei Cao, Dan Maslyk, Juliet Sanchez – Henkel Corporation</td>
<td>Niloofar Shakoorkazadeh, Shwa Chandra Jangam, Pranav Ambhore, Han Chien, Amir Hannah, Subramanian Iyer – University of California</td>
<td>Fan Yang, Sheng Liu, Zhwen Chen – Wuhan University; Zhaoxia Zhou, Cariyu Liu, Stuart Roberson, Chinging Liu – Loughborough University; Li Liu – Wuhan University of Technology</td>
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**Refreshment Break: 9:15-10:00 a.m.**
### Program Sessions: Thursday, May 30, 1:30-5:10 p.m.

<table>
<thead>
<tr>
<th>Session 19: MEMS, Sensors, &amp; IoT</th>
<th>Session 20: Fan-Out and Heterogeneous Integration</th>
<th>Session 21: 5G, mm-Wave and Antenna-in-Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Packaging Technologies</td>
<td>Committee: Interconnections</td>
<td>Committee: High-Speed, Wireless &amp; Components</td>
</tr>
</tbody>
</table>

**Session 1: 1:30 PM - A MEMS-Microphone in a Fan-Out Wafer Level Package**


**Session 2: 1:55 PM - Fan-Out Wafer Level Packaging - A Platform for Advanced Sensor Packaging**

Tanja Braun, Karl-Friedrich Becker, Ole Holck, Ruben Kahle, Pascal Graap, Markus Wohrmann, Rolf Aschenbrenner – Fraunhofer IZM; Steve Veges, Marc Dreissigacker, Klaus-Dieter Lang – Technical University Berlin

**Session 3: 2:20 PM - 3D-MID Evaluation and Validation for Space Applications**

Ettene Hirt, Klaus Ruzicka – Art of Technology AG; Benedikt Wigger, Maximilian Barth, Rafet Salih, Florian Janek – Hahn-Schickard; Ernst Muller – Institute for Microintegration, University of Stuttgart

**Session 4: 3:30 PM - High-Temperature Pressure Sensor Package and Characterization of Thermal Stress in the Sensor and Operation up to 500 °C**

Nilavazhagan Subbiah, Qingming Feng, Kevin Ali Beltran Ramirez, Juergen Wilde – University of Freiburg, IMTEK; Gudrun Bruckner – CTR AG

**Session 5: 3:55 PM - Development of 3D WLCSP With Black Shielding for Optical Finger Print Sensor for the Application of Full Screen Smart Phone**

Daqian Yu, Yichao Zou, Xin Xu, Aihua Shi, Zhiyi Xiao – Huatian Technology (Kunshan) Electronics Co., Ltd.

**Session 6: 4:20 PM - Micro Fountain-Like Resonators**

Jianfeng Zhang, Jintang Shang, Bin Luo, Zhaoxi Su – Southeast University

**Session 7: 4:45 PM - Novel Additively Manufactured Packaging Approaches for 5G/mm-Wave Wireless Modules**

Tong-Hong Lin, Alile Ed, Jimmy Hester, Bijn Tehran, Manos Tentzeris – Georgia Institute of Technology; J. Bto – Texas Instruments, Inc.

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**Refreshment Break: 2:45-3:30 p.m.**

**Session 8: 4:30 PM - Next-Generation of 2 to 7 Micron Ultra-Small Microvias for 2.5D Panel Redistribution Layer by Using Laser and Photolithography Technologies**

Fuhan Liu, Chandrasekharan Nair, Atom Watanabe, Bart H. DeProspo, Rao R. Tummala – Georgia Institute of Technology; Atsushi Kubo – Tokyo Ohka Kogyo Co., Ltd.

**Session 9: 4:30 PM - Advanced Wafer Level Package Solutions for 60GHz WiGig (802.11ad)**

Dapeng Wu, Robin Dahlskog, Erik Ojefors, Mats Carlsson – Sivers IMA AB

**Session 10: 4:30 PM - Advanced Fan-Out Wafer Level Packaging**


**Session 11: 4:30 PM - Multiple RDL on Fan-Out Packages**

Gahui Kim, Kiran Son, Dogeun Kim, Young-Bae Park – Andong National University; Seok-Hyun Lee – Samsung Electronics Company, Ltd.

**Session 12: 4:35 PM - Antenna and Module Design Considerations on the Interfacial Adhesion of Cu RDL for Fan-Out Wafer Level Packaging**

Chun-Chia Chu, Cheng-Yu Ho, Shun-Pu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.

**Session 13: 4:40 PM - Effects of Dielectric Curing Conditions on the Interfacial Adhesion of Cu RDL for Fan-Out Wafer Level Packaging**

Gahui Kim, Kiran Son, Dogeun Kim, Young-Bae Park – Andong National University; Seok-Hyun Lee – Samsung Electronics Company, Ltd.

**Session 14: 4:45 PM - Novel Additively Bonding With Sub-mm Alignment Accuracy for Millimeter Wave SiGe BiCMOS Wafer Level Packaging and Heterogeneous Integration**

Christian Wipf, Mehran Kaynak – Innovations for High Performance Microelectronics; Bernhard Rebhan, Peter Keperesi, Helmut Kurz, Gerald Silberer, Josef Meiler – EV Group, Inc.

**Session 15: 4:45 PM - Integrated Compact Planar Inverted-F Antenna (PIFA) With a Shorting Via Wall for Millimeter-Wave Wireless Chip-to-Chip (C2C) Communications in 3D-SiP**

Sheng-Chi Hsieh, Lucus Chu, Cheng-Yu Ho, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.
### Program Sessions: Thursday, May 30, 1:30-5:10 p.m.

<table>
<thead>
<tr>
<th>Session 22: Advanced Substrates and Interconnect Technology</th>
<th>Session 23: High Bandwidth 3D &amp; Photonics Integration</th>
<th>Session 24: Advancements in Solder Joint Characterization and Reliability Evaluation</th>
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<tbody>
<tr>
<td><strong>Committee:</strong> Materials &amp; Processing</td>
<td><strong>Committee:</strong> Interconnection joint with Photonics</td>
<td><strong>Committee:</strong> Applied Reliability</td>
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<tr>
<td><strong>Session Co-Chairs:</strong></td>
<td></td>
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<tr>
<td>Mikkel Miller</td>
<td>Bingyou Zhang</td>
<td>Scott Savage</td>
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<tr>
<td>EMD Performance Materials</td>
<td>Broadcom, Inc.</td>
<td>Medtronic Microelectronics Center</td>
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<td>Email: <a href="mailto:dingyouzhang.brcm@gmail.com">dingyouzhang.brcm@gmail.com</a></td>
<td>Email: <a href="mailto:scott.savage@medtronic.com">scott.savage@medtronic.com</a></td>
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<tr>
<td>Kimberly Yess</td>
<td>Takaaki Isigwe</td>
<td>Pei-Haw Tsao</td>
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<tr>
<td>Brewer Science, Inc.</td>
<td>Keio University</td>
<td>Taiwan Semiconductor Manufacturing Company, Ltd.</td>
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<td>Email: <a href="mailto:isigwe@apji.keio.ac.jp">isigwe@apji.keio.ac.jp</a></td>
<td>Email: <a href="mailto:PHTSAO@tms.com">PHTSAO@tms.com</a></td>
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<tr>
<th>1. 1:30 PM - Temporary SiC-SiC Wafer Bonding Compatible with High Temperature Annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fengwen Pu, Tadatomo Suga, National University of Tokyo; Miyuki Uomoto, Takehito Shimatsu – Tohoku University</td>
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<tr>
<th>2. 1:55 PM - Ultra-Thin Glass to Ultrathin Glass Bonding Using Laser Sealing Approach</th>
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<tr>
<td>Messaoud Bedjou, Jean Brun, Johnny Amirian – CEA-LETI</td>
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<tr>
<th>3. 2:20 PM - Development of Resins for Bumpless Interconnections and Wafer-On-Wafer (OWOW) Integration</th>
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</thead>
<tbody>
<tr>
<td>Naoko Araki, Shoji Maetani – Daicel Corporation; Young Suk Kim, Soichi Kodama – DISCO Corporation; Ch. Hsiao, H. Chang, C. Lin – Industrial Technology Research Institute; Takayuki Ohba – Tokyo Institute of Technology</td>
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<tr>
<th>4. 3:30 PM - Development of Novel Photosensitive Dielectric Material for Reliable 2.1D Package</th>
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<tr>
<th>5. 3:55 PM - An Advanced Solder Resist with Strong Adhesion and High Resolution for High-Density Packaging</th>
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<tr>
<th>6. 4:20 PM - Solution of Warpage Behavior for Ultra-Thin FC-FCSP by Control of EMC Properties</th>
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<tbody>
<tr>
<td>Chika Arayama, Takahiro Akashi, Yasunari Tomita, Naoki Kanagawa – Panasonic Corporation</td>
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<tr>
<th>7. 4:45 PM - Innovative Socketable and Surface-Mountable BGA Interconnections</th>
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<tr>
<td>Omikar Gupte, Kratse Teoh, Vanessa Smet, Rao Tummala – Georgia Institute of Technology</td>
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**Refreshment Break: 2:45-3:30 p.m.**

<table>
<thead>
<tr>
<th>1. 1:30 PM - A Highly Reliable 1.4um Pitch Via-Last TSV Module for Wafer-to-Wafer Hybrid Bonded 3D-SOC Systems</th>
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</thead>
<tbody>
<tr>
<td>Stefaan Van Huylenbroeck, Joeri De Vos, Ziad El-Mekki, Geraldine Jameson, Nina Tutunyuan, Karthik Muga, Michele Succhi, Andy Miller, Gerald Beyer, Eric Beyne – IMEC</td>
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<tr>
<th>2. 1:55 PM - Nanoscale Topography Characterization for Direct Bond Interconnect</th>
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<tr>
<td>Bongsub Lee, Pawel Mirozek, Gill Fountain, John Posthill, Jeremy Theil, Rajesh Katkar, Laura Mirkarimi – Xpen University</td>
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<tr>
<th>3. 2:20 PM - Fabrication and Carbon-Based Interconnects for 3D ICs</th>
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<tbody>
<tr>
<td>Andreas Nylander, Marlene Bornmann, Yifeng Fu, Andrei Voroblev, Johan Liu – Chalmers University of Technology; Jie Zhao, Zhibin Zhang – Uppsala University</td>
</tr>
</tbody>
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<tr>
<th>4. 3:30 PM - 3D Silicon Photonics Interposer for Tb/s Optical Interconnects in Data Centers with Double-Side Assembled Active Components and Integrated Optical and Electrical Through Silicon Via on SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bogdan Siru, Yann Eichhammer, Oppermann Herrman, Tolga Tekin – Fraunhofer Institute for Reliability and Microintegration; Victor Salorov, Jochen Kraft – AMS AG; Xin Yin, Johan Bawinkel – Interuniversitair Micro-Electronica Centrum IMEC; Christan Neumeyer – VERTILAS GmbH; Francesco Soraci – Fraunhofer Heinrich-Hertz Institute</td>
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<tr>
<th>5. 3:55 PM - Flip-Chip III-V-to-Silicon Photonics Interfaces for Optical Sensor</th>
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<tr>
<td>Yves Martin, Jason S. Orcutt, Chi Xiong, Laurent Schaies, Tymon Barwicz, Martin Glodde, Swetha Kanlapurkar, Eric J. Zhang, William M. J. Green – IBM Corporation; Victor Dolores-Calzadilla, Ariane Sigmund, Martin Moehle – Fraunhofer Heinrich-Hertz Institute</td>
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<tr>
<th>6. 4:20 PM - Extremely Low-Profile Single Mode Fiber Array Coupler Suitable for Silicon Photonics</th>
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<tr>
<td>Mitsuharu Hirano, Akira Furuya, Hideki Machida, Koichi Koyama, Yasunori Murakami, Kazunori Tanaka – Sumitomo Electric Industries, Ltd.</td>
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<tr>
<th>7. 4:45 PM - Micro Lens Array Assembly for Optical Organic Substrates</th>
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<tbody>
<tr>
<td>Patrick Jacques, Richard Langlois – IBM Bromont; Koji Maseuda, Masao Tokunari, Hsiang Han Hsu – IBM Tokyo Research Lab; Paul Fortier – IBM Corporation</td>
</tr>
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<tr>
<th>8. 5:00 PM - A Study of Various Substrate Models and its Effect on Board-Level Solder Joint Reliability</th>
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</thead>
<tbody>
<tr>
<td>Van Lai Pham, Huayan Wang, Jiequng Xu, Vishnu Veeraraghavan, Seungbea Park – Binghamton University; Yuling Ni – Qualcomm Technologies, Inc.; Charandeep Singh – Coming, Inc.</td>
</tr>
</tbody>
</table>
Program Sessions: Friday, May 31, 8:00-11:40 a.m.

Session 25: Wafer Level Packaging Fan-In-Fan-Out Structure and Materials
Committee: Packaging Technologies

Session Co-Chairs:
Albert Lan
Applied Material, Inc.
Email: Albert.Lan@amat.com

Christophe Zinck
Advanced Semiconductor Engineering Inc.
Email: Christophe.zinck@aseeu.com

1. 8:00 AM - 3D Fan-Out Package Technology with Photosensitive Through Mold Interconnects
Kenitaru Mori, Sochi Yamashita, Takafumi Fukuda, Masahiro Sekiguchi, Hirokazu Ezawa, Shuzo Akejma – Toshiba Electronic Devices and Storage Corporation

2. 8:25 AM - Effects of the Materials Properties of Epoxy Molding Films (EMFs) on Fan-Out Packages (FOPs) Characteristics

3. 8:50 AM - Mechanism of Moldable Underfill (MUF) Process for RDL-1st Fan-Out Panel Level Packaging
Lin bu, Faxing Che, Vempati Srinivasa Rao, Xiaowu Zhang – Institute of Microelectronics

4. 10:00 AM - Study of the Board Level Reliability Performance of a Large 0.3 mm Pitch Wafer Level Package
Bernd Waidhas, Jan Porschwitz, Christoph Pietryga, Thomas Wagner, Beth Keser – Intel Corporation

5. 10:25 AM - Study of Board Level Reliability of eWLB (Embedded Wafer Level BGA) for 0.35mm Ball Pitch
Seung Wook Yoon, Yeow Kheng Lim, Seng Guang Chow, Kang Hae Lee, NW Lu, YenYao Chi, Benson Lin – STATS ChipPAC Pte. Ltd.

6. 10:50 AM - Board Level Reliability Study of Fan-Out Single Die Package With 350um Bump Pitch
Chieh Lung Lai, Gu Yan Lin, Tz Yuan Chao, Chun Hung Lu, Yih Sin Chen, Feng Lung Chen – Siliconware Precision Industries Co., Ltd.

7. 11:15 AM - The Analysis for Bump Resistance Improvement by Optimizing the Sputter Condition

Session 26: High-Speed Signaling for HPC and Memory
Committee: High-Speed, Wireless & Components

Session Co-Chairs:
Rockwell Hsu
Cisco Systems, Inc.
Email: rohss@csco.com

Jaemin Shin
Qualcomm Technologies, Inc.
Email: jaemins@qti.qualcomm.com

1. 8:00 AM - Hybrid Prepreg Conventional Build-Up Laminate for 112Gbit/s SerDes

2. 8:25 AM - PI/SI Analysis and Design Approach for HPC Platform Applications
Sungwook Moon, Chamin Jo, Seungki Nam – Samsung Electronics Company, Ltd.

3. 8:50 AM - PoP LPDDR5 (6.4 Gbps) NTODT and 1-Tap DFE for Signal Integrity Enhancement
Sunil Gupta – Qualcomm Technologies, Inc.

4. 10:00 AM - OpenCAPI Memory Interface Signal Integrity Study for High-Speed DDR5 Differential DIMM Channel With Standard Loss FR-4 Material and SNIA SFF-TA-1002 Connector
Biao Ca, Jose Heggie, Kyle Giesen, Jyunan Tang, Brian Connolly, Kyu Hyoung Kim, Daniel Drees – IBM Corporation; Zheng Fan, Rocky Huang, Luyun Yi, Qiao Qi Chen, Yifan Huang, Stephen Smith – Amphenol ICC

5. 10:25 AM - Effectiveness of Equalization and Performance Potential in DDR5 Channels with RDI/MM(s)
Nanju Na, Thomas To – Xilinx, Inc.

6. 10:50 AM - Inductive Link for 3D Stacked Chip to Chip Communication
Xiao Sun, Nicolas Pantano, Soon-Wook Kim, Geert Van der Plas, Eric Beyne – imec

7. 11:15 AM - System Co-Design of a 600V GaN FET Power Stage With Integrated Driver in a QFN System-in-Package (QFN-SIP)
Jie Chen, Yong Xie, Trombley Django, Rajen Murugan – Texas Instruments, Inc.

Session 27: Advanced Biosensors and Bioelectronics
Committee: Emerging Technologies

Session Co-Chairs:
Zhuo Li
Fudan University
Email: zhuo.li@fudan.edu.cn

Jimin Yao
Intel Corporation
Email: jimin.yao@intel.com

1. 8:00 AM - Microfabricated Biodissolvable Probe for Electrical Neural Signal Recording
Sayaj Bhuvanendran, Nair Gourikutty, Ruta Lim – Institute of Microelectronics, A*STAR

2. 8:25 AM - Stretchable, Implantable Nanomembrane Biosensor for Wireless, Real-Time Monitoring of Hemodynamics
Robert Herbert, Woon-Hong Yeo – Georgia Institute of Technology

3. 8:50 AM - A Wearable Passive pH Sensor for Health Monitoring
Sakai Mondal, Saranraj Karuppuswami, Rachel Steinhornst, Premjeet Chahal – Michigan State University

4. 10:00 AM - Novel Packaging Structure and Processes for Micro–Size Thin Film Batteries (TFB) to Enable Miniaturized Healthcare Internet-of-Things (IoT) Devices

5. 10:25 AM - Printed Temporary Tattoo for Skin-Mounted Electronics
Sammul Tuominen, Päivi Marttusalo – Tampere University

6. 10:50 AM - Thermoset Polymers for Bioelectronic Interfaces: Engineering of Thermomechanical Properties
Alexandra Joshi-Irmé, Walter E. Voit, Joseph J. Pancrazio, Melanie Ecker – The University of Texas at Dallas
Program Sessions: Friday, May 31, 8:00-11:40 a.m.

Session 28: Embedded Substrates and Integrated Technologies

Committee: Assembly and Manufacturing Technology

Session Co-Chairs:
Christia Bojkov
Qorvo, Inc.
Email: cbojkov@qorvo.com
John H. Lau
ASM Pacific Technology
Email: John.lau@asmpt.com

Wefeng Liu, William Uy, Alex Chan, Dongkai Shangguan – Flex, Ltd.; Andy Behr, Takatoshi Abe, Tomohiro Fukao – Panasonic Corporation

1. 8:00 AM - Development of Flexible Hybrid Electronics Using Reflow Assembly with Stretchable Film
   Wefeng Liu, William Uy, Alex Chan, Dongkai Shangguan – Flex, Ltd.; Andy Behr, Takatoshi Abe, Tomohiro Fukao – Panasonic Corporation

2. 8:25 AM - Highly Compact RF Transceiver Module using High Resistive Silicon Interposer With Embedded Inductors and Heterogeneous Dies Integration
   Gabriel Pares, Jean-Philippe Michel, Edouard Deschaux, Pierre Ferris, Ayssar Serhan, Alexandre Giry – CEA-LETI

3. 8:50 AM - Process Induced Wafer Warpage Optimization for Multi-Chip Integration on Wafer Level Molded Wafer
   Yi-Pin Chou, Tsung-Chu Chiou, Hsiang-Yi Hsu, Chih-Lung Chiu – National Taiwan University; Chao-Shung Chou, Chia-Yi Chen, Yu-Cheng Hsu – Powerchip Corporation

4. 10:00 AM - Improvement Structure for Package Substrate with Embedded Thin Film Capacitor
   Tomoyuki Akahoshi, Daisuke Mizutani – Fujitsu Laboratories, Ltd.; Kei Fukui, Shogo Yamazaki, Hidehiko Fujisaki – Denko Corporation of Technology; Pulugurtha Markondeya – Florida State University; Aurangzeb Shawl, Alantu Shao, Wei-Ju Su, Wei-Tsung Lin – Advanced Micro Devices, Inc.

5. 10:25 AM - 3D Packaging with Embedded High-Power-Density Passives for Integrated Voltage Regulators
   Teng Sun, Robert Spumey, Atomy Watanabe, Himani Shama, Ruo Hee Lee, Viso Lin, Chang-Fu Lin, C. Key Chung – Siliconware Precision Industries Co., Ltd

6. 10:50 AM - A Novel Panel Level Double Side-Embedded Package for Small Size Power Devices
   Kupeng Ding, Mian Huang – Shenzhen Siptory Technology Co., Ltd.; Zhichao Wu, Jian Cai – National Tsing Hua University; Weifeng Liu, William Uy, Alex Chan, Dongkai Shangguan – Flex, Ltd.; Takanori Kojima – Denko Corporation of Technology; Pulugurtha Markondeya – Florida State University; Aurangzeb Shawl, Alantu Shao, Wei-Ju Su, Wei-Tsung Lin – Advanced Micro Devices, Inc.

7. 11:15 AM - EMI Shielding on Electronic Packages Realized by Electrolytic Plating
   Mustafa Oezkoek, Eckart Klusmann, Sven Lamprecht – Atootech Germany GmbH; Katharina Kreftt, – Qualcomm Technologies, Inc.

Session 29: Electromigration and Innovative Reliability Test Methods

Committee: Applied Reliability

Session Co-Chairs:
Keith Newman
Advanced Micro Devices, Inc.
Email: keith.newman@amd.com
Pilin Liu
Intel Corporation
Email: pilin.liu@intel.com

1. 8:00 AM - Effect of Intermetallic Compound Growth on Electromigration Failure Mechanism in Low-Profile Solder Joints

2. 8:25 AM - Effect of Grain Orientation and Microstructure Evolution on Electromigration in Flip-Chip Solder Joint
   Xing Fu, Ruoho Yao – South China University of Technology; Yunfei En, Bin Zhou, Si Chen, Yun Huang – CEPREI

3. 8:50 AM - Highly (111)-Oriented Nanotwinned Cu for Redistribution Lines in 3D IC With High Electromigration Resistance
   I-Hsin Tseng, Chih-Han Tseng, Yu-Jin Li – National Chiao Tung University; Benson Lin, Chia-Cheng Chang – MediaTek, Inc.

4. 10:00 AM - Non-Destructive Failure Analysis of Various Chip to Package Interaction Anomalies in FC-BGA Packages Subjected to Temp Cycle Reliability Testing

5. 10:25 AM - Assessment of Accelerometer versus LASER for Board Level Vibration Measurements
   Varun Thukral, Maileh Cahu, Jeroen Zaal, Jeroen Jalink, Romuald Roucou, Rene Rongen – NXP Semiconductors

6. 10:50 AM - Effect of Process Parameters on the Long-Run Print Consistency and Material Properties of Additively Printed Electronics
   Pradeep Lall, Armit Abrol, Naluki Kohari, Jeff Suhling – Auburn University

7. 11:15 AM - A Viscoelastic-Based Fatigue Reliability Model for the Polyimide Dielectric Thin Film
   Yu-Chen Chang, Tz-Cheng Chu – National Cheng Kung University; Yu-Ting Yang, Yi-Hsiao Tseng, Xi-Hong Chen – Advanced Semiconductor Engineering, Inc.

Session 30: Assembly and Process Modeling

Committee: Thermal/Mechanical Simulation & Characterization

Session Co-Chairs:
Suresh K. Sitaraman
Georgia Institute of Technology
Email: suresh.sitaraman@me.gatech.edu
Kuo-Ning Chiang
National Tsinghua University
Email: knchiang@pme.nthu.edu.tw

1. 8:00 AM - Explicit FE Failure Prediction of Interfaces and Interconnect in Potted Electronics Assemblies Subject to High-G Acceleration Loads
   Pradeep Lall, Kalyan Domala – Auburn University; John Deep – Air Force Research Laboratory; Ryan Lowe – ARA

2. 8:25 AM - Numerical Simulation on the Formation Process of Metal Droplets by Pneumatic Diaphragm Drop-On-Demand Technology
   Kun Ma, Sheng Liu, Zhwen Chen, Churui Wang, Li Liu – Wuhan University of Technology

3. 8:50 AM - On the Curing-Induced Residual Stresses After Molding Processes: Mold Shrinkage, Chemical Shrinkage or Both?
   Bongsae Han, Changsu Kim, Sukrut Phansalkar – The University of Maryland

4. 10:00 AM - Realistic Solder Joint Geometry Integration with Finite Element Analysis for Reliability Evaluation of Printed Circuit Board Assembly
   Chun Sean Lau, Ning Ye, Hem Takiar – Western Digital Corporation

5. 10:25 AM - Multi-Physics Modelling and Experimental Investigation – An Original Approach for Laser-Dicing/Grooving Process Optimization
   Jeff Mouroujadji, Dominique Drouin – University of Sherbrooke; Oswaldo Chacon, Francis Santerre – IBM Corporation

6. 10:50 AM - Thermal Characteristics of Vertically Integrated GaN/SiC-on-Si Assemblies: A Comparative Study
   Kimmo Raslainen, Christian Fager – Chalmers University of Technology; Per Ingeljag, Peter Melin – Ericsson AB; Torbjorn M. J. Nilsson – Saab AB; Matthias Thorsell – Chalmers University of Technology

Refreshment Break: 9:15-10:00 a.m.

4. 10:00 AM - Non-Destructive Failure Analysis of Various Chip to Package Interaction Anomalies in FC-BGA Packages Subjected to Temp Cycle Reliability Testing

5. 10:25 AM - Assessment of Accelerometer versus LASER for Board Level Vibration Measurements

6. 10:50 AM - Effect of Process Parameters on the Long-Run Print Consistency and Material Properties of Additively Printed Electronics

7. 11:15 AM - A Viscoelastic-Based Fatigue Reliability Model for the Polyimide Dielectric Thin Film

8. 11:40 AM - Comprehensive Investigation on Warpage Management of FOPLP with Multi Embedded Ring Designs
   Chang-Chun Lee, Yan-Yu Liu, Pe-Chen Huang – National Tsing Hua University; Fussen Hsu, Puru Bruce Lin, Cheng-Ta Ko, Yu-Hua Chen – Unimicron Technology Corporation
### Program Sessions: Friday, May 31, 1:30-5:10 p.m.

<table>
<thead>
<tr>
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<td><strong>Committee:</strong> Packaging Technologies</td>
<td><strong>Committee:</strong> Assembly and Manufacturing Technology</td>
<td><strong>Committee:</strong> Thermal/Mechanical Simulation &amp; Characterization</td>
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<td><strong>Session Co-Chairs:</strong></td>
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<td>Young-Gon Kim</td>
<td>Habib Hichri</td>
<td>Han Young Jeon</td>
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<td>Integrated Device Technology, Inc.</td>
<td>SUSS MicroTec Photonic Systems, Inc.</td>
<td>SUSS MicroTec, Inc.</td>
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<tr>
<td>Email: <a href="mailto:Young.Kim@idt.com">Young.Kim@idt.com</a></td>
<td>Email: <a href="mailto:Hichri@suss.com">Hichri@suss.com</a></td>
<td>Email: <a href="mailto:hichri@suess.com">hichri@suess.com</a></td>
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<td>Kuo-Chung Yee</td>
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<td>Taiwan Semiconductor Manufacturing Company Ltd.</td>
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<td>Email: <a href="mailto:kceyee@tsmc.com">kceyee@tsmc.com</a></td>
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<tr>
<td><strong>1. 1:30 PM - Development of High Power and High Junction Temperature SiC Based Power Packages</strong></td>
<td><strong>1. 1:30 PM - An RDL-First Fan-Out Panel Level Package for Heterogeneous Integration Applications</strong></td>
<td><strong>1. 1:30 PM - A Sequential Finite Volume Method / Finite Element Analysis of a Power Electronic Semiconductor Chip</strong></td>
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<tr>
<td><strong>3. 2:20 PM - Innovative Flip-Chip Package Solutions for Automotive Applications</strong></td>
<td><strong>3. 2:20 PM - High-Density Flexible Substrate Technology with Thin-Chip Embedding and Partial Carrier Release Option for IoT and Sensor Applications</strong></td>
<td><strong>3. 2:20 PM - Thermal Cycling Simulation and Sensitivity Analysis of Wafer Level Chip Scale Package with Integration of Metal-Insulator-Metal Capacitors</strong></td>
</tr>
<tr>
<td>Tom Tang, Dawid Ho, Mark Liao, Jensen Tsai, Yu-Po Wang, Boxiang Fang – Siliconware Precision Industries Co., Ltd.</td>
<td>Kai Zoschke, Piotr Mackowiak, Ha-Duong Ngo, Christian Tschoban, Carola Fritsche, Kevin Kröhner, Thorsten Fischer, Ivan Ndp – Fraunhofer IZM; Klaus-Dieter Lang – Technical University Berlin</td>
<td>Yong Liu, Bill Chen – ON SEMICONDUCTOR; Yi Zhou, Suresh K. Starasman – Georgia Institute of Technology</td>
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<tr>
<td><strong>4. 3:30 PM - Reliability of Laminated Bond Structure Using (Cu,Ni)/Sn TLP Bonding With AI Interlayer for High-temperature Power Electronics Packaging</strong></td>
<td><strong>4. 3:30 PM - Advance Embedded Packaging for Power Discrete Device</strong></td>
<td><strong>4. 3:30 PM - Effect of Time-Dependent Bulk Modulus on Reliability Assessment of Automotive Electronic Control Unit</strong></td>
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<tr>
<td><strong>5. 3:55 PM - Silver Sintering on Organic Substrates for the Embedding of Power Semiconductor Devices</strong></td>
<td><strong>5. 3:55 PM - Large Panel Size Bonder with High Performance and High Accuracy</strong></td>
<td><strong>5. 3:55 PM - Thermal and Mechanical Simulations for Fan-out Wafer-Level Packaging Technology: Introduction of a &quot;Solder Heatsink&quot;</strong></td>
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<tr>
<td>Alexander Schiffmacher, Lorenz Litsenberger, Juergen Wilde – University of Freiburg, IMTEK; Till Huesgen – Hochschule Kempten, University of Applied Science</td>
<td>Hubert Selhofer, Hugo Pristauz, Andreas Playr – Besi Austria GmbH</td>
<td>Loic Marmat, Mathilde Cartier, Gabriel Pares, Dominique Noguet – CEA-LETI</td>
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<tr>
<td><strong>7. 4:45 PM - Pb-Free, High Thermal and Electrical Performance Driven Die Attach Material Development for Power Package</strong></td>
<td><strong>7. 4:45 PM - Study of the Properties of AlN PMUT used as a Wireless Power Receiver</strong></td>
<td><strong>7. 4:45 PM - Ultra-thin Package Board Level Drop Impact Modeling and Validation</strong></td>
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<td>Dwayne Shirley</td>
<td>Craig Gaw</td>
<td>Craig Danovitch</td>
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<td>Email: <a href="mailto:dwayne.shirley@ieee.org">dwayne.shirley@ieee.org</a></td>
<td>Email: <a href="mailto:c.gaw@ieee.org">c.gaw@ieee.org</a></td>
<td>Email: <a href="mailto:ksakuma@us.ibm.com">ksakuma@us.ibm.com</a></td>
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<td>1. 1:30 PM - Flexible Graphene-Glass Fiber Composite Film with Ultra-High Thermal Conductivity and Mechanical Strength as Highly Efficient Thermal Interface Materials</td>
<td>1. 3:30 PM - Development of 2.3D High Density Organic Package Using Low Temperature Bonding Process with Sn-Bi Solder</td>
<td>1. 3:30 PM - Multilayer Trench Decoupling Capacitor Using Stacked Layers of BST and LNO</td>
</tr>
<tr>
<td>Nan Wang, Lilei Ye – SHT Smart High Tech AB; Shuqin Chen – Shanghai University; Johan Liu – Chalmers University of Technology</td>
<td>Shota Miki, Hiroshi Taneda, Naoki Kobayashi, Kyoshi Oi, Koji Nagai, Toshinori Koyama – Shinko Electric Industries Co., Ltd.</td>
<td>Todd Schumann, Sheng-Po Fang, Yong-Kyu Yoon – University of Florida; Jongmin Yook, Dongu Kim – Korea Electronics Technology Institute</td>
</tr>
<tr>
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<td>Pranav Ambohore, Boris Vaibsd, Umesha Mogera, Ujash Shah, Timothy Fisher, Mark Goorsky, Subramoniam Iyer – University of California Los Angeles</td>
<td>Todd Hamilton, Je Chen, Rajen Murugan – Texas Instruments, Inc.</td>
</tr>
<tr>
<td>3. 2:20 PM - Design of Mixed Spherical and Platelet h-BN Particles Filled Polymer-Based Thermal Interface Material for Power Electronics with Enhanced Thermal Conductivity by Finite Element Modeling and Experimental Characterization</td>
<td>3. 2:20 PM - Interconnect Scheme for Die-to-Die and Die-to-Wafer Level Heterogeneous Integration for High-Performance Computing</td>
<td>3. 2:20 PM - Integrating Solid-State Protection With a RF-MEMS Switch for Achieving ESD Robustness</td>
</tr>
<tr>
<td>4. 3:30 PM - Wafer-Level Integration of Thin Silicon Bare Dies within Flexible Label</td>
<td>4. 3:30 PM - Ultra-Wide Micro Bumps Interconnection Matrix for High-Energy Particle Detection: Process and Assembly</td>
<td>4. 3:30 PM - A “Zero Height” Small-Size Low-Cost RF Interconnect Substrate Technology for RF Front Ends For M.2 Modules and Sip</td>
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<tr>
<td>Mohammed Alhendi, Darshana Weerawarge, Jack Lombardi, Mark Poliks – Binghamton University; Azar Aizadeh – General Electric</td>
<td>Ning Zhao, Shi Chen, Yunpeng Wang, Haitao Ma – Dalian University of Technology, C.M.L. Wu – City University of Hong Kong</td>
<td>Claudio Alvarez, Mohamed Bellarej, Madhavan Swaminathan – Georgia Institute of Technology</td>
</tr>
<tr>
<td>6. 4:20 PM - In-Situ investigation of Organic Additive Interactions in Copper Electroplating Solutions with Surface Enhanced Raman Spectroscopy (SERS)</td>
<td>6. 4:20 PM - Development of a No Reflow Cu Pillar Bump to Improve Chip/Package Interconnection Performance</td>
<td>6. 4:20 PM - RF Inductors Integrated in Organic Packaging</td>
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Wednesday, May 29, 2019
Session 37: Interactive Presentations 1
Time: 9:00 AM – 11:00 AM
Committee: Interactive Presentations
Session Co-Chairs:
Nam Pham
IBM Corporation
Email: npham@us.ibm.com
Pavel Roy Paladhi
IBM Corporation
Email: Pavel.Roy.Paladhi@ibm.com

Comprehensive Solution for Micro Bump Capanility Control

Structural Enhancement for a CMOS-MEMS Microphone Under Thermal Loading by Taguchi Method
Chun-Lin Lu, Meng-Kao Yeh – National Tsing Hua University

A Methodology to Correct In-Fixture Measurement of Impedance by a Machine Learning Model
Bo-Siang Fang, Cha-Chui Lai, Ying-Wei Lu, Kuan-Ta Chen, Don-Son Jiang – Siliconware Precision Industries Co., Ltd.

Material and Structure Design Optimization for Panel-Level Fan-Out Packaging
Dao-Long Chen – Advanced Semiconductor Engineering, Inc.

A High Entropy Alloy as Very Low Melting Point Solder for Advanced Electronic Packaging
Li Pu, Xiuchen Zhao, Zhiqunghua Hou – Beijing Institute of Technology; Quanfeng He, Yong Yang – City University of Hong Kong; King-Ning Tu – City University of California, Los Angeles

A Versatile Fan-Out Infrastructure Based on Die-Stencil Substrate Promoted by an Advanced Multifunctional Temporary Bonding Material
Xiao Liu, Baron Huang, Hong Zhang, Lisa Kirchner, Rama Pulgadda, Tony Fiam – Brewer Science, Inc.

Low-Temperature and Pressureless Microfluidic Electrosol Bonding Process for Vertical Interconnections
H. T. Hung, S. Yang, T. A. Wu, C.R. Kao – National Taiwan University; Y. H. Chen – Unimicron Technology Corporation

3D Integration of CMOS-Compatible Surface Electrode Ion Trap and Silicon Photonics for Scalable Quantum Computing
Jing Tao, Yu Dian Lim, Nam Pham Chiew – Nanyang Technological University; Yong Yu Li, Anak Agung Alt Apriyana, Lin Bu – IME-STAR; Peng Zhao, Chuan Seng Tan – Nanyang Technological University; Luca Guidioni – University Paris Diderot

RTD Sensor Based Approach for Maintaining Thermal Uniformity During TCB Process
Salwa Ben Jemaa, Julien Sylvestre – University of Sherbrooke; Pascale Gagnon, IBM

Fully-Filled, Highly-Reliable Fine-Pitch Interposers with TSV Aspect Ratio >10 for Future 3D-LSI/IC Packaging

Wireless Transfer of Power and Data via a Single Resonant Inductive Link
Yi-Chen Hsieh, Li-Ting Hwang, Shiang-Hwa Yu – National Sun Yat-Sen University

Adaptive Patterning of Optical and Electrical Fan-Out for Photonic Chip Packaging
Ahmed Elmoji, Andres Desmet, Jeroen Missinne, Hannes Ramon, Joris Lambrecht Peter De Heyn, Marriana Pantouvaki, Joris Van Campenhout, Geer Van Steenberghe – Ghent University

Low Surface Reflectance at Near Infrared Wavelength Thermoplastic Optical Lens Without AR Coating

Characterization of Aerosol Printed Copper and Silver Nanoparticle Inks for Millimeter-Wave Applications
Cameron Crump, Christopher Oakley, John Albrecht, John Papapolymerou, Premjeet Chahal – Michigan State University; Kyle Byers – Honeywell International, Inc.

Characterization of Fine-Pitch Hybrid Bonding Pods Using Electrical Misalignment Test Vehicle

3D Printed Interposer Layer for High-Density Packaging of IoT Devices
Saikat Mondal, Mohd. Ifwat Mohd. Ghazali, Kanishka Wijewardena, Deepak Kumar, Premjeet Chahal – Michigan State University

New Developments of Copper Plating Technology for Embedded Power Chip Packages
Yung-Da Chiu – Advanced Semiconductor Engineering Inc.

Moisture Dependent Mechanical Behavior of Underfill Encapsulants
Promod Chowdhury, Jeffrey C. Suhling, Pradeep Lall – Auburn University

Effects of Electromigration on Microstructural Evolution and Mechanical Properties of Preferred Orientation IMC Interconnects for 3D Packaging
Minghong Huang, Lin Zou – Dalian University of Technology

Telemetry for Implantable Biosensors
Ryan Green, Erdem Topsakal – Virginia Commonwealth University

Low-Temperature Cu-Cu Bonding using Nano-Cu Paste Sintering in Pt-Catalyzed Formic Acid Vapor
Fengwen Mu, Tadatomo Suga – The University of Tokyo; Hui Ren, Lei Liu – Tsinghua University; Yinghui Wang – Institute of Microelectronics, Chinese Academy of Sciences; Guisheng Zou – Tsinghua University

Ultra-Thin QFN-Like 3D Package with 3D Integrated Passive Devices
Ayd Ghanam – 3DS Technologies; Niek van Haare, Birgit Brandstatter, Sebastian Kernjes-Besi; Julian Bravin – EV Group, Philippe Meunier – NXP Semiconductors

3D Glass Panel Embedding (GPE) for Superior Bandwidth, Power-Efficiency and Cost than Current Approaches
Siddharth Ravichandran, Fuhan Liu, Vanessa Smet, Mohanalangam Kathaperumal, Ryo Tummala – Georgia Institute of Technology; Shuhei Yamada – Murata Manufacturing Co., Ltd.

Polyimide Integration of Heterogeneous Dice
Paul Jo, Ting Zheng, Muhammad Bakir – Georgia Institute of Technology

Highly Efficient Low Leakage Current RF Tunable Capacitors using Silver Doped Barium Strontium Titanate
Todd Schumann, Kyong-Tae Kim, Sheng-Po Fang Yong-Yu Yoon – University of Florida

High-Temperature Aging Effects in SAC and SAC+X Lead Free Solders
Mohmmad Alman, KM Rafidah Hassan, Jeffrey C. Suhling, Pradeep Lall – Auburn University

Wednesday, May 29, 2019
Session 38: Interactive Presentations 2
Time: 2:00 PM – 4:00 PM
Committee: Interactive Presentations
Session Co-Chairs:
Pat Thompson
Texas Instruments, Inc.
Email: patrick.thompson@ti.com
Rao Bonda
Amkor Technology, Inc.
Email: rao.bonda@amkor.com

Laudering Reliability of Electrically Conductive Fabrics for E-Textile Applications
Jeffrey Lee – Integrated Service Technology, Inc.; WeiFeng Liu – Flex, Ltd.

Preconditioning Technologies for Sputtered Seed Layers in FOPLP
Johannes Weichert, Jürgen Weichert, Andreas Erhardt – Evatec Corporation; Lars Boettcher – Fraunhofer IZM; Kay Viehweger – Fraunhofer IZM ASSID

Impact of Thermal Boundary Resistance on the Thermal Design of GaN-on-Diamond HEMTs
Huaixin Guo, Yuechuan Kong, Tangsheng Chen – Nanjing Electronic Devices Institute

Measuring the Electric Properties of Thin-Film Shape Memory Polymers in Physiological Conditions
Daniel Del Nero, Alexandra Joshi-Imre, Walter Voit – University of Texas at Dallas
Evaluation of WLP Dielectrics for High Voltage Applications
Marcus Paech, Michael Toepfer – Fraunhofer IZM

Mitigating the Effects of Microvortices in High-Re Deterministic Lateral Displacement by using Symmetric Airfoil-Shaped Pillars
Brian Dincau, Kawkblab Ahasan, Jong-Hoon Kim – Washington State University

Plasma Dry Process Technology Development of Glass-Epoxy Film on the Silicon Substrate to Fabricate RDL for Future GPU/Al Application
Takahide Murayama, Muneyuki Sato, Akiyoshi Suzuki, Atsuhiro Inori, Tetsushi Fujinaga, Yasuhiro Monkawa – ULVAC, Inc.

Fully Solid-State Integrated Capacitors Based on Carbon Nanofibers and Dielectrics with Specific Capacitances Higher than 200 nF/mm²
Amin Saleem, Rickard Andersson, Maria Bylund, Charlotte Goemare, Guilhem Pacot, Shafiq Kabir, Vincent Desmaris – Smoltek

Application of Fan-Out Panel Level Packaging Techniques for Development of Flexible Hybrid Electronics Systems
Wei-Yuan Cheng, Shau-Fei Cheng – Industrial Technology Research Institute

Structuring of Laser Activated Polymers for Sensor Applications
Kevin Cromwell, Sebastian Bengsch, Maximilian Aue, Marc Wurz – Leibniz University

A Deep Learning Approach for Volterra Kernel Extraction for Time Domain Simulation of Weakly Nonlinear Circuits
Thong Nguyen, Xinying Wang – University of Illinois

224G Package Interconnect Study Based on a New Neural Network Modeling Approach
Hui Liu, Qian Ding, Penglin Niu – Intel Corporation

High-Performance Reliability of SiP Module by Mold Encapsulation with EMI Shielding
Yu-Chou Tseng, Kuo-Hsien Liao, Alex Chen, Mark Gerber – Advanced Semiconductor Engineering, Inc.

Study of the Effect and Mechanism of a Cap Layer in Controlling the Statistical Variation of Via Extrusion
Golshahr Jalalvand, Tengfei Jiang – University of Central Florida

Least-Squares Method Built in Processing Model of Finite Element Analysis Utilized to Obtain Accurate Prediction for Non-Axisymmetric Warpage of 2L ETS MUF FCCSP SiP
Chi-Sung Chen, Nicholas Kao, Poyu Liao, Ssu-Cheng Lai, Don Son Jiang – Siliconware Precision Industries Co., Ltd.

Three-Dimensional Copper Foam-Filled Elastic Conductive Composites with Simultaneously Enhanced Mechanical, Electrical, Thermal and Electromagnetic Interference (EMI) Shielding Properties
Tan Lu, Han Gu, Tao Zhao, Yougen Hu, Pengli Zhu, Rong Sun – Shenzhen Institute of Advanced Technology, CAS; Ching-Ping Wong – Georgia Institute of Technology

Vertical Interconnect Technology for Enlarging Capacity on Micr-Solid Thin-Film Rechargeable Battery
Akhiro Horibe, Kunaki Sueoka, Risa Miyazawa, Hiroyuki Mori – IBM Corporation

Dynamic Characteristics Evaluation on NCF Under Challenging Conditions and its Application
Tonomon Nakamura, Hiroshi Shibaara, Osamu Watanabe, Tetsuya Utano, Daisuke Tani, Sug Chungcisus Toru Maeda, Doug Day – Shinkawa Ltd; Hidekazu Yagi, Royji Kojima – Dexerials Corporation

Electrical and Mechanical Simulation With Finite-Element Model of Printed Inset Feed Microstrip Patch Antenna Under Uniaxial and Biaxial Bending
Yi Zhou, Ruizhen, Naihong Li Amoli, Sridhar Sivapurupavan, Mohamed Bellaredj, Madhavan Swaminathan, Suresh Starman – Georgia Institute of Technology

Effects of Oven and Laser Sintering Parameters on the Electrical Resistance of IJP Nano-Silver Ink on Mesoporous PET Before and During Fatigue Cycling
Gurvinder Singh Khinda, Maan Z. Kakos, Mohammmed Ahendi, Jack P. Lombardi, Darshana L. Weerawarne, Mark D. Polks, Peter Borgesen – Binghamton University; Nancy C. Stoffel – GE Global Research

The Poisson’s Ratio of Lead-Free Solder – The Often Forgotten but Important Material Property
KM Rafidah Hassan, Mohammad Alam, Jeffrey C. Suhling, Pradeep LaI – Auburn University

Multilayer Glass Substrate with High-Density Via Structure for Inorganic Based Multi-Chip Packaging Module
Toshihiko Iwai, Taiji Sakai – Fujitsu Laboratories, Ltd.

Adhesive Laser Metal Deposition on Silicon
Arad Azar, Matthias Daemer, Scott Schiffris – Binghamton University

UV-Stationary and Transparent Polymer Modifications for Roll-to-Roll Processed Solar Photovoltaic (PV) Module Packaging
Jinho Hah, Michael Sulkis, Minsoo Kang, Kyungsik (Jack) Moon, Samuel Graham, C. P. Wong – Georgia Institute of Technology

Adhesive Laser Metal Deposition on Silicon
Arad Azar, Matthias Daemer, Scott Schiffris – SUNY Binghamton

PCB Microstrip Line Far-End Crosstalk Mitigation by Surface Mount Capacitors
Zhaqing Chen – IBM Corporation

Systematic Failure Mode Based Underfill Characterization Platform for Super Large FCGBA
Xiao Hu, Jiu Li, Shujun Dai, Shuming Lv, Chi Zhang, Shujie Cai, Nan Zhao, Xiongcai Kuang – HiSilicon Technologies Co., Ltd. A Huawei Company

New Cost-Effective Via-Last Approach by “One-Step TSV” After Wafer Stacking for 3D Memory Applications
Masaya Kawano, Xiang-Yu Wang, Qin Ren – Institute of Microelectronics

Microstructure and Property Changes in Cu/Sn-SnB/Si/Al Micro Solder Joints During Thermomigration
Yu-An Shen, Shiqi Zhou, Hiroshi Nishikawa – Osaka University; Jiahui Li – City University of Hong Kong; K. N. Tu – University of California, Los Angeles

Chiplet Microassembly Printer
Eugene Chow, Brad Rupp, Anne Plochweitz, Sergey Butykov, Yunda Wang, Matthew Shreve, Sourabh Raychaudhuri, Lara Crawford, Jeng Ping Lu – Palo Alto Research Center Incorporated

Simulation and Experimental Validations of EM/TM/SM Physical Reliability for Interconnects Utilized in Stretchable and Foldable Electronics
Chang-Chun Lee, Oscar Chuang – National Tsing Hua; Chia-Ping Hsien – National Taiwan University; Wei-Yuan Cheng, Steve Chu – Industrial Technology Research Institute

A Complex Integrated Circuit Structure Transformation, Modeling and Simulation Method
Daxing Wang, Yudan Pi, Wei Wang, Yufeng Jin – Peking University

A Study on the Optimization of O2 Plasma Parameters on the Peel Adhesion Strength and Solder Wettability of SnBi58 Based Anisotropic Conductive Films
Shuye Zhang, Tiesong Lin, Peng He – Harbin Institute of Technology; Ming Yang – Hisilicon Optoelectronics Co., Ltd.; Kyung-Wook Pak – Korea Advanced Institute of Science and Technology

Numerical Analysis of the Influence of Polymeric Materials on a MEMS Package Performance Under Humidity and Temperature Loads
Mahesh Yalagach, Peter Filipp Fuchs – Polymer Competence Center Leoben GmbH; Luca Viero – AMS AG; Qi Tao – AT&S

Electromigration-Induced-Sn Grain Rotation in Lead-Free Flip Chip Solder Bumps
Mingliang Huang, Jianpeng Kuang, Hongyu Sun – Dalian University of Technology

Low-Cost MT-Ferrule-Compatible Optical Connector for Co-Packaged Optics using Single-Mode Polymer Waveguide
Akhiro Noniki, Takuji Amano – National Institute of Advanced Industrial Science and Technology

Characterization of Coated Silver Wire Bond Interface Using TEM
Murali Sarangapani, Eric Tan, Swee Seng, Jason Wong Chin Yeung – Heraeus
Interactive Presentations: Thursday, May 30, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

Thursday, May 30, 2019
Session 40: Interactive Presentations 4
Time: 2:00 PM – 4:00 PM
Committee: Interactive Presentations
Session Co-Chairs:
Mark Eben
Kyocera Corporation
Email: mark.eben@kyocera.com

Jeffrey Lee
iST-Integrated Service Technology, Inc.
Email: jeffrey_lee@istgroup.com

Die Thickness Optimization for Preventing Electro-Thermal Fails Induced by Solder Voids in Power Devices
Dario Vitello, Andrea Albertinetti, Marco Rovitto – STMicroelectronics

Reversed Pulsed Electrodeposition of Nanostructured Nickel Tungsten With Controlled Grain Structure as an Effective Diffusion Barrier Layer
Nalza Dadvand – Texas Instruments, Inc.

3-T Decoupling Capacitors for Improved LPDNR4/4X/5 System
Sunli Gupta – Qualcomm Technologies, Inc.

Improved Correlation Between Accelerated Board Level Reliability (BLR) Testing and Customer BLR Results Using a Hybrid Closed-Form/Finite Element Methodology
Maxim Serebreni, Natalie Hernandez, Gil Sharon, Nathan Blattau, Craig Hillman – DFR Solutions

Fabrication and Reliability Demonstration of 3 μm Diameter Photo Vias at 15 μm Pitch in Thin Photosensitive Dielectric Dry Film for 2.5 D Glass Interposer Applications

Pre-Cure Modification of Electrically Conductive Adhesive for Low-Temperature Interconnection
Jinto George, David Danovitch – University of California, Los Angeles; Tim Shirley – Keysight Technologies

RLD-1st Fan-Out Panel Level Packaging (FOPLP) for Heterogeneous and Economical Packaging
Nagendra Sekhar Vasarla, Srinivasa Rao Vempati, F. B. Viswanath, Ritesh Jain, Huthasana Kalyanam – Intel Corporation

Epoxies Coatings with Surface Modified Silicon Carbide Fillers for High-Temperature Molding Compounds
Fan Wu, Nicholas C. Mitchell, Bo Song, Kyoung-Sik Moon, C. P. Wong – Georgia Institute of Technology

Ultra-Low Resistivity and High Electrical Stability Silo-Ag ECAs Produced from Curing Chemistry Optimization for Flexible Electronics
Xueqiao Wang, Kyoung-sik Moon, C. P. Wong – Georgia Institute of Technology; Bo Song – GLOBALFOUNDRIES

Physics of Failure Based Simulation and Experimental Testing of Quad Flat No-Lead Package
Jia-Shen Lan, Mei-Ling Wu – National Sun Yat-Sen University

Eji Nakamura, Keiji Matsumoto – IBM Research; Andrea Fasoli, Luisa Bozano – IBM Research; Hiroyuki Mori – IBM Research

An Assessment of Thermocompression in 2.5D Packaging
Jieferg Xu, Huayan Wang, Jing Wang, Stephen R. Cain, S. B. Park Binghamton University; Scott McCann, Ho Hyung Lee, Gamil Refai-Ahmed – Xilinx, Inc.

Diffusion Enhanced Drive sub 100 °C Wafer Level Fine-Pitch Cu-Cu Thermocompression Bonding for 3D IC Integration
Asis Kumar Panigrahi, Tнал Ghosh, Siva Rama Krishna Vanjani, Shiv Govind Singh – Indian Institute of Technology, Hyderabad

Extremely Detailed Package Level Thermal Modeling for an Enhanced Understanding of Passive Cooling Techniques in Wireless Products
Daniel Cox, Bhagyaashree Ganore, Richard Perry, Sidharth Dalmia – Intel Corporation

Development of Sheet Type Molding Compound for Panel Level Package
Akira Nakao, KazuhiroDohi, YuSuzuki, Masakazu Hirose – Sanyu Rec Co., Ltd.

Defect Detection for the TSV Transmission Channel Using Machine Learning Approach
Huan Liu, Runiu Fang, Yufeng Jin – Peking University; Min Miao – Beijing Information Science and Technology University

Direct Printing of Heat Sinks, Cases and Power Connectors on Insulated Substrate using Selective Laser Melting Techniques
Rabib Khazaka, Donatien Martineau, Tonl Yousef, Thanh Long Le, Stephane Azzopardi – Safran

Novel Solder Pads for Self-Aligned Flip-Chip Assembly
Yves Martin, Swetha Kamalpurkar, Nathan Marchach, Jae-Woong Nah, Tymon Barwicz – IBM Corporation

Integration and Characterization of InP Dies on Silicon Interconnect Fabric
Eric Sorensen, Boris Vaisband, SivaChandra Jangam, Subramanian S. Iyer – University of California, Los Angeles; Tim Shirley – Keysight Technologies

Server CPU Package Design Using PoINT Architecture

Highly Reliable Die Attach Silver Joint with Pressure-Less Sintering Process
Shai Chen, Christine LaBarbers, Ning-Cheng Lee – AMD Corporation; William Shambach, Jordan Palmer – Rochester Institute of Technology; Xuanyi Ding – Cornell University

Research on Applied Reliability of BGA
Solder Balls in Extreme Marine Environment
Liyuan Lian, Tao Lu, Daqun Luo – MIIT Fifth Electronics Research Institute

Influence of Single/Double Sweeping Modes and Sweeping Voltage Increments/Polarities on Measurement of TSV Leakage Current
Qinghua Zeng, Jing Chen, Yufeng Jin – Peking University

Preparation and Application of Cu-Ag Composite Solder Preform for Power Electronic Packaging
Dongxiao Zhang, Zhiwen Chen, Li Liu – Wuhan University of Technology
Zhaoxi Zhou, Canyu Liu, Stuart Robertson, Changqin Liu – Loughborough University

Improving the Solder Wettability via Atmospheric Plasma Technology
Sagung Kencana, Yee-Wen Yen, Yu-Lin Kuo – National Taiwan University of Science and Technology; Wallace Chuang, Eckart Schellkes – Robert Bosch Taiwan Co.

Orthogonal Quilt Packaging 3D Integration for High Energy Particle Detectors
Jason Kulick, Tian Liu, Carlos Ortega – Indiana Integrated Circuits, LLC; Christopher Kenney, Julie Segal Stanford University; Gary Bernstein – University of Notre Dame

Electroless Plating on 3D Printed Parts for RF Circuit Applications
Nicholas Bannon, Mohd Ifwat Mohd Ghazali, Amanpreet Kaur, Premjeet Chahal – Michigan State University

Carbonized Electrodes for Electrochemical Sensing
Mohammad Aminul Haque, Nicole McFarlane – The University of Tennessee, Knoxville; Nickolay V. Lavrik, Mohammad Aminul Haque, Nicole McFarlane – The University

2.5 D Glass Interposer Applications
2.5 µm Diameter Photo Vias at 15 µm Pitch in Thin Photosensitive Dielectric Dry Film for 2.5 D Glass Interposer Applications

Pre-Cure Modification of Electrically Conductive Adhesive for Low-Temperature Interconnection
Jinto George, David Danovitch – University of California, Los Angeles; Tim Shirley – Keysight Technologies

RLD-1st Fan-Out Panel Level Packaging (FOPLP) for Heterogeneous and Economical Packaging
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Ultra-Low Resistivity and High Electrical Stability Silo-Ag ECAs Produced from Curing Chemistry Optimization for Flexible Electronics
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Physics of Failure Based Simulation and Experimental Testing of Quad Flat No-Lead Package
Jia-Shen Lan, Mei-Ling Wu – National Sun Yat-Sen University

Eji Nakamura, Keiji Matsumoto – IBM Research; Andrea Fasoli, Luisa Bozano – IBM Research; Hiroyuki Mori – IBM Research

An Assessment of Thermocompression in 2.5D Packaging
Jieferg Xu, Huayan Wang, Jing Wang, Stephen R. Cain, S. B. Park Binghamton University; Scott McCann, Ho Hyung Lee, Gamil Refai-Ahmed – Xilinx, Inc.

Diffusion Enhanced Drive sub 100 °C Wafer Level Fine-Pitch Cu-Cu Thermocompression Bonding for 3D IC Integration
Asis Kumar Panigrahi, Tнал Ghosh, Siva Rama Krishna Vanjani, Shiv Govind Singh – Indian Institute of Technology, Hyderabad

Extremely Detailed Package Level Thermal Modeling for an Enhanced Understanding of Passive Cooling Techniques in Wireless Products
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Development of Sheet Type Molding Compound for Panel Level Package
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Defect Detection for the TSV Transmission Channel Using Machine Learning Approach
Huan Liu, Runiu Fang, Yufeng Jin – Peking University; Min Miao – Beijing Information Science and Technology University

Direct Printing of Heat Sinks, Cases and Power Connectors on Insulated Substrate using Selective Laser Melting Techniques
Rabib Khazaka, Donatien Martineau, Tonl Yousef, Thanh Long Le, Stephane Azzopardi – Safran

Novel Solder Pads for Self-Aligned Flip-Chip Assembly
Yves Martin, Swetha Kamalpurkar, Nathan Marchach, Jae-Woong Nah, Tymon Barwicz – IBM Corporation

Integration and Characterization of InP Dies on Silicon Interconnect Fabric
Eric Sorensen, Boris Vaisband, SivaChandra Jangam, Subramanian S. Iyer – University of California, Los Angeles; Tim Shirley – Keysight Technologies

Server CPU Package Design Using PoINT Architecture

Highly Reliable Die Attach Silver Joint with Pressure-Less Sintering Process
Shai Chen, Christine LaBarbers, Ning-Cheng Lee – AMD Corporation; William Shambach, Jordan Palmer – Rochester Institute of Technology; Xuanyi Ding – Cornell University
3D Power Packaged Device Thermo-Mechanical Modeling and Stress Analysis After Reliability Trials
Lucrezia Guarno – STMicroelectronics

High-Density Ultra-Thin Organic Substrate for Advanced Flip Chip Package

Millimeter Wave Dual Polarization Design Using Frequency Selective Surface (FSS) for 5G Base-Station Applications
Chi-Hau Yang, Chung-Yi Hsu, Li-Tyng Hwang – National Sun Yat-Sen University.

Low-Loss Additively Deposited Ultra-Short Copper Paste Interconnections in 3D Antenna-Integrated Packages for 5G and IoT Applications
Atom Watanabe, Yiteng Wang, Markonduya R. Pulugurtha, Vanessa Smet, Manos Tentzeris, Rao Tummala – Georgia Institute of Technology; Nobuo Ogura – Nagase & Co., Ltd.

Direct Bonding of Low-Temperature Heterogeneous Dielectrics
Serena Iacovo, Lan Peng, Alain Phommahaxay, Fumihiro Inoue, Etienne Paradis, David McCann, Ho Hyung Lee, Gamal Refai-Ahmed – Xilinx, Inc.

Modelling and Experimental Demonstration of Microfluidic Cooling for a Heterogeneous 2.5D IC
Sreejith Kochupurackal Rajan, Md Obaidul Hossen, Thomas Sarvey, Ankit Kaul, Muhammad Bakir – Georgia Institute of Technology; Gary May – University of California, Davis

On-Chip ESD Monitor
Kannan Kalappurakkal Thanskkpan, Boris Vaisband, Subramanian S. Iyer – University of California, Los Angeles

Preparation and Characterization of Electroplated Cu/Graphene Composite
Xin Wang, Jan Cai, Yang Hu – Tsinghua University

Quantifying the Impact of RF Probing Variability on TRL Calibration for LTCC Substrates
Ömer Faruk Yıldız, David Dahl, Christian Schuster – The Institut für Theoretische Elektrotechnik

Effects of NCF and UBM Materials on Electromigration Reliabilities of Sn-Ag Microbumps for Advanced 3D Packaging
Kirak Son, Gahyu Kim, Hyodong Ryu, Young-Cheon Kim, Jeong Sam Han, Young-Bae Park – Andong National University; Gyu-Tae Park – Amkor Technology, Inc.; Ho-Young Son, Nam-Seog Kim – SK hynix Inc.; Cheol-Woong Yang – Sungkyunkwan University

Ag Diffusion Control Through Sn Bump on a Sequential Plating Based Process
Abderahim EL Amrani, Etienne Paradis, David Danovitch, Dominique Drouin – University of Sherbrooke

Mechanical Reliability Assessment of Cu6Sn5 Intermetallic Compound and Multilayer Structures in Cu/Sn Interconnects for 3D IC Applications
Jui-Yang Wu, C. Robert Kao – National Taiwan University

A Study on the Anchoring Polymer Layer (APL) Anisotropic Conductive Films (ACFs) With Self-Exposed Surface of Conductive Particles for Ultra-Fine Pitch Chip-on-Glass (COG) Applications
Dal-Jin Yoon, Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

Bending Properties of Fine Pitch Flexible CIG (Chip-in-Flex) Packages Using APL (Anchoring Polymer Layer) ACFs (Anisotropic Conductive Films)
Ji-Hye Kim, Dal-Jin Yoon, Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

Effect of the Curing Properties and Viscosities of Non-Conductive Films (NCFs) on Sn-Ag Flip Chip Solder Bump Joint Morphology and Reliability
HanMin Lee, SeYong Lee, SangMyung Shin, Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; Tae Jin Choi, SooH Park – Doosan Corporation Electro-Materials BG

Experimental Investigations on Vertical Ultrasonic Assisted Low-Temperature Sintering Process
Henning Seefisch, Jens Twiefel – Leibniz University Hannover

Pressureless Transient Liquid Phase Sintering Bonding of Sn-58Bi with Ni Particles for High-Temperature Packaging Applications
Kyung Deuk Min, Kwang-Ho Jung, Choong-Jae Lee, Seung-Boo Jung – Sungkyunkwan University

Epoxy/Cyanate Ester Copolymer for High-Temperature Encapsulant Applications
Jiaoxiang Li, Kyung-Sik Moon, C. P. Wong – Georgia Institute of Technology

Low-Temperature Ag-Ag Direct Bonding Technology for Advanced Chip-Package Interconnection
Jiaq Wu, Chin C. Lee – University of California, Irvine

Reliability of Micro-Alloyed SnAgCu Based Solder Interconnections for Various Harsh Applications
Sinan Su, Francy Akkara, Anto Raj, Seth Gordon, Sharath Snidhar, Sasivubtramanee Thitirunyanasambandam, Sa’ad Hamasha, Jeffery Suhling, John Evans – Auburn University; Cong Zhao – Apple, Inc.

A Miniaturized and High-Performance 28GHz AiP with Integrated Metamaterials
Mei Xue – IMECAS

Automatic Transient Thermal Impedance Tester for Quality Inspection of Soldered and Sintered Power Electronic Devices on Panel and Tile Level

Time 0 Void Evolution and Effect on Electromigration
Jiefeng Xu, Van Lai Pham, Huayan Wang, Stephen R. Cai, S.B. Park – Binghamton University; Scott McCann, Ho Hyung Lee, Gamal Refai-Ahmed – Xilinx, Inc.

Quintuple Band Quarter Wavelength Stub Using Unbalanced Bridged CRLH Transmission Lines
Renuka Bowroothu, Seeha Hwangbo, Yong-Kyu Yoon – University of Florida

Product Level Design Optimization for 2.5D Package Shock Impact Reliability
Huayan Wang, Jing Wang, Jiefeng Xu, Vanlai Pham, Seungbae Park – Binghamton University; HoHyung Lee, Gamal Refai-Ahmed – Xilinx, Inc.

Microstructure of Sn-Ag-Cu (SAC) Solder Joints by Mass-Reflow (MR) and Thermo-Compression Bonding (TCB) Process
Jinho Hah, Jack Moon, CP Wong – Georgia Institute of Technology; Yongja Kim – Samsung Electronics Company, Ltd.

Novel Decapsulation Method for Silver-Based Wire Bond Semiconductor Packages with High Reliability Using Mixed Salt Acid Chemistry
Yong Ja Kim – Samsung Electronics Company, Ltd.; Jinho Hah, Kyung Sik (Jack), C. P. Wong – Georgia Institute of Technology
2019 TECHNOLOGY CORNER EXHIBITS

Today’s high-tech companies are being very selective in choosing the conferences and trade shows where they will exhibit their products and services. Each year more companies have determined that ECTC provides them the opportunity to identify superior prospects. The primary reason is that the engineers and managers who attend ECTC hold decision-making positions at the world’s leading electronics equipment and component manufacturers. The attendees are attracted by ECTC’s strong technical program and excellent Exhibition attendance. Authors in the field believe that ECTC offers the best forum for presenting their work. Exhibit hours will be from 9:00 AM to Noon and 1:30 to 6:30 PM on Wednesday, May 29, and 9:00 AM to Noon and 1:30 to 4:00 PM on Thursday, May 30. The demand for booths in the exhibit hall continues to be very high, and once again all booths are already reserved. Following is a list of exhibitors as of Feb. 5, 2019. The 2019 Exhibit Brochure, a current exhibitor list, and a booth layout showing the available booths can be found on the ECTC web site at www.ectc.net under the heading Exhibits. Should you need additional information or have questions, call Joe Gisler at +1-480-288-6660 or email gislerhj.ectc@etv.net.

HOTEL RESERVATIONS

The Cosmopolitan of Las Vegas • 3708 S. Las Vegas Blvd. • Las Vegas, NV 89109 USA

Hotel reservations for ECTC can be made one of two ways:

1) Contact The Cosmopolitan of Las Vegas at +1-877-551-7772 and reference the ECTC Conference to receive the conference rate of US$166 per night.

or …

2) Log onto www.ectc.net and click on the Location tab near the top of the page to find a special online hotel registration link.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for ECTC. Be advised that you may receive emails about booking a hotel room for ECTC from third-party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. ECTC’s only authorized site for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that you have personally used in the past to book travel. Please be advised, there are scam artists out there, and if it’s too good to be true, it likely is. Should you have any questions about booking a hotel room, please contact ECTC staff at: lrenzi@renziandco.com

CONFERENCE REGISTRATION FOR ECTC:

Online: Submit your registration electronically via www.ectc.net. Your registration must be received by the cutoff date, May 2, 2019, to qualify for the early registration discounts.

You may contact our registration staff at lrenzi@renziandco.com for additional information. Payment can be made by Visa, Mastercard, or American Express.
## 2019 ECTC REGISTRATION INFORMATION

<table>
<thead>
<tr>
<th>Conference Registration</th>
<th>Advance Registration</th>
<th>Door Registration</th>
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<tbody>
<tr>
<td>IEEE Member</td>
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<tr>
<td>Attendee (full ECTC conference)</td>
<td>US$750</td>
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<td>Attendee (Joint ECTC + Itherm conferences)</td>
<td>$1000</td>
<td>$1160</td>
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<td>Attendee One-Day Registration</td>
<td>$565</td>
<td>$565</td>
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<tr>
<td>Speaker or Chair (full ECTC conference)</td>
<td>$625</td>
<td>$765</td>
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<td>Speaker or Chair One-Day Registration</td>
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<tr>
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<tr>
<td>Attendee or Speaker (full conference)</td>
<td>$315</td>
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### Exhibits

| Access to Exhibits Only (not attending conference) | $25 | $25 |
| Exhibit Booth Attendant | $0 | $0 |

### Professional Development Courses (PDCs)  
*Note: all PDCs include a luncheon*

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<tr>
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<td>Full PDC (both a.m. and p.m.)</td>
<td>$605</td>
<td>$710</td>
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<td>Single PDC (a.m. or p.m.)</td>
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<td>Full PDC (both a.m. and p.m.) or Single PDC</td>
<td>$130</td>
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### Other Registration Options

| Extra Proceedings | $100 | $100 |
| Extra Luncheon Tickets | $65 | $65 |
| Cancellation Fee | $50 | $50 |

Please log onto [www.ectc.net/registration](http://www.ectc.net/registration) to register for the 2019 ECTC.

There will be no refunds or cancellations after May 2, 2019. Please note that a $50 cancellation fee will be in effect for all cancellations made on or prior to May 2, 2019. Substitutions can be made at any time.

For additional information about registration or ECTC please contact us at:

Renzi & Company, Inc. • Phone: +1-703-863-2223 • Email: renziandco2@gmail.com

*If you join IEEE BEFORE you register for the 2019 ECTC you can save on registration fees and receive a Electronics Packaging Society (EPS) membership free for one year!*

To take advantage of this offer, visit: [https://www.ieee.org/membership-application/public/join.html?grade=Member&promo=EPS2019FREE](https://www.ieee.org/membership-application/public/join.html?grade=Member&promo=EPS2019FREE)

At the URL, create your IEEE Web Account. Once complete, proceed to the Shopping Cart and enter EPS2019FREE in the promotion code box. Click “Apply” and the Shopping Cart will be updated to show the discount. Use your new IEEE membership ID number and register for ECTC at the discounted IEEE Member Rate.

*Non-IEEE members can join IEEE and save $100 or more on ECTC registration and receive EPS membership free for 2019. Existing IEEE members receive a free EPS membership for the remainder of 2019 with ECTC registration.*
## CONFERENCE SPONSORS

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### GOLD

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Advance Registration through May 2, 2019 – Hotel Reservations through April 26, 2019
For more information, visit: www.ectc.net

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Walt Disney World Swan & Dolphin Resort
Lake Buena Vista, Florida, USA
May 26-29, 2020