ECTC 2017

The 67th Electronic Components and Technology Conference

CALL FOR PAPERS

May 30 - June 2, 2017
Walt Disney World Swan & Dolphin Resort
Lake Buena Vista, Florida, USA

Introduction

On behalf of the IEEE Electronic Components and Technology Conference (ECTC) Program Committee, it is my pleasure to invite you to submit an abstract for the 67th ECTC, to be held May 30 – June 2, 2017, at the Walt Disney World Swan and Dolphin Resort, Lake Buena Vista, Florida, USA. This premier international conference, sponsored by the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society, covers a wide spectrum of electronic packaging technology topics, including components, materials, assembly, interconnect design, device and system packaging, wafer level packaging, Si photonics, LED and IoT, optoelectronics, 2.5D and 3D integration technology, and reliability.

The ECTC Program Committee, with more than 200 experts from broad-ranging technical areas, is committed to creating an engaging technical program for all. ECTC typically attracts more than 1,300 attendees from over 25 countries. The 66th ECTC in Las Vegas had a record number of 1,436 attendees, with 392 papers and interactive presentations featured in 41 sessions. The 67th ECTC will continue with that tradition by being the premium venue to showcase all the latest developments in the electronic components industry where packaging has become a way to achieve device and system performance scaling.

The 67th ECTC program will include six parallel technical sessions in the mornings and afternoons over three days, along with other special topic panel discussions to present high-level trends and best practices in the industry. Professional Development Courses (PDCs) will also be offered by world-class experts, enabling participants to broaden their technical knowledge base. The technical program and PDCs will be supplemented by Technology Corner Exhibits, which provide an opportunity for leading companies in the electronic components, materials, and packaging fields to exhibit their latest technologies and products. The 66th ECTC featured a record number of 104 exhibition booths.

As the Program Chair of the 67th ECTC, I invite you to submit an abstract between 250 and 750 words that describes the scope, content, and key points of your proposed technical paper at www.ectc.net. You are also welcome to submit proposals for PDCs. The deadline for abstract and proposal submission is October 10, 2016. Manuscripts conforming to the ECTC format are due by February 24, 2017, for inclusion in the Conference Proceedings. All abstracts and manuscripts must be original, free of commercial content, and non-confidential. On behalf of the ECTC Program Committee, I look forward to seeing you at the Walt Disney World Swan and Dolphin Resort in Lake Buena Vista, Florida, USA at the 67th ECTC, May 30 – June 2, 2017.

Mark Poliks
67th ECTC Program Chair
Binghamton University, Binghamton, NY USA

Major Topics

Advanced Packaging: Fan-Out, 2.5 & 3D, TSV and Interposer, Heterogeneous Integration and SiP, Embedded and Advanced Substrates, MEMS & Sensors, Automotive, Power Module, Wearable & IoT, Bio and Medical, RF, Microwave, Millimeter-Wave & EMI, High Performance Computing and Data Center, Wafer Level & Panel Level Process, Advanced Flip-Chip, Advanced CSP and POP.

Applied Reliability: Advanced Package Reliability (Including TSV/2.5D/3D Packaging, WCSP, Fan-Out, Embedded Technologies), Challenges in SiP Reliability, Interconnect Reliability (Including Flip-Chip, Wire-Bond), LED, RFID, High Voltage Packaging and IoT Reliability, System Level Reliability Testing/Modeling, Reliability Test Methods and Life Models, Physics of Failure, Failure Analysis Techniques and Materials Characterization, Drop and Dynamic Mechanical Reliability, Probabilistic Design for Reliability (PDfR), Automotive Reliability Requirements.

Assembly and Manufacturing Technology: Embedded/Hybrid Package Manufacturing Process, Wearable/IoT Package Assembly, Healthcare/Fitness Component Assembly, Warpage Control/Management in Board Level Assembly, Thin Die/Thin Mold/Thin Package Handling and Assembly, Large/Ultra Large Package (SiP, SIM, MCP) Integration and Processing, Panel Level Manufacturing for WLP, Dicing and Singulation.

Emerging Technologies: Wearable and Medical Electronics, Flexible, Bendable, Stretchable, Disposable, or Dissolvable Packaging, Bio-Sensor Packaging, Implantable Device Packaging, New Materials and Methods for Packaging Microfluidics, MEMS and NEMS, Nano-Battery. 3D Printing, Self-Alignment and Assembly, New Additive Packaging Process Technologies and Materials. Novel Substrates, Materials and Approaches to Interconnects and Packaging, Packaging for Wireless, Photovoltaic, Redundancy, Repair, Security, Anti-Counterfeiting, Components for Internet of Things (IoT) and Smart Electronics, Heterogeneous Integration. Compact & Autonomous Sensor Packaging, Wafer Level Integrated Silicon Photonics.

High-Speed, Wireless & Components: Modules & Sub-Systems; High-Speed, RF to THz Devices & Passive Components, Mixed-Signal; Electrical Modeling and Design; Advanced Components: Materials, Structures, Fabrication and Characterization; Power and Signal Integrity; High-Speed Data Transfer/Communications; Power Modules, Power Management; Integrated Voltage Regulators (IVR); LTE, WLAN, 5G, mm Wave and THz T/R Modules; Radars; Imagers; Wearable and Sensor Technologies for Internet of Things (IoT); Flexible Electronics; 3D Printed RF Components and Modules; Automotive Sensors; RF-MEMS, RF-Opto, RFID and Tagging; M2M Platforms; Proximity Sensors; Ambient Intelligence; Wireless Power; Wireless Sensor and Computing Nodes; Wearable and Biomedical Electronics.

Interconnections: Fan-Out and Fan-In, Wafer- and Panel-Level Interconnects, 2.5D/3D, TSV Interconnect Structures for Heterogeneous Integration and SiP, Co-Designs and Process/Performance Trade-Off, Thermal/Mechanical/Electrical Tests & Reliability, Embedded Systems; Si/Glass/Organic Interposers, PoP, WLCSP, Flip-Chip, Solder Bumping and Cu Pillar, TC Bonding, IMC Interconnect, Wirebonds, RDL, Conductive Adhesives, Flexible Substrates, Power Modules, Wearables, Interconnects for Bio-Medical, Automotive, Bio-Sensor, Energy Harvesting, and Harsh Environments.

Materials & Processing: Wafer Level Packaging, Panel Processing & Materials, Next Generation Packaging Substrates, Flexible and Wearable Electronics, Carbon Electronics, Battery Materials, 3D Materials and Processing, Emerging Electronic Materials, Novel Conductive and Non-Conductive Adhesives, Solder Alloys, Photoresist, Dielectrics and Under-Fill, Molding Compounds, Thermal Interface Materials, Optoelectronic Materials.

Thermal/Mechanical Simulation & Characterization: Thermal, Mechanical Simulation and Characterization Including: Component, Board and System Level Modeling for Microelectronics, e.g., 3D Interconnects (TSV, Stacked Die, etc.), 2.5D Packaging (Si, Glass, Flexible Interposer, etc.), Wafer-Level-Package (WLP), Ball-Grid-Array (BGA), Embedded Packages with Active and Passive Components, System-in-Package (SiP), Power Electronic Modules, LED Packaging, and MEMS; Fab/Thin Wafer Handling, Wire Bonding and Assembly Manufacture Process; Reliability Modeling Related Fracture Mechanics, Fatigue, Electromigration, Warpage, Delamination/Moisture, Drop Test, Material Constitutive Relations and Characterization; Novel Modeling Including Multi-Scale and Multi-Physics Techniques and Solutions; Measurement Methodologies, Characterization and Correlations.

Optoelectronics: Integrated Photonics Modules, Fiber Optical Interconnects, Advanced Optical Connectors, Optical Waveguide Circuits, Optical Printed Circuit Board, Mid-Board/On-Board Optical Modules, Silicon and III-V Photonics Packaging, Optical Chip-Scale and Heterogeneous Integration, Micro-Optical System Integration and Photonic System-in-Package, 3D Photonics Integration, Optoelectronic Assembly and Reliability, Materials and Manufacturing Technology, High-Efficiency LEDs and High Power Lasers, Integrated Optical Sensors.

Interactive Presentations: Abstracts may be submitted related to any of the nine major program committee topics listed above. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

Visit the ECTC website (www.ectc.net) for additional conference information.

Call for Professional Development Courses

See page two.

Abstract and Manuscript Submission

You are invited to submit an abstract between 250–750 words that describes the scope, content, and key points of your proposed paper via our website at www.ectc.net. Additional details on how to submit abstracts electronically can be found on the ECTC website under the "Author Information" tab. Submitted abstracts become the property of ECTC, and ECTC reserves the right to publish the abstracts accepted for the conference. ECTC also reserves the right to prohibit, limit, or reject any editing of submitted abstracts. Abstracts accepted for the conference may not be edited until manuscript submission. Abstracts must be received by **October 10, 2016**. Your submission must be cleared by management and co-authors as applicable and include the affiliation, contact telephone number, and email address for all authors, besides the mailing address for the presenting author. Please select two different program subcommittees in order of preference that should evaluate your paper for acceptance. Authors will be notified of paper acceptance with instructions for publication by December 10, 2016. At the discretion of the Program Committee, submitted abstracts may be considered for Interactive Presentation sessions.

Manuscripts conforming to the ECTC format are due in final form for publication in the Conference Proceedings by February 24, 2017. **Manuscripts not submitted by this date may be removed and replaced in the final program at the discretion of the Program Committee.** The submitted content must be original, previously unpublished, non-confidential, and without commercial content. All submitted manuscripts are checked for plagiarism and excessive self-duplication of previously published work through the IEEE CrossCheck system. For additional information regarding abstract and paper submission, please contact:

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Special Paper Recognition

Best Paper Award: Each year the ECTC selects the best paper whose author(s) receive an ECTC personalized wall plaque and share a check for $2,500.

Best Interactive Presentation Award: Each year the ECTC selects the best Interactive Presentation paper whose author(s) receive an ECTC personalized wall plaque and share a check for $1,500.

Outstanding Paper Award: An outstanding conference paper is also selected for special recognition by the ECTC. The author(s) receive a personalized wall plaque and share a check for $1,000.

Outstanding Interactive Presentation Award: An outstanding Interactive Presentation paper is also selected for special recognition by the ECTC. The author(s) receive a personalized wall plaque and share a check for $1,000.

Intel Best Student Paper Award: Intel Corporation is sponsoring an award for the best paper submitted and presented by a student at ECTC. The winning student will be presented with a wall plaque and a check for $2,500. See next column for details.

Technology Corner Exhibits

Reserve Your Space Early!

Exhibit your products or services to more than 1,200 engineers and managers from all areas of the microelectronics packaging industry. These include: materials & processes for semiconductor packaging, assembly and interconnect technologies, test & other equipment, market research, and research centers.

Two days: May 31 and June 1, 2017

With 100 of 110 exhibition booths at the 67th ECTC reserved already, mostly by returning exhibitors from the 66th ECTC, applications are still being accepted for participation in the Technology Corner Exhibits. For information and an application contact Joe Gisler at gislerhj.ectc@mediacombb.net. Additional information is available at **www.ectc.net** under Technology Corner Exhibits.

Contribution and Visibility Opportunities through Sponsorship

ECTC also offers excellent opportunities for contributions, promotion and visibility through gala, badge lanyard, USB flash drive proceedings, media, internet kiosk, luncheon, refreshment break, program, and student reception sponsorships. Additional information is available at www.ectc.net under Sponsors. Please contact:

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Call for Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on topics described on the previous page. From the proposals received, 16 PDCs will be selected for offering at the 67th ECTC on Tuesday, May 30, 2017. Each selected course will be given a minimum honorarium of $1,000. In addition, instructors of the selected courses will be offered the speaker discount rate for the conference. Attendees of the PDCs will be offered Continuing Education Units (CEUs). These CEUs are recognized by employers as a formal measure of participation and attendance in "noncredit" self-study courses, tutorials, symposia and workshops.

Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the ECTC website at www.ectc.net by **October 10, 2016.** Authors will be notified of course acceptance with instructions by December 10, 2016. If you have any questions, contact:

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IEEE CPMT Society Travel Award

IEEE CPMT is pleased to continue the CPMT Travel Grant Program for the 67th ECTC. The goals of this award are to foster maximum student participation in the ECTC and to recognize students with superior ECTC papers.

Description: Grants are available to apply towards actual travel expenses, including airfare, hotel, and meals. Grants will be awarded competitively, based on abstracts submitted by student authors. The student who is named as the primary author of each winning abstract will receive a travel grant.

Eligibility: The competition is open to all full-time graduate students enrolled at an accredited institution in a program of study within the scope of ECTC. The student must be listed as the primary author on the abstract. A maximum of two authors (one per paper) from any one institution will receive a travel grant.

Application Process: To apply, check the "IEEE CPMT Society Travel Grant" box in the "Awards" section of the online abstract submission form. Pre-selected abstracts based on technical committee scores will be requested to submit an extended abstract.

Intel Best Student Paper Award

Intel Corporation is sponsoring an award for the best paper submitted and presented by a student at the ECTC. The winning student will be presented with a wall plaque and a check for $2,500.

Eligibility: To be considered for the award, the student must be a full-time student for at least one semester after the conference conclusion. The student must be the lead author and present the paper at the 67th ECTC. It is the convention at ECTC for the presenter to be listed as the first author. Finalists will be determined by review of the completed manuscripts by the judging committee. Manuscripts will be reviewed for relevance to the competition topics, technical content, and originality. The author of the best student paper will be notified after the conference and must submit an affidavit from the student's faculty advisor certifying that the student meets the eligibility requirements.

Application Process: To enter the Intel Best Student Paper Award competition, please check the "Intel Best Student Paper Award" box in the "Awards" section of the online abstract submission form.

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