## PDC #1 – ACHIEVING HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIAL CONSIDERATIONS

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Ning-Cheng Lee is the Vice President of Technology of Indium Corporation. He has been with Indium since 1986. Prior to joining Indium, he was with Morton Chemical and SCM. He has more than 20 years of experience in the development of fluxes and solder pastes for SMT industries. In addition, he also has very extensive experience in the development of underfills and adhesives. He received his PhD in polymer science from University of Akron in 1981, and BS in chemistry from National Taiwan University in 1973. Ning-Cheng is the author of book "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies", and co-author of book "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials". He is also the author of book chapters for several lead-free soldering books. He received several best conference papers awards from SMTA and IPC. He was honored as 2002 Member of Distinction from SMTA, 2003 Lead Free Co-Operation Award from Soldertec, 2006 Exceptional Technical Achievement Award from CPMT, 2007 Distinguished Lecturer from CPMT, 2009 Distinguished Author from SMTA, and 2010 Electronics Manufacturing Technology Award from CPMT.

## PDC #2 - FAN-OUT WAFER LEVEL PACKAGING

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Beth Keser has over 17 years' experience in the semiconductor industry. Beth received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. in Materials Science and Engineering at the University of Illinois at Urbana-Champaign. Beth's development of materials and packaging technologies for the semiconductor industry has resulted in 8 patents, 10 patents pending, and over 40 publications in this area. Currently, Beth is the Fan-Out Wafer Level Packaging Technology Manager at Qualcomm, San Diego. Before joining Qualcomm in 2009, Beth Keser was instrumental in developing 2 packaging technologies during her career at Motorola and Freescale Semiconductor. Beth led the Wafer-Level Chip Scale packaging team at Motorola, which included directing the activities of process engineering, package characterization, package reliability, and mechanical modeling. In addition, Beth Keser was the lead technologist and manager of the Redistributed Chip Packaging Technology (RCP). Beth led the team that developed this technology for 6 years. Beth developed several process and material solutions for this new technology. Beth is an IEEE Senior Member whose volunteer activities and professional society responsibilities include: CPMT Board of Governors 2012-2014, 2015 General Chair, 2013 Program Chair, 2012 Assistant Program Chair and Advanced Packaging Sub-committee member 2000-present.

## PDC #3 - PACKAGE FAILURE ANALYSIS - FAILURE ANALYSIS AND ANALYTICAL TOOLS

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Rajen Dias graduated with a MS and PhD in Materials Science from Lehigh University and joined Intel in 1984. He is currently a Principal Engineer in the Assembly Technology Development Quality & Reliability Group. His main areas of responsibility are in understanding failure modes and mechanisms of new package technologies and in developing next generation analytical tools and techniques for the failure analysis. He is a past General Chair of ECTC and a member of IEEE.

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Deepak Goyal graduated (PhD in Materials Science) from State University of New York, Stony Brook in 1990 and joined Intel as Failure analysis engineer. He is currently the Manager of the Assembly Materials Technology Lab at Intel. His group supports the materials and failure analysis of the Assembly technology development at Intel and next generation of analytical tools and techniques. He was the chair of the Assembly and Analytical Forum sponsored by the International Sematech in 2002. He is a senior member of the IEEE.

## PDC #4 – NEXT FRONTIER IN ELECTRONICS: SYSTEM SCALING FOR SMALL AND ULTRA-SMALL SMART MOBILE, WEARABLE, MEDICAL, AND IOP SYSTEMS

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Prof. Rao Tummala is a Distinguished and Endowed Chair Professor in MSE and ECE, and Founding Director of PRC, an NSF ERC at Georgia Tech. He is well known as an industrial technologist, technology pioneer, and educator. Prior to joining Georgia Tech, he was an IBM Fellow, pioneering such major technologies as the first plasma display and the first and next three generations of 100 chip multi-chip packaging. He is the father of LTCC and System-On-Package technologies. As an educator, Professor Tummala was instrumental in setting up the largest Academic Center in Electronics systems at Georgia Tech involving more than 200 PhD and MS students, 25 faculty from ECE, ME, MSE and CHE, and 70 companies from the US, Europe and Asia, all working together with an integrated approach to research, education and industry collaborations in ultraminiaturized and mega-functional System-on-Package

technologies. He received his B. E in Metallurgy from Indian Institute of Science, Bangalore and his PhD from University of Illinois, USA.

Prof. Tummala has published more than 500 journal and conference technical papers, holds 90 US patents and inventions; authored and edited the first modern packaging reference book—Microelectronics Packaging Handbook (Van Nostrand, 1988), the first undergrad textbook—Fundamentals of Microsystems Packaging (McGraw Hill, 2001) and the first graduate textbook introducing System-On-Package technology, comparing and contrasting it with SOC, SIP and 3D ICs. He is a Fellow of IEEE, IMAPS, and the American Ceramic Society, and member of the National Academy of Engineering in US and in India. Dr. Tummala was the President of both IEEE-CPMT and the IMAPS Societies.

He has received more than 30 industry, academic and professional society awards including the highest faculty award from Georgia Tech, and Distinguished Alumni from University of Illinois and Indian Institute of Science; Bangalore, India and IEEEs David Sarnoff, Major Education and Field Awards.

## PDC #5 – POLYMERS AND NANOCOMPOSITES FOR ELECTRONIC AND PHOTONIC PACKAGING

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Prof. C. P. Wong is currently Dean of the Faculty of Engineering at the Chinese University of Hong Kong. He is on a no pay long leave from Georgia Institute of Technology (GT) where he is a Regents' Professor and the Charles Smithgall Institute Endowed Chair at the School of Materials Science and Engineering He received his B.S. degree from Purdue University, and his Ph.D. degree from the Pennsylvania State University. After his doctoral study, he was awarded a two-year postdoctoral fellowship with Nobel Laureate Professor Henry Taube at Stanford University. Prior to joining GT in 1996, he was with AT&T Bell Laboratories for many years and became an AT&T Bell Laboratories Fellow in 1992 for his seminal contributions to low-cost high-performance packaging of semiconductor devices and components. His research interests lie in the fields of polymeric electronic materials, electronic, photonic and MEMS packaging and interconnect, interfacial adhesions, nano-functional material syntheses and characterizations, nano-composites such as well-aligned carbon nanotubes, graphenes, lead-free alloys, flip chip underfill, ultra high k capacitor composites and novel lotus effect coating materials. He received many awards, among those, the AT&T Bell Labs Fellow Award in 1992(the most prestigious Technical Award bestowed by Bell Labs), the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society Outstanding Sustained Technical Contributions Award in 1995, the IEEE Third Millennium Medal in 2000, the IEEE Educational Activity Board(EAB) Outstanding

Education Award in 2001, the IEEE CPMT Society Exceptional Technical Contributions Award in 2002, the Georgia Tech Class 1934 Distinguished Professor Award(the highest Award bestowed by GT to the faculty) in 2004, named holder of the Charles Smithgall Chair(one of the two GT Institute-Endowed Chairs) in 2005, the GT Outstanding PhD Thesis Advisor Award, the IEEE Components, Packaging and Manufacturing Technology Field Award in 2006(hailed as "Father of Modern Semiconductor Packaging"), the Sigma Xi's Monie Ferst Outstanding Educational Award in 2007, the Society of Manufacturing Engineers' Total Excellence in Electronic Manufacturing Award in 2008 and the IEEE CPMT David Feldman Award in 2009. He holds over 50 U.S. patents, and has published over 1,000 technical papers, co-authored and edited 10 books and is a member of the National Academy of Engineering of the USA since 2000.

Author Bio 2:
Dr. Daniel Lu is the Vice President of Product Development and Technical Customer Service of the Henkel Corporation in Asia Pacific. Prior to joining Henkel, he worked for the R&D department of Intel Corp (AZ, USA), as a Sr. Scientist for 7 years. He also had worked for Lucent Technologies, Amoco's Electronics Materials Division, and the Electronics Materials Group of National Starch and Chemical Company before. He has extensive experience in electronic packaging especially on materials and processing. He received his MS and PhD degrees on Polymer Science and Engineering from Georgia Institute of Technology in 1996 and 2000, respectively. Dr. Lu received many awards including the IEEE/CPMT Outstanding Young Engineer Award in 2004, the IEEE ECTC best poster paper in 2007, Intel's most patent filing in 2003-2007, Intel Divisional Recognition Awards in 2002, 2003, and 2007, Intel most patent granting of the year for 2006 and 2007. Dr. Lu has published more than 50 technical papers, wrote chapters for five books, and holds more than 80 US patents. He is the editor of the book "Materials for Advanced Packaging (2008)" and co-author of the book "Electronically Conductive Adhesives with Nanotechnologies (2009)". He has been serving key roles in organizing international electronic packaging conferences and teaching professional development short courses in these conferences. Dr. Lu is a senior member of IEEE, an Associate editor of IEEE Transactions on Advanced Packaging and Journal of Nanomaterials, and an editorial board member of Nanoscience & Nanotechnology-Asia. Dr. Lu is a member of CMPT Board of Governor Member-at-large.

## PDC #6 – INTEGRATED THERMAL PACKAGING AND RELIABILITY OF POWER ELECTRONICS

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Dr. Patrick McCluskey (Ph.D. 1991, Materials Science and Engineering, Lehigh University, Bethlehem, PA) is an Associate Professor of Mechanical Engineering at the University of Maryland, College Park, where he conducts research in the Center for Advanced Life Cycle Engineering (CALCE) in the areas of thermal management, reliability, and packaging of electronic microsystems for use in extreme temperature environments and high power applications. Dr. McCluskey has published more than 100 refereed technical articles on these subjects, and has edited three books. He has also served as technical chairman for multiple international conferences and workshops, and is an associate editor of the IEEE Transactions on Components, Packaging, and Manufacturing Technology. Dr. McCluskey has provided short courses on extreme temperature electronics and power electronics for companies in the Aerospace, automotive, motor drives, energy exploration and generation, and defense industries. He is a fellow of the International Microelectronics and Packaging Society (IMAPS), and is a member of ASME, IEEE, and SAE.

Author Bio 2:
Dr. Avram Bar-Cohen is an internationally recognized leader in the development and application of thermal science and engineering to microelectronic and optoelectronic systems. In his present role at the Defense Advanced Projects Agency (DARPA) and through his professional service in IEEE and ASME, he has helped to define and guide the field of thermal packaging. He is an honorary member of ASME and Fellow of IEEE, as well as Distinguished University Professor in the Department of Mechanical Engineering at the University of Maryland, where he served as Chair from 2001 to 2010. Bar-Cohen is the recipient of the IEEE CPMT Field Award for 2014 and has been previously recognized with the IEEE CPMT Society's Outstanding Sustained Technical Contributions Award (2002), among other awards from IEEE, ASME, and ICHMT. Bar-Cohen was the founding chair of the IEEE Intersociety Conference on Thermal Management in Electronic Equipment (ITHERM) in 1988 and served as the Editor of the CPT Transactions (1995-2005). He is the Editor-in-Chief of the Encyclopedia of Thermal Packaging (WSPC, 2012) and has co-edited 23 books, authored/co-authored 3 books and over 400 technical papers, delivered 70 keynotes, plenary and invited lectures, and holds 8 US and 3 Japanese patents.

## PDC #7 - FUNDAMENTAL CONCEPTS OF RELIABILITY AND MECHANICS IN ELECTRONIC PACKAGING

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Shubhada is currently a Senior Reliability Engineer at Intel Corporation. She graduated with Technical Engineering degree from University of Maryland, College park. In her 12 years career at Intel she has worked on developing reliability models, defining use conditions for knowledge based methodology and developing Q&R tools and methods for product-package-platform risk

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Sandeep Sane received his Ph.D. from California Institute of Technology, Pasadena in Aerospace Engineering with major in Solid Mechanics. He holds M.S. in Aeronautics, California Institute of Technology and B of Tech in Mechanical Engineering from Indian Institute of Technology, Bombay (Mumbai). Sandeep is currently a Principal Engineer in the Assembly and Test Technology Development (ATTD) organization, Intel Corp., Chandler. Sandeep has filed for more than 15 patents and has published several technical articles in various conferences and journal proceedings. He is also a recipient of numerous awards across Intel for his technical contributions. He is a member of ASME and an active member of organizing committees for ASME and IEEE conferences. He has strong background in technical problem solving, people management, planning and execution.

## PDC #8 – FUNDAMENTALS OF ELECTRICAL DESIGN AND FABRICATION PROCESSES OF INTERPOSERS INCLUDING THEIR RDLs

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Ivan Ndip received his M.Sc. and Ph.D. degrees in electrical engineering from the Technical University Berlin, Germany. In 2002, he joined Fraunhofer-IZM as a Research Engineer and worked on signal integrity modeling/design and on antenna design/integration. Since 2006, he has been a Senior Research Engineer and the Manager of RF & High-Speed System Design Group. He leads research activities that focus on electromagnetic modeling/design and optimization of antennas and RF/high-speed interposers/boards/modules/systems. Since 2008 Dr. Ndip has also been a Lecturer at the Technical University Berlin. He taught PDCs at the 43rd, 44th, 45th and 46th International Symposiums on Microelectronics in USA. He also taught PDCs at ECTC'12 and ECTC'13. Dr. Ndip has more than 120 publications in referred journals/ conference proceedings, and has won 6 best paper awards. He is a recipient of the Tiburtius-Prize, awarded yearly for outstanding Ph.D. dissertations in the State of Berlin. He is also the recipient of the 2012 Fraunhofer-IZM Research Award. He Chairs the Signal/Power Integrity Committee at IMAPS. He was Technical Co-chair of the 44th and 45th, the Technical Chair of the 46th, and is the General Chair of the 47th, International Symposium on Microelectronics in USA. He is a Senior Member of IEEE.

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Michael Töpper studied Chemistry (Diploma) and earned a PhD in Material Science. Since 1994 he is at the joint institutes Fraunhofer IZM and TU Berlin currently heading research projects in the area of WLP with a focus on polymeric materials. In 2006 he was a visiting professor at the University of Utah in Salt Lake City. Michael is the Technical Chair of IEEE-CPMT for WLP and was on the ECTC committee for emerging technologies for 5 years. He has published 4 book chapters and was author and co-author of over 200 technical publications and conference presentations. He is a Senior Member of IEEE.

PDC #9 – FLIP CHIP TECHNOLOGIES

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Eric Perfecto has over 30 years of experience at IBM working in the development of advanced packages for high-end systems. He holds an M.S. in Chemical Engineering from the University of Illinois and an M.S. in Operations Research from Union College. Until 2000, Eric worked on the development and implementation of multi-level thin films on ceramic substrates, leading projects in photolithography, chemical etching, photosensitive polyimide, pattern electroplating and bonding metallurgies for C4 joining, wire-bonding and LGA. He is currently the C4 Development Chief Technologist responsible for UBM and Pb-free solder implementation, and yields improvements for 3D applications. Eric has published over 50 external papers, including two best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds over 30 US patents, and has been honored with two IBM Outstanding Technical Achievement Awards. Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. He has achieved senior member status from IEEE, IMAPS and Society of Plastic Engineers. He is currently an elected member of the Board of Governors of the CPMT society of IEEE.

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Dr. Shengmin Wen, Sr. Manager, 3D CSP Product Group, Amkor Technology. He Joined Amkor Technology, Chandler, AZ, USA, in 2009, and has been working on chip scale package (CSP), package on package (PoP), and through mold via (TMV) products with flip chip packaging technologies, including the most advanced fine pitch Cu Pillar with TC/NCP assembly process. He previously worked for IBM/Infineon DRAM Development Alliance, Infineon Technologies AG, and Qimonda AG on various types of packaging technologies. Dr. Wen received his Ph.D. in Theoretical and Applied Mechanics from Northwestern University, Evanston, IL, USA, researching on fatigue and reliability of electronic materials, where he created and published a science based fatigue theory. Dr. Wen's technical expertise is in the areas of flip chip packaging solutions to CSP and PoP, package warpage control, package technology

reliability, and advanced packaging platform development and management. During past 16 years of semiconductor experience, he worked on research, development, production and business management. He has been actively participating and contributing to industry technical conferences, including ECTC, iMAPS, ITherm, IRPS, and ICEPT.

## PDC #10 - WAFER LEVEL CHIP SCALE PACKAGING

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## PDC #11 - MOISTURE AND MEDIA INFLUENCE ON MICROELECTRONIC PACKAGE RELIABILITY

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Tanja Braun studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. Since 2000 she is working with the group Assembly & Encapsulation Technologies and since 2012 she is deputy head of this group. Her field of research is process development of assembly and encapsulation, the qualification of these processes using both non-destructive and destructive tools and polymer encapsulant analysis using thermal / thermo-mechanical / rheological analysis methods. Recent

research is focused on reliable sensor packaging for automotive and bio-medical application as well as on wafer and panel level mold embedding technologies. In 2013 she received her Dr. from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun has organized as a workshop leader several short courses at international conferences or customized workshops for industrial partners in the field of microelectronic packaging. She also holds several patents in the field of advanced packaging.

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Hans Walter received his diploma degree in material science from Martin-Luther-University of Halle-Wittenberg (Germany) in 1995. From 1995 to 1999 he was a staff member of the department of Engineering Science at Martin-Luther-University. In 1995 he joined the Fraunhofer IZM Berlin where he is now a senior scientist. In 2003 he received his PhD in material science from the Martin-Luther-University for the work focusing comprehensive evaluation of toughness behavior of epoxy resin with miniature compact tension specimens and influence of moisture of the fracture properties. He was responsible for the implementation of the µ-material testing lab. From 2000 to 2010 he has been co-worker with the medium sized enterprise Angewandte Micro Messtechnik (AMIC). Since 2010 he is responsible manager of the group Micro-Nano-Reliability in the department Environmental and Reliability Engineering. His field of research is analysis of thermo mechanical properties of packaging relevant materials and modeling, evaluation of interface reliability, lifetime estimation, investigation of critical environmental conditions, and development of new test methods in the micro-nano range. In 2008 he received a Fraunhofer IZM Award for new designed test methods for materials testing with miniaturized sample geometry. Hans Walter has organized short courses and workshops for several partners in the field of reliability assessment. Furthermore, he currently gives lectures on the field of microsystems technology at the HTW-Berlin, University of Applied Sciences, Berlin. He has published several papers in the fields of micro-materials measurement techniques, fracture behavior, moisture induced properties and thermo-mechanical analysis from materials of electronic applications and has presented his papers at several international conferences.

## PDC #12 - THERMAL AND MECHANICAL SIMULATION TECHNIQUES FOR IC PACKAGE YIELD, RELIABILITY, AND PERFORMANCE

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Kamal Karimanal is the Founder of Cielution LLC, which is an Engineering simulation software and services company serving the electronics supply chain. Dr. Karimanal has served in several engineering simulation focused roles at IERC, Fluent Inc., ANSYS Inc., Globalfoundries, and Juniper Networks. Dr. Karimanal has contributed to several detailed and compact modeling methodologies which are being widely used by the electronics industry today. He has written several conference and journal papers and online application notes. Dr. Karimanal received his PhD in Mechanical Engineering from The University of Texas at Austin.

## PDC #13 - POLYMERS FOR ELECTRONIC PACKAGING

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Dr. Jeff Gotro has over thirty two years' experience in polymers for electronic applications and composites having held scientific and leadership positions at IBM, AlliedSignal, Honeywell, and Ablestik Laboratories. He has published 60 technical papers (including 4 book chapters) in the field of polymeric materials for advanced electronic packaging applications, holds 13 issued US patents, and has 8 patents pending. Jeff is an expert in thermosetting polymers and he has received invitations to speak at Gordon Research Conferences (Thermosetting Polymers and Composites). He has presented numerous invited lectures and short courses at national technical conferences. Jeff was an Adjunct Professor at Syracuse University in the Dept. of Chemical Engineering and Materials Science from 1986-1993. Jeff is a member of the Product Development and Management Association (PDMA), American Chemical Society (ACS), the Institute for Management Consultants (IMC), the Forensic Expert Witness Association (FEWA), and a Fellow of the International Microelectronics and Packaging Society (IMAPS). In 2014, he received the John Wagnon Technical Achievement Award from IMAPS. Jeff has a Ph.D. in Materials Science from Northwestern University with a specialty in polymer science and a B.S. in Mechanical Engineering/Materials Science from Marquette University.

## PDC #14 – NOVEL INTERCONNECT AND SYSTEM INTEGRATION TECHNOLOGIES

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Muhannad S. Bakir received the B.E.E. degree (summa cum laude) from Auburn University, Auburn, AL, in 1999 and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech) in 2000 and 2003, respectively.
He is currently an Associate Professor and the ON Semiconductor Junior Professor in the School of Electrical and Computer Engineering at Georgia Tech. Dr. Bakir is the recipient of the 2013 Intel Early Career Faculty Honor Award, 2012 DARPA Young Faculty Award, 2011 IEEE CPMT Society Outstanding Young Engineer Award, and was an Invited Participant in the 2012 National Academy of Engineering Frontiers of Engineering Symposium. He is also a recipient of the Semiconductor Research Corporation (SRC) Inventor Recognition Awards (2002, 2005, and 2009). Dr. Bakir and his research group have received fourteen conference and student paper awards including five from the IEEE Electronic Components and Technology Conference (ECTC), four from the IEEE International Interconnect Technology Conference (IITC), and one from the IEEE Custom Integrated Circuits Conference (CICC). Dr. Bakir is an Editor of IEEE

Transactions on Electron Devices, an Associate Editor of IEEE Transactions on Components, Packaging and Manufacturing Technology, and was a Guest Editor of the June 2011 Special Issue of IEEE Journal of Selected Topics in Quantum Electronics. He is also a member of the International Technology Roadmap for Semiconductors (ITRS) technical working group for Assembly and Packaging (AP).

## PDC #15 - PACKAGE FAILURE MECHANISMS, RELIABILITY, AND SOLUTIONS

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Darvin R. Edwards joined Texas Instruments in 1980 after receiving the B.S. degree in Physics from Arizona State University. He has been responsible for developing integrated test structures to evaluate chip/package interactions, improving the thermal performance of TI's products, and for leading the Dallas package modeling team for fifteen years. Elected TI Fellow in 1999, he was most recently responsible for Analog Si/Pkg interactions within the Semiconductor Packaging Group before retiring in 2013. Darvin is currently a consultant specializing in helping companies solve package reliability problems and in overcoming thermal issues. He serves as Member at Large for the IEEE CPTM society and is on the program committee of the Electronics Components and Technology Conference. Darvin has authored and co-authored over 50 papers and articles in the field of IC packaging, has written two book chapters, and holds 20 US patents.

## PDC #16 - 3D IC SI INTEGRATION AND 3D SI PACKAGING

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Author Bio:
3D IC packaging and 3D IC integration are different. In general, the TSV (through-silicon via) separates 3D IC packaging from 3D IC integration because the latter use TSVs, but 3D IC packaging does not. TSV is the heart of 3D IC integration. It provides the opportunity for the shortest chip-to-chip, and the smallest pad size and pitch of interconnects. The potential high volume manufacturing of 3D IC integration is: (1) memory-chip stacking, (2) wide I/O memory (or logic-on-logic), (3) wide I/O DRAM, wide I/O 2, HMC, and HBM, and (4) wide I/O interface (or 2.5D IC integration). In this presentation, the supply chains and the critical steps such as FEOL, MOL, BEOL, TSV, MEOL (middle-end-of-line), assembly, and test and their ownerships for high-volume manufacturing for those 4 groups of 3D IC integration will be discussed. The 3D IC packaging, which has been keeping 3D IC integration away from volume production, will be briefly mentioned first. Key enabling technologies such as TSV forming and filling, front and backside metallization, RDL, temporary bonding and de-bonding, and microbumping, assembly and reliability will be presented and discussed. All the materials are based on the papers and books published by the lecturer and others.