1. ACHIEVING HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIALS CONSIDERATIONS

Course Leader: Ning-Cheng Lee – Indium Corporation

Ning-Cheng Lee is the Vice President of Technology of Indium Corporation. He has been with Indium since 1986. Prior to joining Indium, he was with Morton Chemical and SCM. He has more than 20 years of experience in the development of fluxes and solder pastes for SMT industries. In addition, he also has very extensive experience in the development of underfills and adhesives. He received his PhD in polymer science from University of Akron in 1981, and BS in chemistry from National Taiwan University in 1973. Ning-Cheng is the author of book "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies", and co-author of book "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials". He is also the author of book chapters for several lead-free soldering books. He received several best conference papers awards from SMTA and IPC. He was honored as 2002 Member of Distinction from SMTA, 2003 Lead Free Co-Operation Award from Soldertec, 2006 Exceptional Technical Achievement Award from CPMT, 2007 Distinguished Lecturer from CPMT, 2009 Distinguished Author from SMTA, and 2010 Electronics Manufacturing Technology Award from CPMT.

2. WAFER LEVEL CHIP SCALE PACKAGING

Course Leader: Luu Nguyen – Texas Instruments

Luu Nguyen is a TI Fellow at Texas Instruments. He's currently in the Packaging R&D Group at Texas Instruments, Silicon Valley Analog, working on various aspects of wafer-level packaging, lead-free and halogen-free, thermal measurement and modeling, design-for-manufacturability, high voltage, and MEMS. He received his Ph.D. in Mechanical Engineering from MIT, and has worked at IBM Research and Philips Research. He co-edited two books on packaging, and has over 200 publications. He has over 70 patents and invention disclosures. He is a Fellow of IEEE and ASME, and a Fulbright Scholar (Finland 2002). He is currently an Associate Editor for the IEEE Transactions on Components, Packaging and Manufacturing Technology. He was a Guest Editor for the Transactions on Electronic Packaging Manufacturing for a special issue on Drop Testing, and the Transactions on Advanced Packaging for two issues on Wafer Level Packaging. He received two Best of Conference Awards (27th IEMT 2002 and InterPack 2005) and eight IMAPS and IEMT Best of Session Conference Awards. Other awards include the 2003 Mahboob Khan Outstanding Mentor Award from the Semiconductor Research Corporation in recognition of contributions to student mentoring, research collaboration, and technology transfer, and the 2004 IEEE CPMT Outstanding Sustained Technical Contributions Award.

3. LED PACKAGING, SYSTEM, AND RELIABILITY CONSIDERATIONS

Course Leader: Xuejun Fan – Lamar University

Xuejun Fan is a Professor in the Department of Mechanical Engineering at Lamar University, Beaumont, Texas. He serves Chair of newly formed sub-committee of Thermal/Mechanical

Modeling and Characterization. Dr. Fan's PDCs have been very well received in the past many years at ECTC. He has given more than 60 tutorials, keynotes, invited talks and short courses worldwide last five years. He is an IEEE CPMT Distinguished Lecturer. Dr. Fan received his Ph.D. degree in solid mechanics from Tsinghua University, Beijing, China in 1989. He earned his Master degree and Bachelor degree in applied mechanics from Tianjin University, Tianjin, China in 1986 and 1984. Dr. Fan has had more than 20 years of experience in academia and semiconductor industry, in particular, 10 years in industry with Intel Cooperation, Philips Research, and the Institute of Microelectronics (IME). His interests and research lie in the areas of design, modeling, material characterization, and reliability in micro-/nano-electronic packaging and microsystems. Dr. Fan received IEEE CPMT Exceptional Technical Achievement Award in 2011. He received the Best Paper Award of 2008 IEEE Transactions on Components and Packaging Technologies. Dr. Fan is an Associate Editor of IEEE Transactions on Components, Packaging and Manufacturing Technologies. He serves as chair, co-chairs, and committee members of various conferences such as ECTC, EPTC, ESTC, EuroSimE, ICEPT, ESREF, EMPT, and ChinaSSL. In his earlier career in China, Dr. Fan was promoted to a full professor at age 27, and became one of the youngest full professors in China. He was the nominee for the title of "1991 Ten Outstanding Youth of China". Dr. Fan has published over 180 technical papers, filed 5 patents, and has published three books.

4. SYSTEM SCALING FOR NEW ERA OF SELF-DRIVING, INFOTAINING AND ELECTRIC CARS

Course Leaders: Rao Tummala and Venky Sundaram – Georgia Institute of Technology

Prof. Rao Tummala is a Distinguished and Endowed Chair Professor in MSE and ECE, and Founding Director of PRC, an NSF ERC at Georgia Tech. He is well known as an industrial technologist, technology pioneer, and educator. Prior to joining Georgia Tech, he was an IBM Fellow, pioneering such major technologies as the first plasma display and the first and next three generations of 100 chip multi-chip packaging. He is the father of LTCC and System-On-Package technologies. As an educator, Professor Tummala was instrumental in setting up the largest Academic Center in Electronics systems at Georgia Tech involving more than 200 PhD and MS students, 25 faculty from ECE, ME, MSE and CHE, and 70 companies from the US, Europe and Asia, all working together with an integrated approach to research, education and industry collaborations in ultraminiaturized and mega-functional System-on-Package technologies. He received his B. E in Metallurgy from Indian Institute of Science, Bangalore and his PhD from University of Illinois, USA.

Prof. Tummala has published more than 500 journal and conference technical papers, holds 90 US patents and inventions; authored and edited the first modern packaging reference book—Microelectronics Packaging Handbook (Van Nostrand, 1988), the first undergrad textbook—Fundamentals of Microsystems Packaging (McGraw Hill, 2001) and the first graduate textbook introducing System-On-Package technology, comparing and contrasting it with SOC, SIP and 3D ICs. He is a Fellow of IEEE, IMAPS, and the American Ceramic Society, and member of the

National Academy of Engineering in US and in India. Dr. Tummala was the President of both IEEE-CPMT and the IMAPS Societies. He has received more than 30 industry, academic and professional society awards including the highest faculty award from Georgia Tech, and Distinguished Alumni from University of Illinois and Indian Institute of Science; Bangalore, India and IEEEs David Sarnoff, Major Education and Field Awards.

Venky Sundaram is the Associate Director of Industry Programs at PRC, Georgia Tech and also serves as Program Manager for the Glass Package Consortium. He has been with the PRC since 1997 focusing on System on a Package (SOP) technology, ultra-high density substrates and systems integration research. He is a globally recognized expert on 3D packaging, substrates and interposers. He is currently serving as the chair of the IEEE CPMT Technical Committee of High Density Substrates, and as the Director of Student Programs on the Executive Council of IMAPS.

5. POLYMERS AND NANO-COMPOSITES FOR ELECTRONIC AND PHOTONIC PACKAGING

Course Leaders: C. P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation

Prof. C. P. Wong is currently Dean of the Faculty of Engineering at the Chinese University of Hong Kong. He is on a no pay long leave from Georgia Institute of Technology (GT) where he is a Regents' Professor and the Charles Smithgall Institute Endowed Chair at the School of Materials Science and Engineering He received his B.S. degree from Purdue University, and his Ph.D. degree from the Pennsylvania State University. After his doctoral study, he was awarded a two-year postdoctoral fellowship with Nobel Laureate Professor Henry Taube at Stanford University. Prior to joining GT in 1996, he was with AT&T Bell Laboratories for many years and became an AT&T Bell Laboratories Fellow in 1992 for his seminal contributions to low-cost high-performance packaging of semiconductor devices and components. His research interests lie in the fields of polymeric electronic materials, electronic, photonic and MEMS packaging and interconnect, interfacial adhesions, nano-functional material syntheses and characterizations, nano-composites such as well-aligned carbon nanotubes, graphenes, lead-free alloys, flip chip underfill, ultra high k capacitor composites and novel lotus effect coating materials. He received many awards, among those, the AT&T Bell Labs Fellow Award in 1992(the most prestigious Technical Award bestowed by Bell Labs), the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society Outstanding Sustained Technical Contributions Award in 1995, the IEEE Third Millennium Medal in 2000, the IEEE Educational Activity Board(EAB) Outstanding Education Award in 2001, the IEEE CPMT Society Exceptional Technical Contributions Award in 2002, the Georgia Tech Class 1934 Distinguished Professor Award(the highest Award bestowed by GT to the faculty) in 2004, named holder of the Charles Smithgall Chair(one of the two GT Institute-Endowed Chairs) in 2005, the GT Outstanding PhD Thesis Advisor Award, the IEEE Components, Packaging and Manufacturing Technology Field Award in 2006(hailed as "Father of Modern Semiconductor Packaging"), the Sigma Xi's Monie Ferst Outstanding

Educational Award in 2007, the Society of Manufacturing Engineers' Total Excellence in Electronic Manufacturing Award in 2008 and the IEEE CPMT David Feldman Award in 2009. He holds over 50 U.S. patents, and has published over 1,000 technical papers, co-authored and edited 10 books and is a member of the National Academy of Engineering of the USA since 2000.

Dr. Daniel Lu is the Vice President of Product Development and Technical Customer Service of the Henkel Corporation in Asia Pacific. Prior to joining Henkel, he worked for the R&D department of Intel Corp (AZ, USA), as a Sr. Scientist for 7 years. He also had worked for Lucent Technologies, Amoco's Electronics Materials Division, and the Electronics Materials Group of National Starch and Chemical Company before. He has extensive experience in electronic packaging especially on materials and processing. He received his MS and PhD degrees on Polymer Science and Engineering from Georgia Institute of Technology in 1996 and 2000, respectively. Dr. Lu received many awards including the IEEE/CPMT Outstanding Young Engineer Award in 2004, the IEEE ECTC best poster paper in 2007, Intel's most patent filing in 2003-2007, Intel Divisional Recognition Awards in 2002, 2003, and 2007, Intel most patent granting of the year for 2006 and 2007. Dr. Lu has published more than 50 technical papers, wrote chapters for five books, and holds more than 80 US patents. He is the editor of the book "Materials for Advanced Packaging (2008)" and co-author of the book "Electronically Conductive Adhesives with Nanotechnologies (2009)". He has been serving key roles in organizing international electronic packaging conferences and teaching professional development short courses in these conferences. Dr. Lu is a senior member of IEEE, and an associate editor of IEEE Transactions on Advanced Packaging and Journal of Nanomaterials, and an editorial board member of Nanoscience & Nanotechnology-Asia. Dr. Lu is a member of CMPT Board of Governor Member-at-large.

6. INTEGRATED THERMAL PACKAGING AND RELIABILITY OF POWER ELECTRONICS

Course Leader: Patrick McCluskey and Avram Bar- Cohen – University of Maryland

Patrick McCluskey (Ph.D. 1991, Materials Science and Engineering, Lehigh University, Bethlehem, PA) is a Professor of Mechanical Engineering at the University of Maryland, College Park, where he conducts research in the Center for Advanced Life Cycle Engineering (CALCE) in the areas of thermal management, reliability, and packaging of electronic microsystems for use in extreme temperature environments and high power applications. Dr. McCluskey has published more than 100 refereed technical articles on these subjects, and has edited three books. He has also served as technical chairman for multiple international conferences and workshops, and is an associate editor of the IEEE Transactions on Components, Packaging, and Manufacturing Technology. Dr. McCluskey has provided short courses on extreme temperature electronics and power electronics for companies in the aerospace, automotive, motor drives, energy exploration and generation, and defense industries. He is a fellow of the International

Microelectronics and Packaging Society (IMAPS), a senior member of IEEE, and a member of ASME, TMS, and SAE.

Dr. Avram Bar-Cohen is a Distinguished University Professor at the University of Maryland, and an internationally recognized leader in the development and application of thermal science and engineering to microelectronic and optoelectronic systems. Through his recent leadership of the thermal sciences portfolio at DARPA and his professional service in IEEE and ASME, he has helped to define and guide the field of thermal packaging. He served as Chair of the Department of Mechanical Engineering at the University of Maryland from 2001 to 2010. An Honorary member of ASME and Fellow of IEEE, Professor Bar-Cohen is the recipient of the IEEE CPMT Field Award for 2014 and has been previously recognized with the IEEE CPMT Society's Outstanding Sustained Technical Contributions Award (2002), among other awards from IEEE, ASME, and ICHMT. Bar-Cohen was the founding chair of the IEEE Intersociety Conference on Thermal Management in Electronic Equipment (ITHERM) in 1988 and served as the Editor of the CPT Transactions (1995-2005). He is the Editor-in-Chief of the Encyclopedia of Thermal Packaging (WSPC, 2012) and has co-edited 23 books, authored/co-authored 3 books and over 400 technical papers, delivered 70 keynotes, plenary and invited lectures, and holds 9 US and 3 Japanese patents.

7. FUNDAMENTALS OF ELECTRICAL DESIGN AND FABRICATION PROCESSES OF INTERPOSERS, INCLUDING THEIR RDLs

Course Leaders: Ivan Ndip and Michael Töpper – Fraunhofer IZM

Ivan Ndip received his M.Sc. and Ph.D. degrees in electrical engineering from the Technical University Berlin, Germany. In 2002, he joined Fraunhofer-IZM as a Research Engineer and worked on signal integrity modeling/design and on antenna design/integration. From 2005 to 2014 he was a Group Manager. Since 2014, he has been Head of the Department of RF & Smart Sensor Systems at IZM, where he leads R&D activities pursued in four Groups on RF/High-Speed Design; Sensor Nodes; WSNs and Micro-Energy Storage/Supply. Ivan is also a Lecturer at the Technical University Berlin. He taught PDCs at the 43rd, 44th, 45th and 46th International Symposiums on Microelectronics in USA. He also taught PDCs at ECTC'12, '13 & '14. Ivan has more than 130 publications in referred journals/conference proceedings, and has won 6 best-paper awards. He is a recipient of the Tiburtius-Prize, awarded yearly for outstanding Ph.D. dissertations in the State of Berlin, and also the recipient of the 2012 Fraunhofer-IZM Research-Award. He chairs the Signal/Power Integrity Committee at IMAPS, and is a Senior Member of IEEE. Ivan was Technical Co-chair of the 44th and 45th, the Technical Chair of the 46th, and is the General Chair of the 47th International Symposium on Microelectronics.

Michael Töpper studied Chemistry (Diploma) and earned a PhD in Material Science. Since 1994 he is at the joint institutes Fraunhofer IZM and TU Berlin currently heading research projects in the area of WLP with a focus on polymeric materials. In 2006 he was a visiting professor at the University of Utah in Salt Lake City. Michael is the Technical Chair of IEEE-CPMT for WLP

and was on the ECTC committee for emerging technologies for 5 years. He has published 4 book chapters and was author and co-author of over 200 technical publications and conference presentations.

8. INTRODUCTION TO MECHANICS BASED QUALITY AND RELIABILITY ASSESSMENT METHODOLOGY

Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation

Shubhada Sahasrabudhe is currently a TD Q&R Engineering Manager at Intel Corporation. She graduated with Mechanical Engineering degree from University of Maryland, College park. She is currently responsible of thermal enabling quality and reliability engineering for Assembly and Test Technology Development (ATTD). In her 12 years career at Intel she has worked on developing reliability models, defining use conditions for knowledge based methodology, developing advanced Q&R statistical models and developing Q&R tools and methods for product-package-platform risk optimization. She has published many Intel internal and external papers in the field of electronic packaging and product modeling, has filed many patents and has taught packaging technology reliability courses at Arizona State University and Packaging Conferences.

Sandeep Sane is a Principal Engineer at Intel. He received his M.S. /Ph.D. from California Institute of Technology, Pasadena in Aerospace Engineering with major in Solid Mechanics. He holds B.S. in Mechanical Engineering from Indian Institute of Technology, Bombay (Mumbai). Sandeep is currently responsible to drive novel technical solutions across packaging technologies in the Assembly and Test Technology Development (ATTD) organization, Intel Corp., Chandler. In the past he managed a technical team of 30 engineers with a charter to deliver fundamental understanding of various mechanical issues in electronic packaging, establish roadmaps for ATTD and work directly with Intel's customers (OEM/ODMs) and suppliers to resolve thermo-mechanical issues. Sandeep has filed for more than 15 patents and have published several technical articles in various conferences and journal proceedings. He is also a recipient of numerous awards across Intel for his technical contributions.

9. THERMO-ELECTRIC COOLERS: CHARACTERIZATION, RELIABILITY, AND MODELING

Course Leader: Jaime Sanchez – Intel

Jaime Sanchez has a Ph.D. in Mechanical Engineering from the University of Kentucky and is a licensed Professional Engineer. He has written various archival publications in the areas of nanoscale heat transfer and molecular simulations, as well as conference presentations on test challenges of high volume manufacturing of microprocessors. He joined Intel in 2008 and his team is in charge of research and development of test equipment used in silicon validation labs. His work is focused on thermal-mechanical design and challenges for test to support all products in Intel's roadmap.

10. FLIP CHIP FABRICATION AND INTERCONNECTION

Course Leaders: Eric Perfecto – GLOBALFOUNDRIES; Shengmin Wen – Synaptics Inc.

Eric Perfecto has 34 years of experience working in the development and implementation of advanced packages. He is currently Principal Member of the Technical Staff at GLOBALFOUNDRIES. Previously, he served as C4 Development Chief Technologist at IBM responsible for UBM and Pb-free solder definition for u-Pillar interconnect, and yield improvements in C4 and 3D wafer finishing. His technical interests include flip chip, 2.5 & 3D fabrication, chip-package interaction, electromigration, multi-level Cu-Polymer wiring structures, and design for manufacturing. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College. Eric has published over 70 external papers, including two best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds over 40 US patents, and has been honored with two IBM Outstanding Technical Achievement Awards. Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. He has achieved senior member status from IEEE, IMAPS and Society of Plastic Engineers. He is a Distinguish Lecturer of the CPMT society of IEEE, and the CPMT Awards Program Director.

Dr. Shengmin Wen is Principal Development Engineer at Synaptics Inc., has 18 years of semiconductor industry experience in the areas of failure analysis, reliability, Si and packaging technology development, testing, qualification, and volume production management. Recent years, he focused on chip scale package (CSP), package on package (PoP), through mold via (TMV) products with Cu Pillar flip chip packaging technologies, including warpage control, substrate technology development, bumping technology, and advanced fine pitch assembly process. He previously worked at Amkor technology where he was a director of 3D CSP Product Group, developing and managing Cu Pillar flip chip technology with mass reflow, thermal compression or a combined multichip packaging technologies. Dr. Wen received his Ph.D. in Theoretical and Applied Mechanics from Northwestern University, Evanston, IL, USA, researching on fatigue and reliability of electronic materials, where he created and published a science based fatigue theory. Dr. Wen has been actively participating and contributing to industry technical conferences to learn, to share and to contribute.

11. FAN-OUT WAFER LEVEL PACKAGING

Course Leader: Beth Keser – Qualcomm Technologies, Inc.

Beth Keser has over 17 years' experience in the semiconductor industry. Beth received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. in Materials Science and Engineering at the University of Illinois at Urbana-Champaign. Beth's development of materials and packaging technologies for the semiconductor industry has resulted in 8 patents, 10 patents pending, and over 40 publications in this area. Currently, Beth is the Fan-Out Wafer Level Packaging Technology Manager at Qualcomm, San Diego. Before joining Qualcomm in

2009, Beth Keser was instrumental in developing 2 packaging technologies during her career at Motorola and Freescale Semiconductor. Beth led the Wafer-Level Chip Scale packaging team at Motorola, which included directing the activities of process engineering, package characterization, package reliability, and mechanical modeling. In addition, Beth Keser was the lead technologist and manager of the Redistributed Chip Packaging Technology (RCP). Beth led the team that developed this technology for 6 years. Beth developed several process and material solutions for this new technology. Beth is an IEEE Senior Member whose volunteer activities and professional society responsibilities include: CPMT Board of Governors 2012-2014, 2015 General Chair, 2013 Program Chair, 2012 Assistant Program Chair and Advanced Packaging Sub-committee member 2000-present.

12. OPERATION, DESIGN, CHARACTERISTICS, AND KEY PARAMETERS OF INTEGRATED SILICON ANALOG COMPONENTS

Course Leader: Badih El-Kareh – Consultant

Badih El-Kareh is an independent consultant, retired IBM and Texas Instruments physicist. He has 45 years' experience in semiconductor device design, process integration, and characterization. This includes the development of advanced Silicon-Germanium low and high voltage CMOS and BiCMOS processes and devices for analog, memory, and digital applications. He has 30 years' experience in academic and industrial teaching and is author of a book on VLSI Silicon Devices, on Modern Semiconductor Processing Technologies, on Silicon Devices and Process Integration, and on Silicon Analog Components. He has authored and co-authored 34 papers and has 50 US patents issued. Dr. El-Kareh is a senior member of the IEEE.

13. DESIGN AND ANALYSIS OF HIGH-PERFORMANCE MEMORY SYSTEMS

Course Leader: Wendem Beyene – Rambus

Wendemagegnehu (Wendem) T. Beyene received his B.S. and M.S. degrees in Electrical Engineering from Columbia University, in 1988 and 1991 respectively, and his Ph.D. degree in Electrical and Computer Engineering from University of Illinois at Urbana-Champaign, in 1997. From 1988 to 1994, he was with the IBM, Microelectronics division, Fishkill, NY, where he worked on design and electrical characterization of advanced multilayer packages. From 1997 to 2000, he was with Hewlett-Packard Company and Agilent Technologies EEsof Davison at Westlake Village, CA working on analog and RF circuit simulation tools. He is currently a Technical Director at Rambus Inc., Sunnyvale, CA and is responsible for signal and power integrity of multi-gigabit memory parallel and serial interface and high-speed link architecture of the development of analysis techniques to define equalization architecture and evaluate timing recovery of high-speed SerDes. He has written over 120 papers in design, modeling, simulation, and measurement of devices and high-speed systems. He is a senior member of IEEE and has served as Guest Associate Editor of a Special Issue on high-speed IO channels in IEEE Transactions on Advanced Packaging in May 2009. Since 2010, he has been associate editor of IEEE Transactions on Components, Packaging and Manufacturing Technology. He also serves on the technical committees of leading international conferences such as IEEE Electronic

Components and Technology Conference (ECTC), IEEE Electrical Performance of Electrical Packaging and Systems (EPEPS), IEEE Workshop on High-Performance Chip, Package, and Systems (HPCPS), IEEE Workshop on Signal and Power Integrity (SPI), IEEE Electrical Design of Advanced Packaging and Systems (EDAPS), and DesignCon.

14. POLYMERS FOR ELECTRONIC PACKAGING

Course Leader: Jeffrey Gotro – InnoCentrix, LLC

Dr. Jeff Gotro has over thirty two years' experience in polymers for electronic applications and composites having held scientific and leadership positions at IBM, AlliedSignal, Honeywell, and Ablestik Laboratories. He has published 60 technical papers (including 4 book chapters) in the field of polymeric materials for advanced electronic packaging applications, holds 13 issued US patents, and has 8 patents pending. Jeff is an expert in thermosetting polymers and he has received invitations to speak at Gordon Research Conferences (Thermosetting Polymers and Composites). He has presented numerous invited lectures and short courses at national technical conferences. Jeff was an Adjunct Professor at Syracuse University in the Dept. of Chemical Engineering and Materials Science from 1986-1993. Jeff is a member of the Product Development and Management Association (PDMA), American Chemical Society (ACS), the Institute for Management Consultants (IMC), the Forensic Expert Witness Association (FEWA), and a Fellow of the International Microelectronics and Packaging Society (IMAPS). In 2014, he received the John Wagnon Technical Achievement Award from IMAPS. Jeff has a Ph.D. in Materials Science from Northwestern University with a specialty in polymer science and a B.S. in Mechanical Engineering/Materials Science from Marquette University.

15. NOVEL INTERCONNECT AND SYSTEM INTEGRATION TECHNOLOGIES

Course Leader: Muhannad Bakir – Georgia Institute of Technology

Muhannad Bakir is an Associate Professor in the School of Electrical and Computer Engineering at Georgia Tech. His areas of interest include three-dimensional (3D) electronic system integration, advanced cooling and power delivery for 3D systems, biosensors and their integration with CMOS circuitry, and nanofabrication technology. Dr. Bakir is the recipient of the 2013 Intel Early Career Faculty Honor Award, 2012 DARPA Young Faculty Award, and 2011 IEEE CPMT Society Outstanding Young Engineer Award. In 2015, Dr. Bakir was elected by the IEEE CPMT Society to serve as a Distinguished Lecturer for a four-year term. Dr. Bakir and his research group have received fourteen conference and student paper awards including five from the IEEE Electronic Components and Technology Conference (ECTC), four from the IEEE International Interconnect Technology Conference (IITC), and one from the IEEE Custom Integrated Circuits Conference (CICC). Dr. Bakir's group was awarded the 2014 Best Paper of the IEEE Transactions on Components Packaging and Manufacturing Technology in the area of advanced packaging.

16. PACKAGE FAILURE MECHANISMS, RELIABILITY, AND SOLUTIONS

Course Leader: Darvin Edwards – Edwards Enterprises

Darvin R. Edwards joined Texas Instruments in 1980 after receiving the B.S. degree in Physics from Arizona State University. He has been responsible for developing integrated test structures to evaluate chip/package interactions, improving the thermal performance of TI's products, and for leading the Dallas package modeling team for fifteen years. He wrote a series of design rules to ensure package reliability, and helped develop such technologies as flip-chip BGA, CSP, WCSP and TSVs. Along the way, he helped introduce HAST and standardized thermal tests. Elected TI Fellow in 1999, he was most recently responsible for Analog Si/Pkg interactions within the Semiconductor Packaging Group before retiring in 2013. Darvin is currently a consultant specializing in helping companies solve package reliability and thermal problems, as well as providing worldwide training. He serves as Member at Large for the IEEE CPTM society and is on the program committee of the Electronics Components and Technology Conference where he has served as chair of the Applied Reliability committee many times. Darvin has authored and co-authored over 60 papers and articles in the field of IC packaging, has written two book chapters, and holds 22 US patents. He has been active with JEDEC, SRC, and iNEMI.

17. 3D IC INTEGRATION AND 3D IC PACKAGING

Course Leader: John Lau – ASM Pacific Technology Ltd.

John H. Lau has been a Sr. Technical Advisor of ASM since July 2014. Prior to that, he was an ITRI Fellow of Industrial Technology Research Institute for 4.5 years, a visiting professor at HKUST for 1 year, the Director of MMC Laboratory with IME Singapore for 2 years and a Senior Scientist/MTS at HPL/Agilent in California, US for more than 25 years. With more than 37 years of R&D and manufacturing experience, he has published more than 435 peer-reviewed papers, 30 issued and pending, and 18 textbooks on wafer-level flip chip technologies, TSV for 3D integration, 3D MEMS packaging, 3D IC integration and packaging, and reliability of 2D and 3D IC interconnections. John received many awards and is an elected ASME Fellow and has been an IEEE Fellow since 1994.

18. THERMO-ELECTRICAL CO-DESIGN OF 3D CHIP STACKS

Course Leader: Ankur Srivastava and Avram Bar-Cohen – University of Maryland

Dr. Avram Bar-Cohen is a Distinguished University Professor at the University of Maryland, and an internationally recognized leader in the development and application of thermal science and engineering to microelectronic and optoelectronic systems. Through his recent leadership of the thermal sciences portfolio at DARPA and his professional service in IEEE and ASME, he has helped to define and guide the field of thermal packaging. He served as Chair of the Department of Mechanical Engineering at the University of Maryland from 2001 to 2010. An Honorary member of ASME and Fellow of IEEE, Professor Bar-Cohen is the recipient of the IEEE CPMT Field Award for 2014 and has been previously recognized with the IEEE CPMT Society's Outstanding Sustained Technical Contributions Award (2002), among other awards from IEEE, ASME, and ICHMT. Bar-Cohen was the founding chair of the IEEE Intersociety Conference on Thermal Management in Electronic Equipment (ITHERM) in 1988 and served as the Editor of

the CPT Transactions (1995-2005). He is the Editor-in-Chief of the Encyclopedia of Thermal Packaging (WSPC, 2012) and has co-edited 23 books, authored/co-authored 3 books and over 400 technical papers, delivered 70 keynotes, plenary and invited lectures, and holds 9 US and 3 Japanese patents.

Dr. Ankur Srivastava is an associate professor at the University of Maryland College Park in the Electrical and Computer Engineering department with a joint appointment with the Institute for Systems Research. He is also the Associate Chair for Graduate Studies and Research for the ECE department. He received his bachelors in technology from the Indian Institute of Technology Delhi in May 1998 with Electrical Engineering major, Masters in Computer Engineering in June 2000 from department of ECE Northwestern University and PhD from CS department of University of California Los Angeles in September 2002. His main area of interest is design methods and runtime control policies for high performance, low energy, low temperature and low power multi-core processors and other VLSI circuits. He is the recipient of the "Outstanding PhD Award" from the Computer Science Department of UCLA and the George Corcoran Memorial Outstanding Teaching Award by the ECE department of University of Maryland. His work has also been recognized by several best paper awards (ISPD 2007, AHS 2011, ISVLSI 2012) and nominations (ICCAD 2003, DAC 2012). He has published more than 100 conference and journal papers, delivered several invited seminars and keynotes and also served on various conferences organizing committees. He is also the Associate Editor for IEEE Transactions on CAD, IEEE Transactions on VLSI and the Integration journal. He has been working at the University of Maryland since October 2002.