10. Fan-Out Wafer/Panel Level Packaging and 3D Chiplet Heterogeneous Integrations

Course Leader: John Lau – Unimicron Technology Corporation

Course Objective:

In this lecture, the following topics will be presented and discussed. Emphasis is placed on the latest developments of these areas in the past three years. Their future trends will also be explored.

Course Outline:

1. Formation of Fan-out Wafer-Level Packaging (FOWLP)
    a. FOWLP Chip-first (die face-down),
    b. FOWLP Chip-first (die face-up), and
    c. FOWLP Chip-last (RDL-first).
2. Fabrication of Redistribution Layers (RDLs)
    a. Polymer and ECD Cu + Etching,
    b. PECVD and Cu damascene + CMP, and
    c. Hybrid RDLs.
3. TSMC InFO-WLP, InFO-PoP, InFO_AiP
4. Formation of Fan-out Panel-Level Packaging (FOPLP)
    a. PCB + SAP,
    b. PCB + LDI,
    c. PCB + TFT-LCD, and
    d. PCB/ABF/SAP + LDI.
5. Wafer vs. Panel: (a) Application Ranges of FOWLP and FOPLP, and (b) Critical Issues of FOPLP
6. Trends in FOWLP and FOPLP
7. System-on-Chip (SoC)
8. Heterogeneous Integration vs. SoC
9. Heterogeneous Integration on Organic Substrates (SiPs)
10. Heterogeneous Integration on Silicon Substrates (TSV-Interposers)
11. Heterogeneous Integration on Silicon Substrates (Bridges)
12. Heterogeneous Integration on RDL Substrates and/or TSV-less Interposers
13. Heterogeneous Integration Trends and
14. Summary

Who Should Attend:

If you are involved with any aspect of the electronics/optoelectronic industry, you should attend this course. Each participant will receive more than 200 pages of handout materials from the lecturer’s books and the papers published by others.

BIO:

John H. Lau has been the CEO of Unimicron Technology since August 2019 and a senior technical advisor of ASM since 2014 and a Senior Scientist/MTS at HP Lab/Agilent in California, US for more than 25 years. With more than 40 years of R&D and manufacturing experience in semiconductor packaging, he has published more than 500 peer-reviewed papers, 30 issued and pending US patents, and 20 textbooks on flip chip technologies, heterogeneous integration WLCSP, FOWLP, BGA, TSV for 3D integration, advanced MEMS packaging, lead-free solder and manufacturing, reliability of 2D and 3D IC interconnections.