13. From Wafer to Panel Level Packaging

Course Leaders: Tanja Braun and Michael Töpper – Fraunhofer IZM

Course Objective:

Panel Level Packaging (PLP) is one of the latest trends in microelectronics packaging. Technology developments towards heterogeneous integration including multiple die packaging, passive component integration in package and redistribution layer or package-on-package also approach larger substrates formats. These are targeted in this course. Manufacturing is currently done on wafer levels up to 12”/300 mm and 330 mm, respectively. For higher productivity and therewith lower costs, larger form factors are introduced. Instead of following the wafer level roadmaps to 450 mm, PLP might be the next big step. PLP has the opportunity to adapt processes, materials, and equipment from other technology areas. Printed Circuit Board (PCB), Liquid Crystal Display (LCD) or solar equipment is manufactured on panel sizes and offer new approaches also for PLP. However, an easy upscaling of technology when moving from wafer to panel level is not possible. Materials, equipment, and processes must be further developed or at least adapted. This course will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging including Fan-out Panel Level Packaging substrate embedding approaches. This will include materials discussion, technologies, applications, and market trends as well as cost modelling.

Course Outline:

- Introduction to Advanced Packaging
- Trends in Wafer Level Packaging
- Fan-In and Fan-Out Wafer Level: Material; Processes; and Applications
- Introduction and Definition of Panel Level Packaging
- Fan-out Panel Level Packaging: Technologies, Challenges and Opportunities
- Substrate Embedding Technologies

Who Should Attend:

Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level Packaging and the transition to Panel Level Packaging should attend. Engineers and managers are welcome as detailed technology descriptions, market trends, applications, and cost modelling are presented.

BIO:

Tanja Braun studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. In 2013 she received her doctorate degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Tanja Braun is head of the group Assembly & Encapsulation Technologies. Recent research is focused on fan-out wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin.

Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun also holds several patents in the field of advanced packaging. In 2014 she received the Fraunhofer IZM research award.

Tanja Braun is an active member of IEEE. She is member of the IEEE EPS Board of Governor (BOG) and Technical Chapter “Materials & Processing” as well as the IEEE EPS Women in Engineering (WIE) delegate.

Michael Töpper has a M.S. degree in Chemistry and a PhD in Material Science. Since 1994 he is with the Packaging Research Team at TU Berlin and Fraunhofer IZM. In 1997 he became head of a research group. In 2006 he was also a Research Associate Professor of Electrical and Computer Engineering at the University of Utah, Salt Lake City. The focus of his work was Wafer Level Packaging applications with a focus on materials. Since 2015 he is part of the business development team at Fraunhofer IZM. Michael Töpper is Senior Member of IEEE-CPMT and has received the European Semi-Award in 2007 for WLP. He has published several book chapters and is author and co-author of over 200 publications.