4. Eliminating Package Failure Mechanisms for Improved Reliability

Course Leader: Darvin Edwards – Edwards Enterprises

Course Objective:

Past and present reliability failure mechanisms that plague semiconductor packages will be explored. Major reliability challenges and failure mechanisms are detailed in critical emerging and high-volume package technologies such as TSVs, FOWLPs, WLCSPs, FC-BGAs, and no lead packages. Topics studied include reliability of TSV-chip interactions, micro bump mechanical reliability, electromigration performance, stress induced ILD damage under bumps and Cu pillars, solder joint reliability, system level issues such as drop and bend reliability, and the impact of aging on reliability performance. For each failure mode, the resultant failure mechanisms and failure analysis techniques required to verify the mechanisms will be summarized. This solutions-focused course concentrates on key process parameters, design techniques and material selections that can eliminate failures and improve reliability, ensuring participants can design-in reliability and design-out failures for faster time to market. Characterization and implementation of test structures and design guidelines that enable reliable first pass products will be described and encouraged. A methodology for early detection of chip/package interaction (CPI) reliability risks will be described.

Course Outline:

1. Introduction to Package Reliability
2. Failure modes vs. Failure Mechanisms
3. FC-BGA Package Failure Mechanisms
4. WLCSPs Package Failure Mechanisms
5. Embedded Die & Fan-Out WLP Failure Mechanisms
6. TSV Failure Mechanisms
7. Materials, Modeling, Design Rules and Reliability
8. Summary

Who Should Attend:

This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions.

Bio:

Darvin Edwards joined Texas Instruments in 1980 with a B.S. degree in Physics from Arizona State University. His responsibilities included developing integrated test structures to evaluate chip/package interactions, improving the thermal performance of TI's products, and leading the Dallas package modeling team for fifteen years. He wrote design rules to ensure package reliability and helped develop such package technologies as flip-chip BGA, CSP, WCSP and TSVs. Along the way, he helped introduce HAST and standardized thermal tests. Elected TI Fellow in 1999, he was most recently responsible for Analog Si/Pkg interactions within the Semiconductor Packaging Group before retiring in 2013. Darvin formed Edwards' Enterprise Consulting LLC in 2014, specializing in helping companies solve package reliability and thermal problems, as well as providing training worldwide. He has served as Member at Large for the IEEE CPTM society and is currently Chair of the Electronics Components and Technology Conference Applied Reliability committee of which he has been a member for 39 years. Darvin has authored and co-authored over 60 papers and articles in the field of IC packaging, has

written three book chapters, and holds 26 US patents. He has been active with JEDEC, SRC, INEMI, and IMAPS.