8. Wafer-Level Chip-Scale Packaging (WCSP) Fundamentals

Course Leader: Patrick Thompson– Texas Instruments, Inc.

Course Objective:

This course will provide an overview of the Wafer Level-Chip Scale Packaging (WLCSP) technology. The market drivers, end applications, benefits, and challenges facing industry-wide adoption will be discussed. Typical WLCSP configurations (bump-on-pad, bump-on-polymer, fan-in, and fan-out) will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other arenas such as RF sensors and MEMS will be reviewed. Future trends covered will include enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra-thin WLCSP, RDL (redistribution layer), stacked WLCSP, MCM in "reconstituted wafers," embedded components, and applications to large format (panel) processing. Since the technology marks the convergence of fab, assembly, and test, discussion will address questions on the industrial supply chain such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, outline, reliability, and equipment applicable? What are the challenges for memory and other complex devices such as ASICs and microprocessors?

Course Outline:

1. WL-CSP definition
2. Trends, Categories, Examples, Challenges, Supply Chain
3. Historical Overview, Package Highlights, Assembly Flow
4. Processing and Reliability: Flex, Temperature Cycling, Drop, Electromigration
5. Fan-Out Technologies
6. Embedded Technologies
7. Conclusions

Who Should Attend:

The course will be useful to the following groups of engineers: newcomers to the field who would like to obtain a general overview of WLCSP; R&D practitioners who would like to learn new methods for solving CSP problems; and those considering WLCSP as a potential alternative for their packaging solutions.

BIO:

Patrick Thompson (M'87, SM'92) earned his BS, MS, and Ph. D. degrees in Chemical Engineering at the University of Missouri-Rolla. He has more than 35 years of experience in advanced packaging research, development, and transfer to manufacturing, contributing to technologies ranging from flip chip fabrication and packaging, flip chip on board and chip scale packages, to multi-chip packaging, MEMS, optoelectronic packaging, and high-performance portable packaging. He has led teams at Bell Labs, AMI Semiconductors, and Motorola (now Freescale). Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he currently leads advanced wafer-level package development and university packaging R&D interactions. Pat is active in industry-consortia and industry-university partnerships, including mentoring SRC custom projects and PhD students. Pat has twelve patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He is a member of the Electronic Components and Packaging Conference technical program committee, where he has held multiple positions, including General Chair of the 2006 ECTC, and is now the Financial Chair. He has served at both the local and Society level of the EPS and is currently the VP of Finance.