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ECTC
The 2023 IEEE 73rd Electronic Components and Technology Conference

Millimeter-Wave Phased Array Frontend Integration and Packaging for Next-Generation Communication and Radar Systems

Thursday, June 1, 2023, 8:00 a.m. – 9:15 a.m.

Chairs: Kevin Gu (Metawave Corp) and Ivan Ndip (Fraunhofer IZM / Brandenburg University of Technology)

ECTC 2023 Plenary Session

Chair
Kevin Gu
Metawave Corp

Chair
Ivan Ndip
Fraunhofer IZM / Brandenburg University of Technology (BTU)

Panelist
Madhavan Swaminathan
Pennsylvania State University

Panelist
Hasan Sharifi
HRL Laboratories

Panelist
Augusto Gutierrez-Aitken
Northrop Grumman Space Systems

Panelist
Shahriar Shahramian
Nokia Bell Labs

Panelist
Alberto Valdes-Garcia
IBM T. J. Watson Research Center

Panelist
Jonathan Hacker
Teledyne Scientific

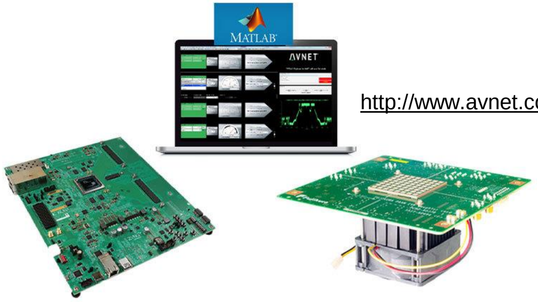
Millimeter-Wave Phased Array Frontend Integration and Packaging for Next-Generation Communication and Radar Systems

Phased arrays are critical components in next generation communication and radar sensing systems. Current state-of-the-art and rapidly-emerging research and development on millimeter-wave front-end implementations have created tremendous opportunities for innovation in packaging technologies. In this plenary panel session, we invite six leading domain experts to present their pioneering works in this area. The panel discussion will be focused on major challenges and latest advancement of packaging and integration technologies for designing and implementing phased array front-end modules including different substrates, interconnects, antennas, hetero-integration of silicon and III-V chips, co-design with RFICs, thermal management, and system demos/prototypes.

Packaging and module integration as a catalyst for **innovation in millimeter-wave** systems

Alberto Valdes-Garcia
Principal Research Scientist, Manager
IBM Research

Cycle of mmWave R&D (5G Example)



http://www.avnet.com/

Avnet-Fujikura-AMD 5G mmWave Phased Array Antenna Module Development Platform

Best mobile network infrastructure award at MWC 2019

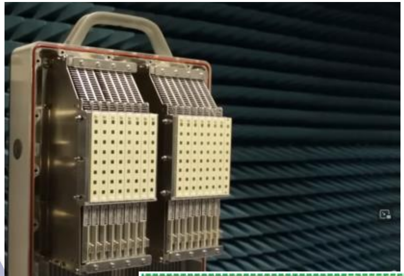
http://www.ericsson.com/spotlight/5G

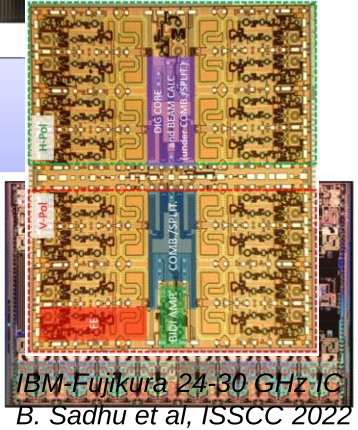
System PoC

Design of new ICs

Package design, module integration

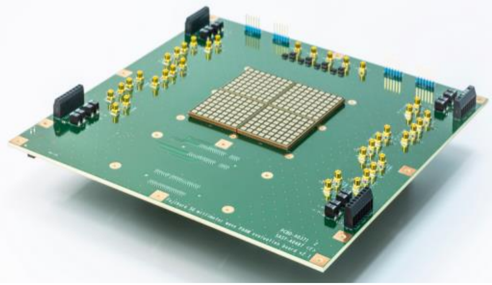
Market release



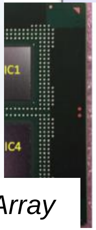


IBM-Fujikura 24-30 GHz IC
B. Sadhu et al, ISSCC 2022

IBM-Ericsson 28-GHz IC
B. Sadhu et al, ISSCC 2017
[Best paper award]



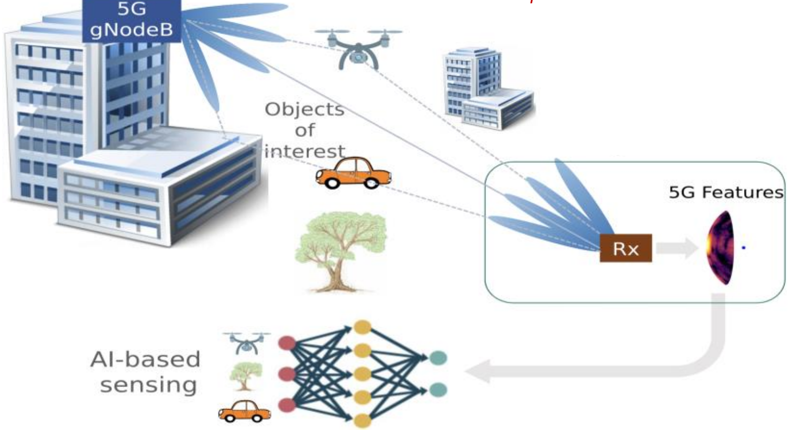
IBM-Fujikura 24-30 GHz 256-Element Array
D. Liu et al, ECTC 2023



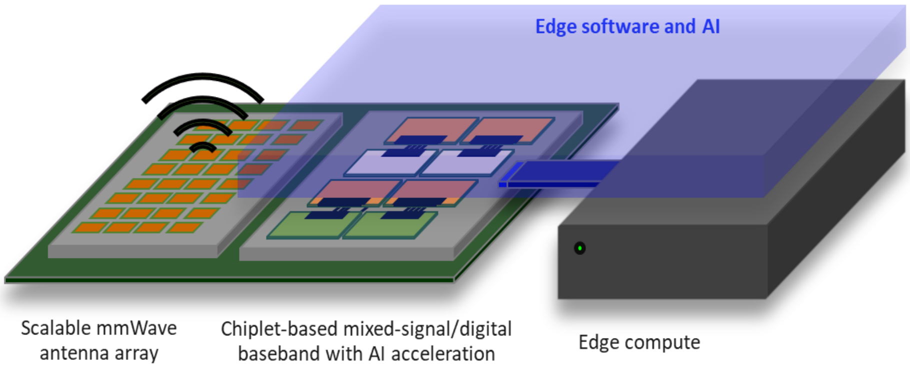
IBM-Ericsson 28-GHz 64-Element Array
X. Gu et al, T-MTT 2019

Next Generation *mmWave Antennas-to-AI* Systems

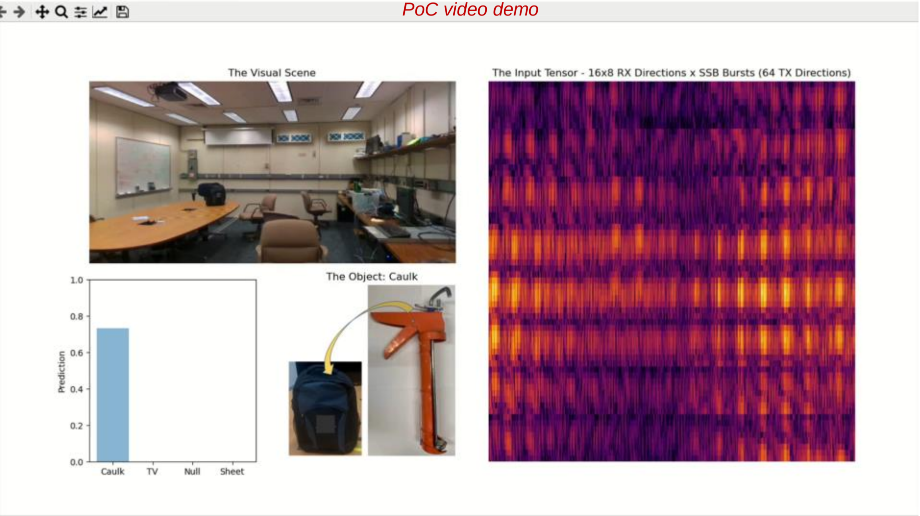
Network as a sensor concept



System realization vision



PoC video demo



Requirements

Heterogeneous integration (HI) for RF and mixed-signal/digital components

Chiplet ecosystem for baseband processing from ADC/DAC to AI accelerators

Power-efficient architectures, components, and algorithms

AiP approaches for scalable arrays at 100-GHz and above

EDA tools for efficient HI design

alizing near-THz nication Systems

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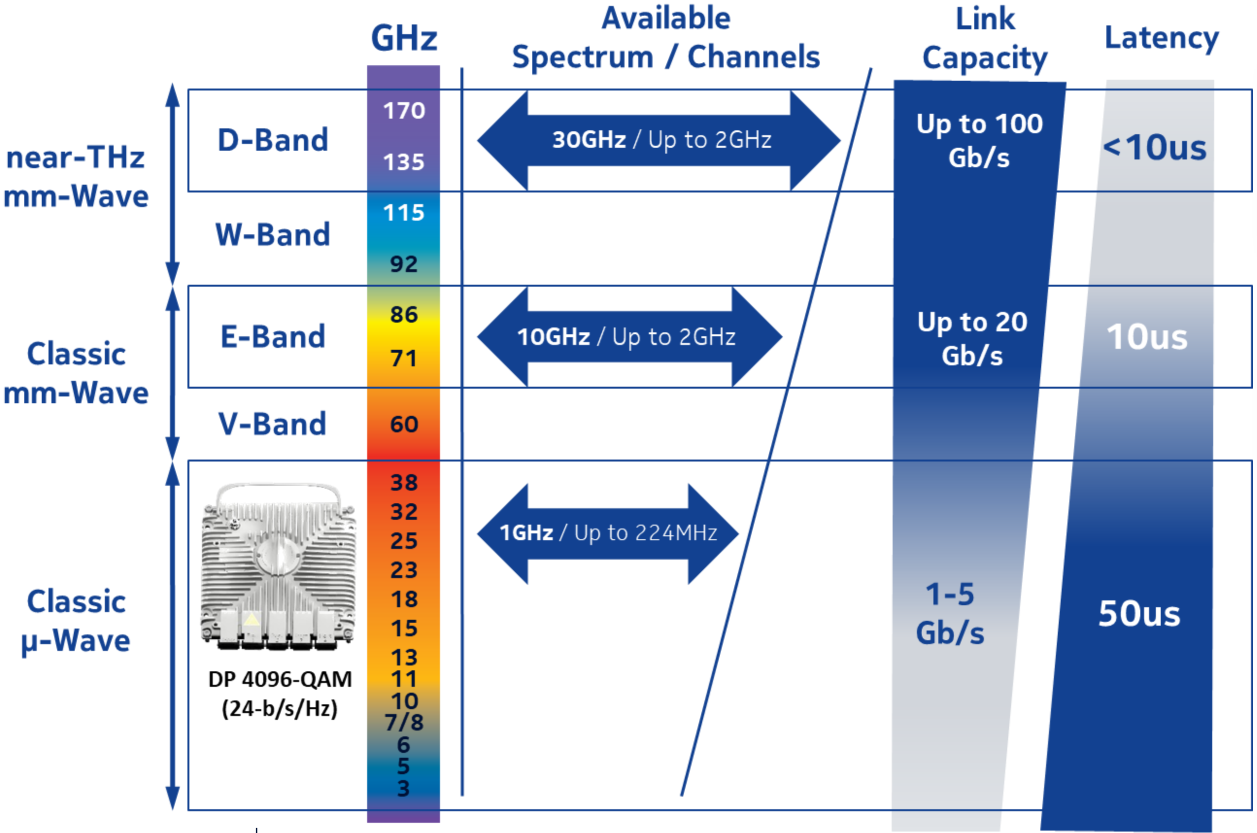
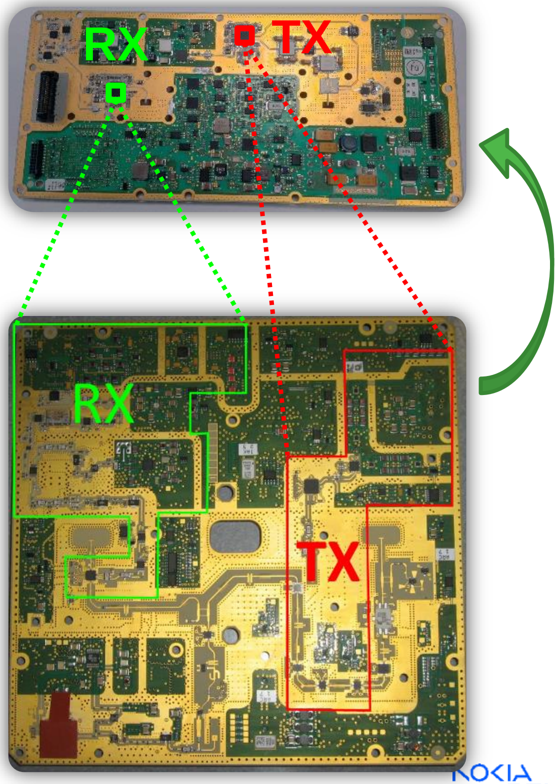
The Evolution of Backhaul Links

From 6GHz – 160GHz & 1Gb/s towards 100Gb/s

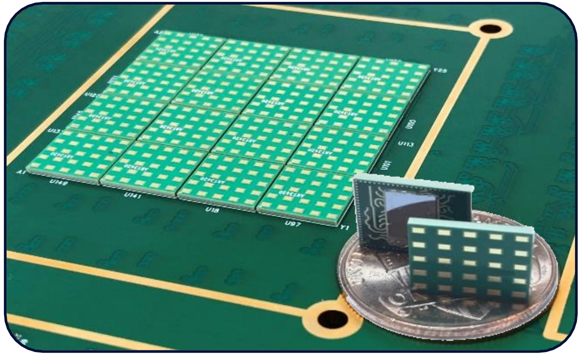


		GHz	Available Spectrum / Channels	Link Capacity	Latency
near-THz mm-Wave	D-Band	170 135	**30GHz** / Up to 2GHz	Up to 100 Gb/s	<10us
	W-Band	115 92			
Classic mm-Wave	E-Band	86 71	**10GHz** / Up to 2GHz	Up to 20 Gb/s	10us
	V-Band	60			
Classic μ-Wave	DP 4096-QAM (24-b/s/Hz)	38 32 25 23 18 15 13 11 10 7/8 6 5 3	**1GHz** / Up to 224MHz	1-5 Gb/s	50us



Radio-on-Glass Platform

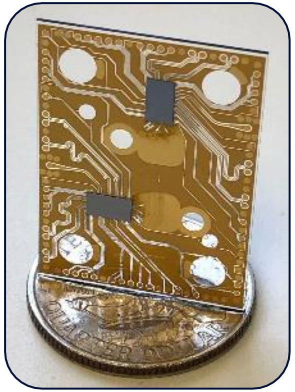
Co-integration of near-THz ICs & Glass Packaging



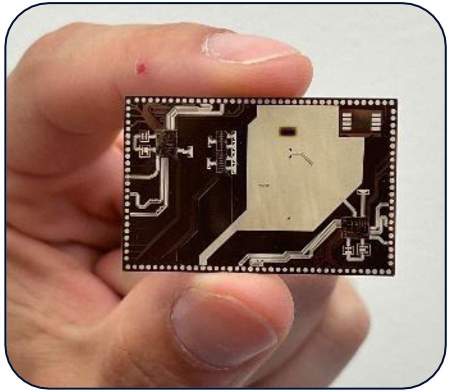
🡐 384-Element W-Band Phased Array on PCB

Innovative packaging materials, processes & co-integration is needed for industrializing low-cost near-THz communication systems.

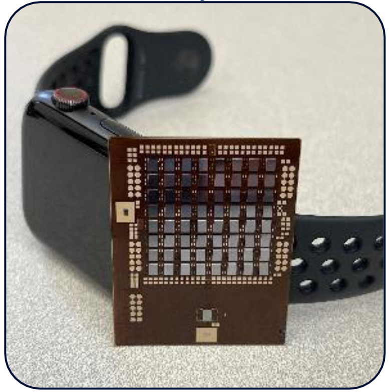
D-Band Radio-on-Glass



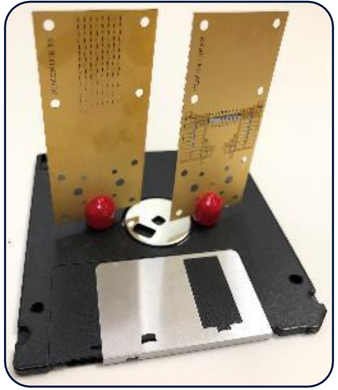
E-Band Backhaul-on-Glass



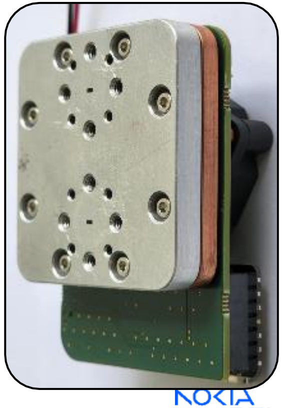
D-Band 2D
Phased Array-on-Glass



D-Band 1D
Phased Array-on-Glass



D-Band PA-on-Glass

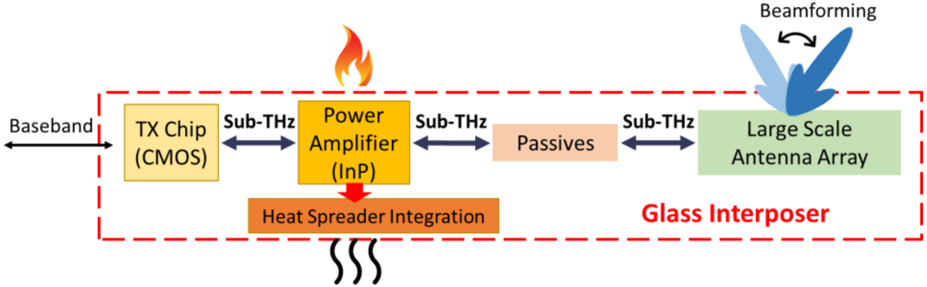


Sub-THz Embedded Glass Packaging (D-Band)

Madhavan Swaminathan

Penn State University

Sub-THz Embedded Glass Packaging (D-Band)



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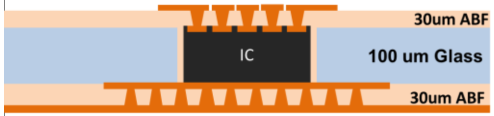
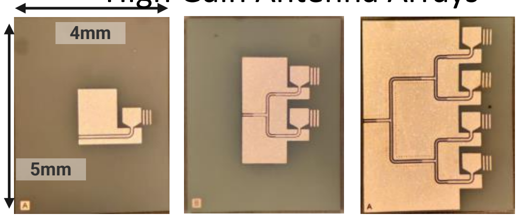
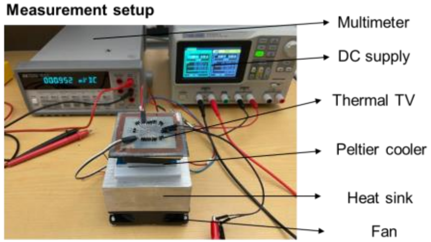


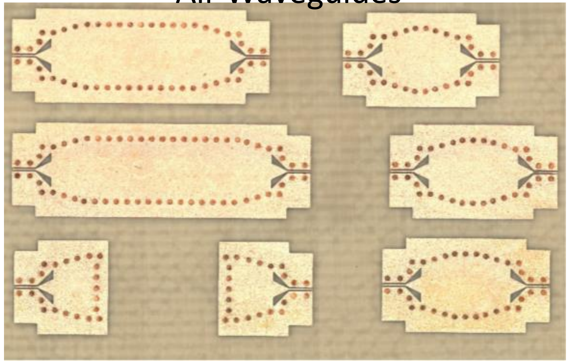
High Gain Antenna Arrays



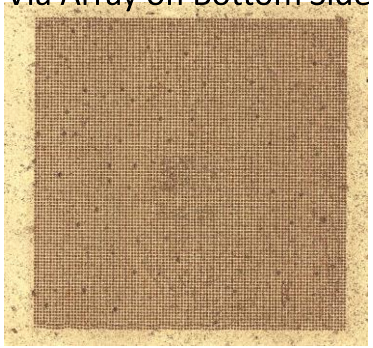


Thermal

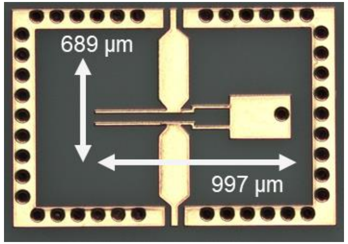
Air Waveguides

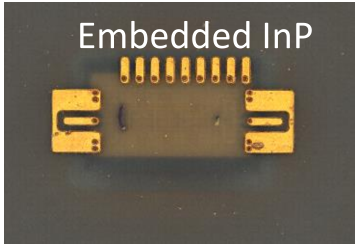


Via Array on Bottom Side



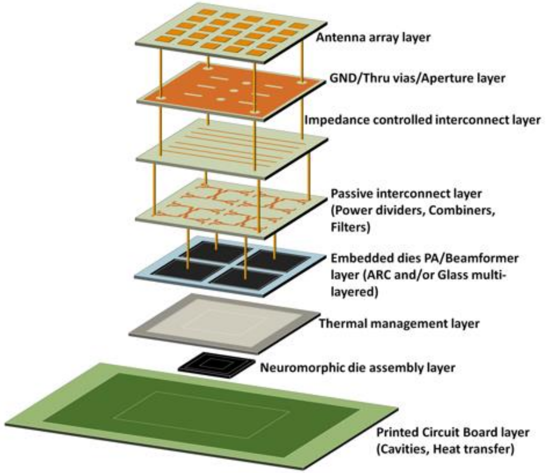
Filters

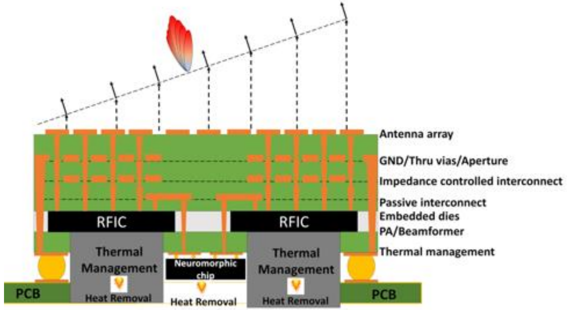




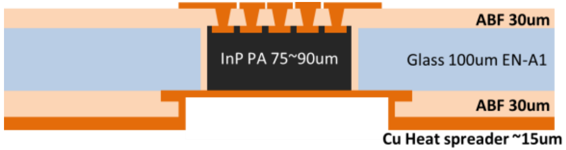
Antenna Array with Embedded CMOS

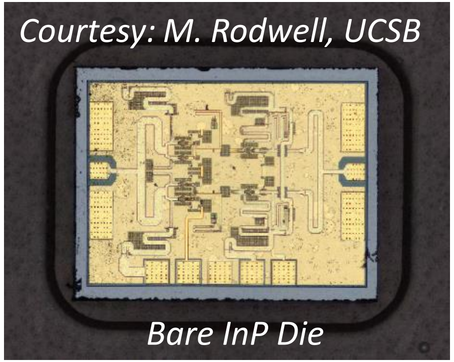
Sub-THz Embedded Glass Packaging Opportunities



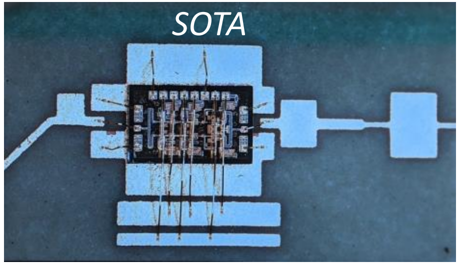


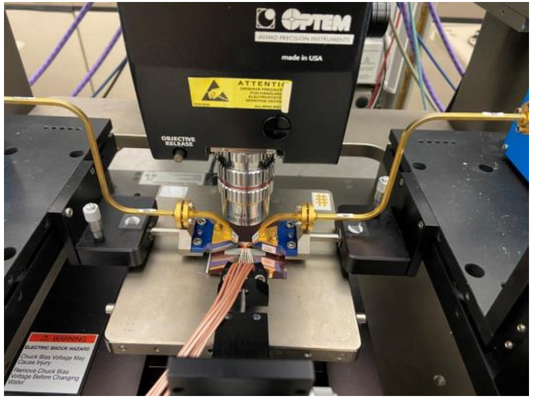
Courtesy: W. Lee et al, PSU

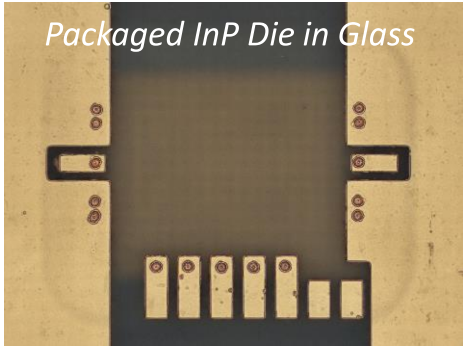



Courtesy: M. Rodwell, UCSB

Bare InP Die


SOTA




Packaged InP Die in Glass

High Performance Compact mmW Phased Array Systems: Challenges and Opportunities for Innovations

Hasan Sharifi
HRL Laboratories

High Performance Compact mmW Phased Array Systems: Challenges and Opportunities for Innovations-1

mmW Phased Array:

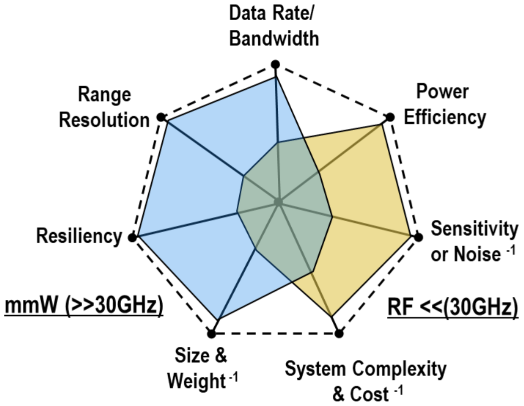
- Offers larger bandwidth (>10x) enabling higher data rate or throughput; Improved range resolution and narrower beam width for radar systems;
- <u>Smaller array size</u>

Challenges:

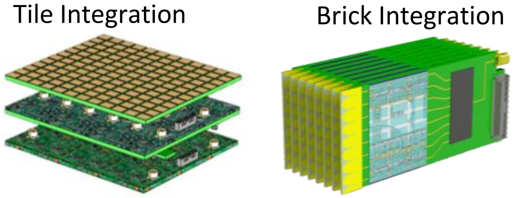
- <u>**System & component levels**</u>**:** Higher atmospheric propagation loss; Lower overall power efficiency and sensitivity at mmW
- <u>**Packaging level**</u>**:** Tighter requirements for assembly and integration at mmW (e.g. λ/2 x λ/2 constraint); Modular & scalable design for large array sizes; Thermal management & reliability; Re-workability

Opportunities for Innovations:

- <u>**System & component levels**</u>**:** New phased array architectures; Co-design & optimization; Utilize semiconductor devices with improved sensitivity and higher power density/efficiency (e.g III-V vs. silicon);
- <u>**Packaging level**</u>**:** 3D Heterogeneous integration (3DHI); Chiplet disaggregation; Fine-pitch, high-density interconnect; Improved thermal management and reliability



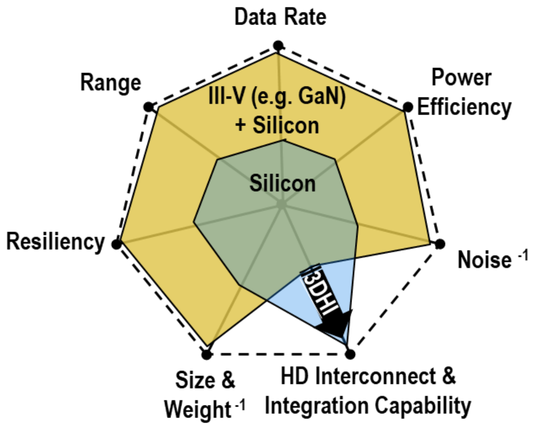
<u>Comparison of mmW (>30GHz) vs. RF</u>

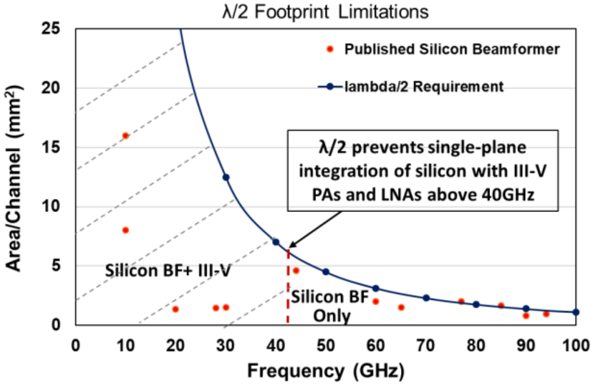


<u>Modular Tile vs. Brick Array Architecture</u>

High Performance Compact mmW Phased Array Systems: Challenges and Opportunities for Innovations-2

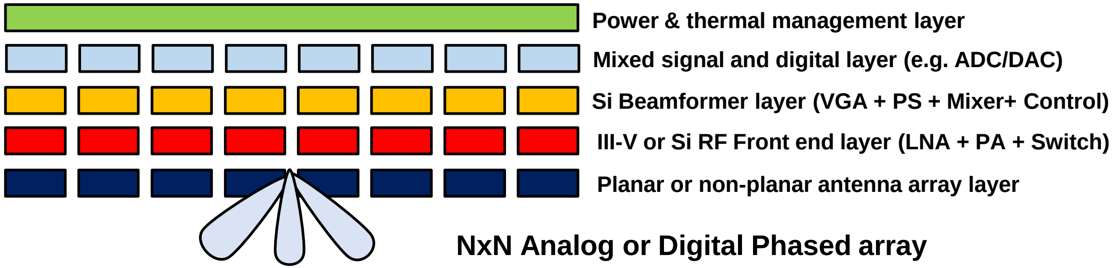
- **III-V device technologies such as GaN overcome shortcomings at mmW due to higher sensitivity, power density and efficiency offering**
  - >10x improvement in size, weight and power (SWaP), sensitivity/SNR, dynamic range, linearity, and resiliency compared to silicon based phased arrays
- **Poses new packaging challenges due to tight spacing constraint (e.g. λ/2) preventing single-plane integration of silicon beamformer and III-V components at mmW**
  - Requires 3D staking and heterogeneous integration (3DHI) of diverse layers with fine-pitch, high-density, low-loss vertical interconnect





High Performance Compact mmW Phased Array Systems: Challenges and Opportunities for Innovations-2

- Requires proper thermal management and heat rejection from each junction/layer and array backside due to higher power density + 3D stack reliability and failure analysis



Power & thermal management layer

Mixed signal and digital layer (e.g. ADC/DAC)

Si Beamformer layer (VGA + PS + Mixer+ Control)

III-V or Si RF Front end layer (LNA + PA + Switch)

Planar or non-planar antenna array layer

NxN Analog or Digital Phased array

- 3DHI unlocks the real estate constraint for mmW Phased Array systems offering unprecedented performance and flexibility over existing systems in radar and communication!

Frontend Integration and packaging for millimeter-wave phased arrays in next-generation communication and radar systems

Augusto Gutierrez-Aitken

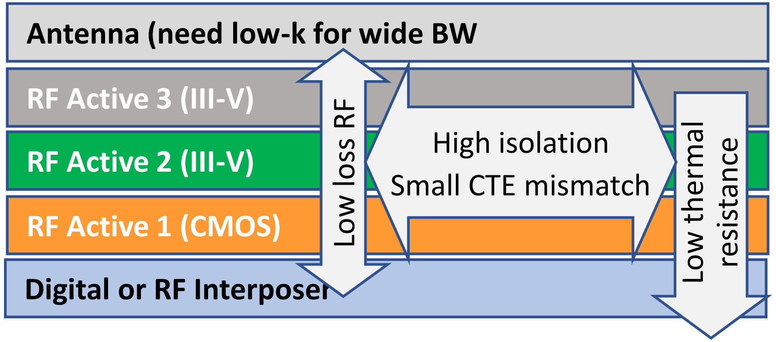
Northrop Grumman Space Systems

Redondo Beach, Ca

June 1st, 2023

Needs and Challenges for Advanced Packaging and 3DHI for High Frequency Arrays, Comm and Radar Systems

Notional 3DHI Front-End Element


Antenna (need low-k for wide BW
RF Active 3 (III-V)
RF Active 2 (III-V)
RF Active 1 (CMOS)
Digital or RF Interposer
Low loss RF
High isolation
Small CTE mismatch
Low thermal resistance

Very challenging $\lambda/2$ spacing at high freq. Need 3DHI

- High performance devices
- Low loss for vertical connectivity
- Low thermal resistance
- Small CTE mismatch
- High x-y isolation
- Rad-hard (Space)

3DHI Needs

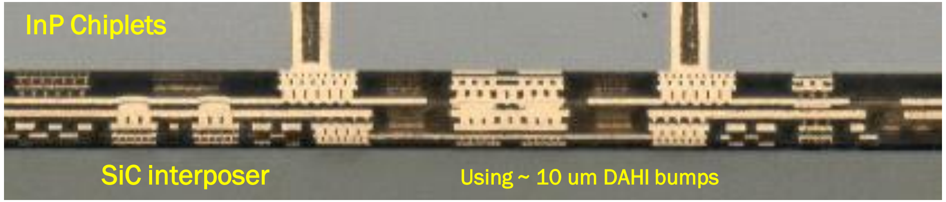
- **Active Technologies**
- High frequency and/or bandwidth
- High gain per dissipated power (dB/mW)
- High PAE (TX PAs)
- Low noise figure (RX LNAs)
- Low 1/f noise (VCOs, etc.)
- High linearity and dynamic range
- **Passives and other components**
- Low loss, high bandwidth interface
- High-Q compact inductors
- Low loss interposers
- Wideband high efficiency antennas
- Photonic and magnetic components

Challenges

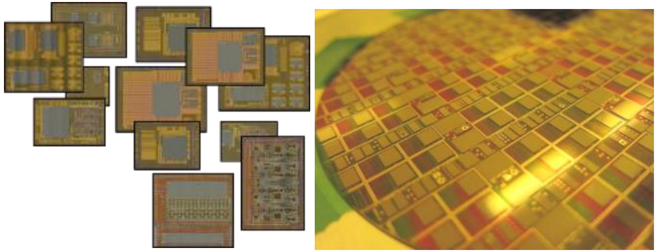
- Reliability of active technologies and heterogeneous interfaces
- Heterogeneous integration impact on active technologies (stress, temperature, etc.)
- mmW 3DHI arrays burn-in
- Radiation (Space Applications)
  - Non-array electronics are inside electronic bays where TID ≤Mrad
  - 3D mmW arrays need to be outside (or near outside environment) where TID ≥Grad
- Thermal Cycle - Significant challenge
  - Low Earth Orbit (LEO) temperature cycle from –170°C to +130°C
  - 5 years mission: ~ 43,000 cycles

Background and Research Highlights in 3DHI

3DHI integration of InP to SiC interposer (>100 GHz Application)

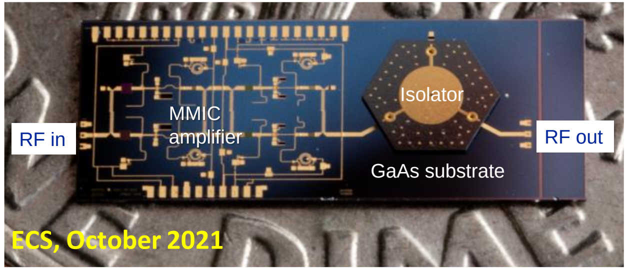


3DHI integration of InP, GaN on CMOS



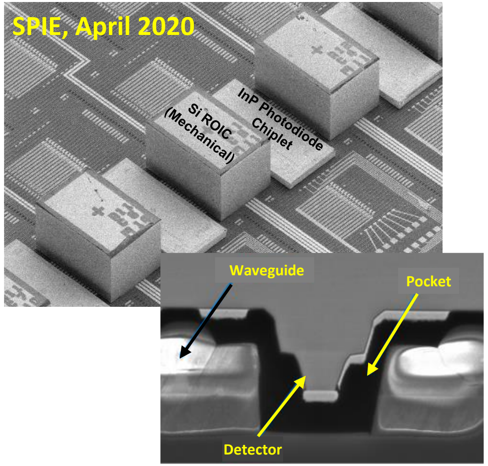
3DHI of InP HBT chiplets to CMOS wafer

3DHI integration of hexaferrite isolator to GaAs MMIC



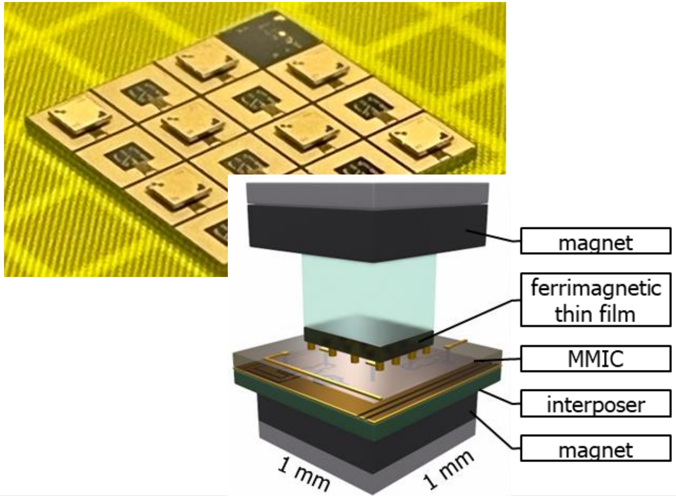
ECS, October 2021

3DHI integration of InGaAs photodiode, CMOS ROIC SiO2 photonic waveguide substrate



SPIE, April 2020

3DHI Filters



Teledyne SLIC
Phased Array Packaging Technology

Jonathan Hacker

TELEDYNE
SCIENTIFIC COMPANY
Everywhereyoulook™

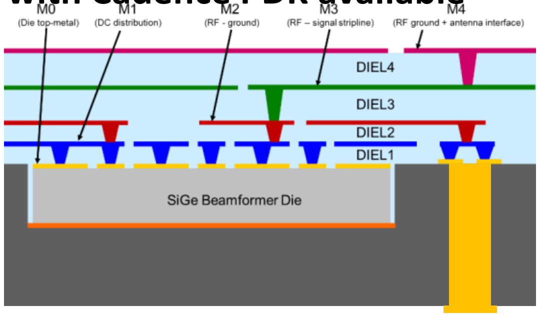
Teledyne’s SLIC Packaging Technology

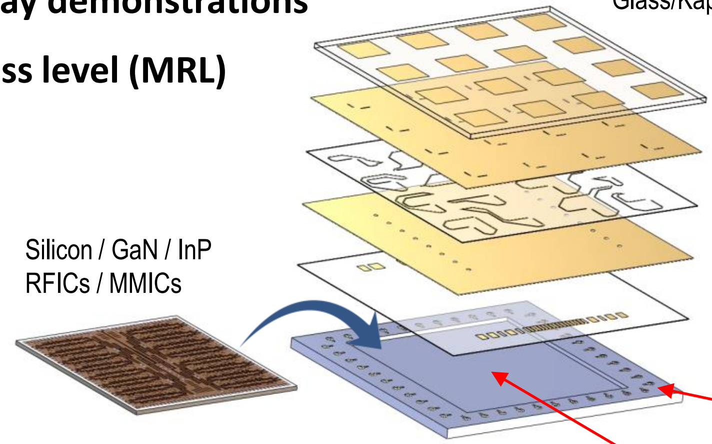
SLIC is a batch-fabricated (wafer-scale) packaging technology optimized for millimeter-wave phased arrays:

- **Integrates heterogenous chips, planar radiating elements, thermal management, and rf interconnect in a silicon micro-machined interposer**
- **Based on an IC grade BCB fine-line interconnect process (10 µm line/space)**
- **Approach validated through numerous phased array demonstrations**
- **Ten years of improving the manufacturing readiness level (MRL)**
- **SLIC technology now offered as a foundry service by Teledyne with Cadence PDK available**

Cross-sectional View

Multi-Layer BCB/Gold RDL optimized for mm-Wave applications





Planar antennas on Glass/Kapton substrate

Interconnect Metallization

Silicon / GaN / InP RFICs / MMICs

Through Substrate Vias

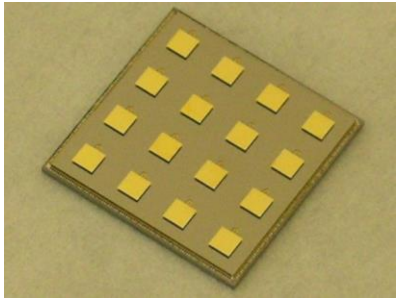
Silicon Interposer

Micromachined recesses lock RFIC/MMIC die into position

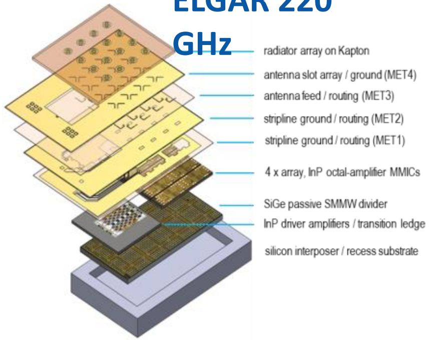
Key Features of SLIC

- **Low-loss impedance-controlled transmission lines**
- **Fine line geometries to support dense compact interconnects (<10 µm line and space, 10 µm via diameter, 10 µm via pitch)**
- **Heterogeneous integration of RFICs, MMICs, Antennas, Transmission-lines, in 2.5D with good thermal properties.**
- **Through substrate vias (TSVs) for backside signal access**
- **Batch fabricable to minimize touch labor and support scalability (for arrays)**

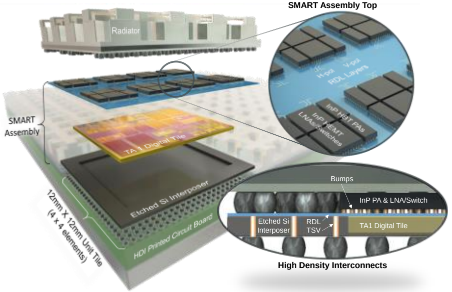
First SLIC Tile (2012)
44 GHz ESA



ELGAR 220 GHz



MIDAS 50 GHz



MFRF W-Band