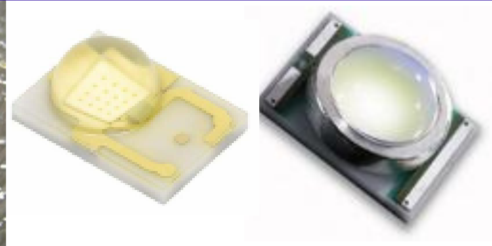
# LED Packaging Challenges

## ECTC 2012

San Diego, CA

Jeff Perkins

perkins@yole.fr



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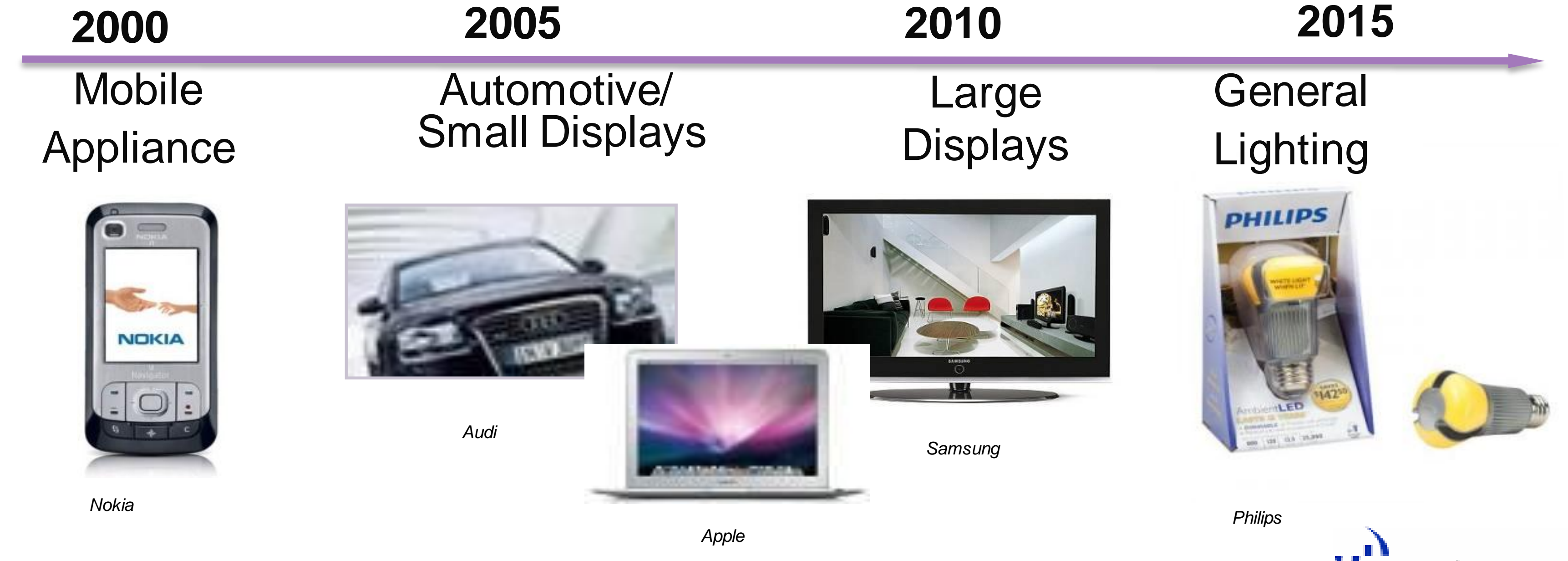
# Recent LED History

- The HB LED market was enabled in the mid 90's with blue LEDs.
- Cell phone provided the first "killer app" (screen and keypad)
- As technology improved, LED addressed larger displays:
  phones → netbooks → notebooks → desktop monitor → large TV
- And now the push is on for General Lighting





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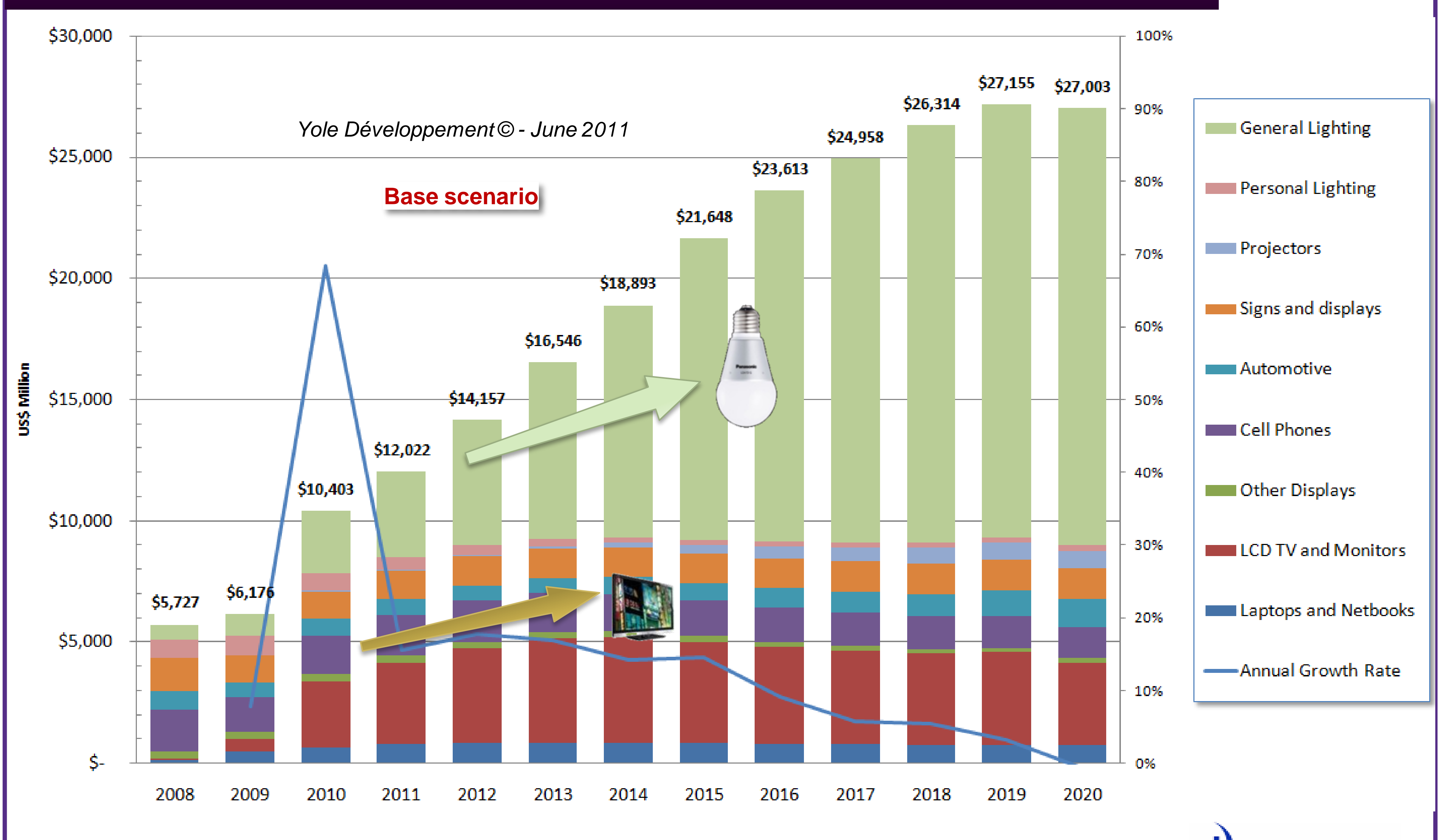
# Revenue Forecast
## *packaged LED die, by application*



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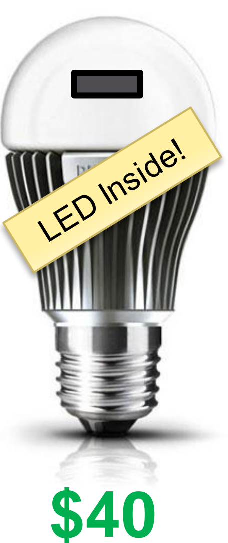
# General Lighting

## Focus is on Cost

**<$1**

**$3-5**




**$40**

*All sources: ~ 800 lumens, warm White, tier 1 brand only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# Total Cost of Light =

## Upfront Cost

## +

## Energy Cost

## +

## Maintenance Cost

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# Total Cost

## $40 LED, $3 CFL, $1 Thomas Edison

$140
$120
$100
$80
$60
$40
$20
$-

Incandescent
CFL
LED

*Sources: Yole Développement*

**Standard A19 Warm white Bulb**
**800 lumen**
**No maintenance cost**
**(residential use)**

0 10,000 20,000 30,000 40,000 50,000
Hours

**At $40 lamp cost, LED total cost remains higher than CFL**



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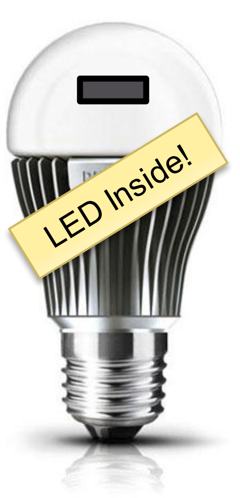
# General Lighting
## people focus on purchase price!

## Upfront Cost




**$10 ?**

*All sources: ~ 800 lumens, warm White, tier 1 brand only



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# Total Cost

## LED at $10

$140
$120
$100
$80
$60
$40
$20
$-

0 10,000 20,000 30,000 40,000 50,000

Hours

Incandescent
CFL
LED

*Source: Yole Développement*

**At $10 LED better than other sources**

**→ trigger for market adoption**



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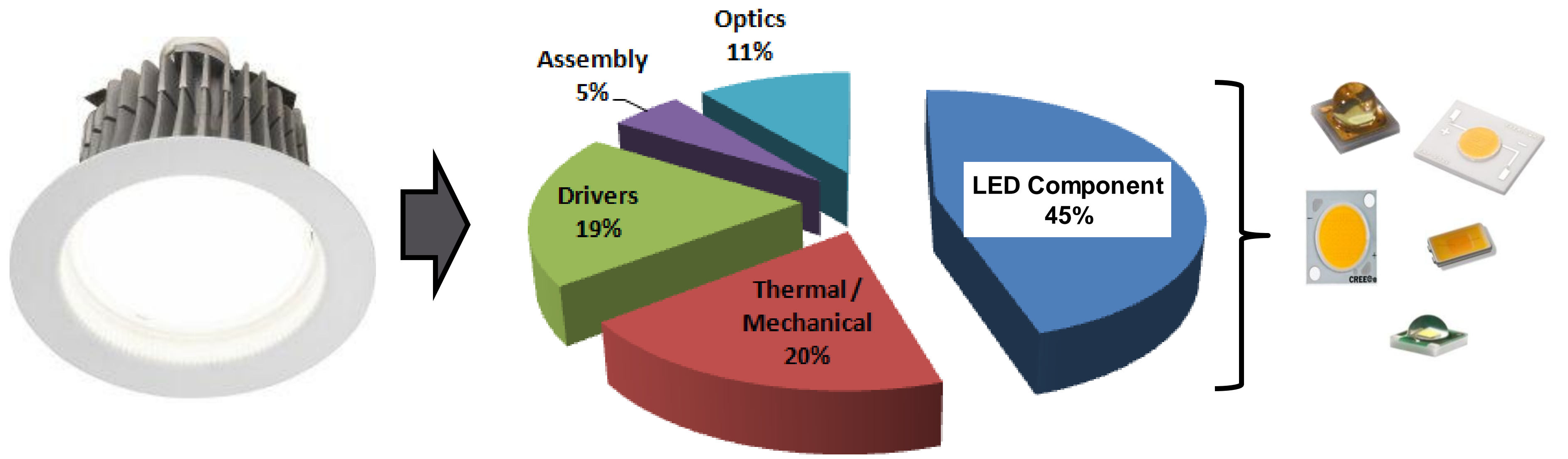
# Luminaire Cost Structure

## LED is only one contributor but represents the single largest opportunity for cost reduction:




*Downlight picture: CREE LR6, Cost breakdown from DOE SSL roundtable 2011, Packaged LED pictures: Cree, Everlight, Osram, Philips Lumileds.*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# Driving Down Cost

## typical cost structure, PACKAGED DIE

## Packaging represents up to 40% of the packaged LED cost

LED Downlight Luminaire Cost Breakdown

- Optics 11%
- Assembly 5%
- Drivers 19%
- Thermal / Mechanical 20%
- LED Component 45%

LED Component breakdown:

- Substrate 11%
- Epitaxy 21%
- Wafer Processing 23%
- Phosphor 11%
- Packaging 34%

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# Key Components of a Packaged LED

Encapsulation / Optic / Phosphor

LED die

*Interface Material #1 (Die Attach)*

Submount (optional)

*Interface Material #2 (Die attach)*

Package Substrate

ESD Protection

Interconnect

Interconnect

Led Package
(picture: Philips Lumileds)

Note: some elements described here can be optional or redundant depending on the exact design choices made by the manufacturer.


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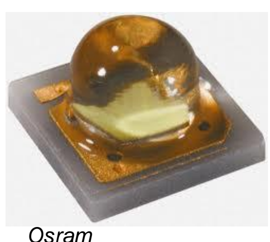
# High-Power LED Packages

## wide variety of solutions

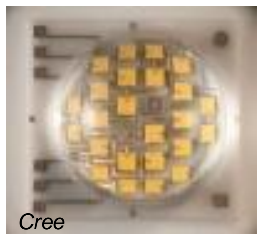
| Single Large Die | Multiple Large Dice | Small/medium dice Array | Single or Multi "Jumbo Die" |
| --- | --- | --- | --- |
| (1 die, typical dimension: 0.5 to 1.5 mm) | (3 to 25 dice, typical dimension: 0.5 to 1.5 mm each) | (20 to 100 dice, typical dimension: 250 to 500 um each) | 1 to 6 dice, typical dimension 2 to 5 mm each) |

Lumileds

Lumileds


Osram

Cree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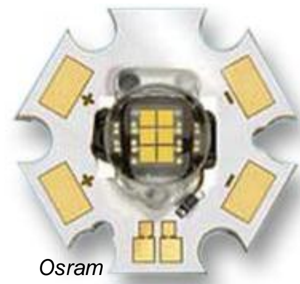
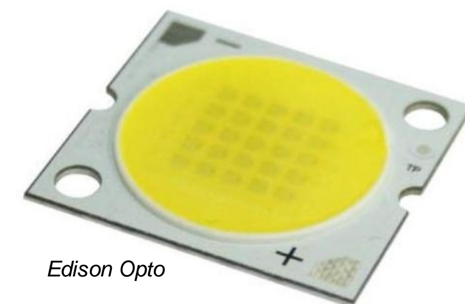
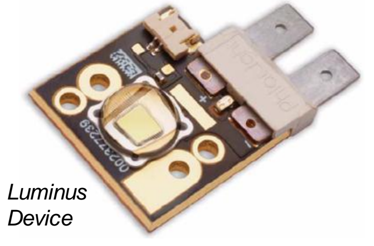
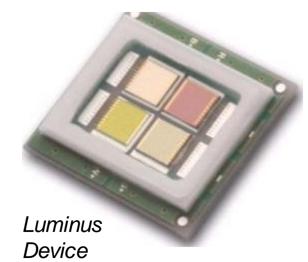

Osram

Osram


Edison Opto


Luminus Device

Luminus Device


Luminus Device

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# Key Technologies & Research Areas
## addressing LED cost of ownership

**Cost Impact**

- **Alternative substrates #2:** Si
- **Epitaxy: Cluster tools - New Epi Technologies**
- **Large Diameters Substrates:** 4", 6", 8"
- **Wafer Level Packaging:** Silicon TSV, Wafer Level Optics
- **Epitaxy – MOCVD:** Higher yields and Throughputs - Improved Material quality
- **Lithography:** Dedicated tools, Higher Throughput
- **Phosphors:** Conversion efficiency, Color Rendering – "IP free" phosphors
- **Phosphors:** Quantum dots Phosphors
- **Testing and Binning:** Wafer Level, Higher throughputs
- **Substrate Separation:** Laser Lift Off, other separation techniques
- **Mirrors:** Resonant Cavities
- **Alternative substrates #1:** GaN, ZnO, Si, ...bstrates
- **Die Singulation** Increased throughputs and yields
- **Encapsulation Materials and Optics:** Ageing and optical properties
- **Mirrors:** Improve reflectivity/electrical properties
- **Thermal Management:** New materials for packaging
- **...trodes:** Transparent contacts/Electrode materials and patterns
- **Surface Texturation:** Patterned substrates / Roughening
- Phot... ...Quasi Photonic Crystals
- **Current Droop / Green Gap / LED Structures**
- **Contacts & Electrodes:** p to n layer VIAS

**Performance Impact**

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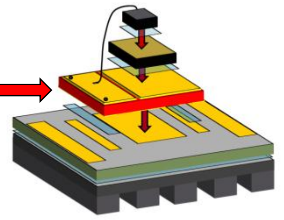
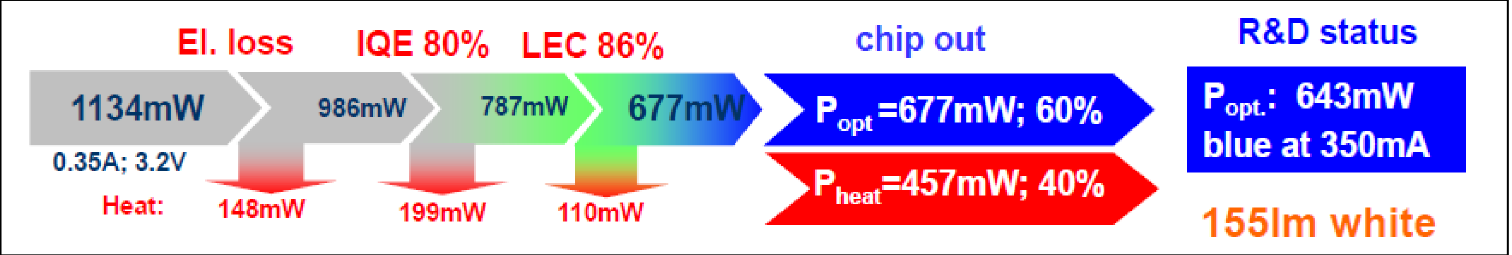
# Thermal Management

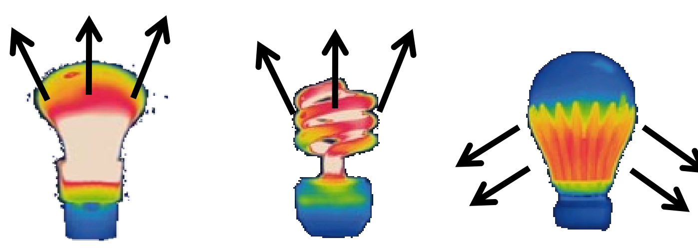





*R&D status of Electrical and optical power flow in packaged LED (source: Osram)*

- **For a 1W LED, 40% of the input power turns into heat.**
- **Most importantly for the packaging task… LED heat is not radiated and has to be removed by conduction:**

| Source | Radiation heat loss | Convection heat loss | Conduction heat loss |
|---|---|---|---|
| Incandescent | 90% | 5% | 5% |
| Fluorescent | 40% | 40% | 20% |
| LED | 10% | 10% | >80% |



*IR imaging of the temperature distribution of LED based, Incandescent and CFL Bulb (Source: Tyrone Turner/National Geographic Society / Corbis)*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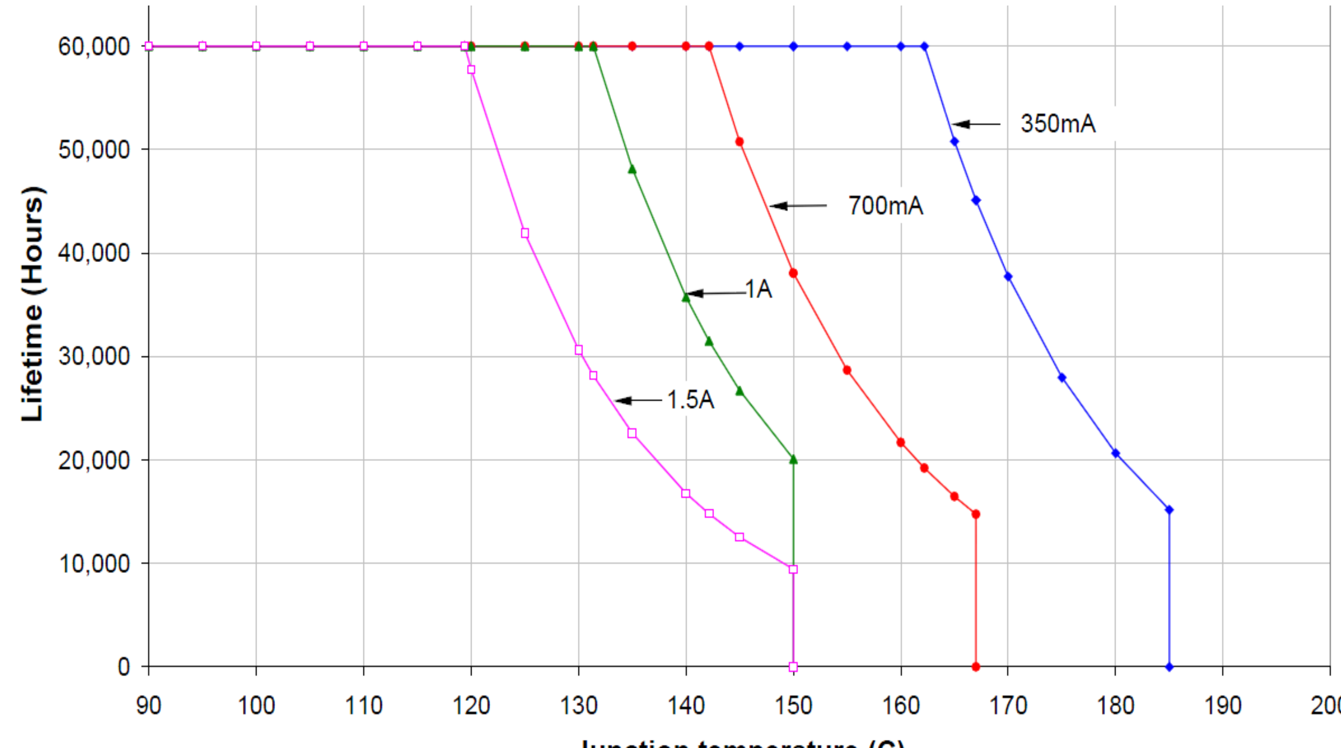
# Thermal Management

- **Heat has a significant impact on LED performance and reliability**
  - **Lifetime: Lumen maintenance, catastrophic failure.**
  - **Energy efficiency: Lumen/Watt, bias voltage.**




*Impact of Junction Temperature on the lifetime of Luxeon K2 at different driving current (source: Philips Lumileds)*

**Thermal management is a critical aspect of LED performance and reliability. An efficient conduction path needs to be built in the package to get heat out**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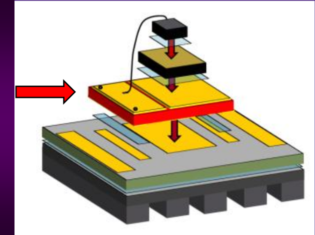
# Thermal Management
## material options



| | Thermal Conductivity (W/m.K) | CTE (ppm/°C) | Cost | comments |
|---|---|---|---|---|
| Lead Frame / Metal Slug | High (Al:150– 230 / Cu: 400) | Low to Medium (Al: 2.7 / Cu:8.9) | Medium | |
| Printed Circuit Board (FR-4) | Low (0.36) | High (13 – 17) | Low | •Available for large panel size |
| Metal Core Printed Circuit Board | Low through dielectric (1 - 2.2) | High (17 - 23) | Medium to high | • Available for large panel size<br>• Operating temperature limited to 140°C |
| CERAMIC | Medium to high (20 – 230) | Medium to high (4.9 – 8) | Medium to high | •Small panel sizes<br>•Very high operating temperatures<br>•Easily handles high power |
| Silicon | High (150) | Low (3.2) | Medium to High | • High potential with TSV technology and wafer Level Packaging |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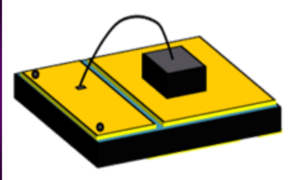
# Interconnects



| Interconnection type | Wire Bonding | Flip Chip |
|---|---|---|
| | LED<br>Package substrate | LED<br>Package substrate |
| LED die structure | Conductive Substrate<br>Vertical Structure on conductive substrate (Metal, SiC, Si, ZnO..)<br>Sapphire substrate<br>Standard MESA Structure | Sapphire substrate<br>Metal<br>Metal<br>Flip Chip MESA Structure |
| Substrate Type | Metal leadframe, ceramic, glass-ceramic, silicon, COB (chip on board on metal-core PCB) | Metal leadframe, ceramic, glass-ceramic, silicon |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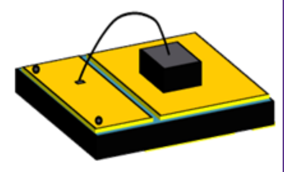
# Interconnects



**Interconnection of large size LEDs**
*by interconnection types (Mu)*



| | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2011-2016 CAGR |
|---|---|---|---|---|---|---|---|---|
| Flip Chip | 494 | 749 | 1188 | 2281 | 4030 | 6395 | 8709 | 63% |
| Vertical, 1 wire bond | 119 | 407 | 918 | 1884 | 3385 | 5448 | 7508 | 79% |
| Standard Mesa, 2 wire bonds | 1364 | 2101 | 3294 | 5751 | 8705 | 11843 | 13814 | 46% |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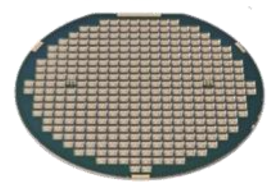
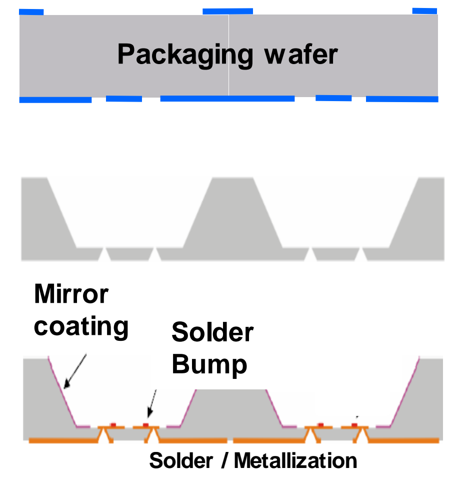
# Wafer Level Packaging

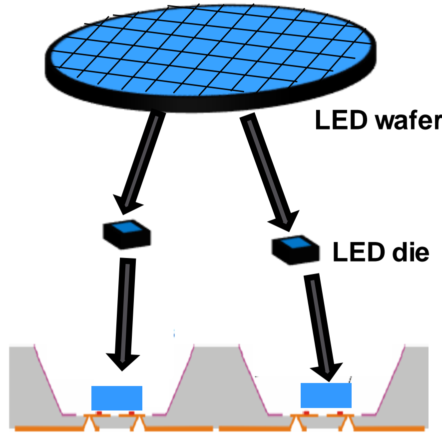


- Packaging of an LED at wafer level, rather than assembling the package of each individual unit after wafer dicing
- LED Wafer Level Packaging leverages experience and technology platforms developed for MEMS, CMOS image sensors and Wafer Level Optics.

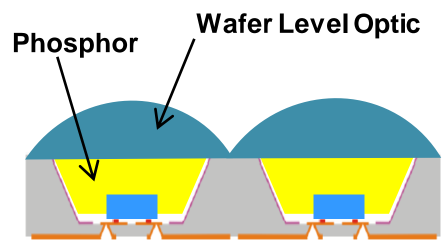
*in this example, the LED chips are singulated <u>before</u> being positioned onto the package wafer (="Chip to Wafer" packaging)*



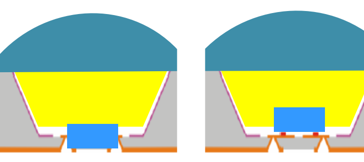

1) Wafer level preparation of the bare package (cavity etching, $SiO_2$ insulation layer, via / bump interconnects, mirrors…)




2) LED die separation + pick and place positioning on the package wafer.




3) Wafer level interconnect, phosphor deposition, encapsulation, optic.



4) LED package separation.

*Overview of Chip to Wafer LED WLP process (Yole, Hymite)*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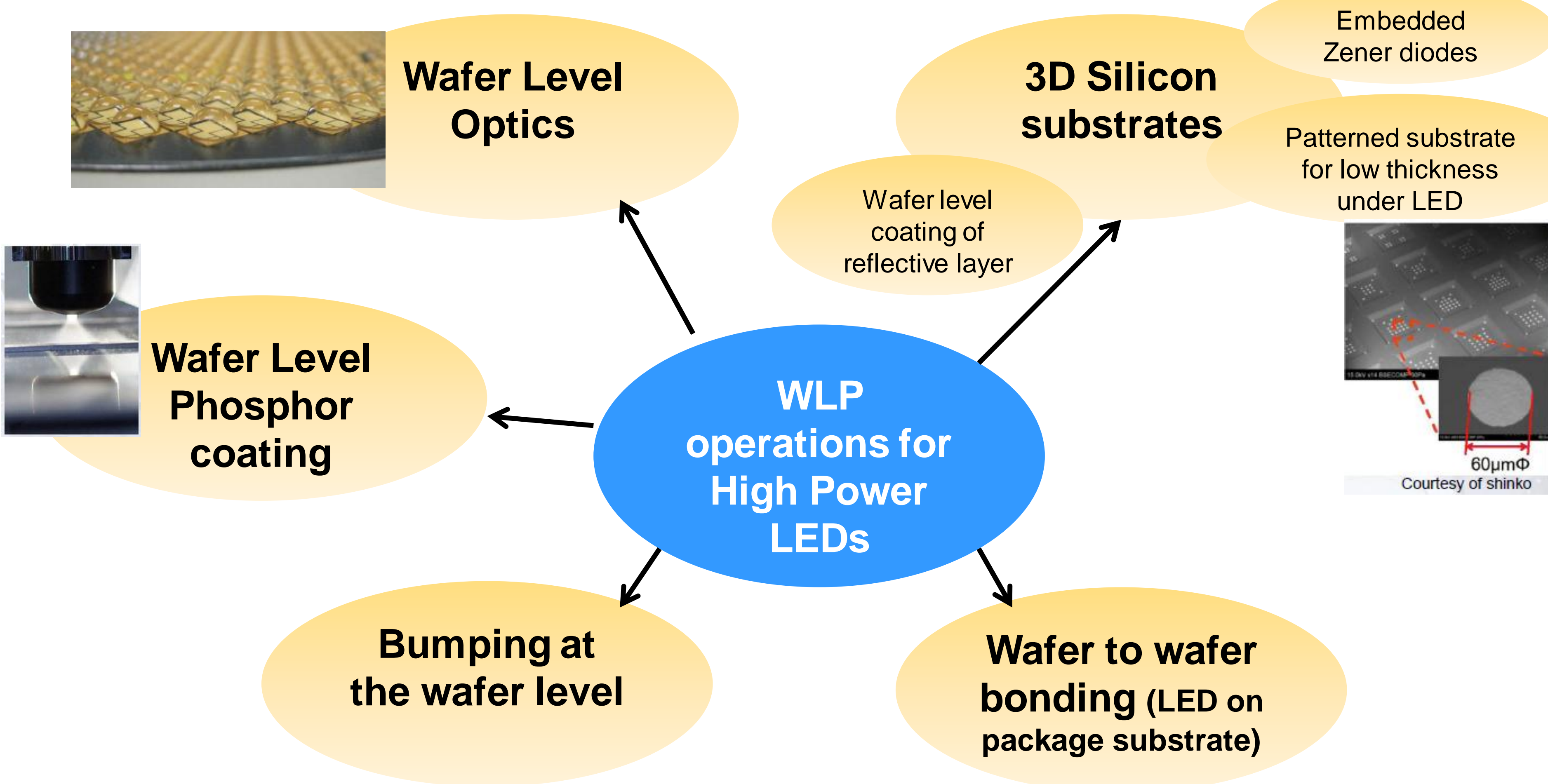
# WLP for High Power LEDs





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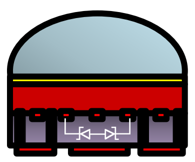
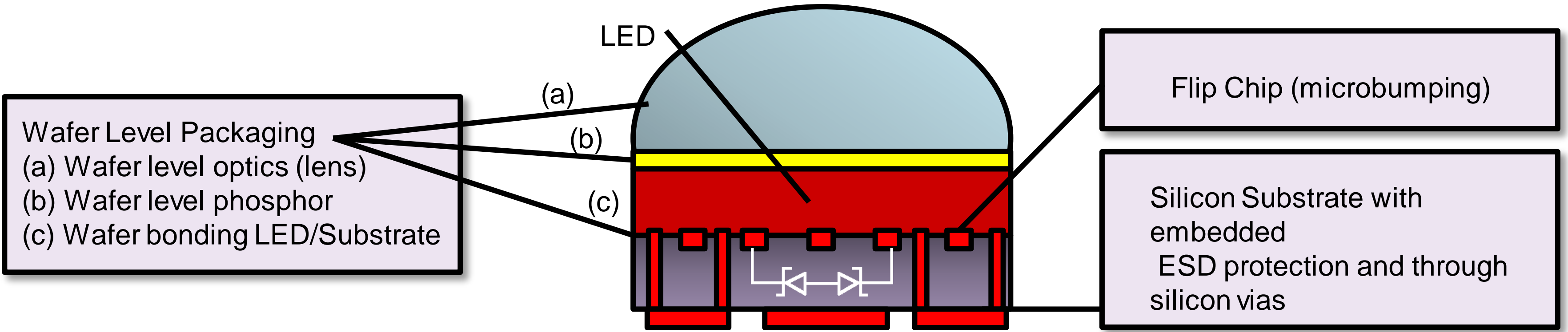
# WLP Long Term Vision:
## Wafer to Wafer packaging?






- **A number of players have roadmaps to a "<u>fully integrated 3D WLP LED package</u>"**
- **Benefits:**
  - **A record small size package in all 3 dimensions**
  - **Excellent thermal properties (thin substrate, copper filled vias) and reliability (low CTE, early ESD protection in the flow)**
  - **Low cost: as LED wafers migrate to 6-inch and possibly 8-inch wafers, the LED industry will access wafer capacity freed by the semiconductor industry (still moving to 12 inch). Also the substrate size shrinks from 10-15mm² today for a 1mm² LED die down to 1mm²-2mm² LED and package size, thus considerably lowering material costs.**
- **Critical technologies to develop are**
  - **Silicon <u>substrates with through silicon vias and embedded zener diodes</u>: as of 2011, only LG Innotek produces such substrates**
  - **LED wafer to substrate wafer bonding**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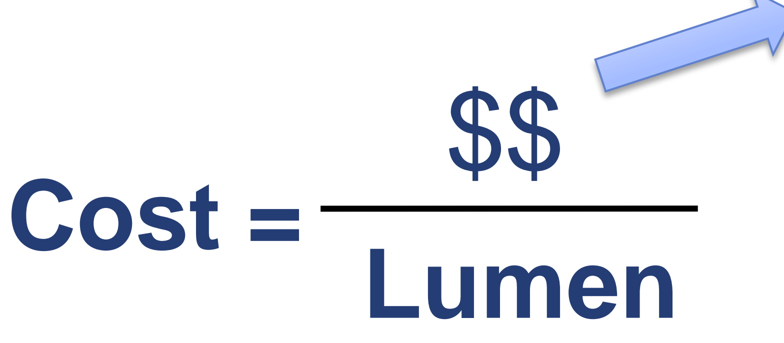
# The Path to Cost Reduction




**Manufacturing Efficiencies**

- *Higher equipment throughput*
- *Higher yields*
- *Economy of scale*
- *Materials*

**> 4x ?**

**LED performance:**

- Higher Efficiency (lumen/W)
- More light / chip (driving current)

**2-3x ?**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# Conclusion

- A 10x cost improvement of packaged LED is required to enable massive adoption of LEDs in general lighting.
- LED can only rely on performance improvement and manufacturing cost reduction to reach the cost targets.
- Packaging represents 40%++ of the cost of a packaged LED and therefore will have to contribute significantly to the cost reduction effort.
- Over time the industry will adopt methods coming from the IC industry such as Wafer Level Packaging.


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# US DOE
# SSL Roadmap

| | Metric | 2010 Status | 2015 Target |
|---|---|---|---|
| **Testing** | Throughput (UPH) | / | 2x Increase |
| | Cost of Ownership | / | 2-3x reduction every 5 years. |
| | $/Units per hour | / | / |
| **Phosphor Materials** | Batch size (kg) | 1 to 5 | >20 |
| | Cost ($/kg) | | 50% reduction every 2-3 years |
| | Material Usage Efficiency | 50% | 90% |
| | PSD Range Uniformity | 30 | 10 |
| | Duv control | 0.012 | <0.002 |
| **Phosphor Deposition** | Thickness Uniformity (1 sigma)% | 5 | 2 |
| | Cost ($/klm) | / | 50% reduction every 2-3 years |
| | Device to Device Reproducibility (SDCM) | 4 | 2 |
| **Packaged LED Metrics** | LED Efficacy (2580-3710K, 80-90 CRI) | 88 lm/W | 184 /lm/W |
| | LED Price (2580-3710K; 35 A/cm2) | 25 $/klm | 3 $/klm |
| | LED Efficacy (4746-7040K, 70-80 CRI) | 134 lm/W | 215 lm/W |
| | LED Price (4746-7040K; 35 A/cm2) | 13 $/klm | 2 $/klm |

*Source: " Solid State Lighting LED Manufacturing Roundtable Summary" – March 2011 (www1.eere.energy.gov/buildings/ssl/)*


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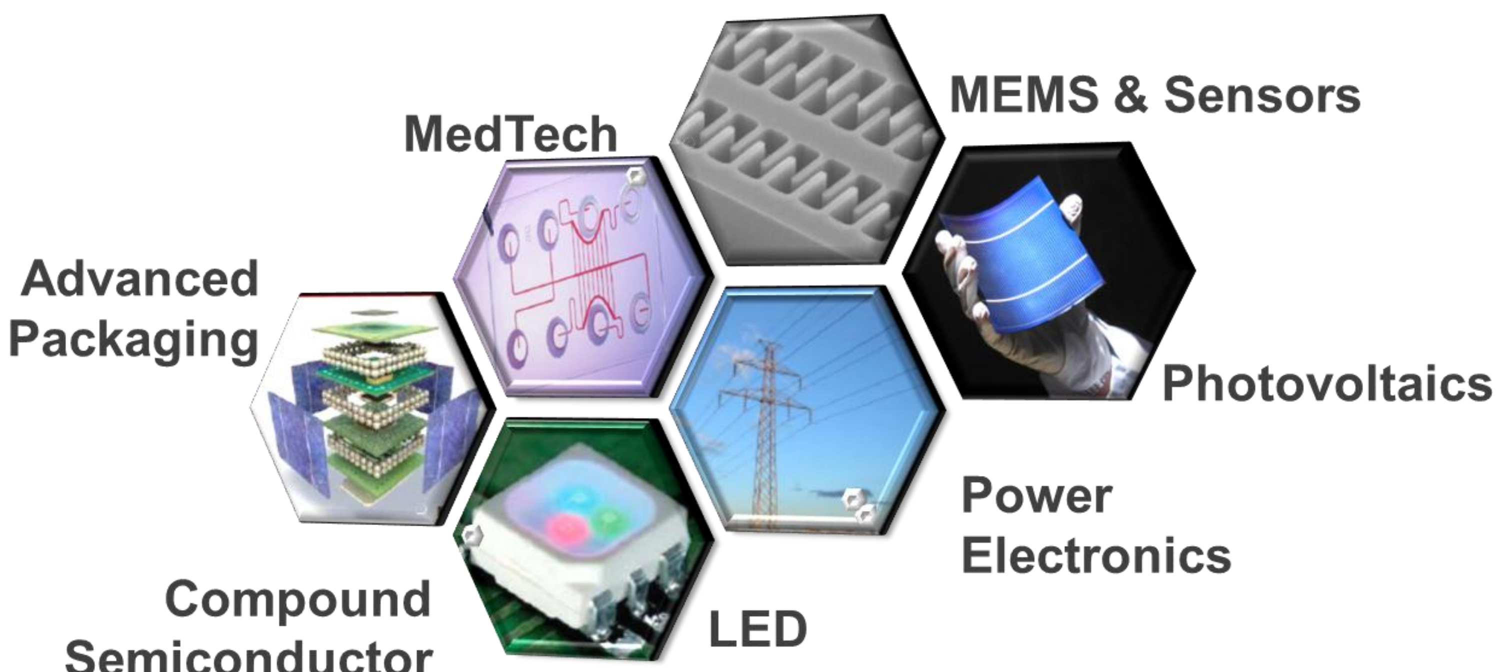


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