Coreless Packaging Technology

for High-performance Application

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Agenda

● SONY’s Coreless Package Status
● What is Coreless Package?
● Advantages in Electrical Design
● Problem and Solution for Assembly Issue
● Next Challenges
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SONY’s Coreless Package Status

Started Mass-Production for CPU application (CELL) with Coreless Substrate from April/2010.

Accumulative shipments of Coreless Package; Over 10 million

Assembly Yield; >99.9%
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What is Coreless Package?

Coreless package
Package with high density wiring by using only build-up process

Coreless Package

Conventional

Coreless Substrate

Build-up Substrate

Lid
Chip

Build-up Layer
Micro-via
Core
Where “Coreless” used for?

High-Speed Signal Datarate Requirement
High-Quality Power Delivery Requirement

Package Cost

Ceramic Sub. FC
Organic Sub. FC (Cored technology)
Organic Sub. WB

“Coreless” can replace… cored substrates for SI/PI improvement!!
several ceramic substrates for Cost down!!
Summary of Advantage and Disadvantage

- Good electrical property, low cost and high wiring-ability by eliminating of core process
- Enhanced assembly technique is needed because of low rigidity

<table>
<thead>
<tr>
<th>Advantage</th>
<th>Disadvantage</th>
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<tbody>
<tr>
<td>✓ Cost reduction by eliminating of core process</td>
<td>✓ Bad chip joint yield in a current assembly process because warpage control is difficult</td>
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<tr>
<td>✓ The limit of C4 layout is extremely little because of the improvement of wiring-ability</td>
<td>✓ Laminate chipping is occurred easily</td>
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<tr>
<td>✓ Good high-speed transmission characteristic</td>
<td>✓ New manufacturing infrastructure for coreless packaging is necessary</td>
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<tr>
<td>✓ Power characteristic of both AC and DC are improved</td>
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Advantages in Electrical Design

Wiring Capability
- Non-PTH structure allows direct signaling, and full-layer signaling.

High PI Performance
- Non-PTH PDN remarkably reduces AC impedance.

High SI Performance
- Coreless signal wiring avoids big return loss at PTHs.
You must make **fan-out region** to fit the C4/line pitch into the big PTH pitch...

- **Direct signaling is available.**
- **All layers can be used as signal layer.**

Designer can use the wiring area with maximum efficiency.
High PI Performance

➢ Why?

Because of the lowest self and highest mutual inductances of package PDN.

\[ L_{\text{total}} = L_{\text{vdd}} + L_{\text{vss}} - 2M \]

Min. chip-to-caps distance (lower L)

Build-up = ~1 mmt
Coreless = ~300 umt

Parallel High Density Via (lower L)

Build-up = 300 pH/1PTH
Coreless = 150 pH/1via
40 pH/4via

Min. VDD-VSS via distance (higher M)

Build-up = 300um
Coreless = 150um

Because of the lowest self and highest mutual inductances of package PDN.
High PI Performance

AC Impedance Improvement (Substrate + decap)

- Coreless package has 25% advantage compared to cored package.
- AC noise becomes lower, then results in system voltage & power reduction.

<table>
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<tr>
<th>Package VDD Impedance [ohm]</th>
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<tr>
<td>10MHz</td>
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<tr>
<td>1GHz</td>
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- 25% Cut

VDD

C4 side

BGA side

VSS

Bottom Decap

Diagram showing AC Impedance Improvement with Cored and Coreless packages.
High SI Performance

Where Coreless can contributes?

- In FC-BGA, the big two of Z0 mismatch points at signal transmission are PTH & ball.
- We cannot remove both of them, but we can remove one of them: PTH.
High SI Performance

Coreless substrate is potentially the widest bandwidth substrate structure.

**Coreless**
- 35-umt Via
  - Via dia: 70/60 um
  - Via pitch: 185 um
  - Via land dia: 120 um

**Standard**
- 800-umt Core
  - PTH dia: 300 um
  - PTH pitch: 600 um
  - PTH land dia: 500um

**Thincore**
- 400-umt Core
  - PTH dia: 120 um
  - PTH pitch: 300 um
  - PTH land dia: 250um

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**Return Loss of Diff. Via only**
- -15dB

**Insertion Loss of Diff. Via only**
- -3dB
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Problem for Assembly

1. Warpage

Build-up Substrate (0.4mm Core)
Warpage value; 104μm

Coreless Substrate
Warpage value; 354μm
Problem for Assembly

2. Warpage behavior at high temperature (1)

※Chip attach area warpage
Solution

To solve disadvantages of coreless, enhanced assembly process is applied

- Warpage; Clumping jig is applied for chip attach process

Key point
- Jig material (Stiffness property, CTE, Flatness)
- Clumping force
- Clumping position

- Laminate chipping; Optimization of machine condition

- Package co-planarity; Enhanced lid attach process
Solution

Without Jig

25°C
150°C
180°C
Reflow peak

With Jig
Package Co-planarity

- Coreless
- Build-up (400μm Core)

※42.5 x 42.5mm Package
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Thank you