Coreless Packaging Technology for High-performance Application

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Agenda

- SONY's Coreless Package Status
- What is Coreless Package ?
- Advantages in Electrical Design
- Problem and Solution for Assembly Issue
- Next Challenges

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SONY's Coreless Package Status

Started Mass-Production for CPU application (CELL) with Coreless Substrate from April/2010.

Accumulative shipments of Coreless Package ; Over 10 million

Assembly Yield ; >99.9%

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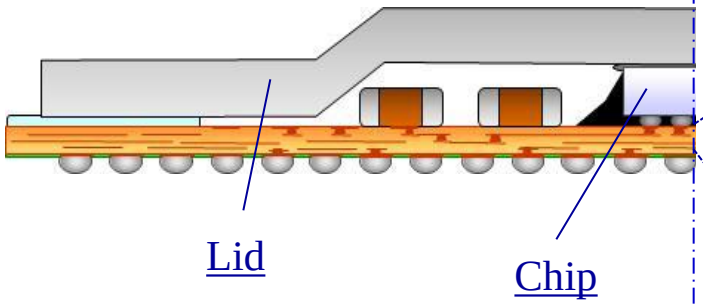
What is Coreless Package ?

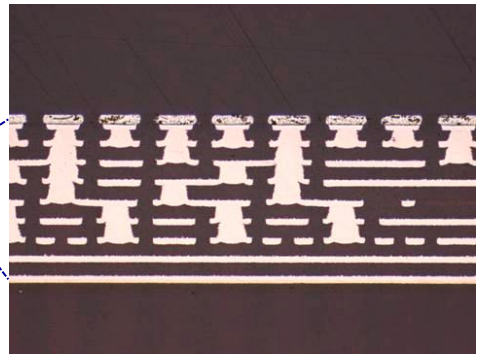
Coreless package

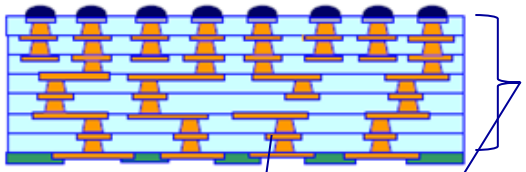
Package with high density wiring by using only build-up process

Coreless Package

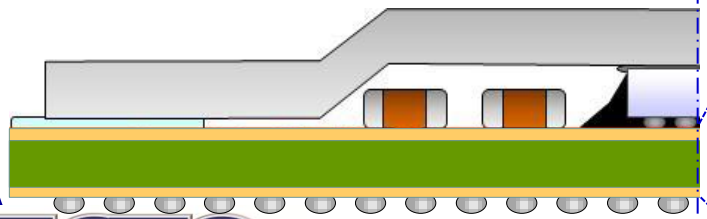


Coreless Substrate

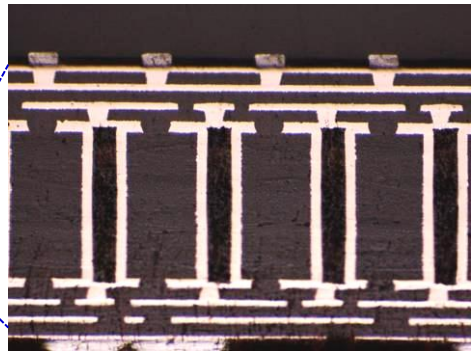


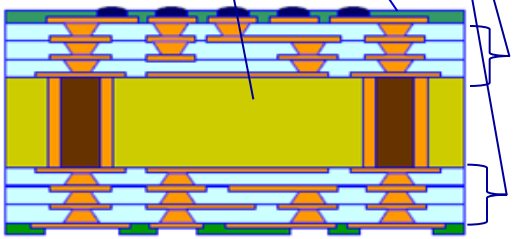


Conventional

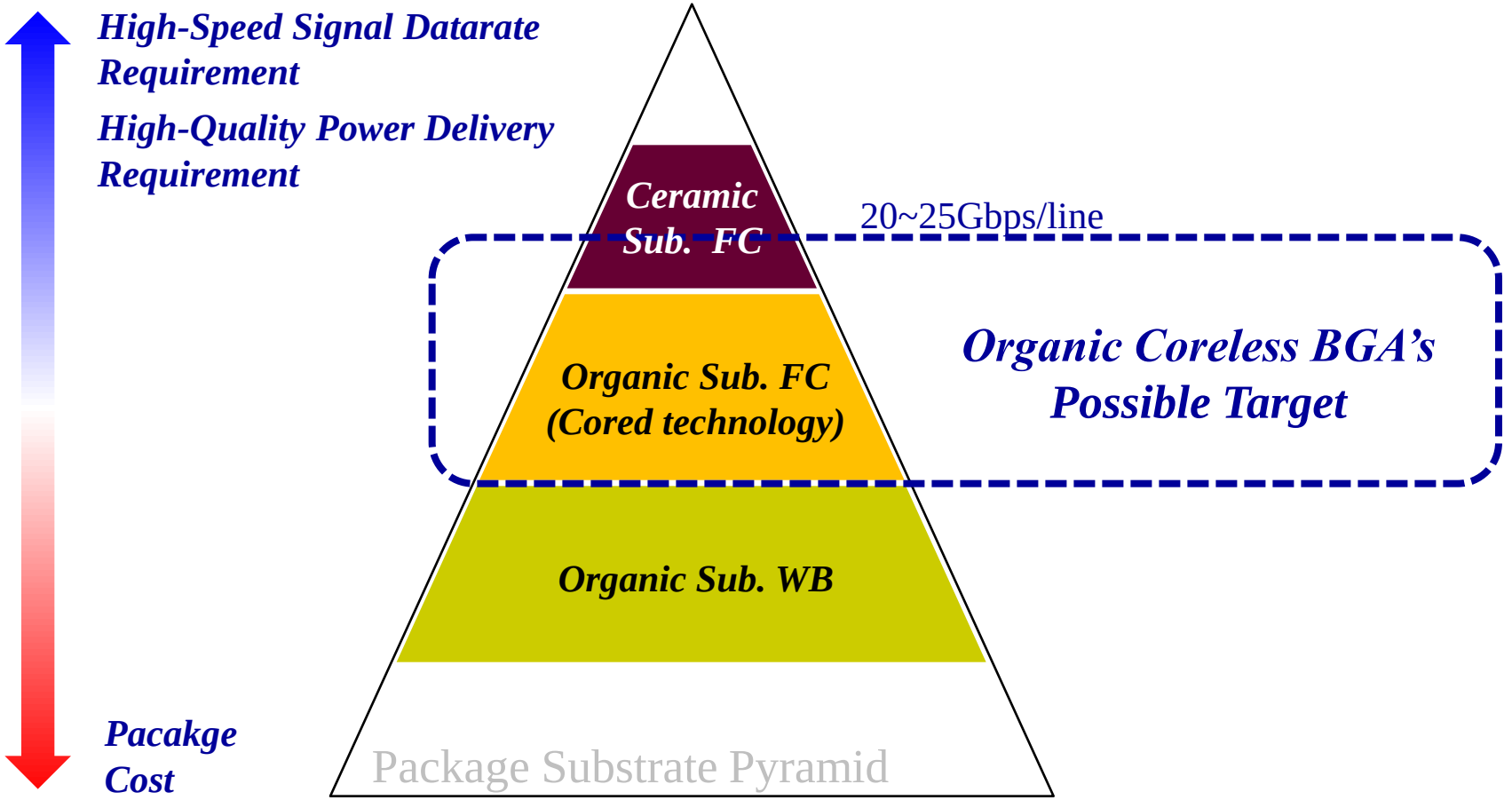


Build-up Substrate





Where “Coreless” used for?



“Coreless” can replace… cored substrates *for SI/PI improvement!!*
several ceramic substrates *for Cost down!!*

Summary of Advantage and Disadvantage

- Good electrical property, low cost and high wiring-ability by eliminating of core process
- Enhanced assembly technique is needed because of low rigidity

Advantage	Disadvantage
✓Cost reduction by eliminating of core process	✓Bad chip joint yield in a current assembly process because warpage control is difficult
✓The limit of C4 layout is extremely little because of the improvement of wiring-ability	✓Laminate chipping is occurred easily
✓Good high-speed transmission characteristic	✓New manufacturing infrastructure for coreless packaging is necessary
✓Power characteristic of both AC and DC are improved	

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Advantages in Electrical Design

(PTH: Plated Through Hole)

Wiring Capability

- Non-PTH structure allows direct signaling, and full-layer signaling.

High PI Performance

- Non-PTH PDN remarkably reduces AC impedance.

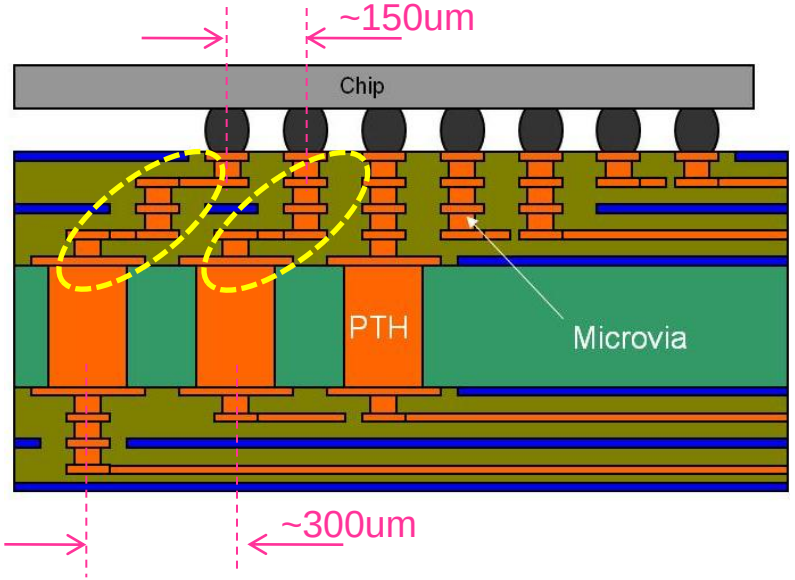
High SI Performance

- Coreless signal wiring avoids big return loss at PTHs.

Wiring Capability

Build-up Package

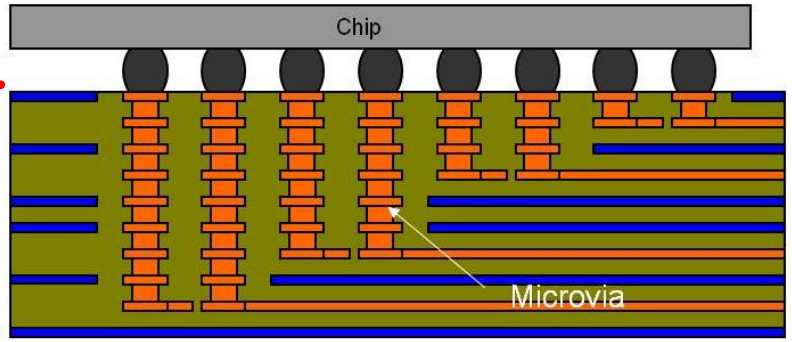
- You must make **fan-out region** to fit the C4/line pitch into the big PTH pitch…



Coreless Package

- Direct signaling is available.
- All layers can be used as signal layer.

Designer can use the wiring area with maximum efficiency.

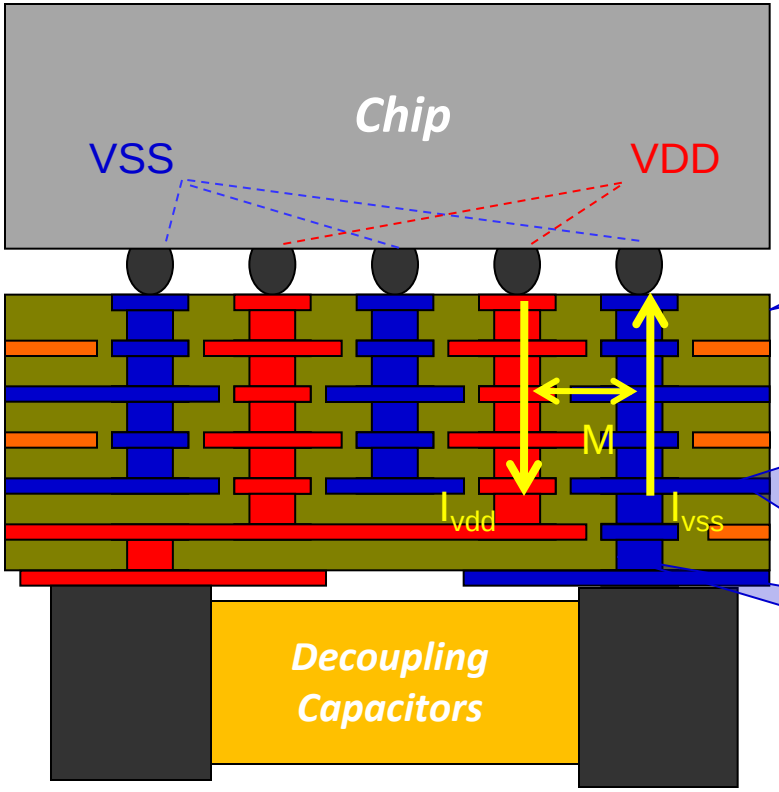


High PI Performance

➢ *Why?*

Because of the lowest self and highest mutual inductances of package PDN.

$L_{total}=L_{vdd}+L_{vss}-2M$



Min. chip-to-caps distance (lower L)

Build-up = ~ 1 mmt

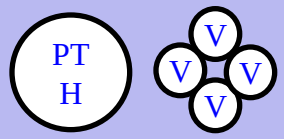
Coreless = ~300 umt

Parallel High Density Via (lower L)

Build-up = 300 pH/1PTH

Coreless = 150 pH/1via

40 pH/4via



Min. VDD-VSS via distance (higher M)

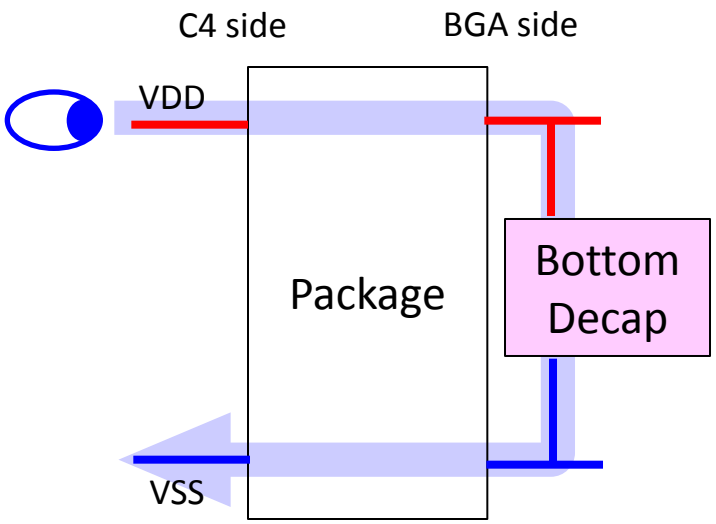
Build-up = 300um

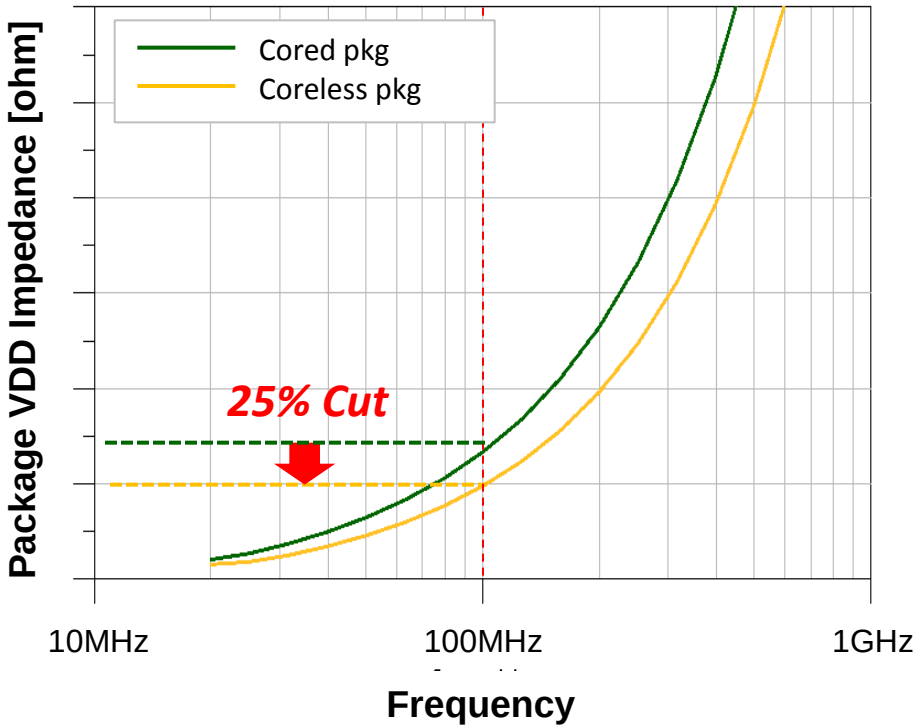
Coreless = 150um

High PI Performance

➢ *AC Impedance Improvement (Substrate + decap)*

- Coreless package has 25% advantage compared to cored package.
- AC noise becomes lower, then results in system voltage & power reduction.



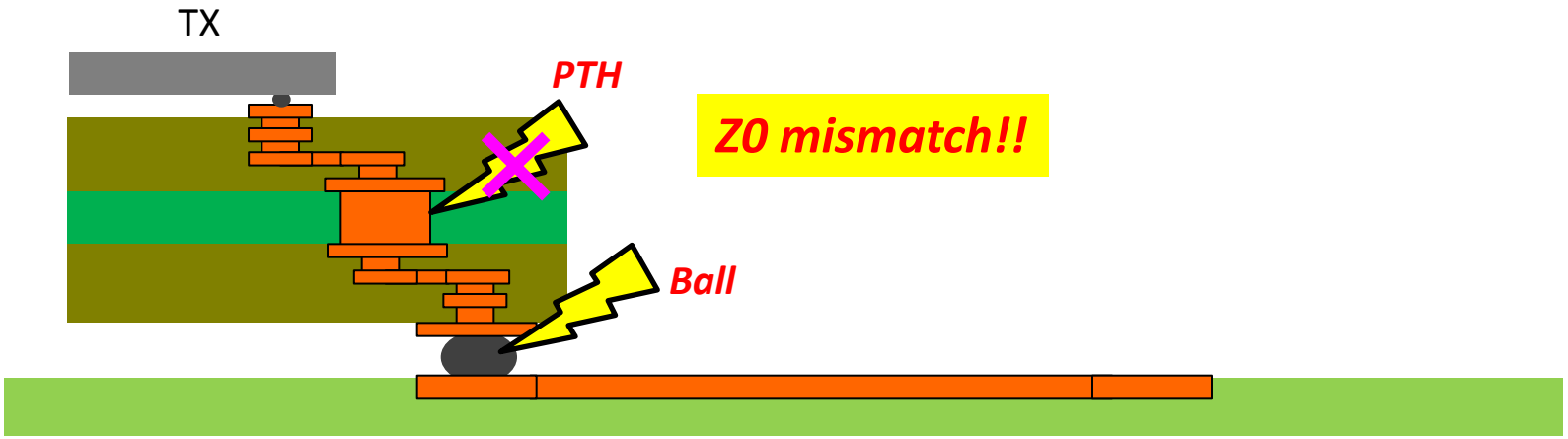


High SI Performance

- ***Where Coreless can contributes?***

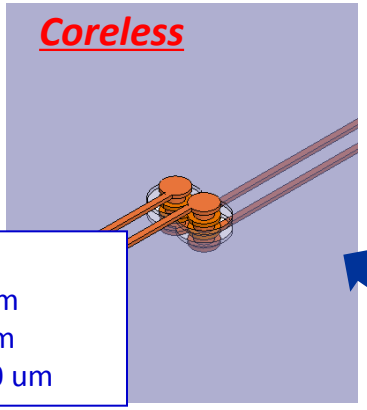
- In FC-BGA, the big two of Z0 mismatch points at signal transmission are PTH & ball.

- We cannot remove both of them, but we can remove one of them: PTH.

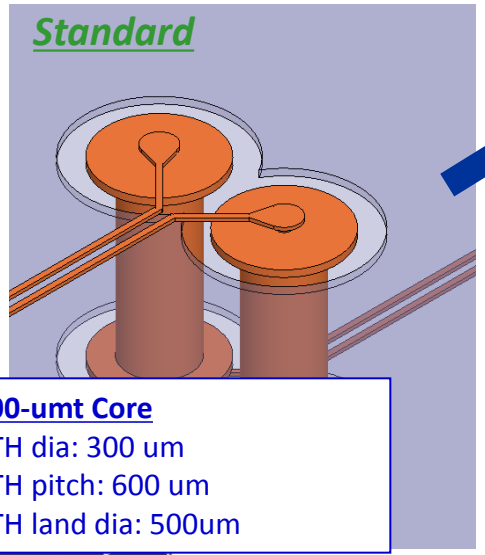


High SI Performance

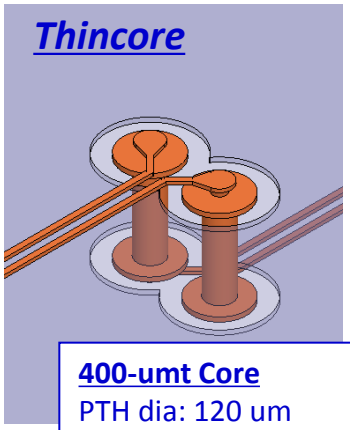
Coreless substrate is potentially the widest bandwidth substrate structure.



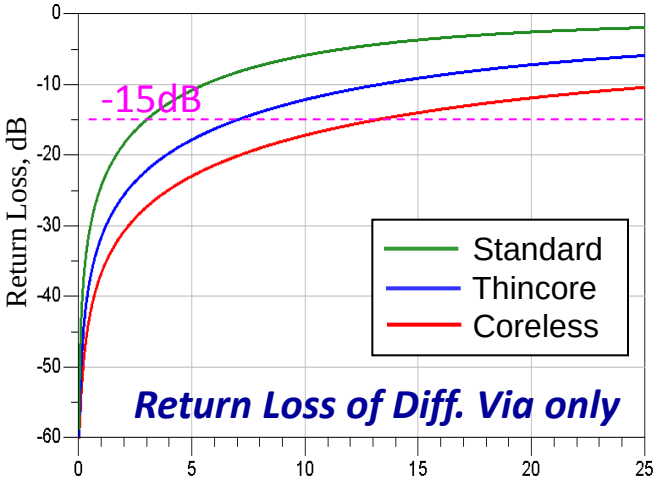
35-umt Via
Via dia: 70/60 um
Via pitch: 185 um
Via land dia: 120 um

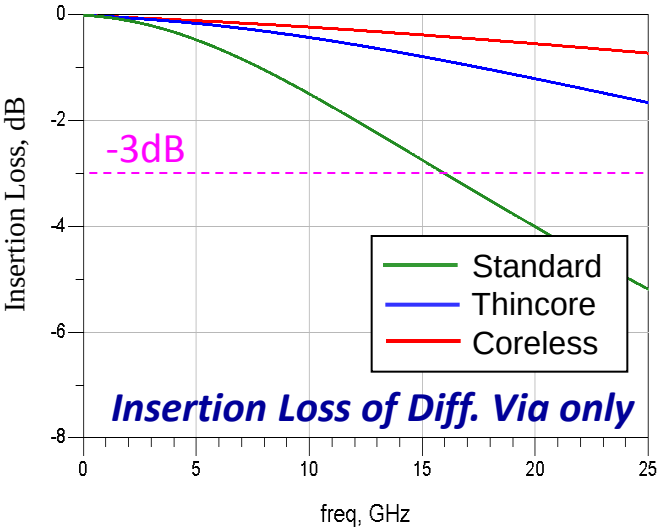


800-umt Core
PTH dia: 300 um
PTH pitch: 600 um
PTH land dia: 500um



400-umt Core
PTH dia: 120 um
PTH pitch: 300 um
PTH land dia: 250um





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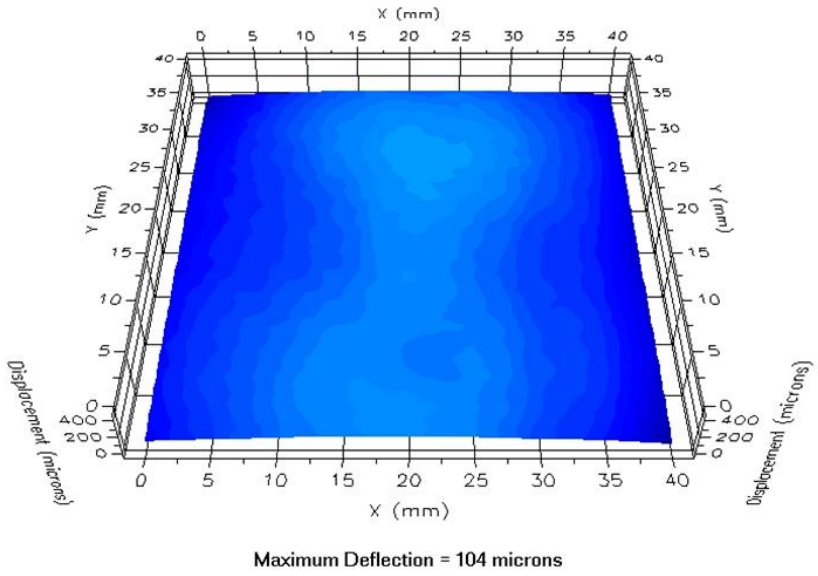
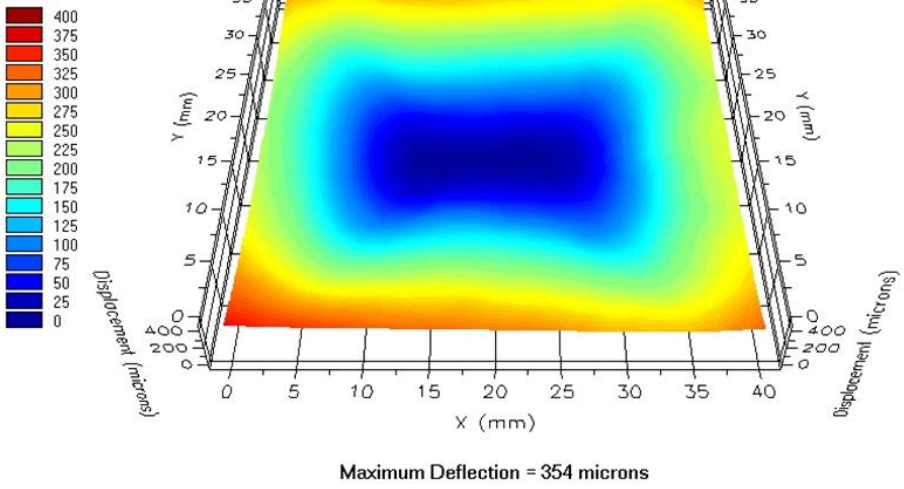
Problem for Assembly

1. Warpage





Build-up Substrate (0.4mmt Core)

Warpage value ; 104μm

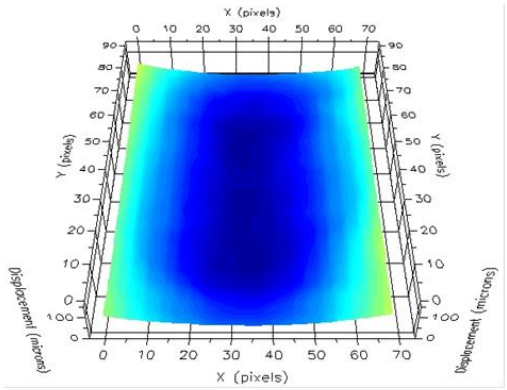
Coreless Substrate

Warpage value ; 354μm

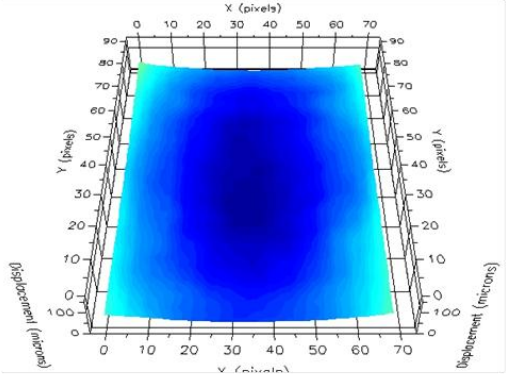
Problem for Assembly

2. Warpage behavior at high temperature (1)

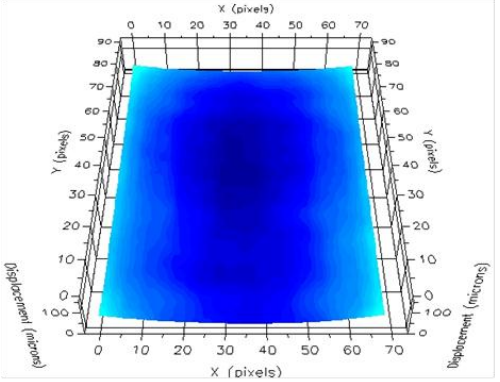
RT



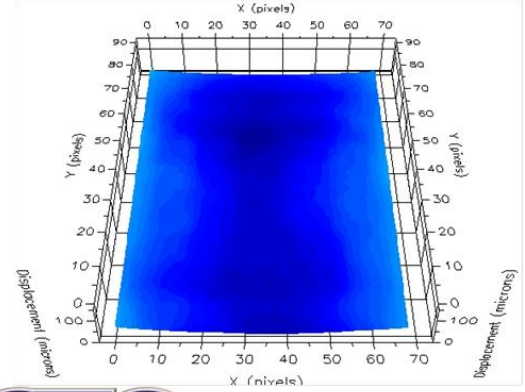
150C



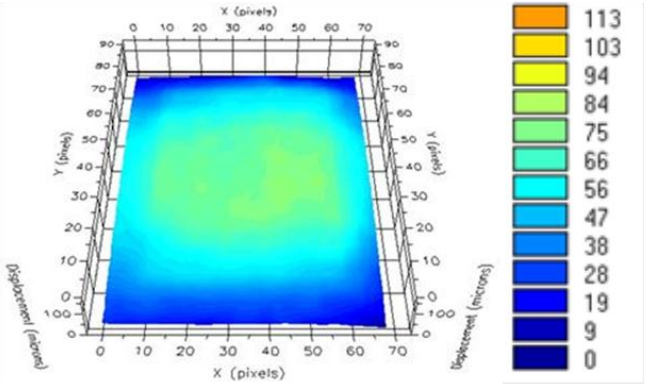
180C



210C



250C



※Chip attach area warpage

Solution

To solve disadvantages of coreless, enhanced assembly process is applied

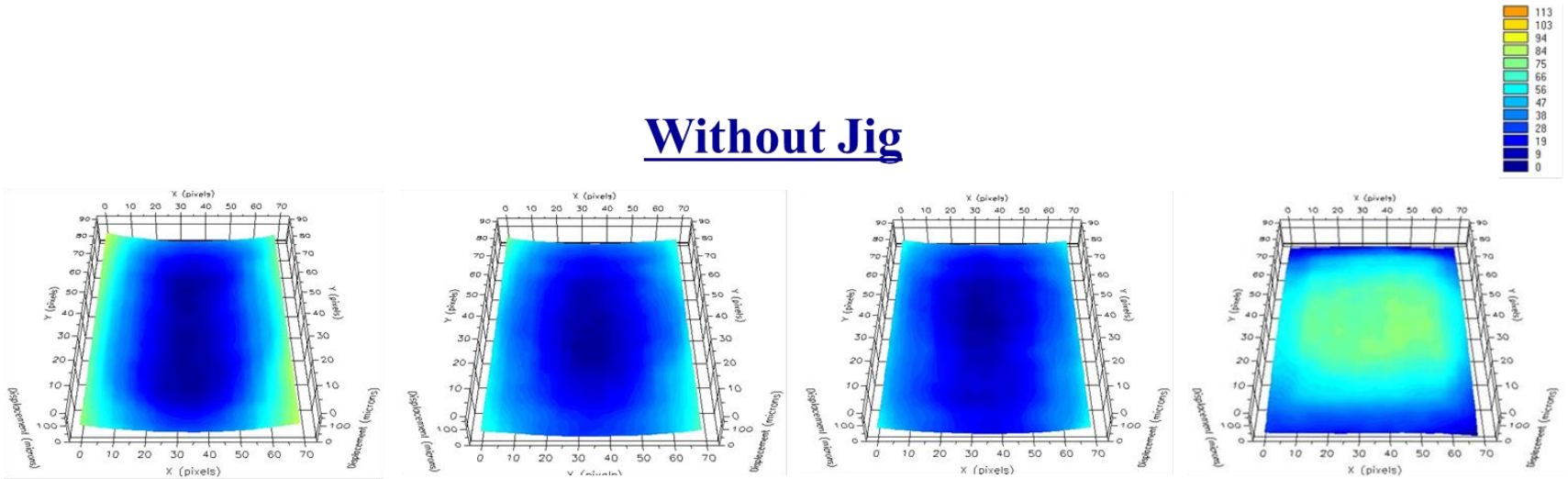
- Warpage ; Clumping jig is applied for chip attach process

  Key point
  - Jig material (Stiffness property, CTE, Flatness)
  - Clumping force
  - Clumping position

- Laminate chipping ; Optimization of machine condition
- Package co-planarity ; Enhanced lid attach process

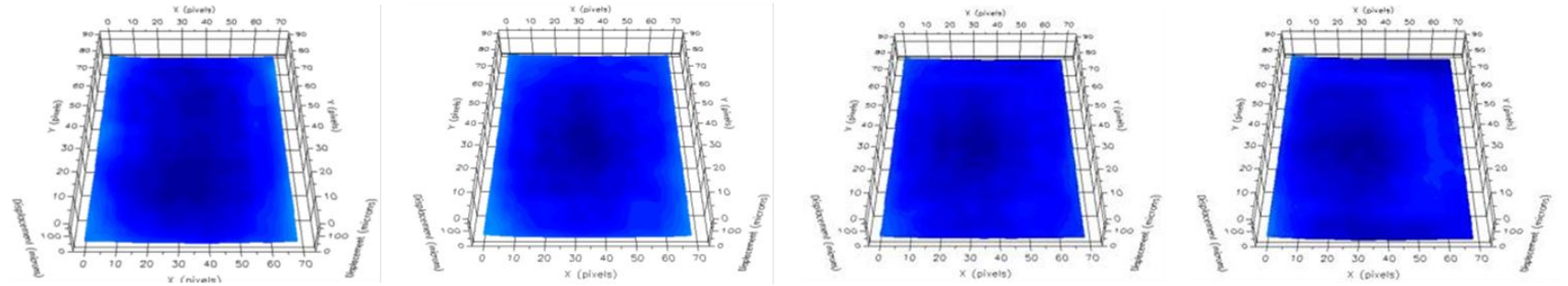
Solution

Without Jig

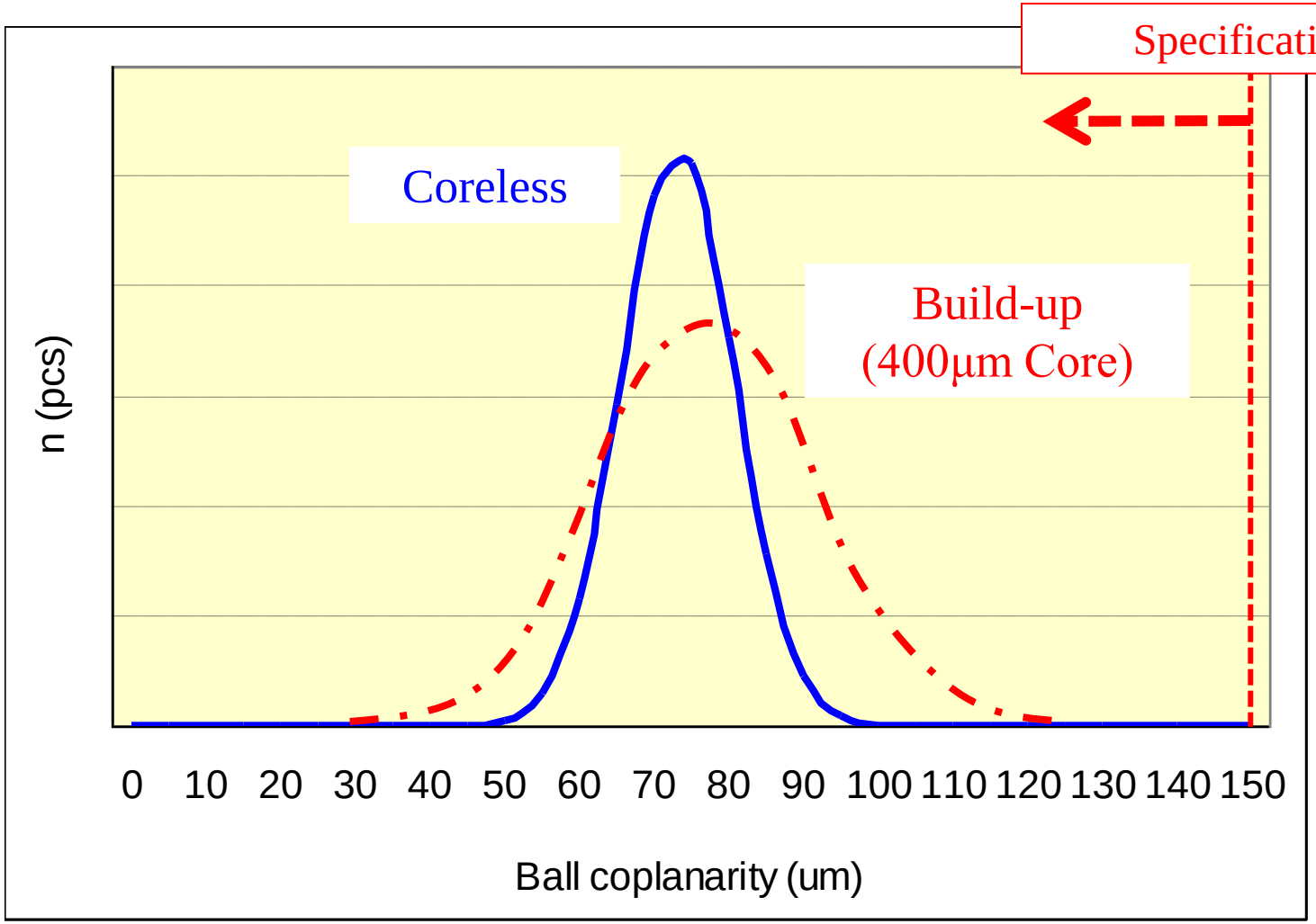


25℃ 150℃ 180℃ Reflow peak

With Jig



Package Co-planarity



※42.5 x 42.5mm Package

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Thank you