The Low Warpage Coreless Substrate for High Speed Large Size Die Packages

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AGENDA

1. Introduction
2. Targets of Development
3. Warpage Control Method Development
    1. Coreless Substrate
    2. Package Assembly
    3. Board Mounting
4. Conclusion

Fujitsu's Technologies

-102 processors are installed in a rack
-32 × 24 = 864 racks are installed
Installed Area: 36m × 38.4m
-88,128 CPUs (705,024cores)

Super Computer Ranking

Rank	Site	Computer/Year Vendor	Cores	R_{max} [Pflops]	Power [MW]
1	RIKEN Advanced Institute for Computational Science(AICS) Japan	K computer, SPARC64 VIIIfx 2.0GHz, Tofu interconnect / 2011	705,024	10.510	12.660
2	National Supercomputing Center In Tianjin China	NVIDIA GPU, FT-1000 8C / 2010 NUDT	186,368	2.566	4.040
3	DOE/SC/Oak Ridge National Laboratory United States	Jaguar - Cray XT5-HE Opteron 6-core 2.6 GHz / 2009 Cray Inc.	224,162	1.759	6.951
4	National Supercomputing Centre in Shenzhen (NSCS) China	Nebulae - Dawning TC3600 Blade, Intel X5650, NVidia Tesla C2050 GPU / 2010 Dawning	120,640	1.271	2.580
5	GSIC Center, Tokyo Institute of Technology Japan	TSUBAME 2.0 - HP ProLiant SL390s G7 Xeon 6C X5670, Nvidia GPU, Linux/Windows / 2010 NEC/HP	73,278	1.192	1.398
6	DOE/NNSA/LANL/SNL United States	Cielo- Cray XE6 8-core 2.4GHz / 2011 Cray Inc.	142,272	1.110	3.980
7	NASA/Ames Research Center/NAS United States	Pleiades - SGI Altix ICE 8200EX/8400EX, Xeon HT QC 3.0/Xeon 5570/5670 2.93 Ghz, Infiniband / 2011 SGI	111,104	1.088	4.102
8	DOE/SC/LBNL/NERSC United States	Hopper - Cray XE6 12-core 2.1 GHz / 2010 Cray Inc.	153,408	1.054	2.910
9	Commissariat a l'Energie Atomique (CEA) France	Tera-100 - Bull bullx super-node S6010/S6030 / 2010 Bull SA	138,368	1.050	4.590
10	DOE/NNSA/LANL United States	Roadrunner - BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz / Opteron DC 1.8 GHz, Voltaire Infiniband / 2009 IBM	122,400	1.042	2.346

Efficiency ratio93.2% / 88,128CPU

Source : 37th TOP500LIST (www.top500.org)

Fujitsu Server Development trend

High Performance Technology

Hardware Barrier

Multi-core / Multi-thread

L2$ on Die

Non-Blocking $
O-O-O Execution
Super-Scalar

Single-chip CPU

Store Ahead
Branch History
Prefetch

High Reliability technology

Cache ECC
Register/ALU Parity
Instruction Retry
Cache Dynamic Degradation
RC/RT/History

SPARC64™ Processor

HPC

UNIX

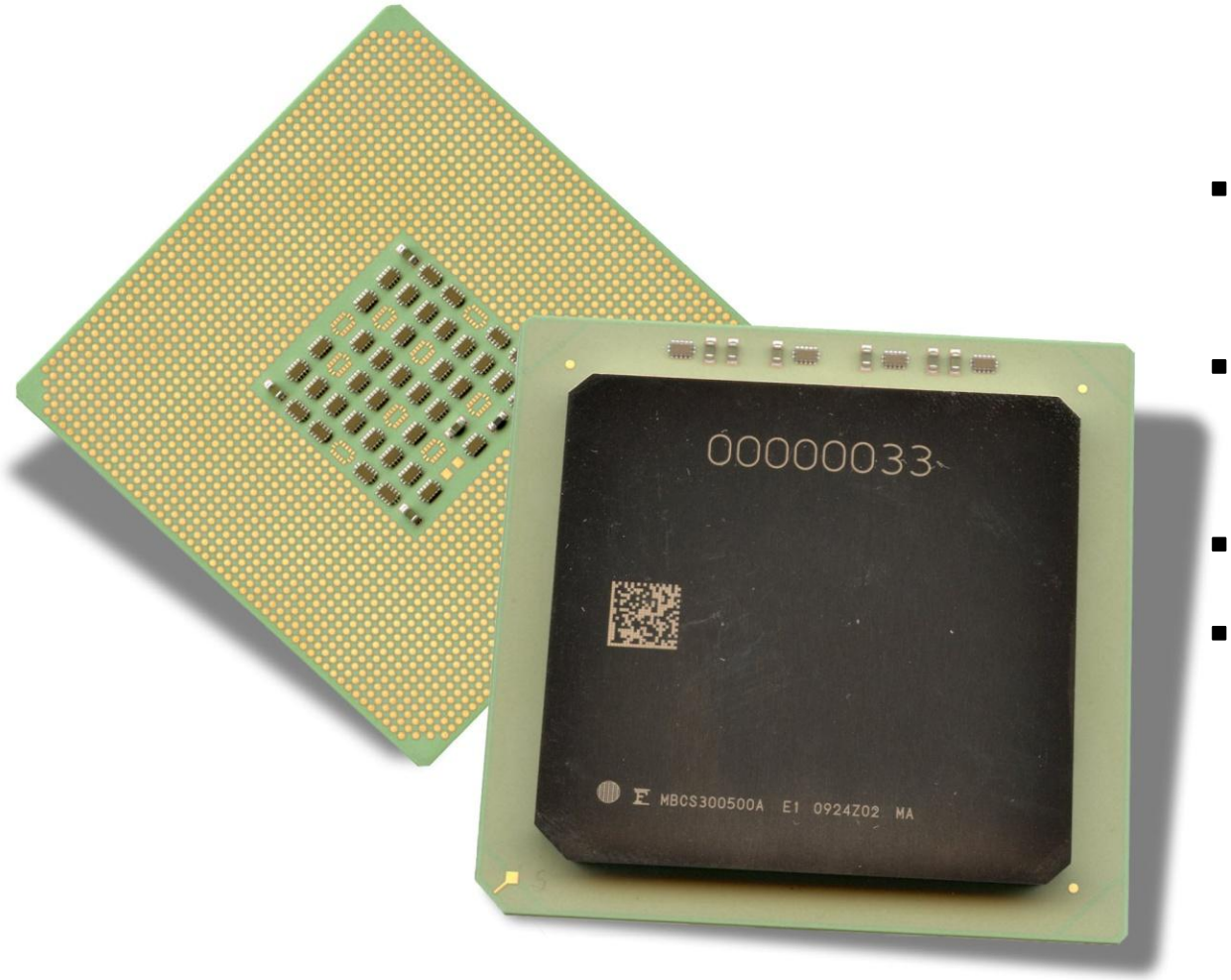
Main Frame

SPARC64 VIIIfx
SPARC64 VII
SPARC64 VI
SPARC64 V+
SPARC64 V
SPARC64 GP
SPARC64 I I
SPARC64
GS21
GS21 900
GS21 600
GS8900
GS8800
GS8600

Technology Generation

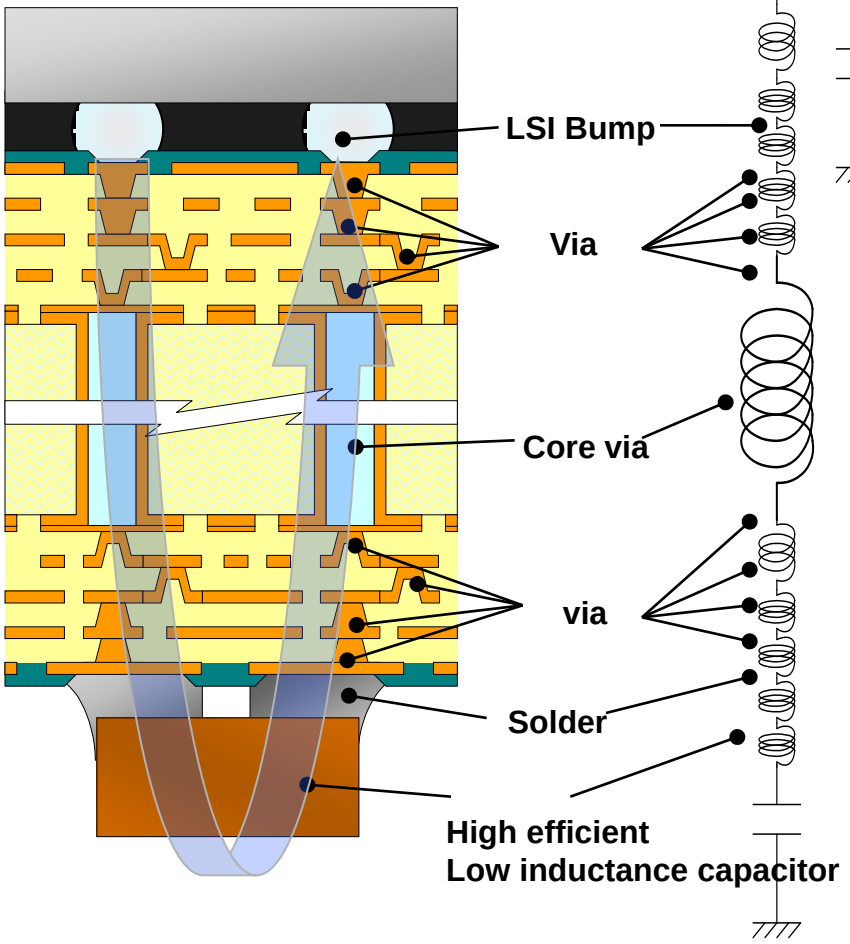
~1995 | 1996 ~1997 | 1998 ~1999 | 2000 ~2003 | 2004 ~2006 | 2007~

CPU Package Outline



- **PKG Size**
  55.5 × 55.5mm
- **Cu-LID Size**
  45.0 × 45.0mm
- **BGA 2408pin**
- **Heat resistance**
  0.06℃/w

Why High Via Density Substrate?



Power Consumption Higher

Power Voltage Lower

Decrease Power noise in High frequency Range

Use Low Inductance Capacitor

Mounting under LSI is efficient

Need low Power-GND roop inductance

Thinner Substrate

Finer Core Via pitch or Core-Less

Full Stacked Thin-Film layer via

Coreless Issue

	Cost	Miniaturization	Inductance	Assembly
Coreless				
Conventional				

Why is not Coreless popular?

Warpage Control Issue

The factors of Warpage

1) **CTE mismatch and Low Young's modulus of package substrate material**
2) **Package assembly technique**
3) **Board mount reflow temperature**

Development Target

Warpage control technique

1. **Coreless Substrate Structure**
   Material composition and Structure control

2. **Package Assembly**
   Warpage Correction control

3. **Board mounting**
   Reflow Temperature control

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Warpage Improvement Method

Using an insulating material with a small CTE mismatch

➡ **We use prepregs**

General Material Combination

Resin = 35ppm/℃ ⟺ **Cu = 17ppm/℃**

Our Material Combination

Prepreg = 15ppm/℃ ⟷ **Cu = 17ppm/℃**

CTE mismatch decreased to 1/9 by prepreg application.

Coreless substrate with all prepreg layers exhibits smaller warpage

Problem of Prepreg in Transmission

Properties	Prepreg	Resin
CTE(@R.T.)	15ppm/℃	35ppm/℃
CTE mismatch with Cu	Small ⇩	Large ⇩
Warpage	Exellent	Poor
Transmission Property	Poor	Exellent

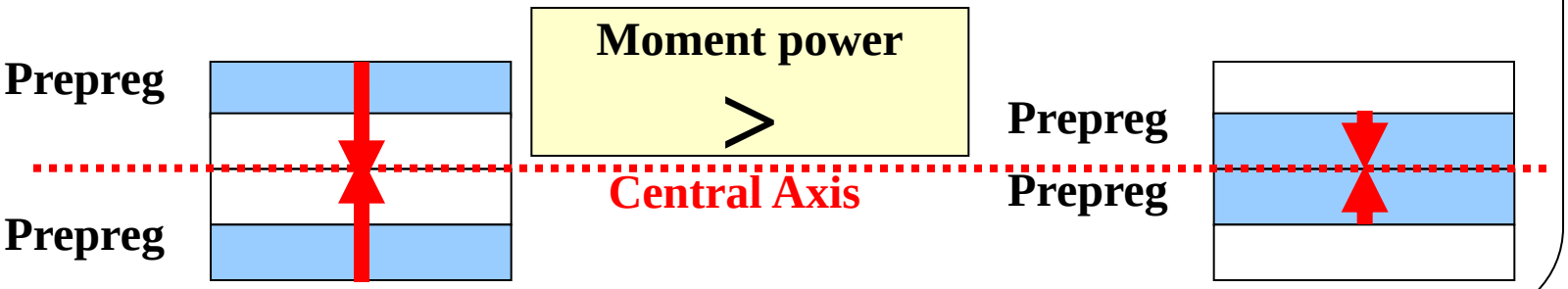
Coreless substrate with all prepreg layers is inferior to transmission property.

Necessary to reduce the prepreg consumption as much as possible, and to control a warpage.

Low warpage and High Trans. Quality

1. Arrangement of prepregs in *external* layers.

To control the warpage by moment power



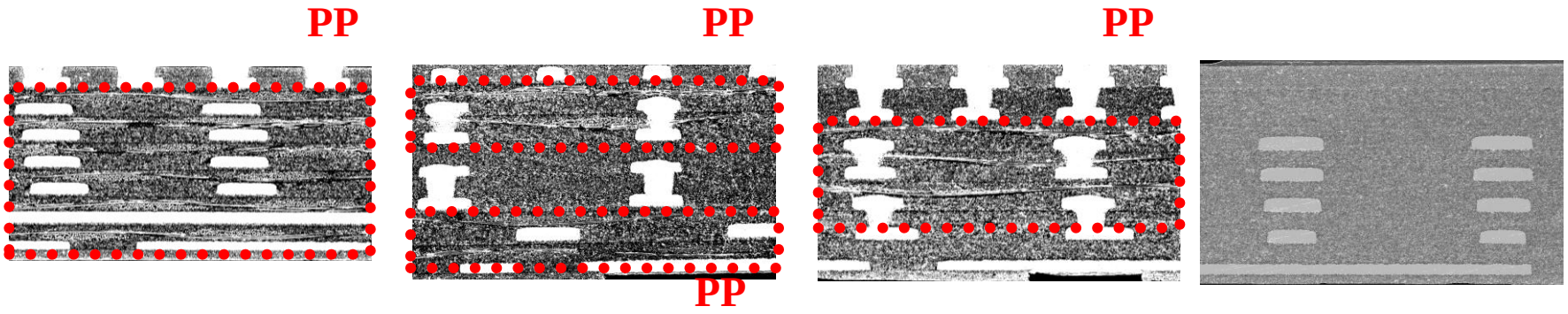
2. Arrangement of resins in *internal* layers.

Skew less transmission property

We propose the coreless structure with external prepregs and internal resins.

Layer Structures of Prepared Coreless

1. All-PP
2. Outer-PP
3. Inner-PP
4. None-PP



Cross-sectional view confirms the PP arrangement difference

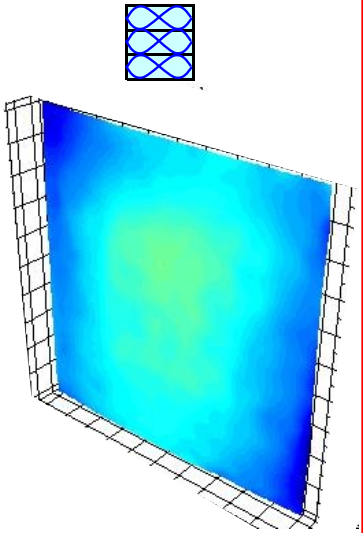
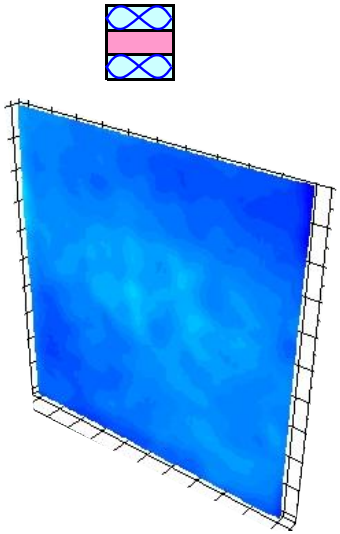
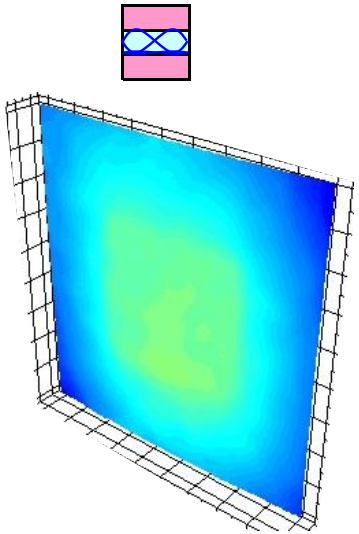
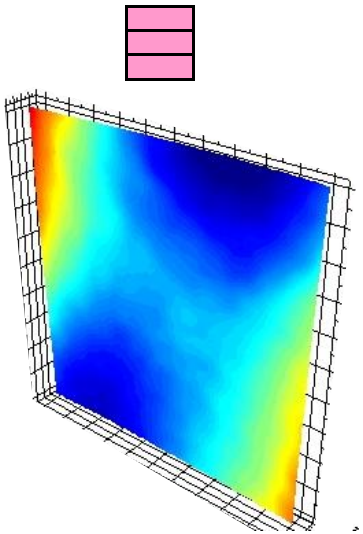
Layer	Layer Structure			
	All-PP	Outer-PP	Inner-PP	None-PP
V2				
V3				
V4				
V5				
V6				
V7				

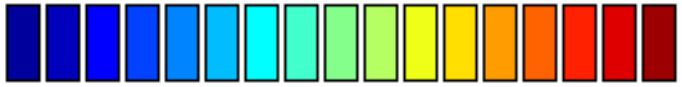
PP layer

Small CTE mismatch Resin layer

Large CTE mismatch

Warpage Measurement Results

All-PP	Outer-PP	Inner-PP	None-PP
			
115	58 **Minimum Warpage**	122	307



We succeeded in reducing the warpage with Outer-PP structure.

Development Target

Warpage control technique

1. Coreless Substrate
   Material composition and Structure control

2. **Package Assembly**
   Warpage Correction control

3. Board mounting
   Reflow Temperature control

Package Substrate Warpage

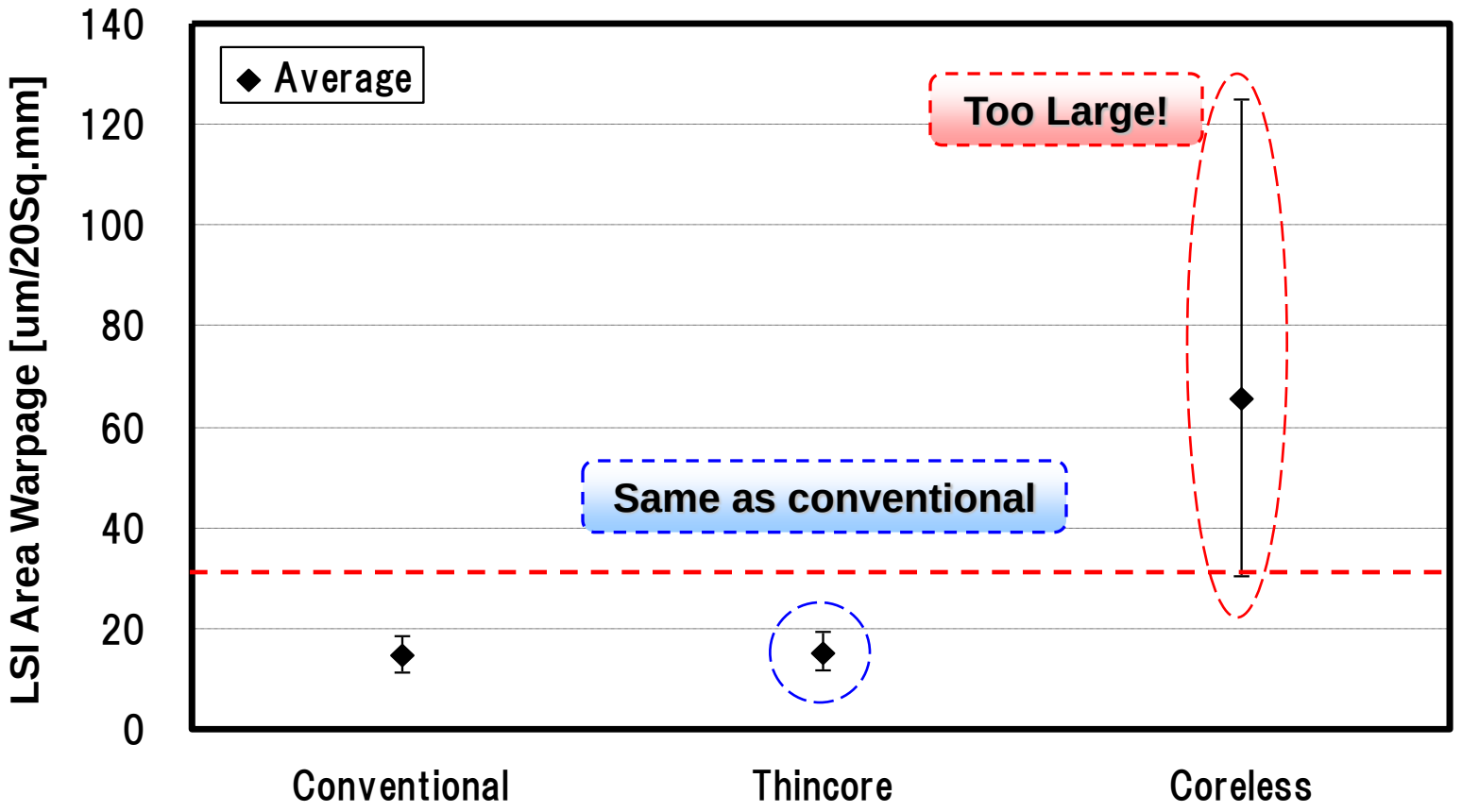


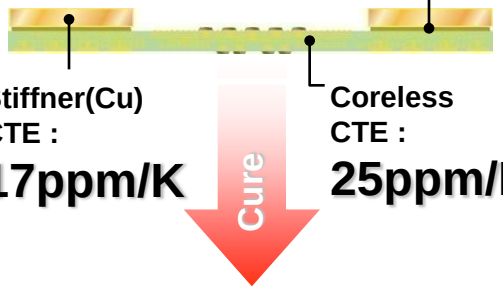
Fig.1 Comparison of LSI area warpage in Each substrate type

Stiffener Assembly Process

<Controlling parameters on Stiffener assembly>

Curing temperature

Thermal curing Adhesive
Curing reaction Temp. : 100<->130C



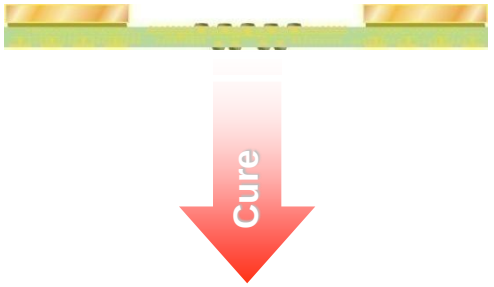
CTE Gap

Stiffner < Coreless

Tensile force dominate during below curing temperature

Tensile force

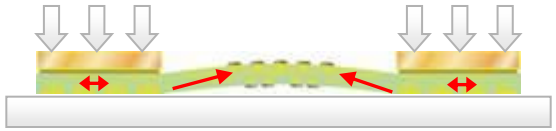
Pressure



Large pressure prevent expansion.

↓

Deformation



Need for process optimization

Process Optimization

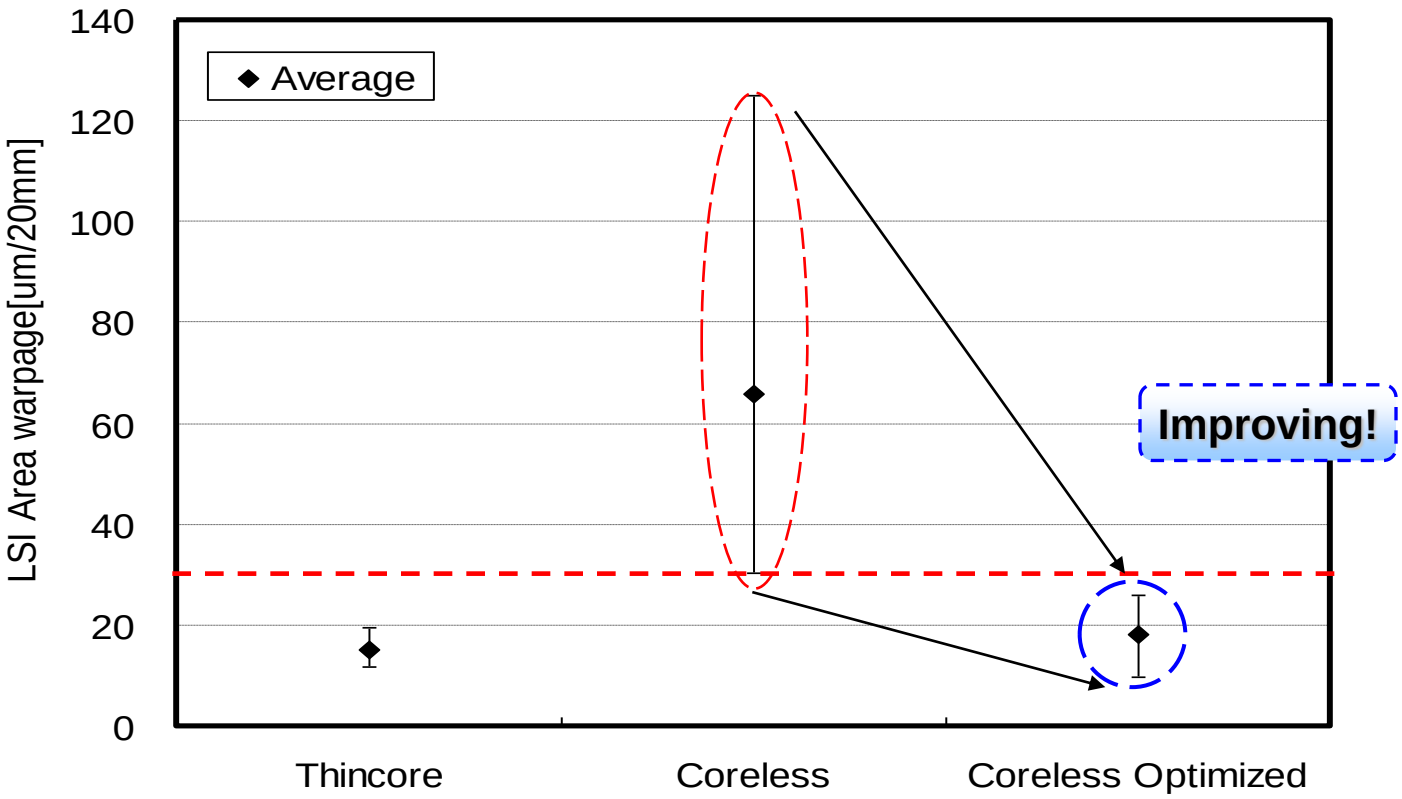


Fig.4 Substrate type and warpage

Optimization of the warpage controlling

Reliability Test Result

Test conditions

Thermal Cycle	-25/+125(cel) 1,000cycles
LSI Size	20mm square, 0.15mm thick
Substrate Size	42.5mm square, 0.3mm thick

20 test pieces were prepared

Pass conditions

Less than twice of the initial resistance

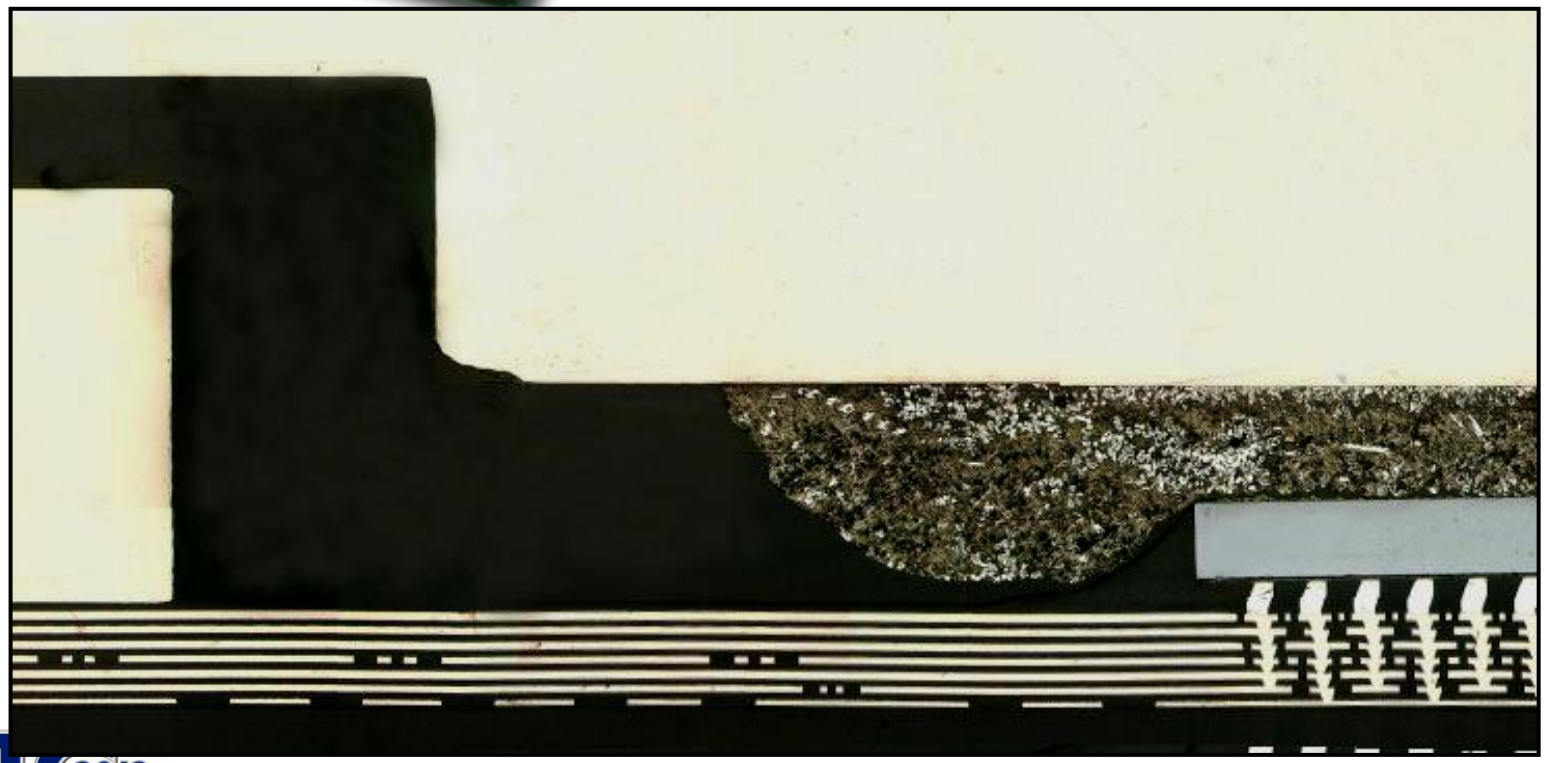
Test results

Sample	1000cycle Reliability Test
All-PP	Passed
Outer-PP	Passed
Inner-PP	Failed
None-PP	Failed

Effective factors for reliability

1. The warpage value at maximum temperature
2. The temperature dependent warpage in cooling process.

Reliability Test Result



Development Target

Warpage control technique

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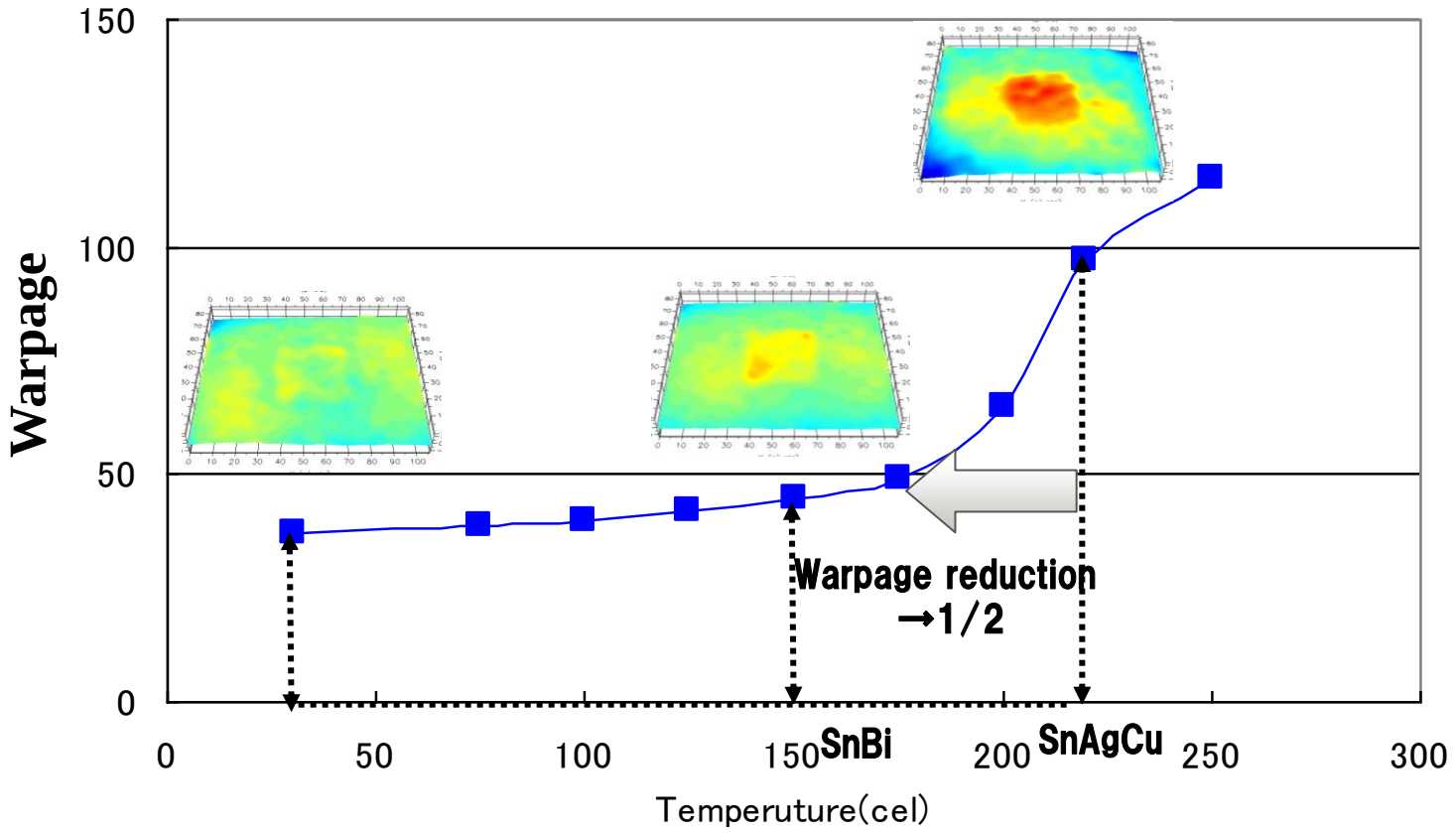
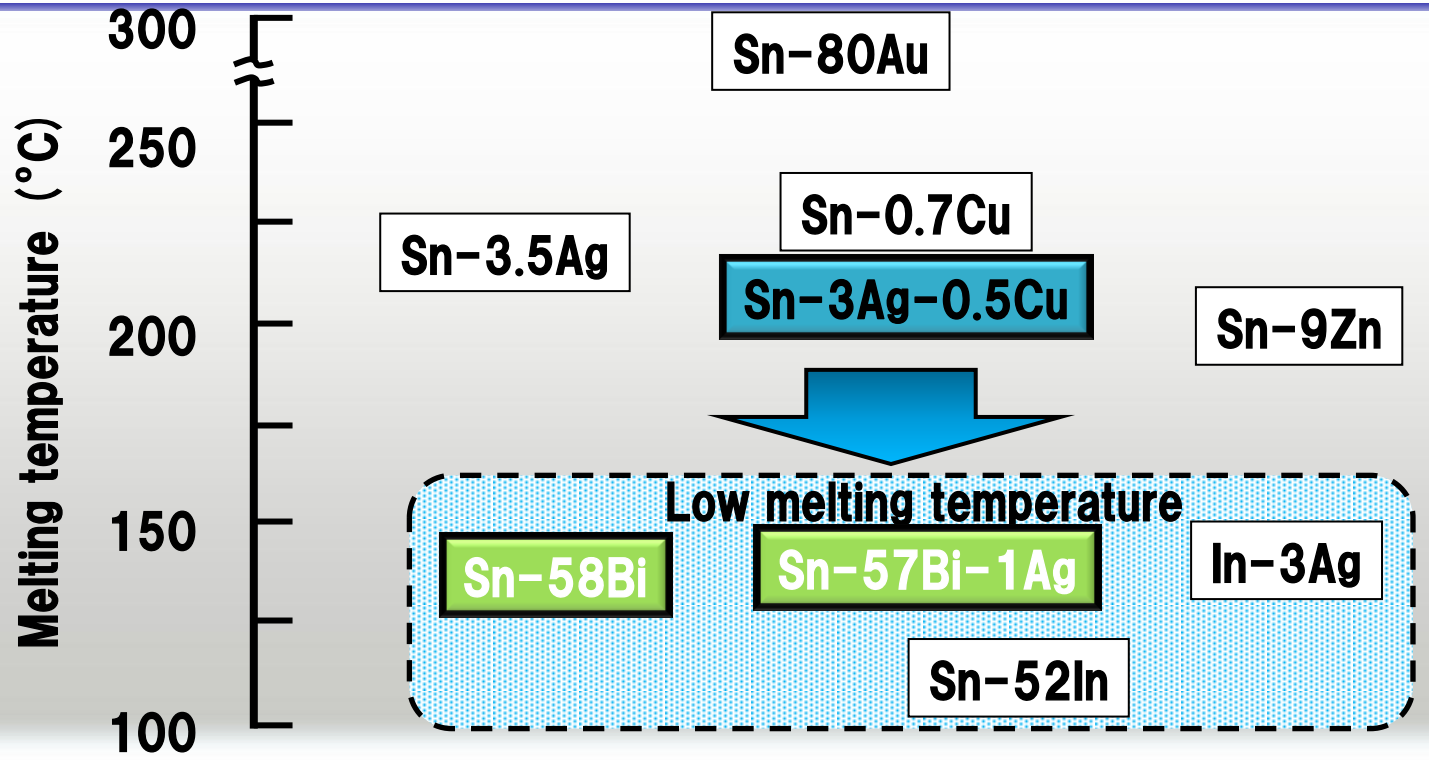
3. **Board mounting**
   Reflow Temperature control

Adopting Low-Temperature Soldering



Reflow Temperature

Candidates of Low-Temperature Solder



Eutectic Composition(mass%)	Melting point (℃)		Price
In-3Ag	144.0	Good	Expensive
Sn-58Bi(-1Ag)	138.0	Good	Reasonable
In-48Sn	120.0	Good	Expensive
In-34Bi	72.7	Too Low	Expensive

Issues of Sn-Bi eutectic Solder

Mechanical Characteristic

Bi : Hard / Brittle ⇒ Less Ductility

High Strain Rate Deformation ⇒ Brittleness Destruction

⇓

Shock Resistant Lifetime Shortening

Temporal Change

Stability Concern under High Temperature Operation

Coarsening of metallographic structure

Growth of reaction layer in the bonded interface

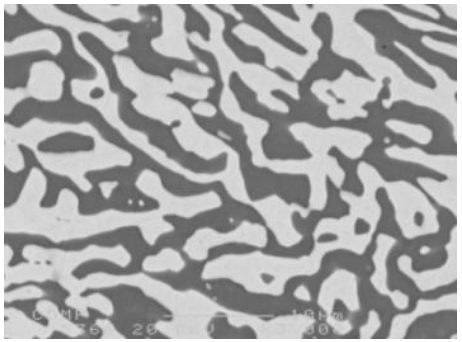
⇓

Improvement by Third element addition

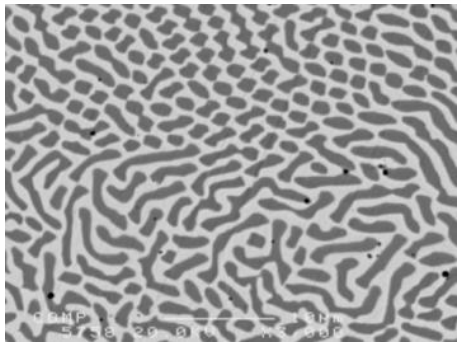
Charactristic Sn-Bi-Sb-Zn

Texture Miniaturization and Ductility improvement by Sb

Conventional Sn-Bi Solder

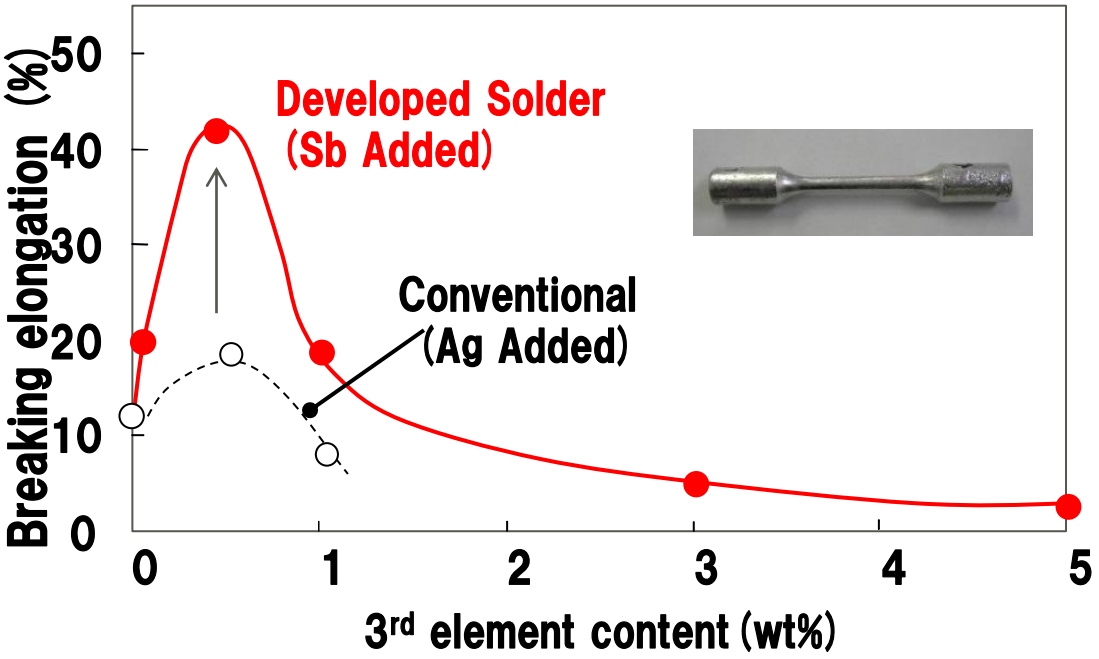


Developed Solder



10μm

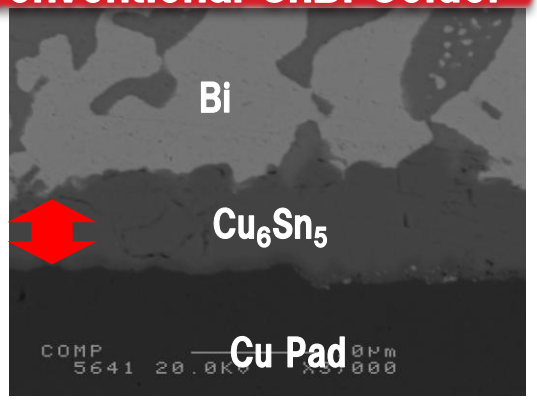
Test Temp. : Room Temp.
Strain Speed: 2×10^{-3} /sec



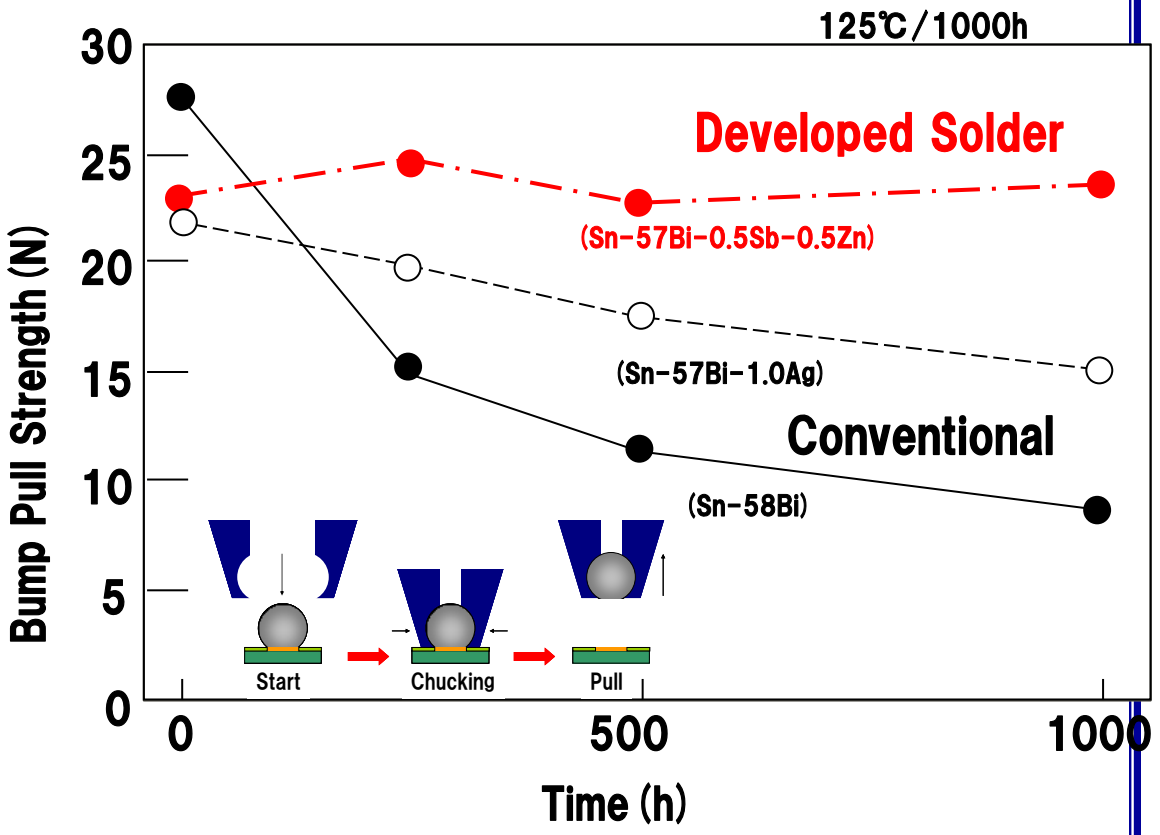
Charactristic Sn-Bi-Sb-Zn

Inhibition of Bi-rich layer constitution, interfacial reinforcement by Zn

Conventional SnBi Solder



Developed Solder



Joint Reliability was Successfully improved

Conclusion

- **The most effective structure to reduce warpage in our study was the application of prepreg materials only in both external layers.**
- **For Coreless Substrate structure, Stiffener assembly materials and appropriate processes enabled the same assembling level as conventional organic substrates.**
- **New Composition of Sn-Bi-Pb-Zn Solder enabling Low temperature reflow that realize low-reflow warpage.**

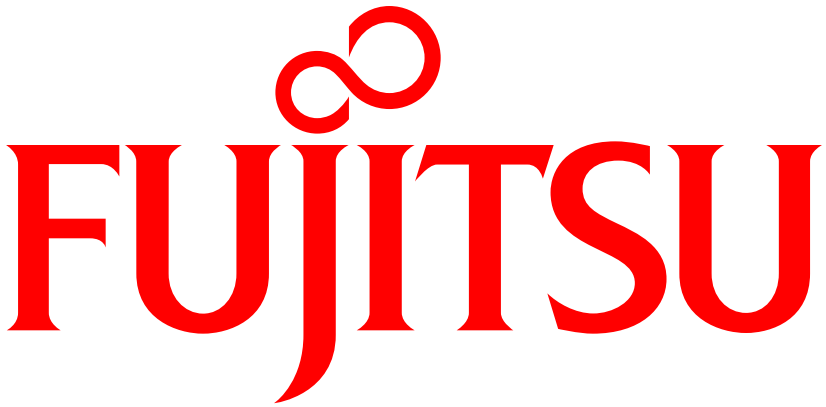
Daisuke Mizutani (Material Analysis)

Mamoru Kurashina (Material Analysis)

Seiki Sakuyama(Material Development)

Kenji Fukuzono (Package Structure Analysis)

Manabu Watanabe(Board Level Reliability)



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