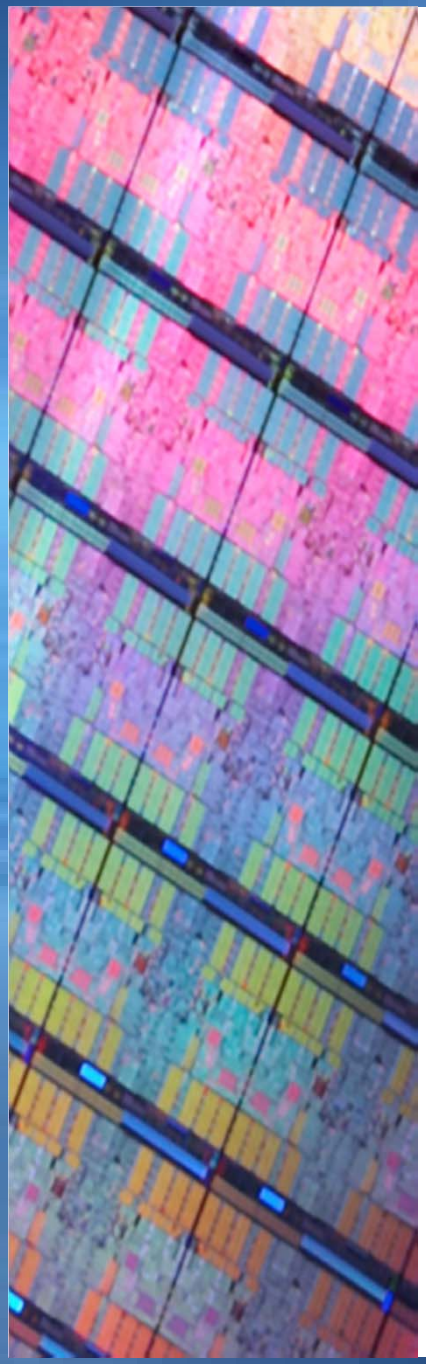
LUXTERA

Photonics Integration in Si P Platform

May 27th 2014

Fiber to the Chip



Overview

Introduction & Goal of Silicon Photonics

Silicon Photonics Technology

Wafer Level Optical Test

Integration with Electronics

Light Source for Silicon Photonics

Packaging of Silicon Photonics Devices

Reliability

Conclusions

Silicon Photonics Introduction

- **Silicon Photonics Technology:**
  - Silicon material system and processing techniques to manufacture integrated optical devices
  - Passive photonic functions + optical modulation + optical detection (+ electronic circuits)
  - Development started in early 2000s when sub 0.5 um lithography became available
  - There are many “flavors” of Si Photonics technology, hence it is difficult to make general statements
- **Goal of Silicon Photonics:**
  - Leverage from the IC industry:
    - Design infrastructure and methodologies
    - Wafer manufacturing and methodologies
    - Packaging & Test infrastructure and methodologies
  - Enable a very high level of integration:
    - Increased functionality and density
    - Simplification of optical/electrical packaging & test

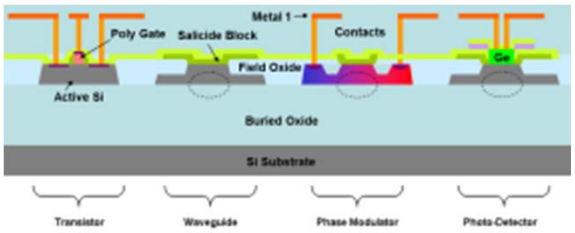
} **REQUIRES VOLUME TO BE MEANINGFUL!**

- **Silicon Photonics Applications:**
  - Most silicon photonics applications are in the area of high-speed communications
  - Also significant efforts emerge in the area of biochemical sensing and sensor applications in general

Silicon Photonics Process Technology & PDK

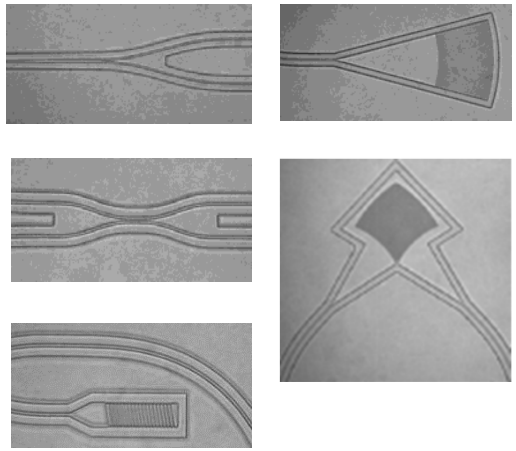
WAFER MANUFACTURING

- SOI wafer
- Litho and etch of photonic structures
- Implants for active devices
- Ge selective Epi for integration of
- Standard BEOL
- Silicon Photonics Foundries:
  - Freescale: mature
  - ST: in qualification



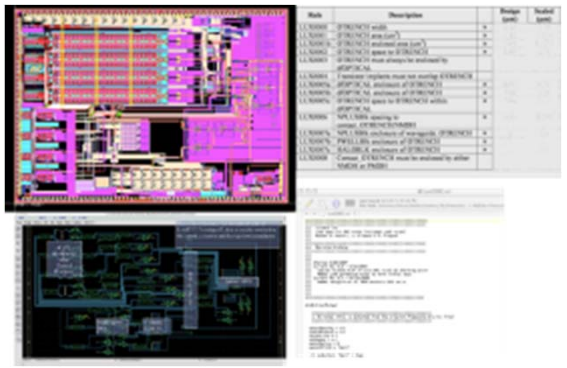
DEVICE LIBRARY

- Passives: waveguides, DC, Y-junctions, WDM
- Light couplers for fixed and uncontrolled polarization
- Phase Modulators
  - High-speed phase modulators
  - Low-speed phase modulators
- Waveguide Photo-detectors:
  - High-speed photo-detectors
  - Monitor photo-detectors



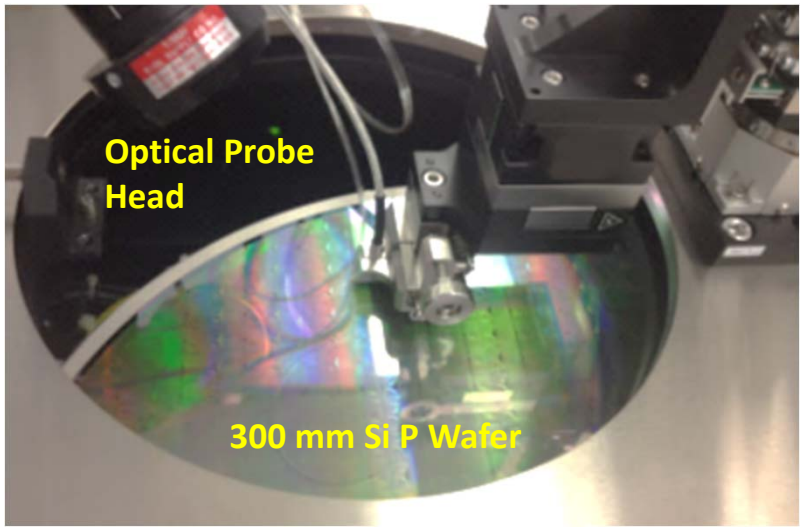
DESIGN INFRASTRUCTURE

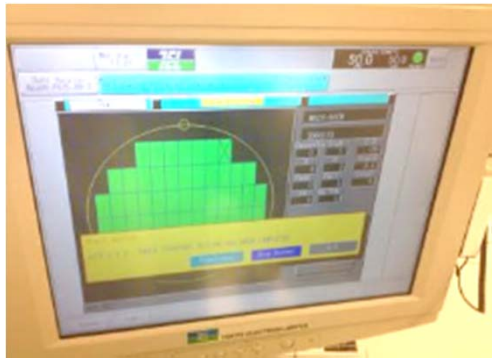
- Cadence based integrated design flow
- Device library with behavioral models and process corners
- Automated Layout
- E-E, O-E, O-O LVS deck w. extraction
- E-E, O-E, O-O DRC deck
- End-to-end simulation capability at PVT corners
- Very similar design environment as electronics

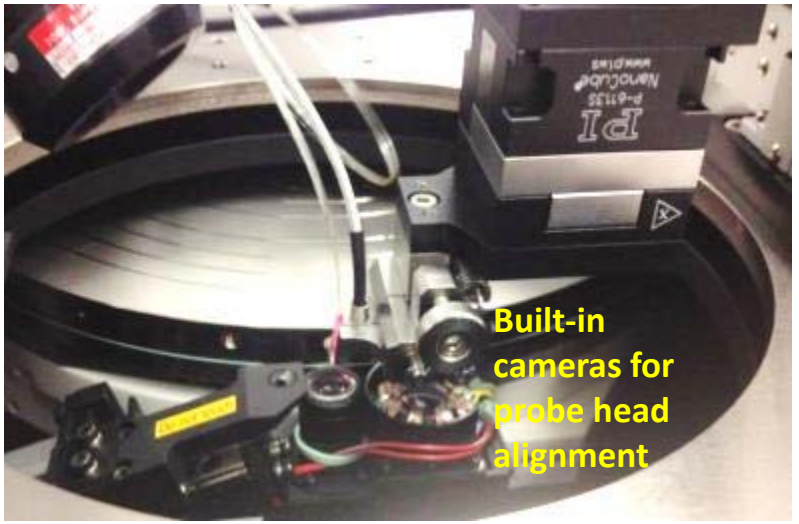


Silicon Photonics Wafer Level Optical Testing

- Based on industry standard TEL Precio prober
- 200 and 300 mm Silicon Photonics wafer testing
- New optical probe-head designed by Luxtera
  - Easy planarization/alignment and fast motion
- Easy test on single wafers, full cassette & FOUPs
  - Faster, less operator-intensive alignment procedure using prober cameras
- 4X faster than previous solution for optical sort
  - New method for FA-to-device alignment, optimized data transfer
- Optical test capability: Gauge R&R: 0.1 dB
- Wafer-scale testing is a work horse for manufacturing and development: Operates ~24/7

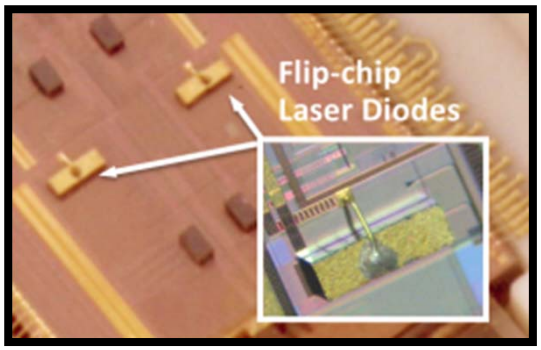


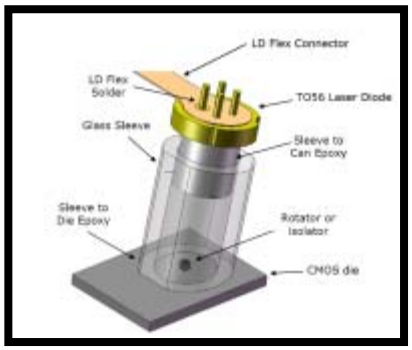


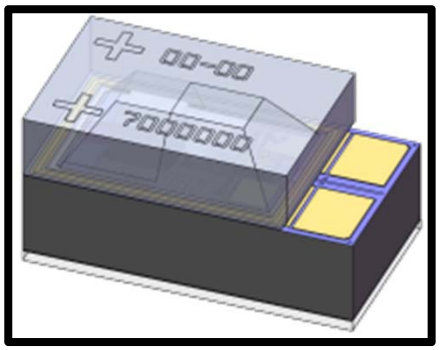


Light Source for Silicon Photonics

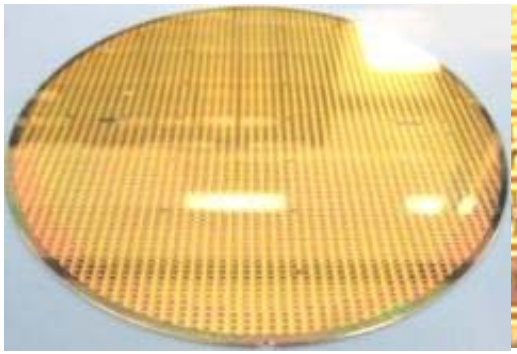
- Most transceiver applications need the light source to be integrated with the Si P die
- Si Photonics offers ability of using a remote light source
- Many types of light sources were explored, finally we settled with a standard InP laser diode in a silicon micro-package

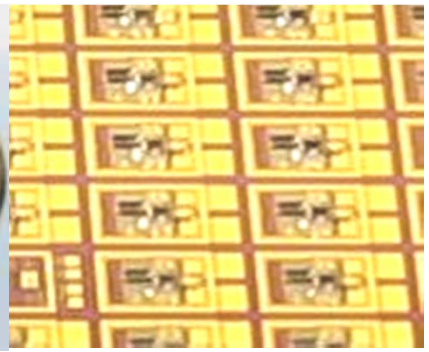






- Incorporates many “lessons learned”:
  - Use a mature InP laser diode
    -> excellent reliability
  - Include an isolator
  - Use efficient coupling scheme into die
  - Wafer level assembly, packaging and test
  - Established burn-in methods





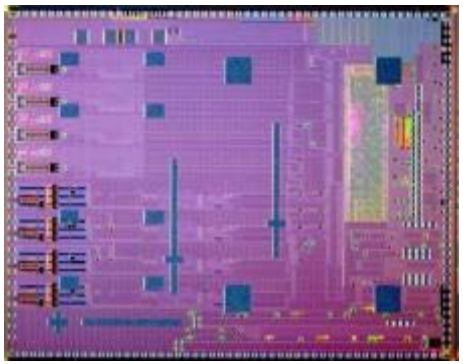
Silicon Photonics: Integration with Electronics

Monolithic integration photonics & electronics

- Single chip solution
- In some cases lowest parasitics between photonic and electronic devices
- More complex manufacturing process (interactions)
- In some cases not area efficient
- Scaling to advanced electronic node is very expensive

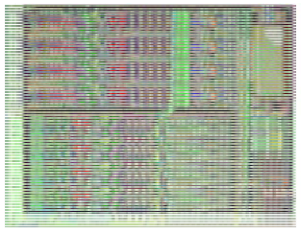
Hybrid integration photonics & electronics

- Multi-chip solution: face-to-face bonding
- Slightly higher parasitics between photonic and electronic devices (Cu Pi pads)
- Decoupling of photonics and electronics processes
- Efficient use of area (photonics doesn't take area on (expensive) advanced electronic node
- Flexible choice of process node electronic circuit
- Straight forward integration with electronic IP from partners



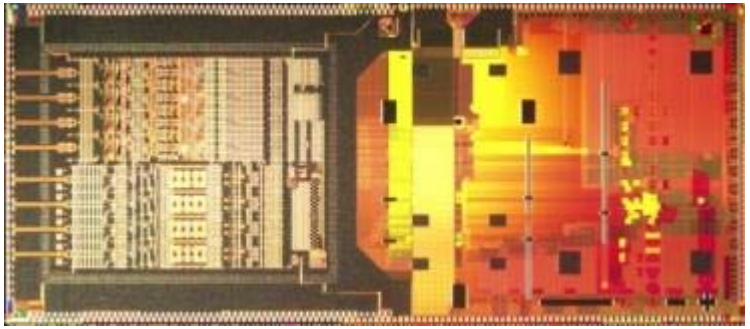
Monolithic electronic and photonic IC

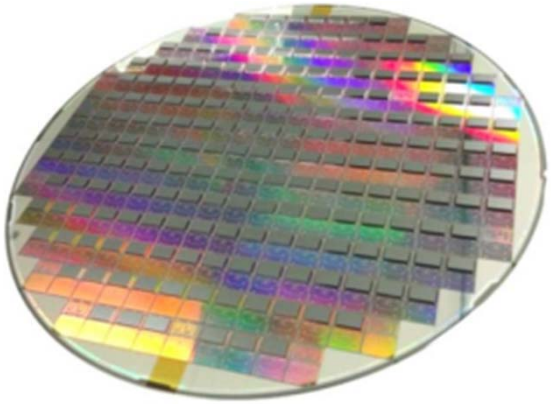
Electronic IC



Micro bump interconnect

Photonic IC





Wafer Level IC assembly

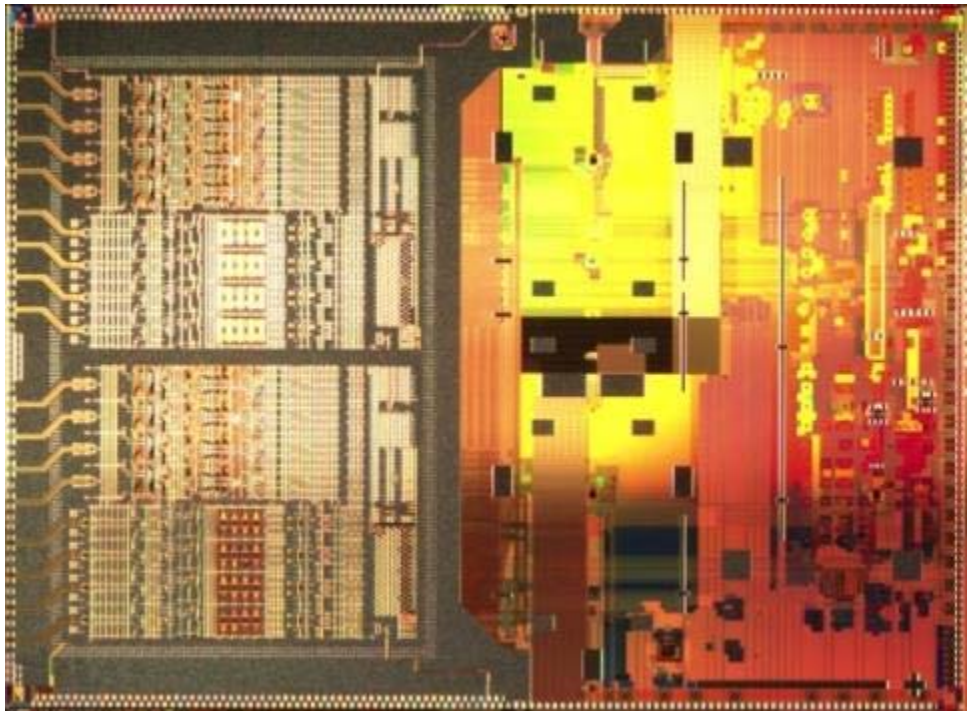
Example: Chipset for 8x28Gbps Transceiver

Electronic-die:

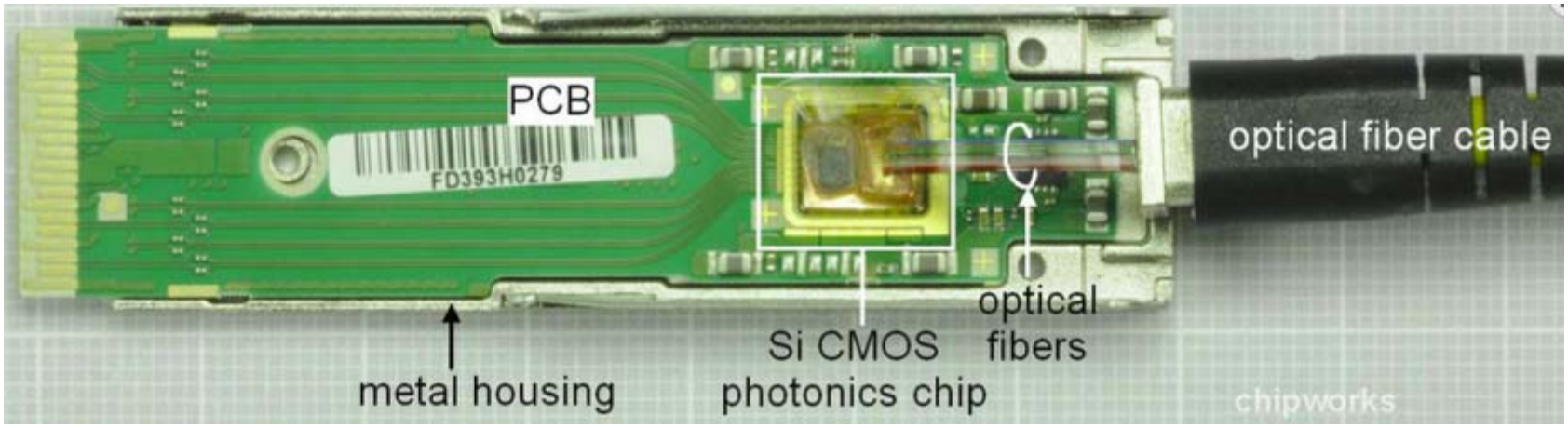
- 28 nm technology
- E-interface with by-passable re-timer & programmable signal conditioning
- BIST
- 2 wire communication
- Laser Driver
- MZI drivers & TIAs
- Digital core

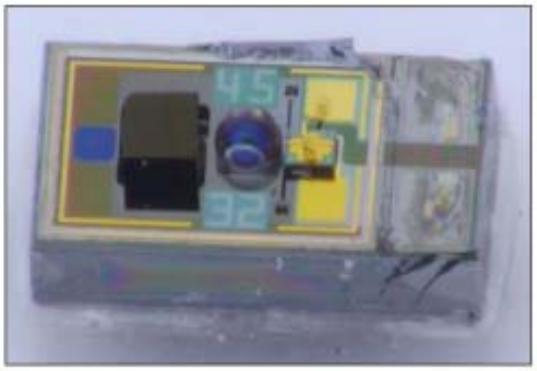
Photonic-die:

- MZIs
- Ge HSPDs
- Ge Monitor PDs for control and monitoring
- BIST
- Photonics assembly features

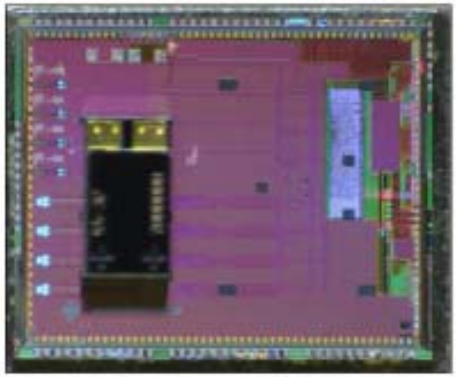


Packaging of Si Photonics based QSFP AOC

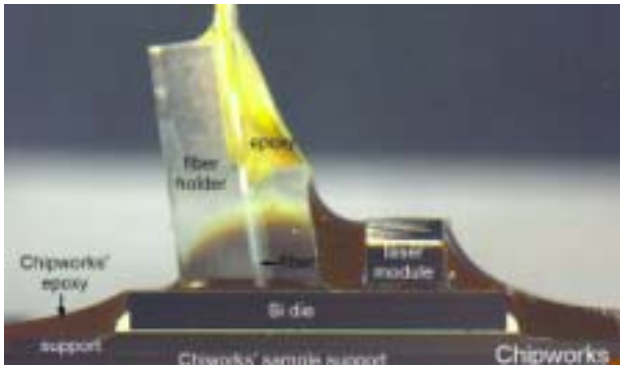




MEMS Laser Source



Silicon Photonic die



Reliability Assurance: Qualification Tests Example 1

System die qualification per JEDEC JESD47:

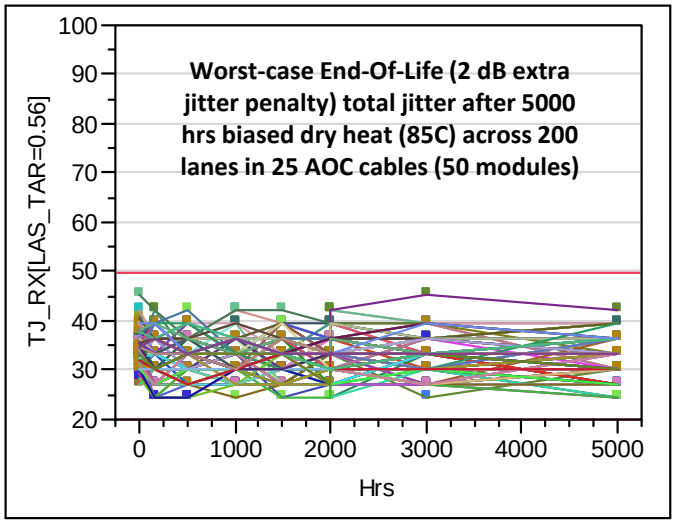
- Performed and passed with both 4x10 G and 4x14 G monolithic chipsets
- The qualification was primarily done on die level
  - Test vehicle consisted of Lotus die packaged in QFP Packages
  - Testing and test vectors same as die optical probe
- HTOL leg was also completed on full QSFP modules since they offered maximum high speed test coverage
- CMOS die functionality was comprehensively verified in 2 different test platforms:
  - Parametric test at room temperature extracting total lane jitter, criterion:
    Worst-case End-Of-Life (2dB extra link penalty) total jitter (PRBS31) meets spec.
  - Extended data-transfer test in an Infiniband switch-box at high temperature (70C) that ensures a BER < 10-14

STRESS	TEST VECHILE	CONDITIONS	SAMPLE SIZE (Number of lots/# per lot)
High Temperature Operating Life (HTOL)	Die	Tj >/ 125 C, Vcc >/ Vccmax, 1000hrs	3 lots/77 units
Hight Temperature Storage Life (HTSL)	Die	Ta >/ 150 C, 1000hrs	3 lots/25 units
Human body Model ESD	Die	Ta = 25 C, +/- 1000 V High-speed pins, +/- 2000V other pins	3 units
Charged Device Model ESD	Die	Ta = 25c, +/-250V all pins	3 units
High Temperature Operating Life (HTOL)	Cable	Tj >/ 108 C, Vcc=1.1xVccmax, 1000hrs	3 lots/50 units

Reliability Assurance: Qualification Tests Example 2

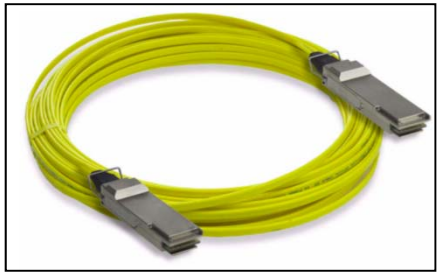
Optical transceiver qualification per Telcordia GR-468-CORE

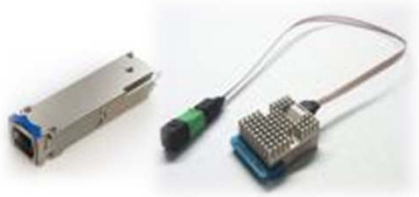
- Successfully passed full Telcordia qualification on two generations of Si Photonics based AOCs
- Tests included:
  - 2000 hrs Biased dry heat (85C) extended to 5000hrs for informational purposes
  - ESD testing on CMOS die followed by 1000hrs of biased dry heat (85C)
  - 1000hrs biased damp heat (85C, 85% R.H.) extended to 2000hrs for informational purposes
  - 100 cycles of thermal cycling from -40 to 85C extended to 500 cycles for informational purposes.
  - 50 cycles of biased thermal cycling with humidity
  - Human body model and Air & contact discharge ESD testing
  - Mechanical vibration and shock testing (with and without attached test board)
  - Fiber cable flex, twist & tensile strength testing
  - Durability of electrical connector
  - Insertion/extraction force measurements
  - Thermal shock testing (0 to 100C)

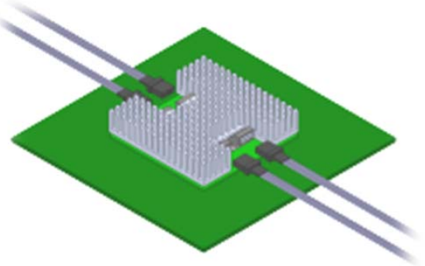


Conclusions

- Silicon Photonics has been **in production since 2009**, the first product was an 4x10 G AOC [now sold by Molex] for initially HPC applications
- **Cloud datacenter** build out drives single mode silicon photonics optical interconnect applications, where it is now already deployed
- Currently in development and qualification of Nx100G parallel single mode products (PSM4 MSA) in various form factors
- Work has already started on **400 G and associated low-cost duplex 100G transceiver products** using a combination of **higher baud rate, PAM-N and WDM**
- Power reduction drives closer integration, first by use of Embedded Optical Modules, later by direct integration with ASICs by a **Photonically Enabled Silicon Interposer** (addition of TSV to Si P flow)







Acknowledgements

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Thank you for your interest.