XILINX
ALL PROGRAMMABLE™

High Performance Memory in FPGAs

Industry Trends and Customer Challenges

Packet Processing & Transport

- > 400G OTN
- Video Over IP
- Software Defined Networks
- Network Function Virtualization

Wireless

- LTE Advanced
- Cloud-RAN
- Early 5G
- Heterogeneous Wireless Networks

Video and Vision

- 8K/4K Resolution
- Immersive Display
- Augmented Reality
- Video Analytics

Cloud and Data Center

- Acceleration
- Big Data
- Software Defined Data Center
- Public and Private Cloud

Industrial IoT

- Machine to Machine
- Sensory Fusion
- Industry 4.0
- Cyber-Physical
- Embedded Vision

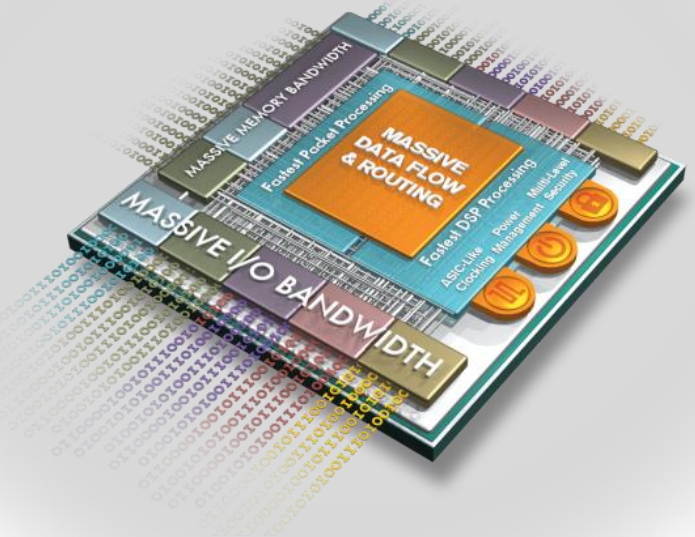
1 Performance & Power Scalability

2 System Integration & Intelligence

3 Security, Safety & Reliability

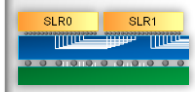
FPGA as System Enabler

VIVADO™
Co-Optimized

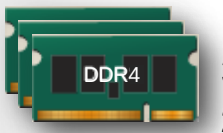


Security
AES-GCM mode,
greater key protection,
more authentication schemes

SSI Technology
Virtual monolithic die



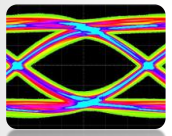
Memory I/O
30% higher data rates
20% lower power



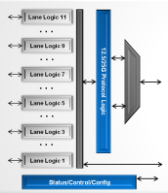
DSP
Wider multipliers,
fewer blocks per function

Block RAM
Hardened data cascading
Improved power, performance

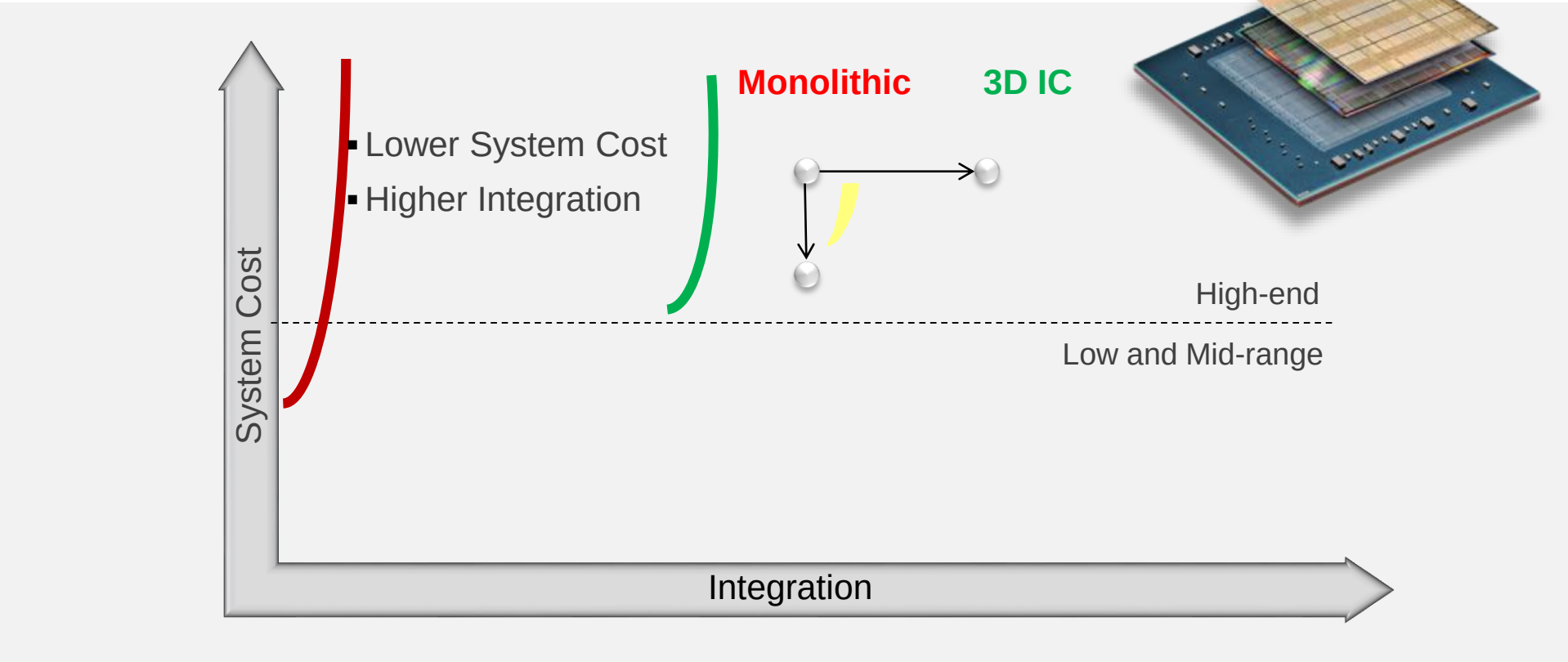
Transceivers
12.5G low speed grade
16G & 28G backplane
33G chip-to-chip



Integrated IP
100G Ethernet MAC
150G Interlaken
PCI Express Gen3



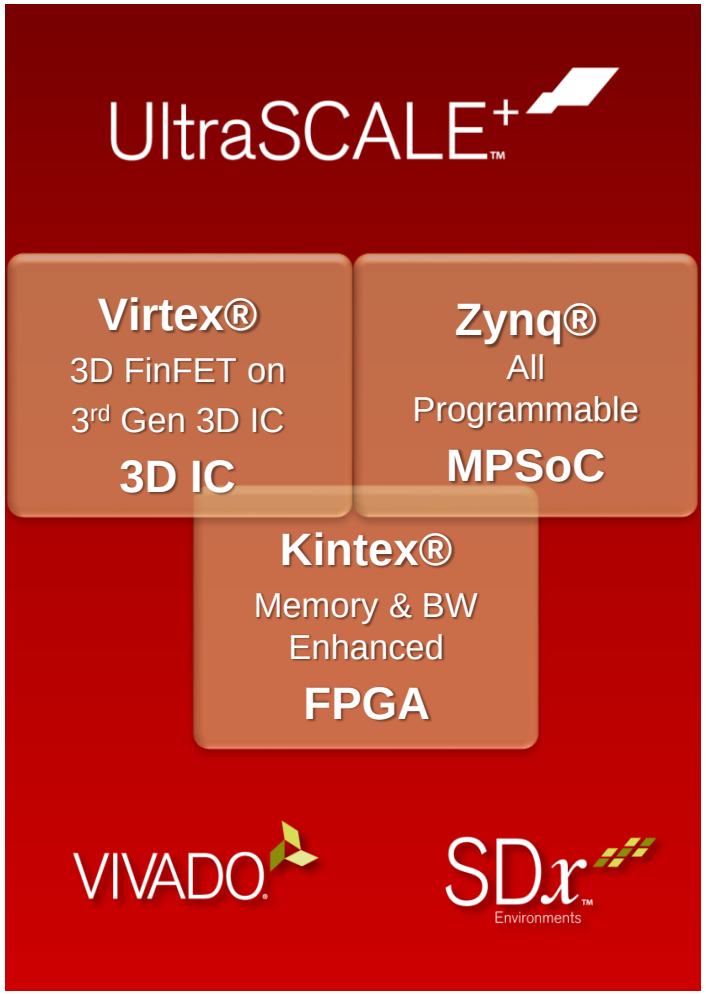
3D-on-3D: Another Industry First



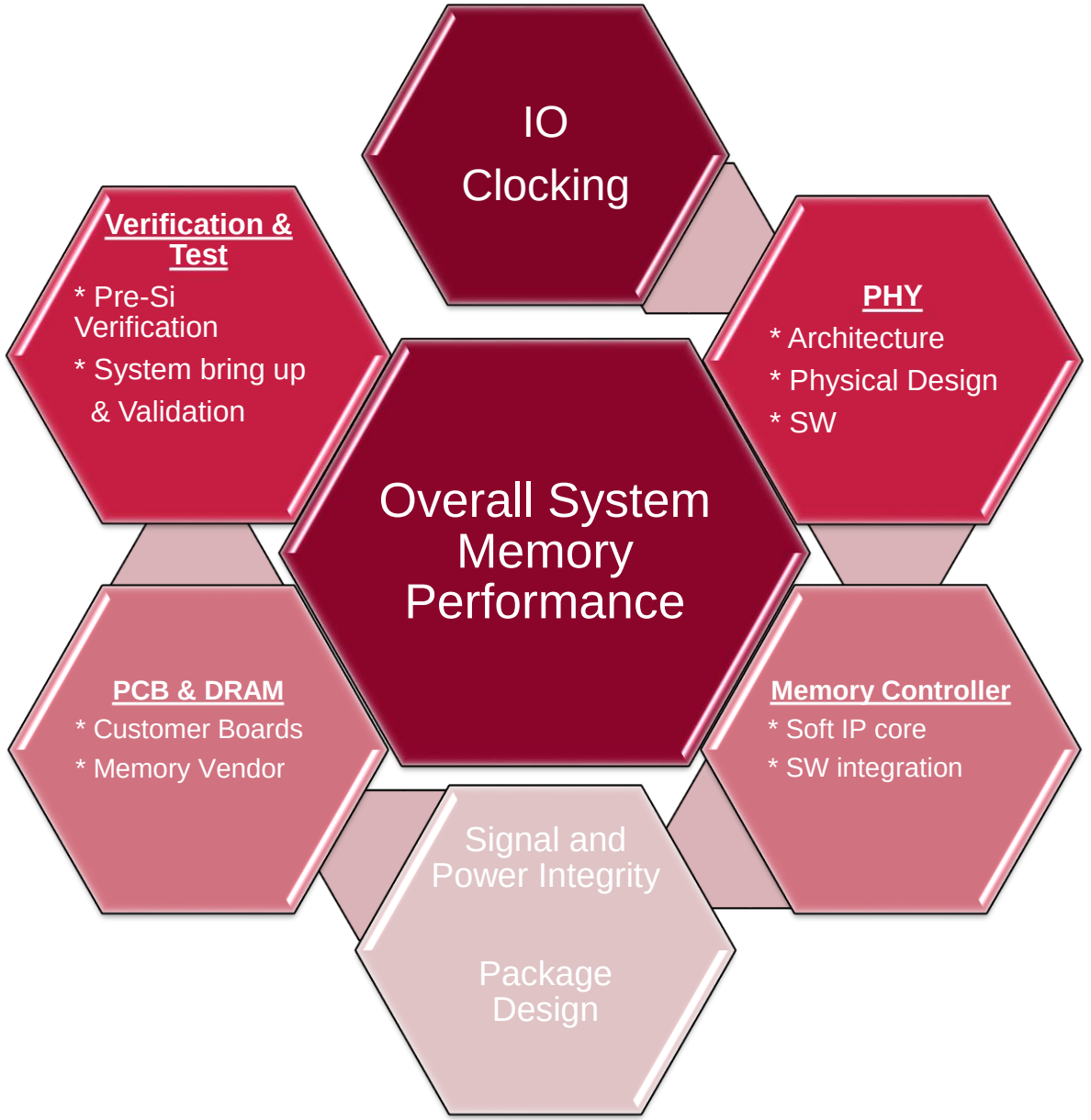
- First 3D Transistors on 3rd Generation 3D ICs
- 3D Transistors: Non-linear improvement in performance/watt over planar transistors
- 3D IC: Non-linear improvements in integration & bandwidth/watt over monolithic ICs

ASIC/CPU ←→ MPSoC

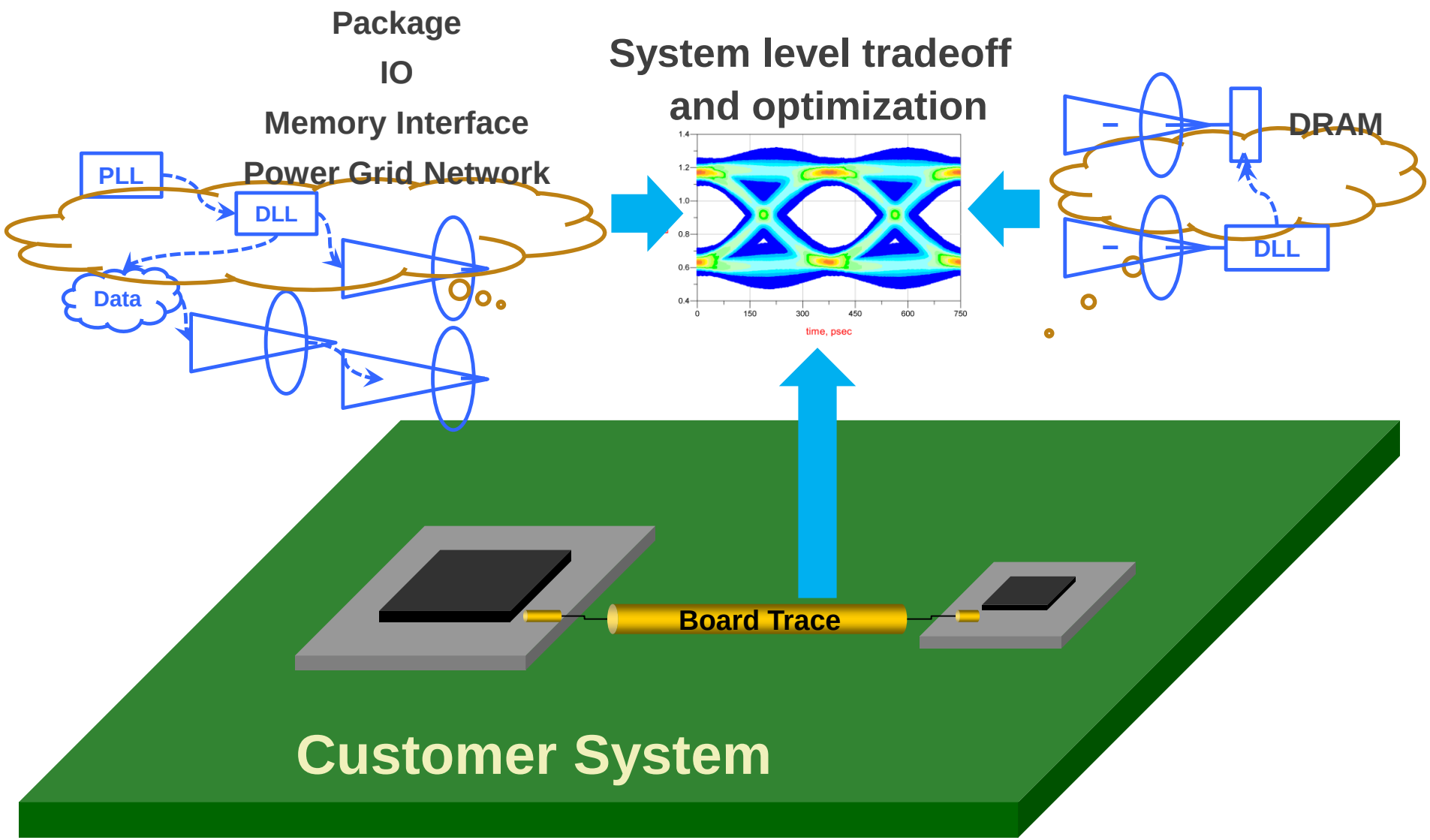
	ASIC/CPU	MPSoC
I/O	6x 2400 Mbps DDR4 (Xeon Phi)	5x 2667 Mbps DDR4 OR 9x 2400 Mbps DDR4
Serial Link	32 PCIe + 3 QPI (Xeon 7) 36 PCIe	104 32.75Gbps GTY Transceivers
Core Vector	Known pipeline and worst case power vector	Dependent on customer design
Clocking	Single trunk clock	Multiple trunk clocks; Highly configurable clocking
Package Supply Rails	Mostly < 10	> 10
Features	Limited features for specific applications	Packed with features to cover variable customer needs (DSP, Networking IP and etc)
Software	N/A	Programmable Circuit



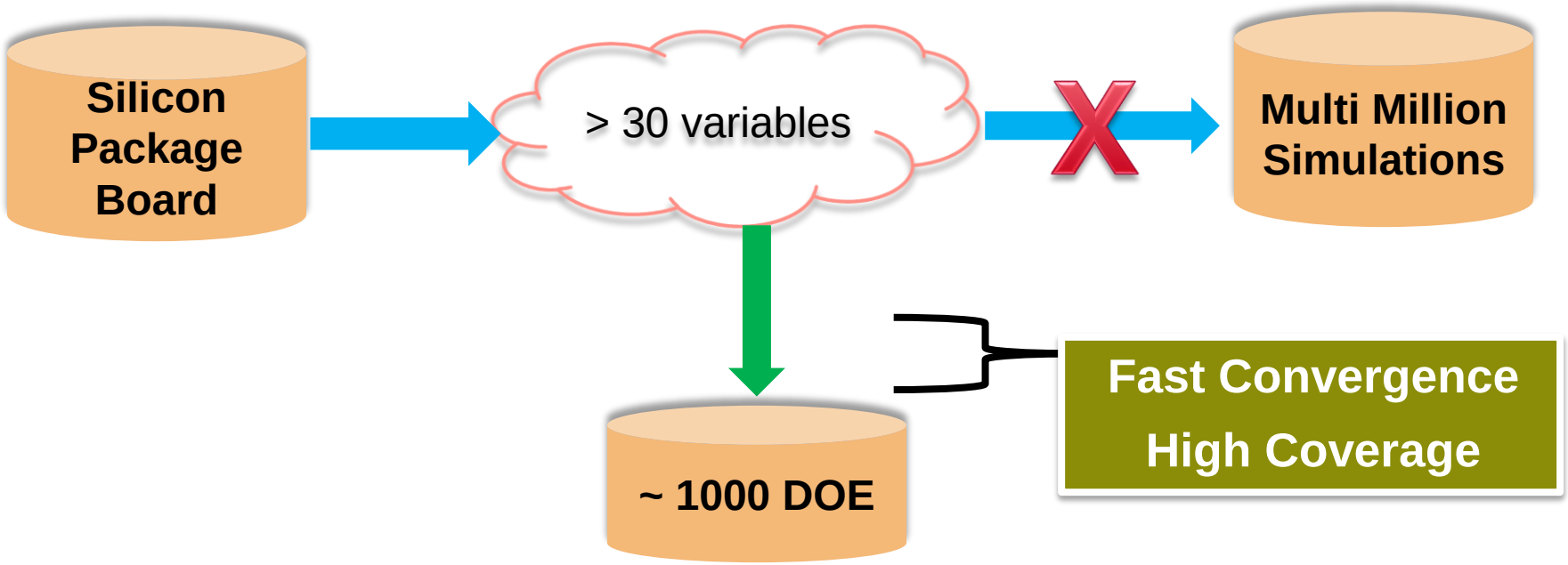
FPGA Memory System Overview

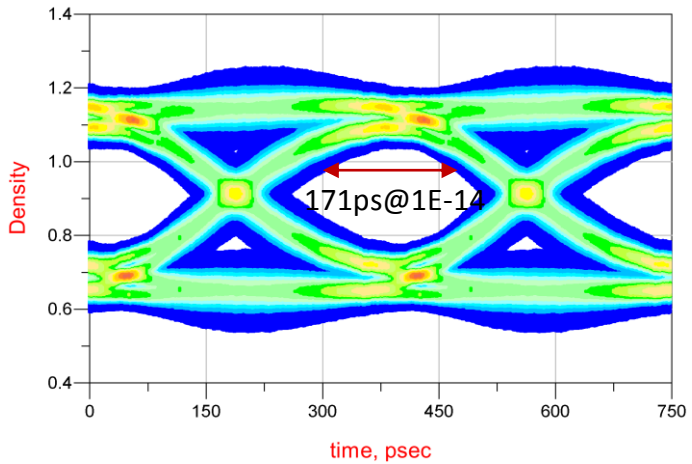


Memory is a *System Level* Optimization Challenge

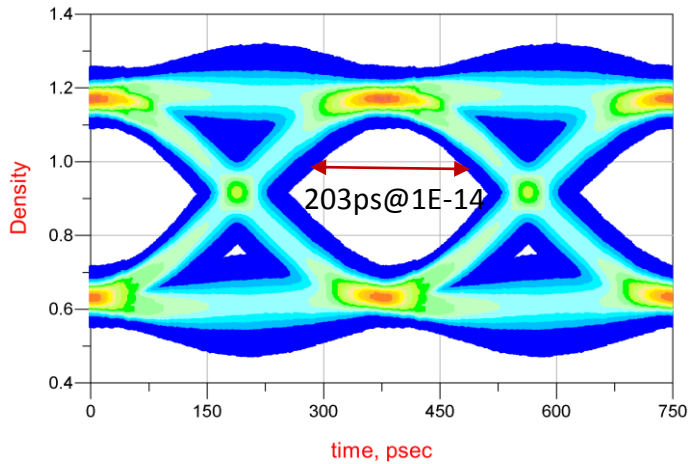


Critical Path DOE Optimization/Simulation





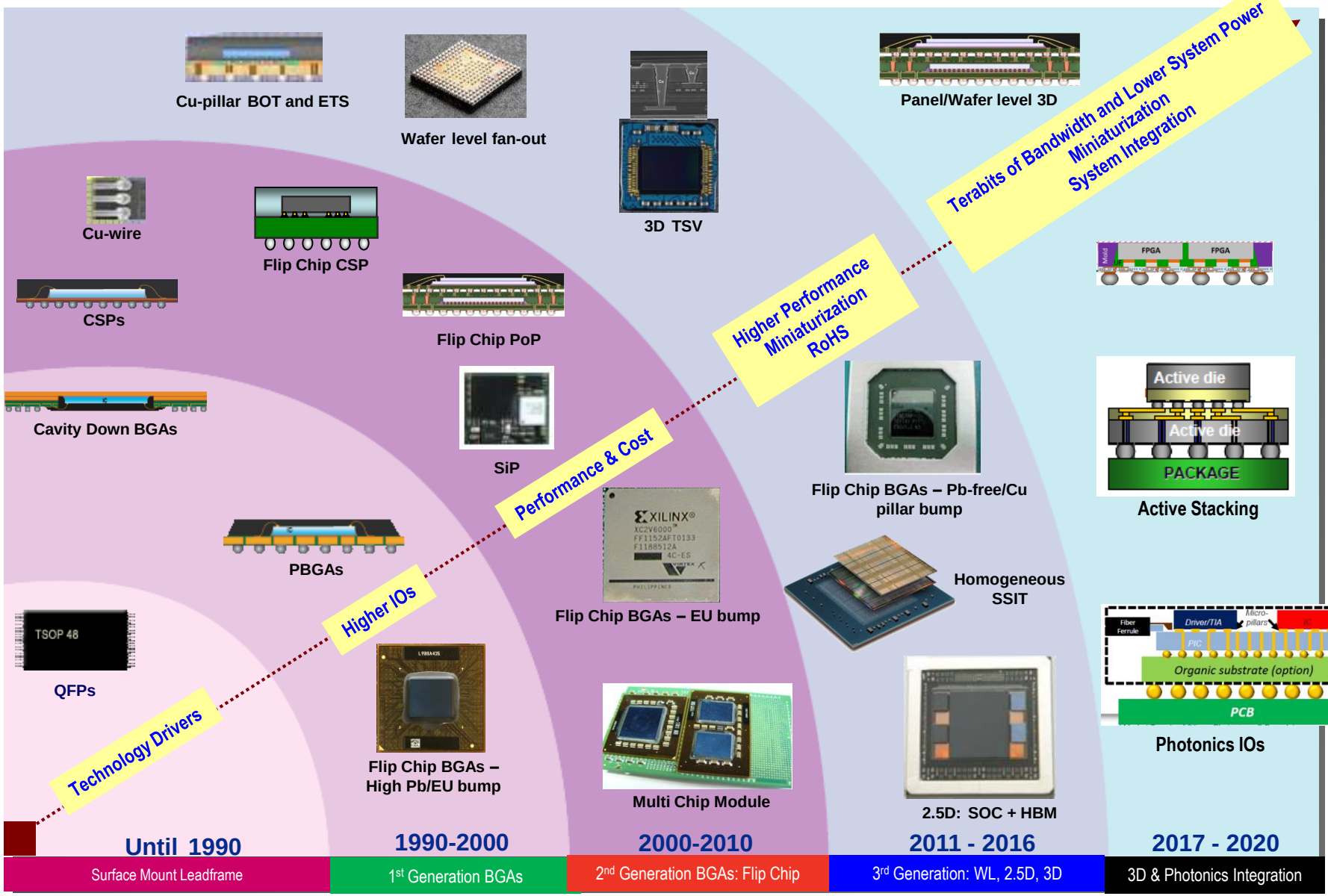
Before



After

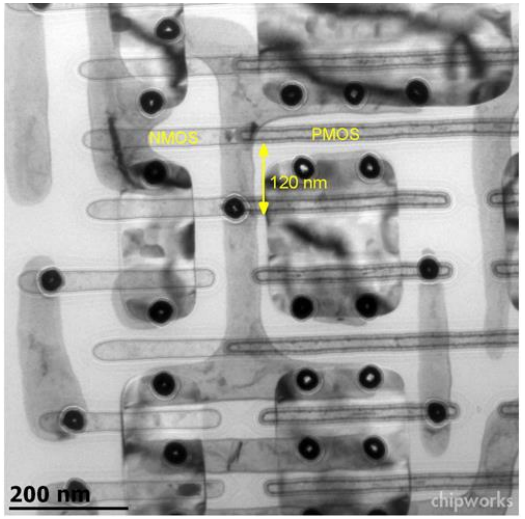
Packaging

A Headache or Opportunity for Innovation and Product Differentiation?

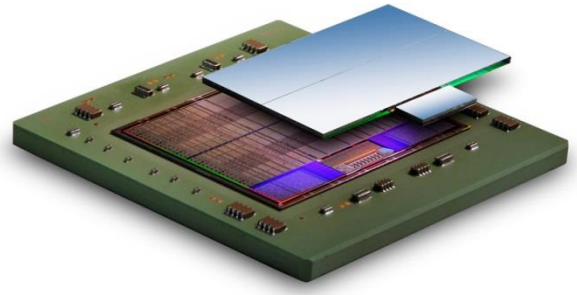


Nanometer to Meter and kHz to 33 Gbps

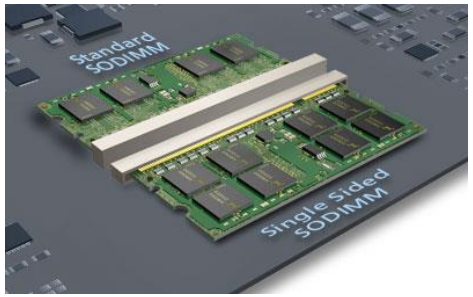
Transistor (nm)



Package (mm)

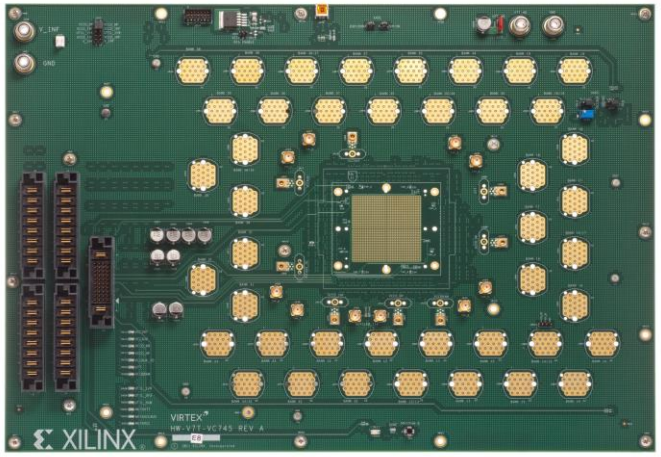


Memory

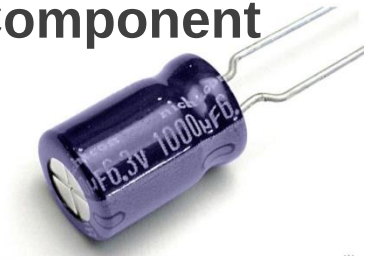


Connectors

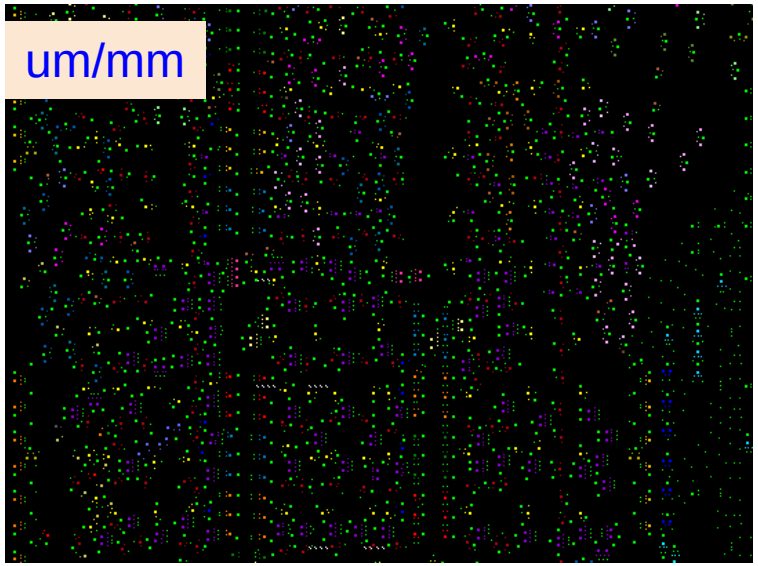
Board (meter/inch)

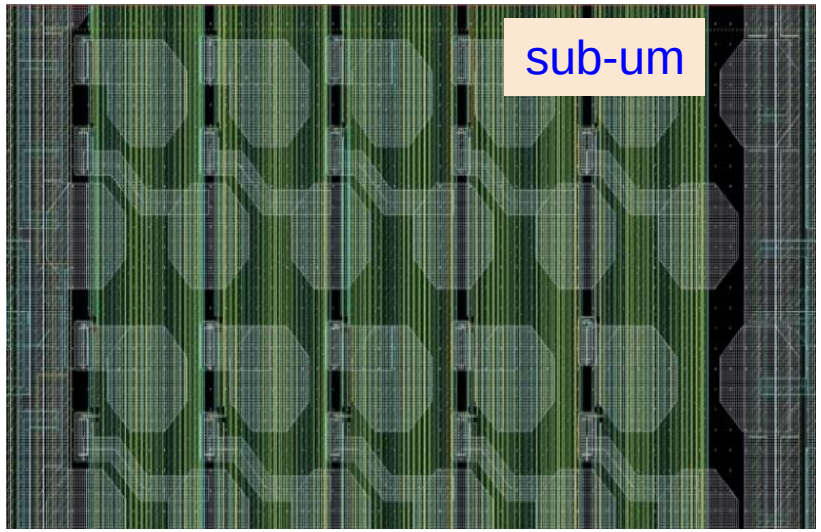


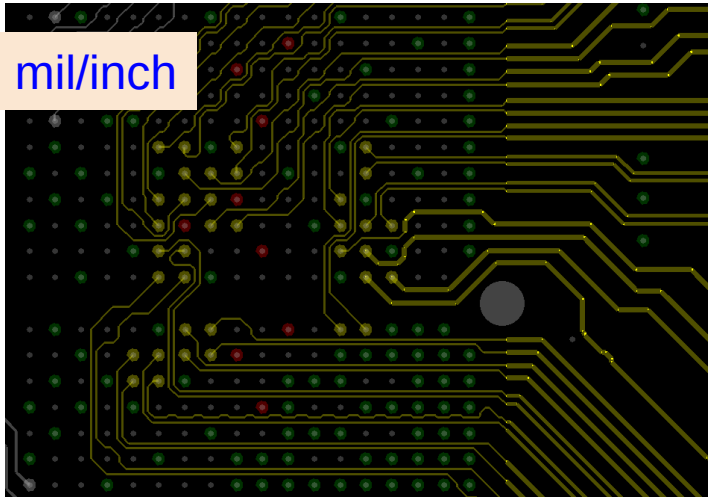
VR Component

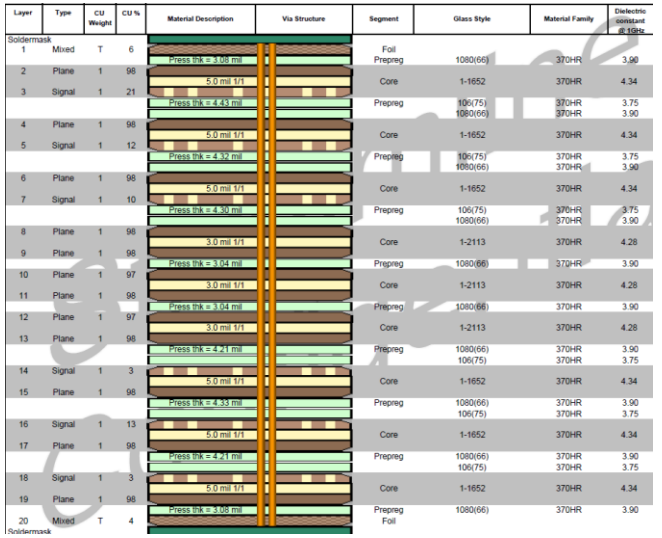


Physical Layout/Stack-up Example





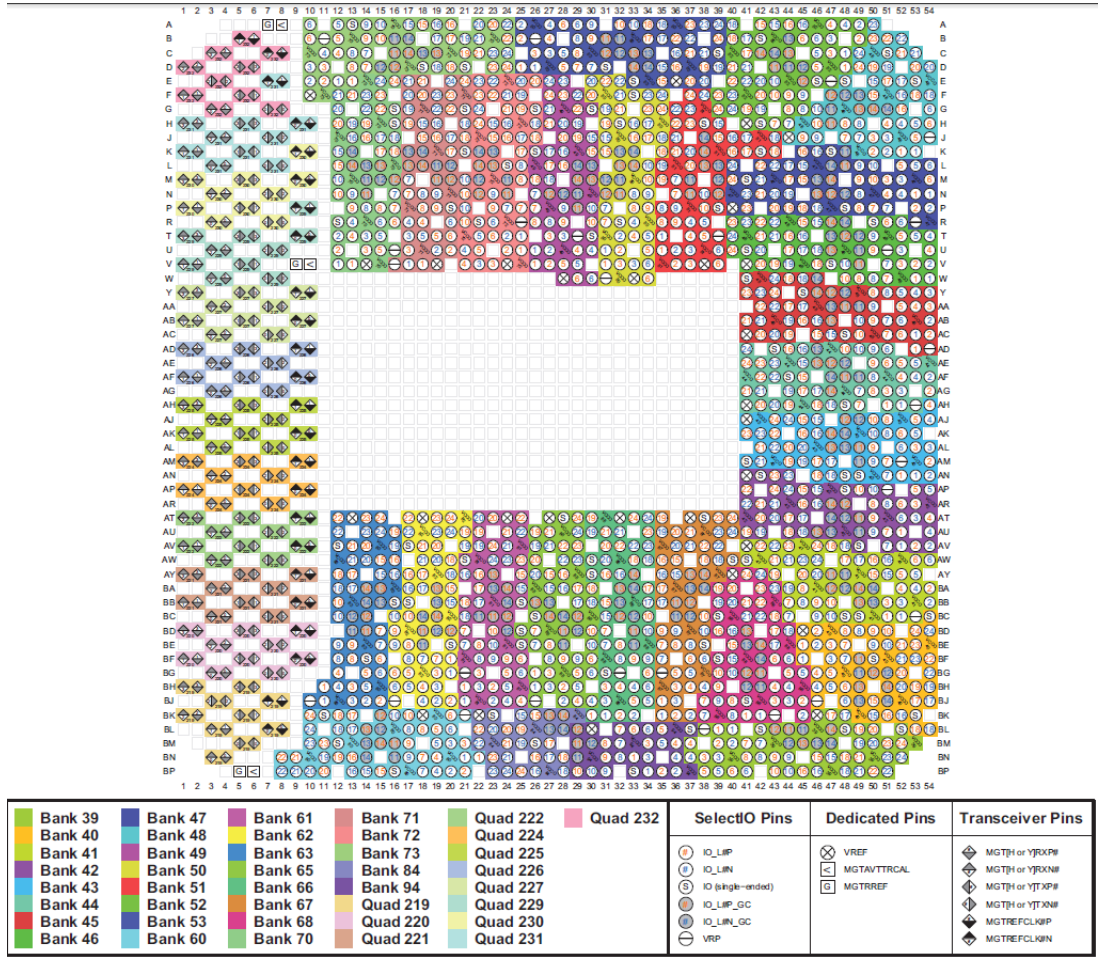


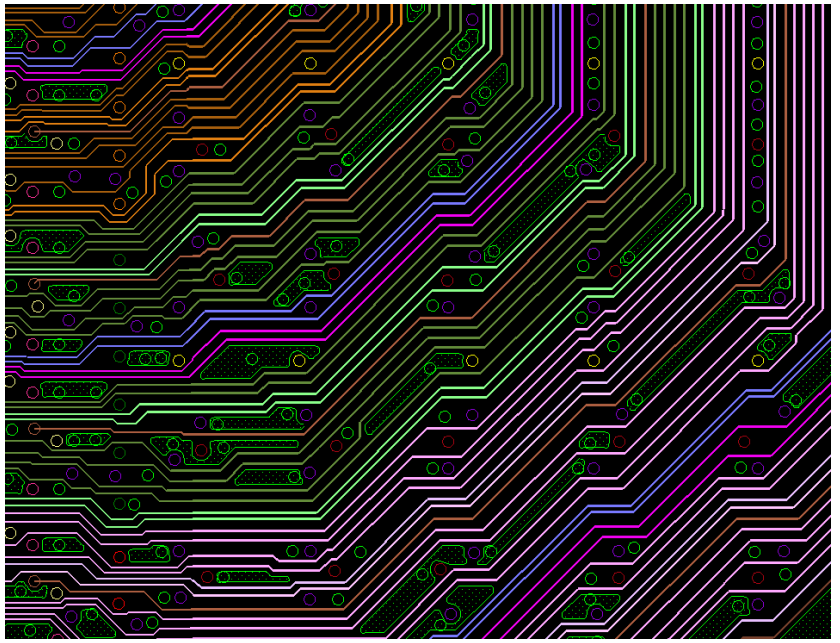


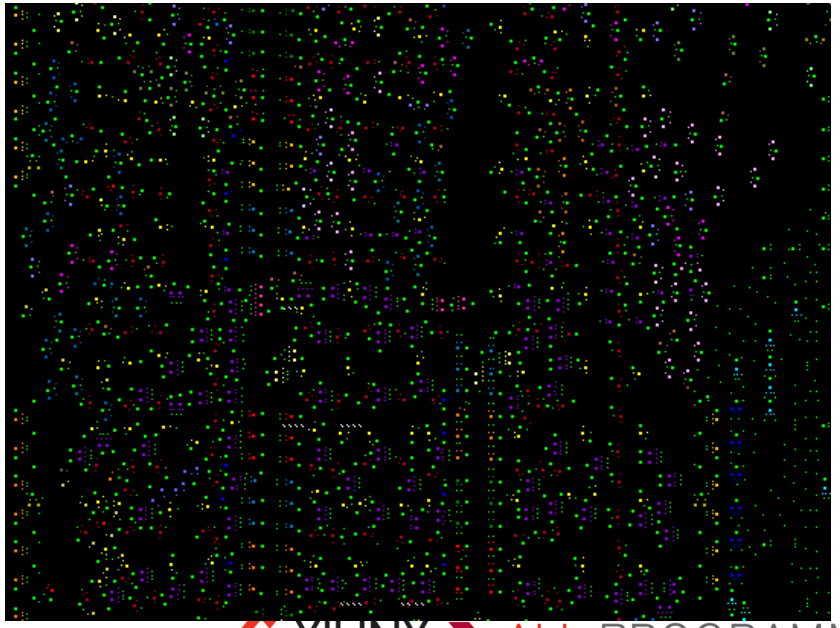
Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment	Glass Style	Material Family	Dielectric constant @ 1GHz
Soldermask									
1	Mixed	T	6			Foil			
				Press thk = 3.08 mil		Prepreg	1080(66)	370HR	3.90
2	Plane	1	98						
				5.0 mil 1/1		Core	1-1652	370HR	4.34
3	Signal	1	21						
				Press thk = 4.43 mil		Prepreg	106(75)	370HR	3.75
							1080(66)	370HR	3.90
4	Plane	1	98						
				5.0 mil 1/1		Core	1-1652	370HR	4.34
5	Signal	1	12						
				Press thk = 4.32 mil		Prepreg	106(75)	370HR	3.75
							1080(66)	370HR	3.90
6	Plane	1	98						
				5.0 mil 1/1		Core	1-1652	370HR	4.34
7	Signal	1	10						
				Press thk = 4.30 mil		Prepreg	106(75)	370HR	3.75
							1080(66)	370HR	3.90
8	Plane	1	98						
				3.0 mil 1/1		Core	1-2113	370HR	4.28
9	Plane	1	98						
				Press thk = 3.04 mil		Prepreg	1080(66)	370HR	3.90
10	Plane	1	97						
				3.0 mil 1/1		Core	1-2113	370HR	4.28
11	Plane	1	98						
				Press thk = 3.04 mil		Prepreg	1080(66)	370HR	3.90
12	Plane	1	97						
				3.0 mil 1/1		Core	1-2113	370HR	4.28
13	Plane	1	98						
				Press thk = 4.21 mil		Prepreg	1080(66)	370HR	3.90
							106(75)	370HR	3.75
14	Signal	1	3						
				5.0 mil 1/1		Core	1-1652	370HR	4.34
15	Plane	1	98						
				Press thk = 4.33 mil		Prepreg	1080(66)	370HR	3.90
							106(75)	370HR	3.75
16	Signal	1	13						
				5.0 mil 1/1		Core	1-1652	370HR	4.34
17	Plane	1	98						
				Press thk = 4.21 mil		Prepreg	1080(66)	370HR	3.90
							106(75)	370HR	3.75
18	Signal	1	3						
				5.0 mil 1/1		Core	1-1652	370HR	4.34
19	Plane	1	98						
				Press thk = 3.08 mil		Prepreg	1080(66)	370HR	3.90
20	Mixed	T	4			Foil			
Soldermask									

FPGA Package Technology Impact

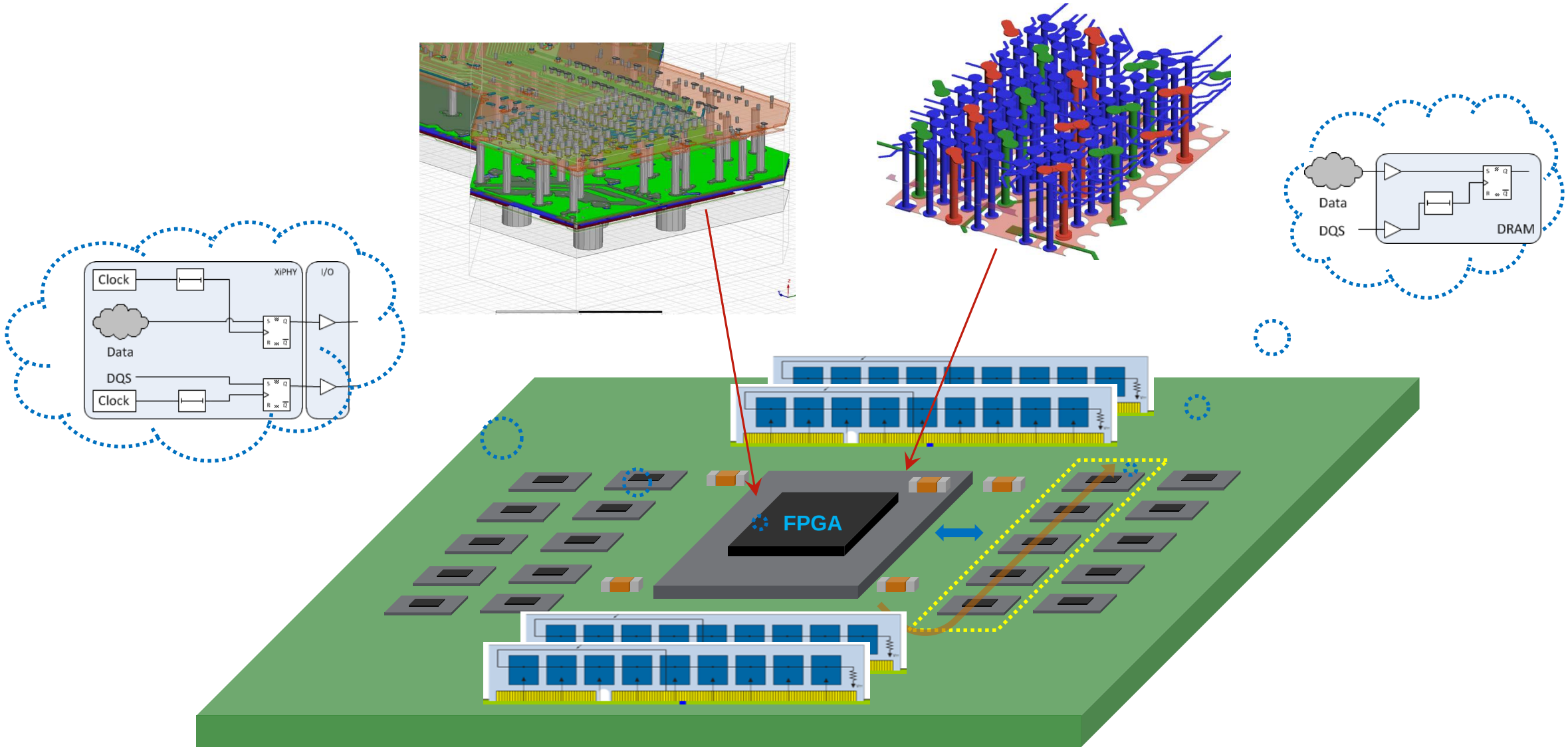
1404 HPIO pins



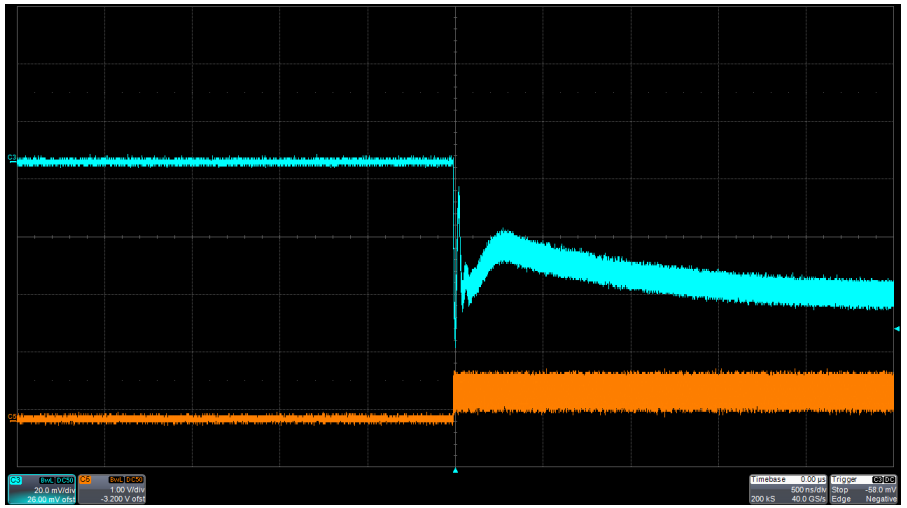


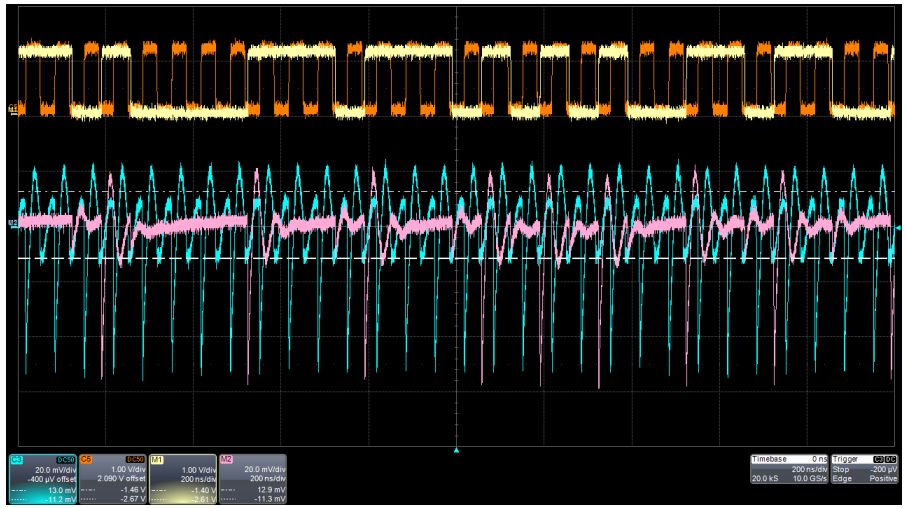


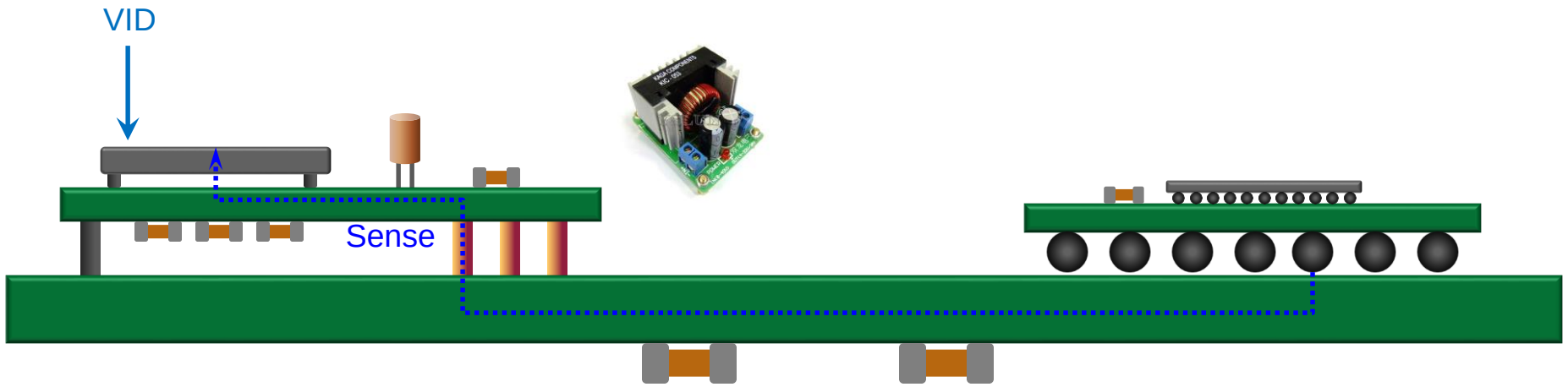
System Memory Channel Design



Power Delivery System Overview

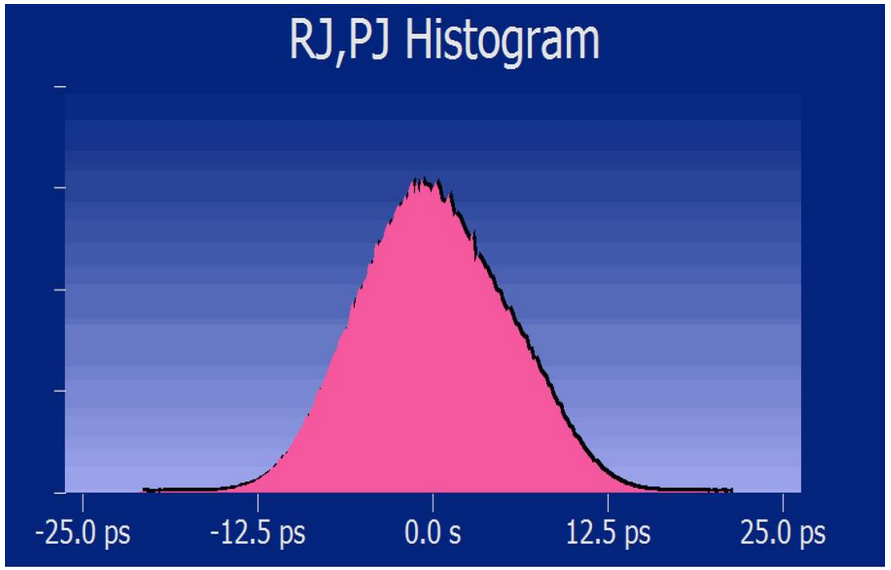




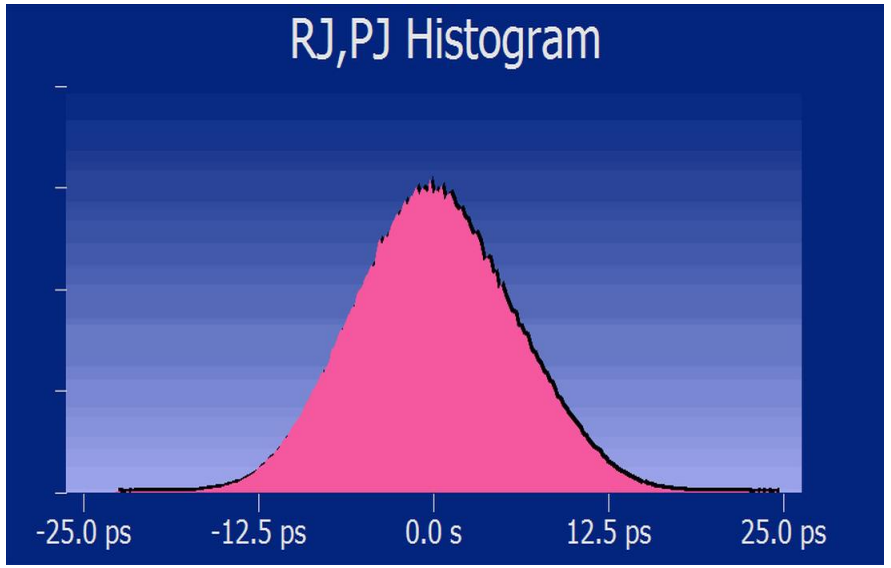


Power Delivery Result → Robust Timing Integrity

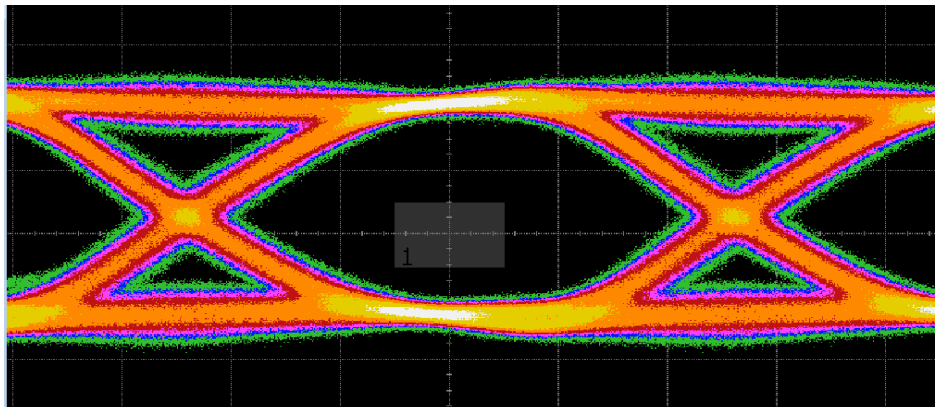
Quiet



Noise



Timing Integrity



FPGA Platform Memory Validation

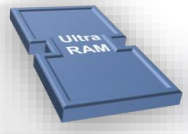
Enhanced at 16nm

Block RAM

Hardened cascading

Power-optimized silicon

New at 16nm

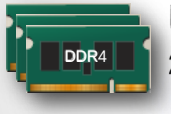


UltraRAM

Massive capacity for SRAM replacement

Enhanced at 16nm

3rd Generation SSI Technology



External Memory

2,400 Mb/s (20nm)

2,667 Mb/s (16nm)

Arch
PHY+IO+Fabric

Software + Tools

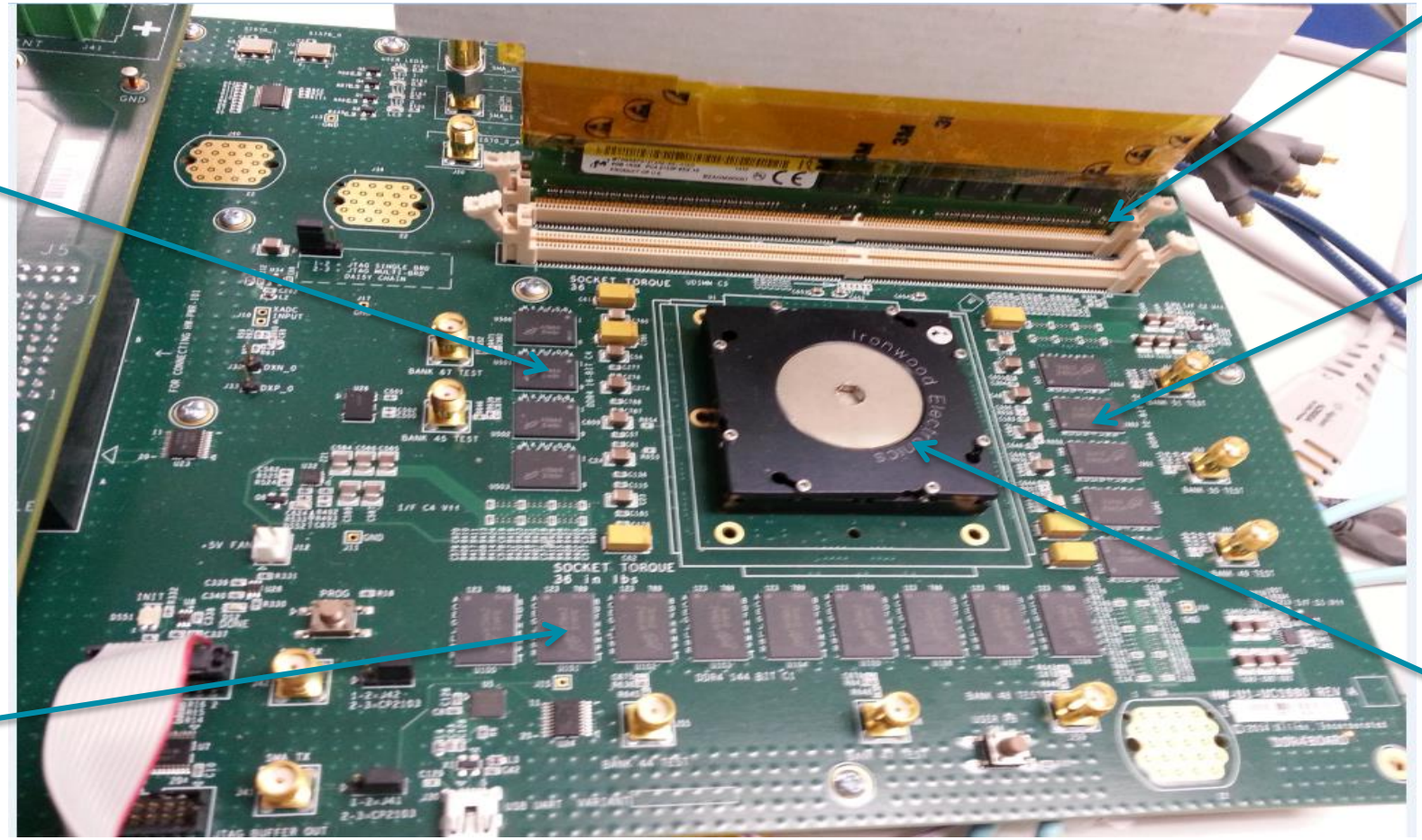
3D + 3D

Package

SI/PI

System Validation

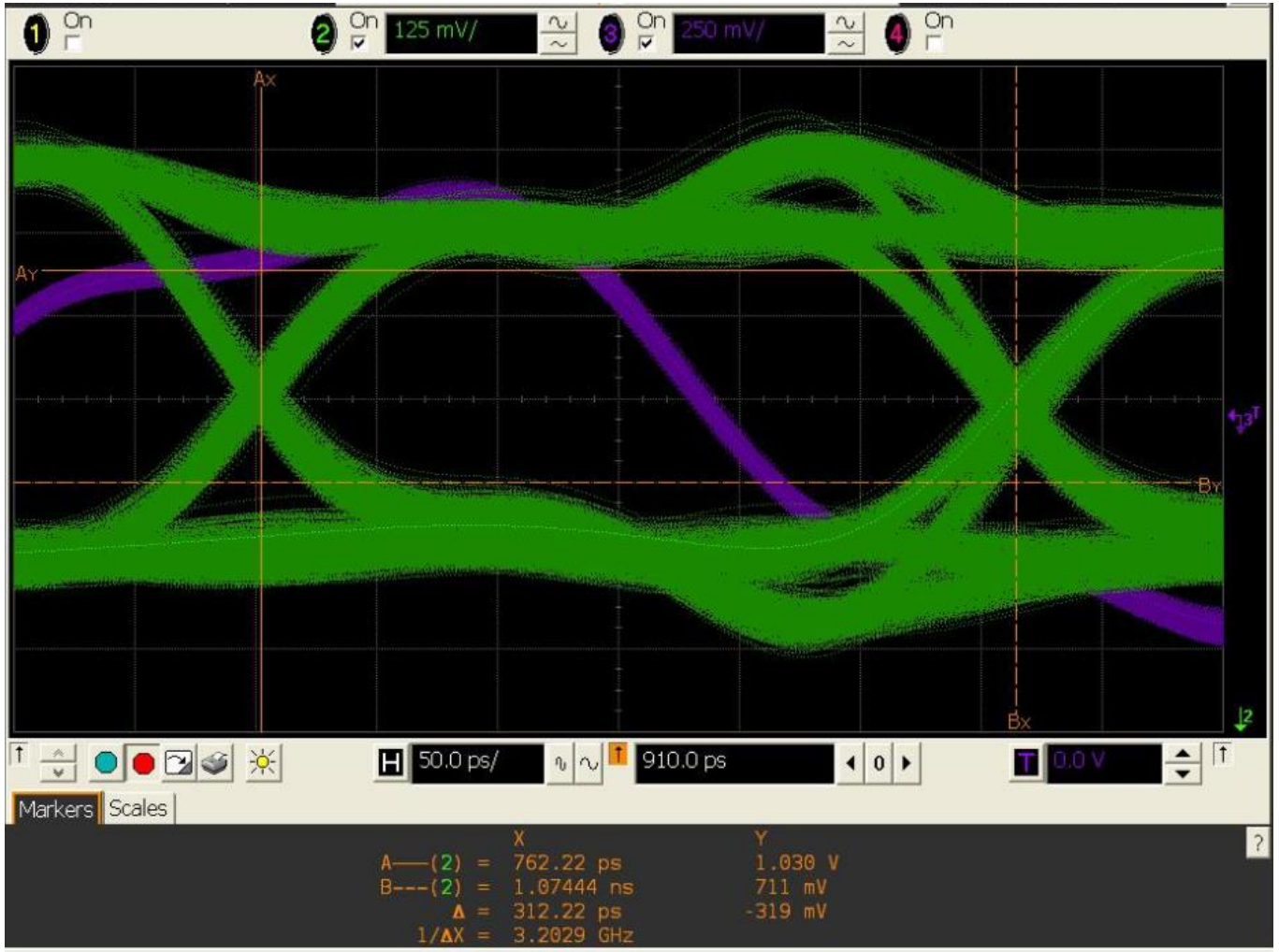
System Validation



DDR4 Memory Write Eye @ 3.2 Gbps

Probes Attachment

Write Data Eye Capture



Challenges

1 Terabyte OTN Switching

800G MAC-Interlaken Bridge

800G Data Center Interconnect

Mobile Backhaul
1 GHz eBand Modem & Packet Processing

Mobile Backhaul
112 MHz PtP MWR Modem & Packet Processing

Test & Measurement Instrumentation

24-Channel Radar
(Beamformer + Pulse Compressor + Doppler Filter)

8x8 100 MHz LTE Remote Radio Head

Dual-Channel Battery-Powered
Public Safety & Military Mobile Radios

Camera-Based Automotive
Driver's Assist Systems (ADAS)

4K Broadcast Cameras

Solid State Drives (SSDs) for Data Center

Video Conferencing

High-Performance Scalable
Programmable Logic Controllers (PLCs)

Q & A