Panel Fan-Out Manufacturing Why, When, and How?

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Scaling or just another FO Packaging Technology?

1) Panel Fan-Out Manufacturing is here for some time already for Embedded and Non-Embedded Packaging Technologies, Chip-First and Chip-Last

Manufacturing Infrastructure

- PCB (AT&S/ECP, Imbera/IMB, Schweizer Electronic/i²Board
- LCD (PTI/PFO, SPLI/PFO, Samsung/PFO, Nepes/nPLP, …)
- Build-up OSAT (J-Devices/WFOP, TDK/SESUB, RDL-First, A

- ➢ Many different formats;
- ➢ Lack of standardization;
- ➢ Design Feature Limits;
- ➢ Yield constraints.

2) The hot topic is: **Scaling of successful FOWLP Technologies to larger manufacturing formats; FOWLP = Embedded Packaging Technology (EPT)**

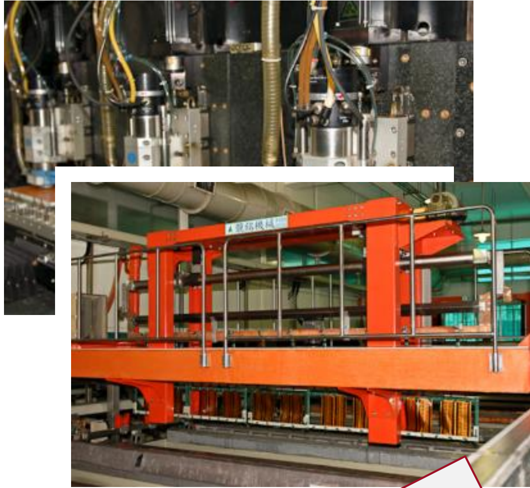
Manufacturing Infrastructure

- Semicond
- Solar Sen
- Silicon Fo

- ➢ EMBEDDING has Chip-First inherent in the technology;
- ➢ Interconnect Technology is Thin-Film RDL (no WB, no FC);
- ➢ Substrate is Moldcompound, or Inorganic Materials (Si or Glass);
- ➢ Interconnect btw die pad and package I/O is formed on die + substrate.

Customer demand:
- Same results (1:1 copy) at lower cost enabled by larger format;
- No additional FO technology, but transfer of construction & BOM.

Wafer- and Panel-Level Manufacturing Environment



IC-Substrate / P
Manufactu
Environ

Yield +

Classical OSAT
w/ Packagin
Backend
ronment

Yield ++

WLP OSAT
w/ Semicon
Fronten
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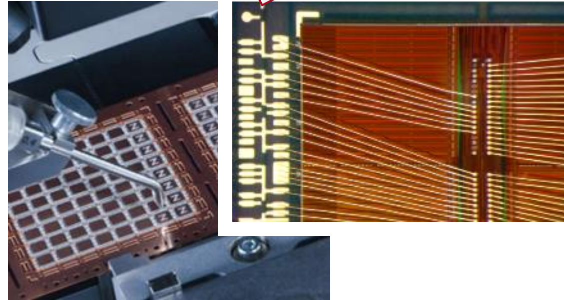
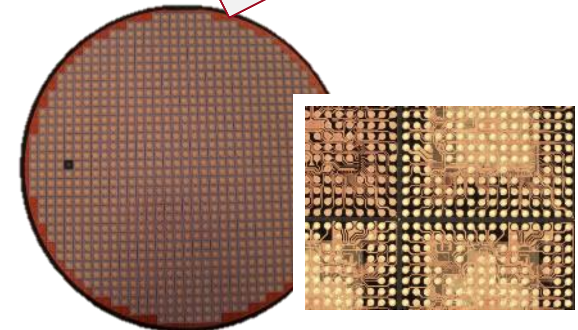
Yield +++





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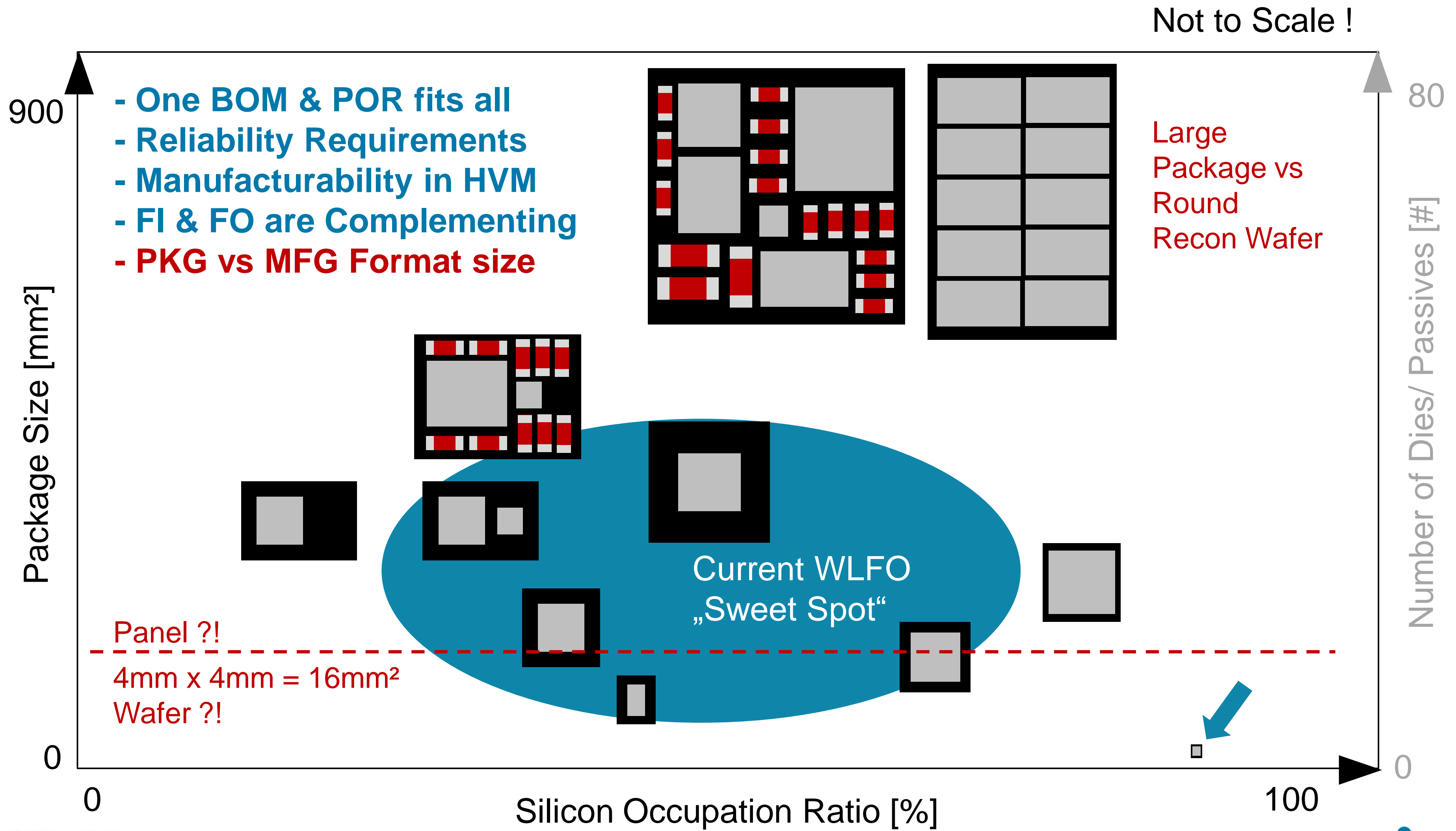
The FOWLP Scaling Dilemma / WLFO Platform Approach



Scaling or just another FO Packaging Technology?

- **Manufacturing Format Scaling is a pure cost saving topic w/o impact on:**

  - Package Construction;
  - Design Features;
  - Bill of Material (BOM);
  - Reliability and Quality;
  - Test results and Yield levels.

FOWLP over FOPLP

- for project start phase
- for fast samples
- for small and medium volumes
- for complex WLSiP, WL3D products

- **Changes to Package Construction and BOM result in modified Packaging Technology and cannot be considered as Manufacturing Format Scaling**

- **Economic Aspects have to be factored into the equation:**

  - FOPLP has to be affordable for the industry (investment, volume, 2nd source, complexity, yield)
  - Deliver components to customer. Components packaged in **fully loaded high yielding** FOWLP line can be cheaper than components packaged in **half-loaded low yielding** FOPLP line !!!

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The FOWLP Scaling Dilemmas / What is it about?

Dilemma 1:

FOWLP manufacturing format scaling to FOPLP has technical challenges;
If solved by change in technology → Another additional "Shade of Fan-Out".

Dilemma 2:

Volumes for FOWLP are coming from high density and Package Stacking solutions e.g. TSMC`s InFO PoP → Requires Semiconductor Environment = Wafer-Level.

Dilemma 3:

FOPLP manufacturing to utilize PCB, LCD or Build-up OSAT material, equipment, processes → Cannot achieve the FOWLP design features and yield levels.

Dilemma 4:

FOWLP is increasingly used for more complex package constructions like WLSiP and WL3D with Passives and MEMS → Complexity, high product mix, low volumes.

„Sweet Spot“ for FOPLP will be in large package sizes, but with low complexity (Single Die, 1L-RDL) and needs stable large volumes to continuously load the line.

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