Panel Fan-Out Manufacturing: Why, When, and How?

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Panel Level Packaging is not a geometrical extension

Silicon Scaling ≠ Package Scaling

relative scaling of silicon and pacakging

10000
1000
100
10

1971 1975 1982 1985 1989 1994 1997 2002 2004 2006 2008 2010 2012 2015

Year

Silicon Scaling

Package Scaling

S. Iyer (UCLA), IEEE Trans CPMT 2016

2.2 x

QFP

1.3 x

BGA

CSP

1.0 x

FI-WLP

Smallest SCP!! STOP Die = Package

Solution for SiP???? – Focus on system-level-scaling

Heterogeneous integration for SiP using *Embedding*

I/O Count

high

medium

small

GPU, CPU + Memory, FPGA

ASIC

RF

Power/WiFi

MEMS/Images

SiP Size

Panel Level is: The intelligent combination of Wafer Level Processing and PCB Processing

I/O Count

high

medium

small

WL

PL

SiP Size

Fraunhofer IZM has formed a consortium for Panel Level Packaging

Goal is to drive Panel Level FO-WLP to a similar performance as WLP but at lower cost