ADVANCED PACKAGING IN THE NEW WORLD OF DATA

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THEMES

- The World Is Becoming More And More Dependent On Data
- Processing Ubiquitous Data Is Heavily Dependent On Advances In System Compute & Comms
- Advances In Systems Performance Require
  - High Bandwidth & Low Power Data Pipes Only Available On “Heterogeneous Integration” on Advanced Packages

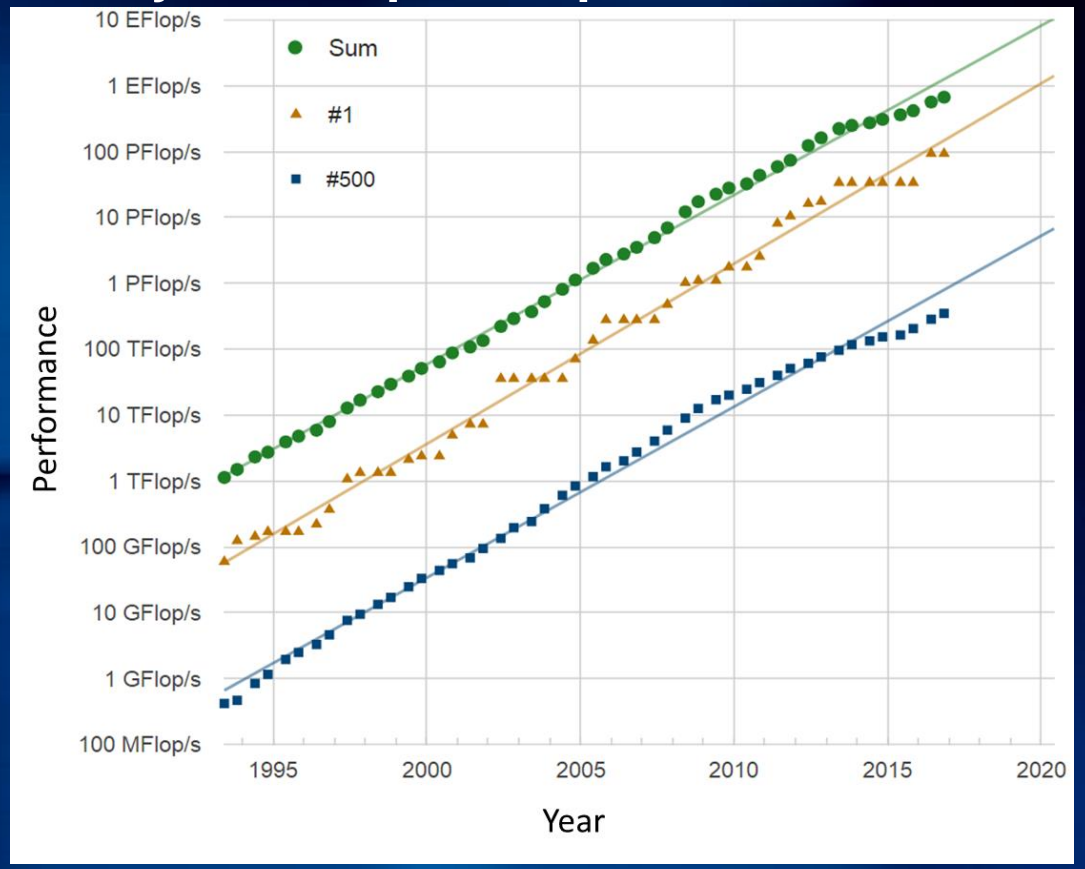
THE AGE OF DATA

BY 2020

AVG. INTERNET USER	1.5 GB OF TRAFFIC / DAY
AUTONOMOUS VEHICLES	4 TB OF DATA / DAY
CONNECTED AIRPLANE	5 TB OF DATA / DAY
SMART FACTORY	1 PB OF DATA / DAY
CLOUD VIDEO PROVIDERS	750 PB OF VIDEO / DAY

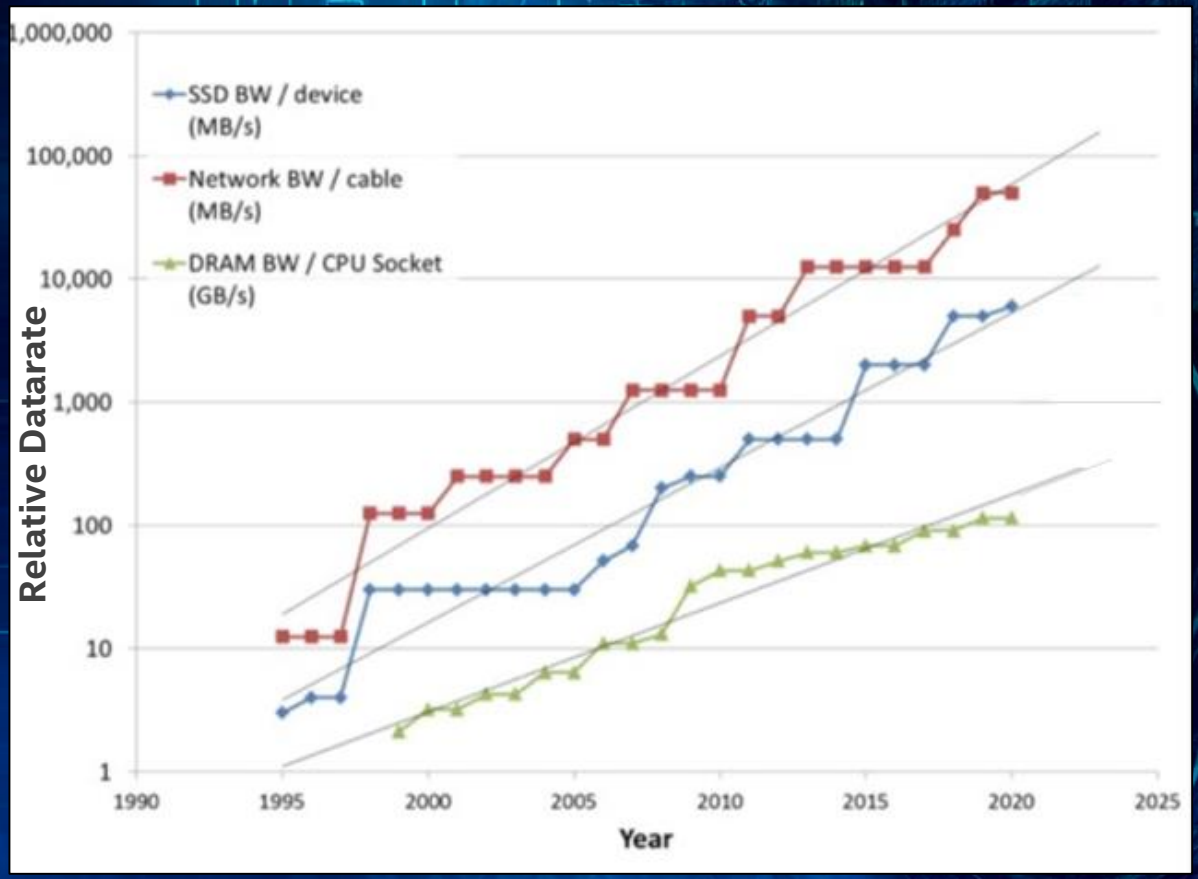
AS DATA DEMANDS GROW…
GREATER COMPUTING PERFORMANCE AND FASTER, WIDER DATA PIPES REQUIRED

Projected Supercomputer Performance



Source: Top500.org

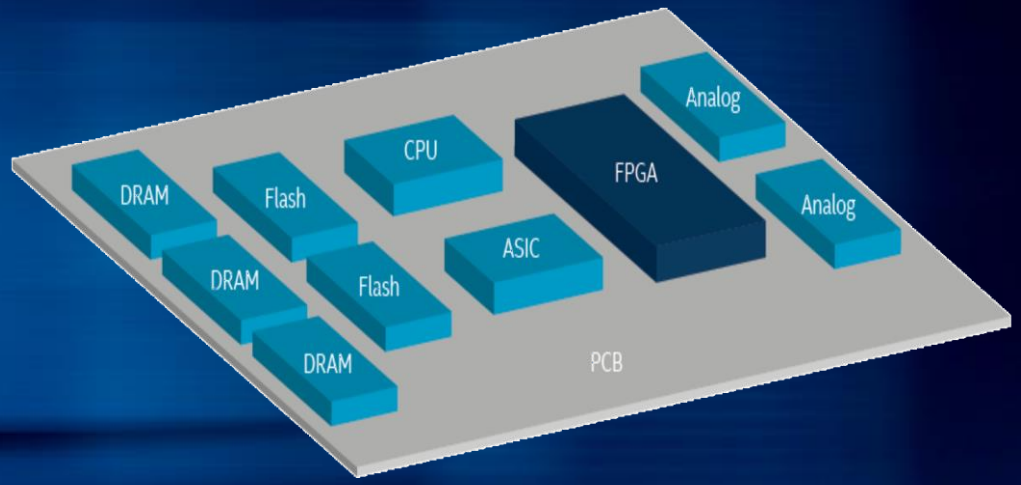
Projected Growth in Comms Datarate

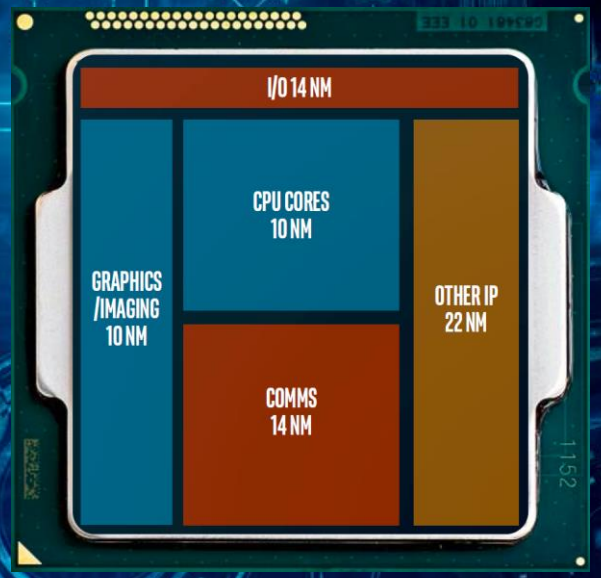


Source: https://itblog.sandisk.com/cpu-bandwidth-the-worrisome-2020-trend/

System Designers Continue to "Raise the Bar" for Overall Performance

ON-PACKAGE HETEROGENEOUS INTEGRATION IS CRITICAL





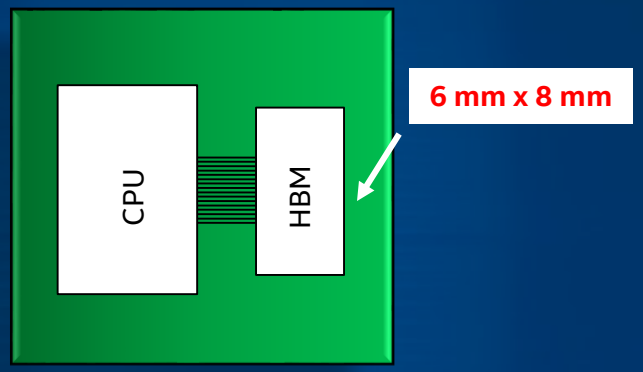
PCB Integration

- Limited Interconnect Density → Limited BW
- Long Interconnects → Increased Power
- Large Form Factor

On-Package Integration

- Lower Power
- Higher Bandwidth
- Heterogeneous Integration of Multiple Nodes, Multiple IP, & Multiple Functions

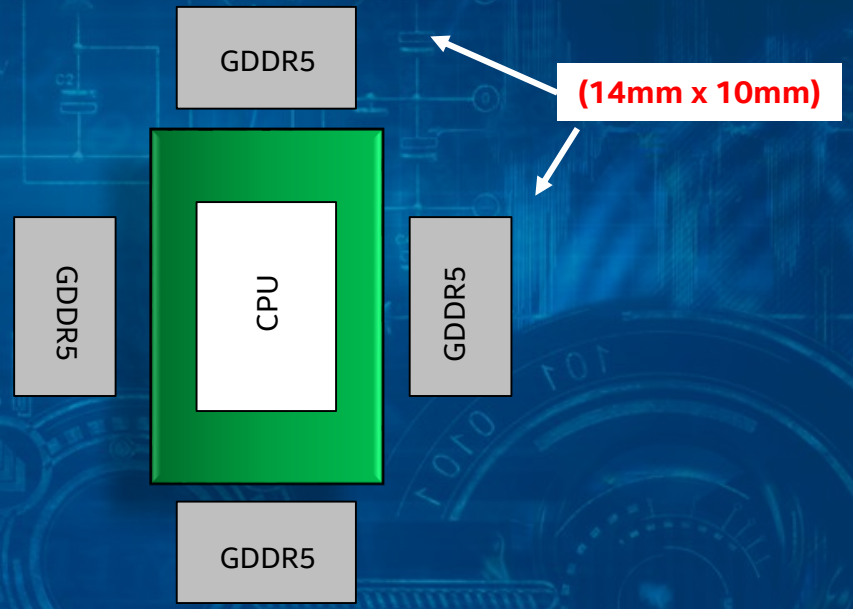
ON-PACKAGE VS. OFF-PACKAGE INTEGRATION



HBM

- Total Capacity 4GB (1GB each)
- Data rate – 1 - 2Gb/s
- Total BW – (128-256) GB/s
- IO Power Efficiency (Energy/bit) – 1X

1. http://www.memcon.com/pdfs/proceedings2015/MKT105_SKhynix.pdf
2. https://www.micron.com/~/media/documents/products/technical-note/dram/tned02_gddr5x.pdf



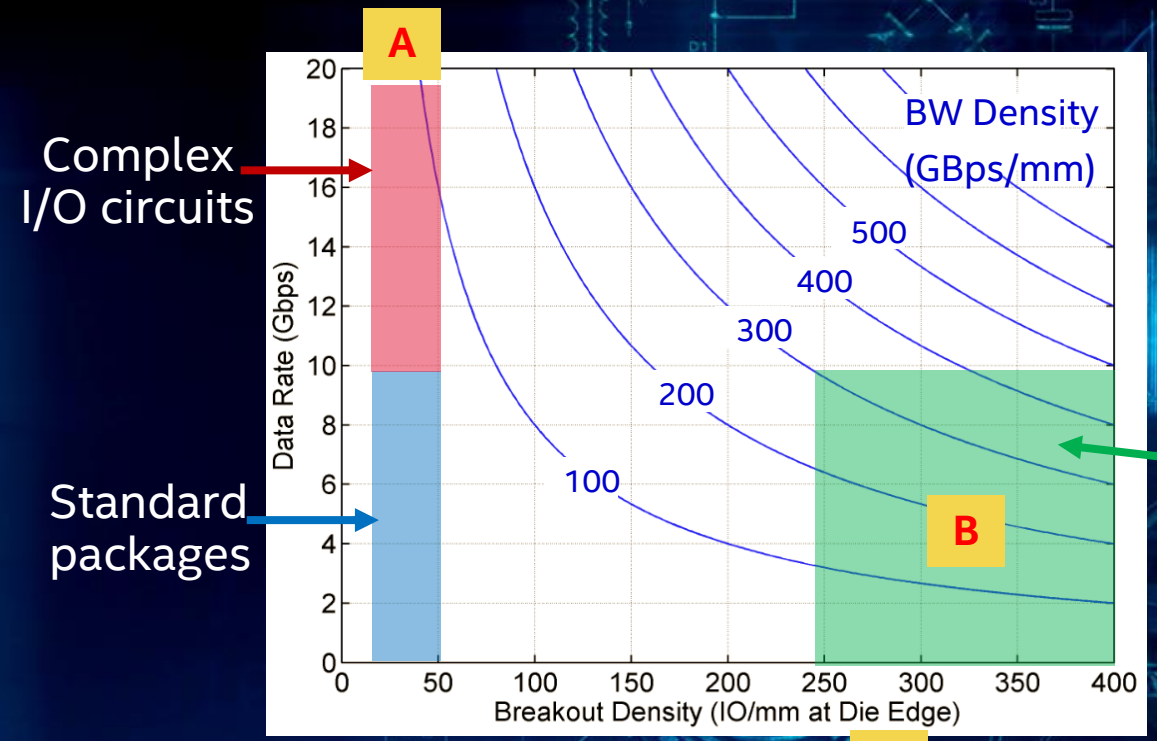
GDDR5x

- Total Capacity 4GB (1GB each)
- Data rate – 12Gb/s
- Total BW – 192 GB/s
- IO Power Efficiency (Energy/bit) – (1.75 – 3)X

On Package Integration is More Compact, Lower Power & Higher BW

ON-PACKAGE SIGNALING

- Advanced packaging technologies can provide tremendous bandwidth density with affordable power consumption
- Improved dielectrics needed to enable higher data rates



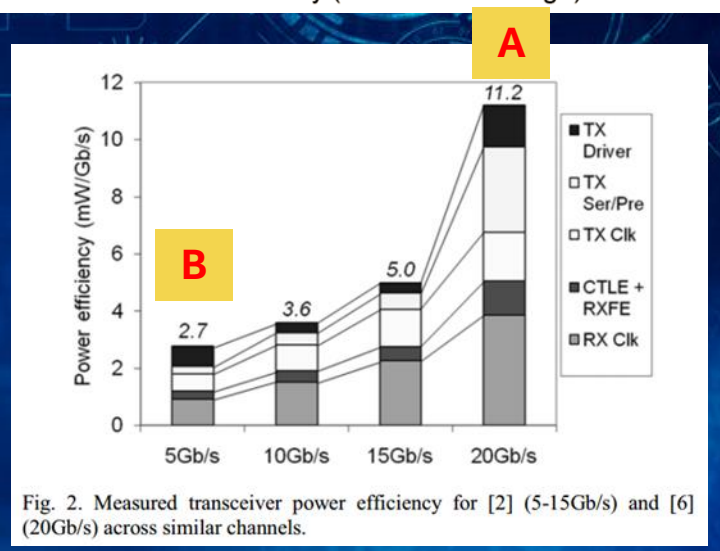


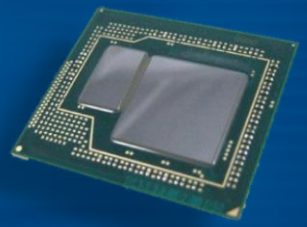
Fig. 2. Measured transceiver power efficiency for [2] (5-15Gb/s) and [6] (20Gb/s) across similar channels.

F. O'Mahony et al., "The future of electrical I/O for microprocessors," in *Proc. IEEE Symp. VLSI Design Automation and Test (VLSI-DAT)*, Apr. 2009, pp. 31–34.

TODAY'S MULTI-CHIP PACKAGING SPECTRUM

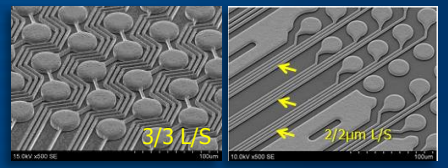
2D/2.5D (Side by Side MCPs)

Organic FCXGA, FCCSP



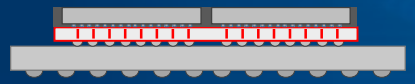
IO/mm/lyr = 28-34
IO/mm^2 = 83-123
Bump Pitch = 110-90µm

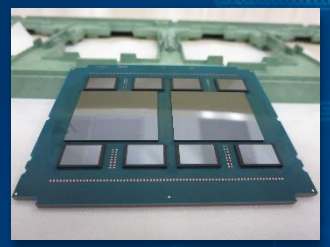
High Density Organic Interposer



IO/mm/lyr = 100+*
IO/mm^2 = 331
Bump Pitch = 55µm

Si Interposer, Intel EMIB





IO/mm/lyr = 250
IO/mm^2 ≥ 331
Bump Pitch ≤ 55µm

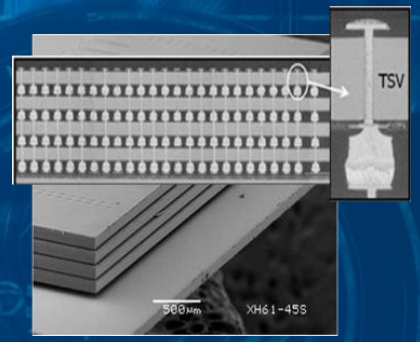
* Oi et al. 2014 ECTC report 2µm L/S, 25µm pad

3D (Die &/Or Package Stacking)

Package Stacking

PoP Pitch 0.27mm

Die Stacking

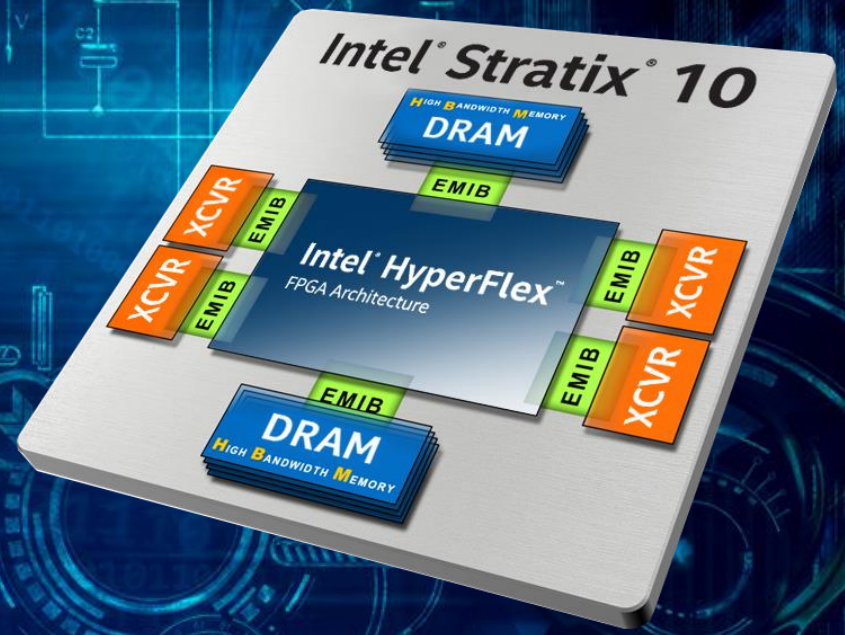


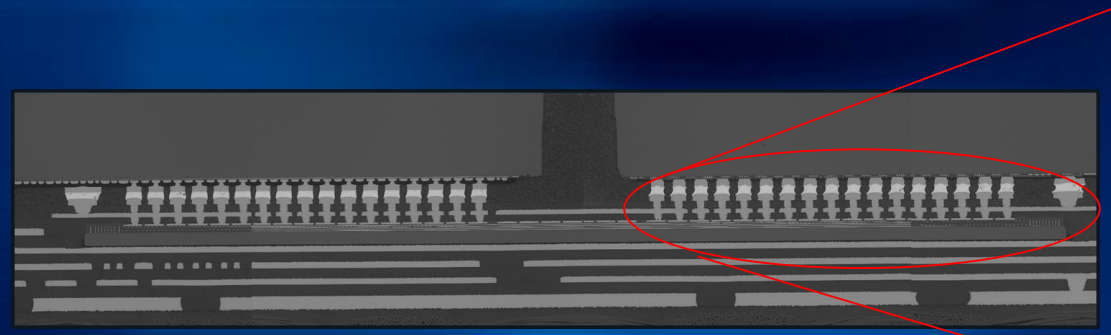
IO/mm = N/A
IO/mm^2 = 625
Bump Pitch = 40µm

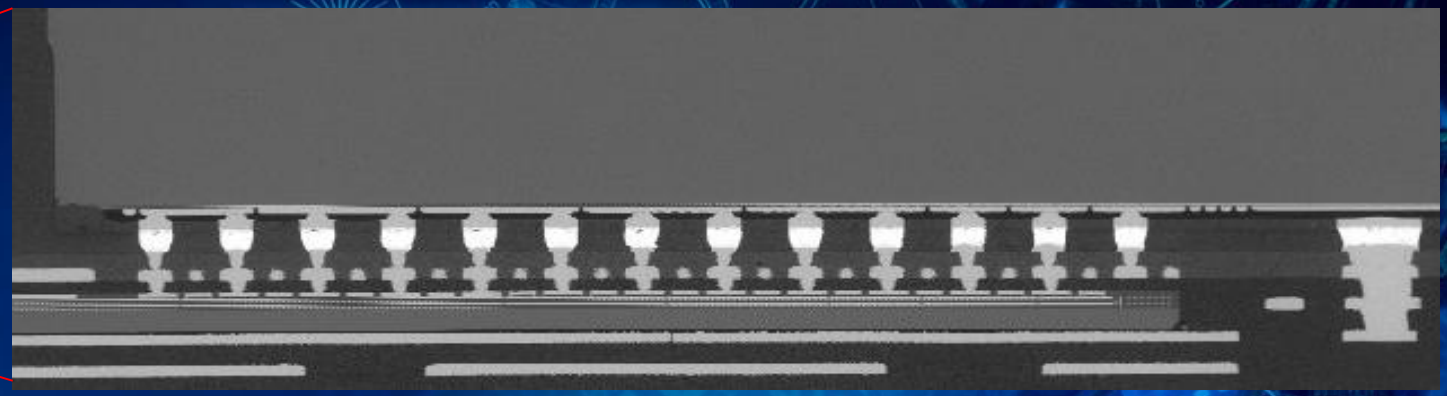
Many Package Options Exist!!
Designers Pick the Optimal Solution for a Specific System

INTEL'S MOST ADVANCED HETEROGENEOUS INTEGRATION TODAY

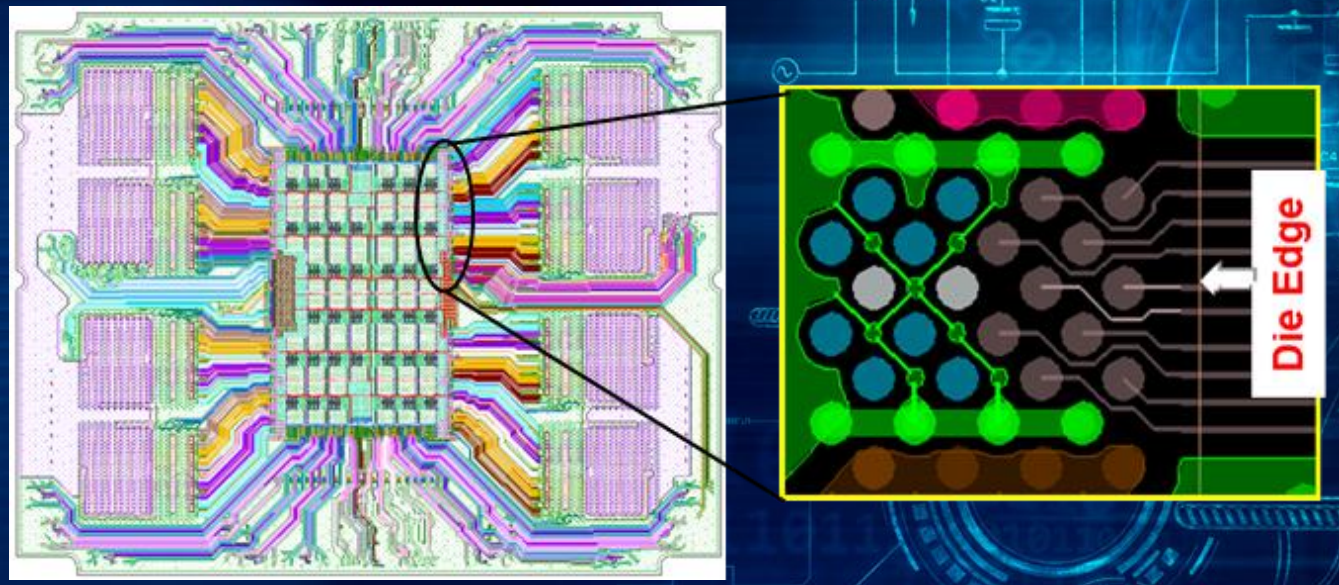
EMIB Provides a cost effective, localized high density, ultra-high Bandwidth/Low Power Interconnect Solution







ADVANCED MULTI-CHIP PACKAGING



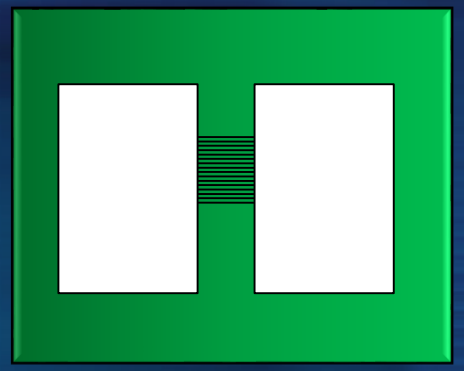
Key Feature Scaling Metrics:

- IO/mm/Layer (Escape Density)
- IO/mm^2 (Die Area)

Package Feature Scaling Must Always keep up with Silicon Scaling

Note: IO here refers to physical bumps and wires

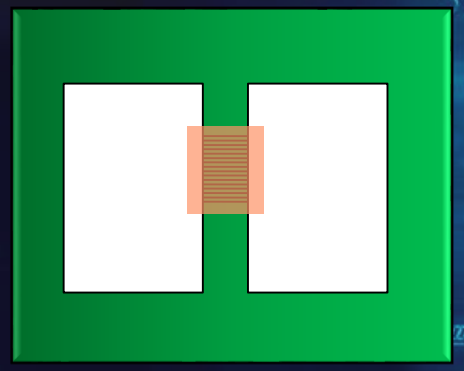
DIRECTIONS FOR HETEROGENEOUS PACKAGING IN THE FUTURE



Traditional MCP
10's of IO/mm
~100 Gb/s BW

Die-Package Interconnect Pitch ~100μm

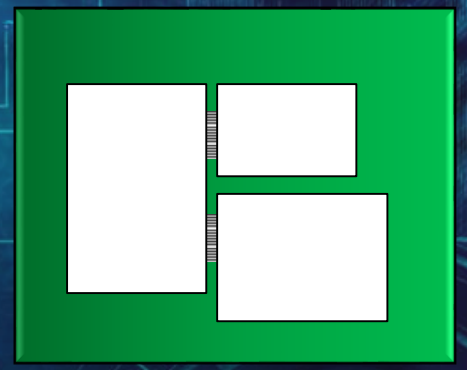
Substrate Technology – Advanced Laminate
Assembly Technology – Reflow CAM
Test Technology – Array Sort Probing



State of the Art MCP
100's of IO/mm
~500 Gb/s BW

Die-Package Interconnect Pitch ~50μm

Substrate Technology – EMIB, (Si Int + Laminate)
Assembly Technology – TCB
Test Technology – Array Sort + Self Test



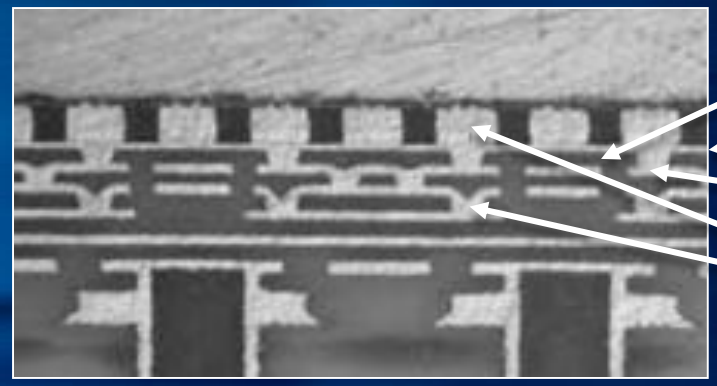
The Future of MCP's
1000's of IO/mm
1+ Tb/s BW

Die-Package Interconnect Pitch ~10μm

Substrate Technology – TBD
Assembly Technology – TBD
Test Technology – TBD

Industry is Challenged to Invent New Solutions for Ultra-high Density Multi-Chip Packaging

PACKAGE TECHNOLOGY WILL BECOME MORE WAFER FAB-LIKE

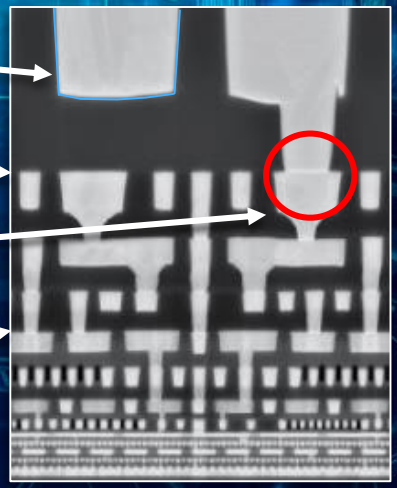


Inorganic Thin Films

Planarization

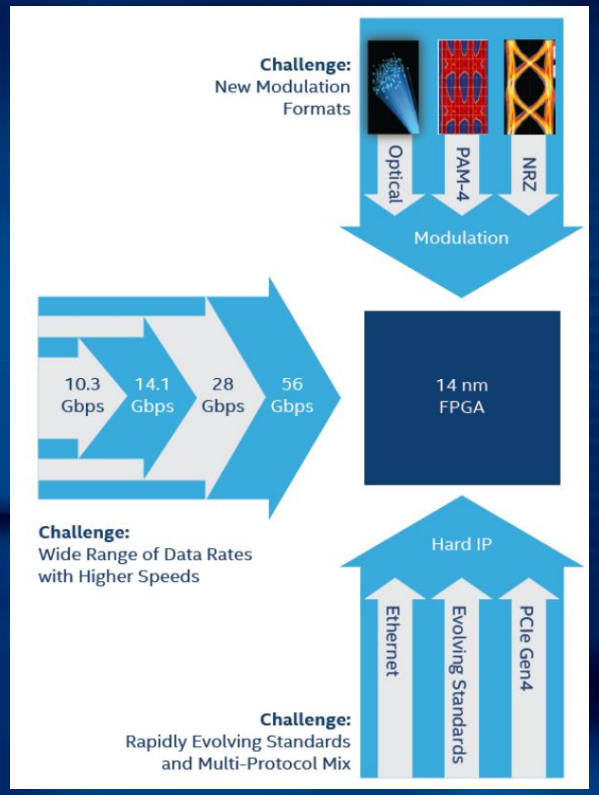
Pad-less Vias

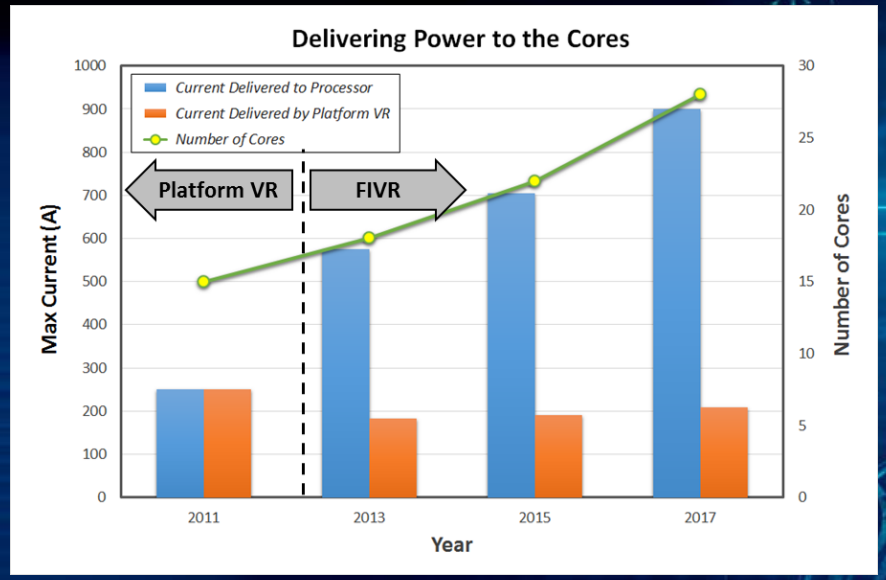
Cu-Cu Bumps & Vias

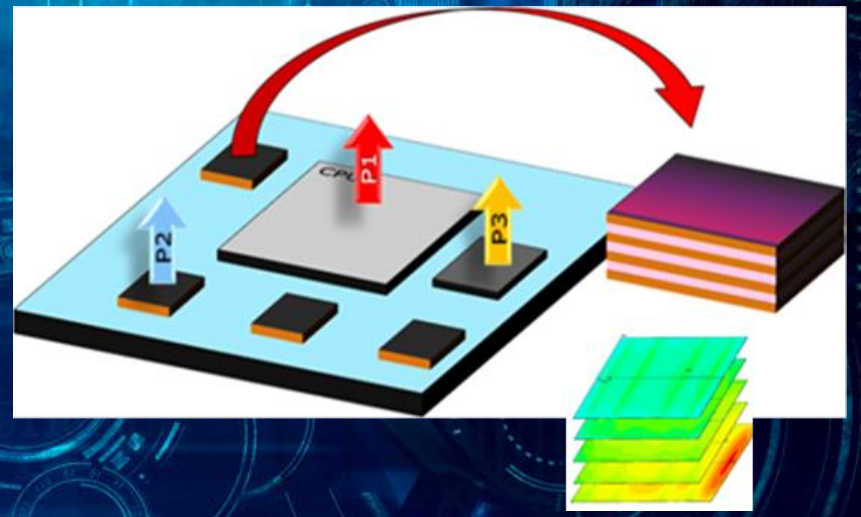


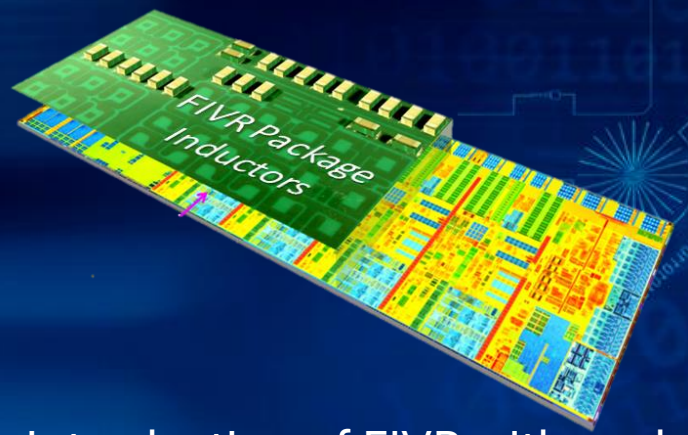
Achieving Interconnect Densities to Support 1+ TB/s on-Package Interconnects Will Require Novel Substrate and Assembly Capabilities

MULTI-CHIP PACKAGES WILL HAVE TO ADDRESS OTHER CHALLENGES





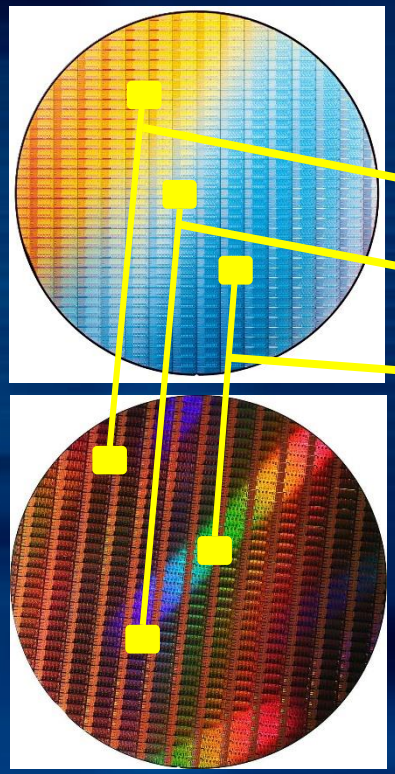




- Enabling Technologies for high Bandwidth, Off-Package Electrical & Optical Signaling Needed
- Introduction of FIVR with package inductors helps current demand
- Improved Inductors Needed
- Improved Thermal Interface Materials (TIMs) and Interface Control Needed for MCPs

A COMPREHENSIVE TEST STRATEGY NEEDED FOR HIGH YIELD MANUFACTURING

Low Defect Density Wafer Fab

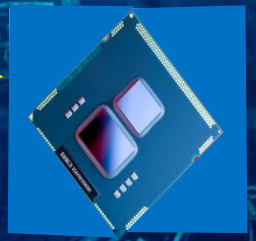


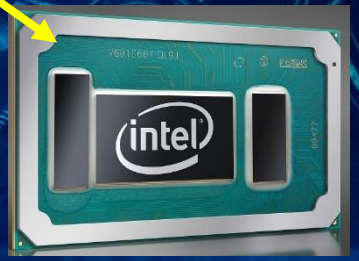
Known Good Die Test
- Binned, Stressed, Low DPM
- Die, Die stacks, WLP, etc
- Internal and external sourcing

Data analytics for Die to Product Targeting
- Matched Config, Speed, Power, etc.
- Inventory and yield management

7TH GEN INTEL® CORE™ PROCESSOR QUICK SUMMARY CHART — S-SERIES

	CORES / THREADS	BASE FREQ.	SCT	UNLOCK	INTEL® GRAPHICS	DYNAMIC FREQUENCY	INTEL® SMART CACHE	DDR4‡ / DDR3L	TDP	INTEL® VPRO™
S-SERIES										
i7-7700K	4/8	4.2	4.5	√	HD 630	1150	8M	2400/1600	91W	-
i5-7600K	4/4	3.8	4.2	√	HD 630	1150	6M	2400/1600	91W	-
i7-7700	4/8	3.6	4.2	-	HD 630	1150	8M	2400/1600	65W	√
i5-7600	4/4	3.5	4.1	-	HD 630	1150	6M	2400/1600	65W	√
i5-7500	4/4	3.4	3.8	-	HD 630	1100	6M	2400/1600	65W	√
i7-7700T	4/8	2.9	3.8	-	HD 630	1150	8M	2400/1600	35W	√
i5-7600T	4/4	2.8	3.7	-	HD 630	1100	6M	2400/1600	35W	√
i5-7500T	4/4	2.7	3.3	-	HD 630	1100	6M	2400/1600	35W	√
i5-7400	4/4	3.0	3.5	-	HD 630	1000	6M	2400/1600	65W	-
i5-7400T	4/4	2.4	3.0	-	HD 630	1000	6M	2400/1600	35W	-
i3-7350K	2/4	4.2	N/A	√	HD 630	1150	4M	2400/1600	60W	-
i3-7320	2/4	4.1	N/A	-	HD 630	1150	4M	2400/1600	51W	-
i3-7300	2/4	4.0	N/A	-	HD 630	1150	4M	2400/1600	51W	-
i3-7100	2/4	3.9	N/A	-	HD 630	1100	3M	2400/1600	51W	-
i3-7300T	2/4	3.5	N/A	-	HD 630	1100	4M	2400/1600	35W	-
i3-7100T	2/4	3.4	N/A	-	HD 630	1100	3M	2400/1600	35W	-





High Yield Packaging
- Substrate test, component test
- Inline metrology
- Process controlled assembly

Package Test
- Integrated test coverage
- System verification
- Yield recovery
- DPM verification

IN CONCLUSION

- Heterogeneous On-Package Integration is a Critical Enabler for the “Age of Data”….Key advantages
  - High Interconnect Density
  - High Bandwidth
  - Compact Integration of Multiple Nodes, Multiple IP, Multiple Functions
- As a community we need to focus on delivering
  - Increasingly High Density Interconnect
  - Power efficient Signaling
  - Efficient Power Delivery
  - Improved MCP Thermals
  - A Comprehensive Test Strategy for High Yield Manufacturing