

## Fan-Out Fans Crowd Conference (/pcdesign/index.php/current-issue/234-forefront/11906-on-the-forefront-1708)

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by E. Jan Vardaman

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### **The annual ECTC revealed exciting advancements on single- and multi-die packages.**

The IEEE Electronics Components and Technology Conference (ECTC) at the end of May welcomed nearly 1,500 attendees to the sunshine state of Florida to discuss the latest developments in electronics packaging technology.

A panel discussion on the first evening focused on the topic Panel Fan-Out Manufacturing: Why, When and How? The panel was designed as a jury, with a customer (Qualcomm) surrounded by round wafer proponents (TSMC, Amkor's Nanium) on one side and panel proponents (Deca Technologies, IZM Fraunhofer consortium) on the other. No conclusion was reached regarding the "right" path to meet customer requests for lower-cost packaging (in this case Qualcomm), but clearly panel processing could be an option. Exactly when panels would move into high-volume manufacturing remained a mystery, but in the audience representatives from Samsung Electro-Mechanics (SEMCO) watched carefully for the reaction. SEMCO continues its development of a panel line, while Nepes and Powertech Technology (PTI) indicate lines are ready. Unimicron continues its research on panel processing and presented a paper discussing stress and warpage for its RDL-first panel FO-WLP.

The most heavily attended sessions were ones for fan-out wafer-level packages (FO-WLP). Fans of FO filled the rooms. Papers focused on multi- and single-die versions of FO-WLP. There were many takers for ASE's fan-out fans, coming in handy for the Florida heat.

While there were many exciting papers, none could top last year's presentation from TSMC describing the dramatic form factor, electrical and thermal performance advantages of the integrated fan-out (InFO) technology. Today, everyone knows TSMC's InFO is used to package Apple's A10 application processor in the bottom package-on-package (PoP) found in the Apple iPhone 7.

Papers from research organizations such as Fraunhofer, ITRI and IME A\*Star, along with companies including Amkor, ASE, Nanium, SPIL, Stats ChipPAC and TSMC, discussed advances with FO-WLP. Researchers at Fraunhofer IZM, in cooperation with Suss MicroTec, introduced an excimer laser dual damascene process for ultra-fine line multilayers with 10µm micro-vias for wafer and panel-level packaging. IME A\* Star described a dry-film process used to form a vertical interconnect structure. A joint paper by Georgia Tech, Suss MicroTec, Disco and Fujifilm Electronic Materials discussed excimer laser ablation and surface planer processes to form embedded trench RDL. Brewer Science discussed a temporary bonding material for FO-WLP. Hitachi Chemical reported on the use of a glass carrier for FO-WLP and ways to control warpage. Stats ChipPAC discussed reliability of eWLB for automotive radar applications. Amkor presented electrical and thermal simulation data for its SWIFT die-last process for PoP. A paper by SavanSys provided a yield comparison of die-first face-down and die-last FO-WLPs. Huatian Technology (Kunshan) Electronics presented its embedded silicon fan-out structure as a low-cost option. ASE presented work on integrated passives for an RF application using panel processing.

Materials and equipment developments were also presented. Lintec described a pick-and-place process using its tape expansion for FO-WLP. Hitachi Chemical described its expanding film and process for FO-WLP. Georgia Tech reported on research on interfacial delamination of mold compound in FO-WLPs. Both TSMC and SPIL discussed mold compounds and warpage. SPIL's presentation focused on warpage in multi-die FO-WLPs.

The latest developments in large-body-size fan-out packages were also discussed. Large-body FO-WLPs are mounted on an organic substrate and targeted at high-performance applications. ASE's fan-out on substrate (FOCoS) presentation included reliability data. A number of companies are considering this large-body version of FO-WLP as a lower-cost alternative to a high-density silicon interposer

solution.

Important WLP developments were also discussed. Qualcomm presented additional data on WLP reliability issues with fine-pitch solder balls (0.35mm) on large die. TSMC discussed risks and issues for WLP for silicon fabricated with low-k dielectric material. IME A\*Star discussed process and reliability for large FO-WLP PoP.

**2.5D and 3D integration.** Some applications require use of a high-density interposer, either silicon (2.5D) or potentially high-density organic. While potential new users remain concerned about reliability, products with silicon interposers from Xilinx and AMD have been shipping for several years. While the sessions for these topics were not as crowded as in years past, a number of ECTC presentations provided excellent reliability discussions. Cisco described many failure mechanisms introduced by 2.5D and 3D integration, including thin die, through silicon vias (TSVs), chip-to-chip interconnection, backside RDL, microbumps, copper contamination, thermal issues, and electrostatic discharge. Test concerns for high bandwidth memory (HBM) were also addressed. Xilinx presented a paper that discussed the improved reliability obtained for the large silicon interposer using polymer core solder balls.

Hitachi Chemical reported on improved materials for 3D stacking. Brewer Science discussed its materials that provide improvements in the debonding process. Invensas reported on use of thermal direct-bond interconnect for 2.5D and 3D.

**Substrate and fine-pitch bump developments.** Progress in fine-pitch bumping was reported. A joint paper with CEA-Leti examined assembly with five and 10µm pitch CuSnAg interconnects. Atotech presented the role of surface finish and barrier layers with 20µm pitch copper pillars. IMEC discussed thermal compress bonding (TCB) developments for fine-pitch bumping. A presentation from UCLA focused on TCB for a two to 10µm bump diameter. CEA-Leti provided a reliability assessment of copper pillar bumps for fine-pitch applications. KAIST talked about non-conductive film (NCF) underfill for fine-pitch bumping. Fraunhofer, Georgia Tech and Loughborough University highlighted new interconnect developments.

Asahi Glass, ASE, Corning and NTK reported on glass substrate developments. A number of presentations focused on embedded technology. Fujitsu described its embedded multilayer thin-film capacitor substrate for a CPU. Infineon discussed laminate chip embedding technology for thin die. GE and Shinko Electric described a new embedded die in flex substrate for power devices. Amkor's J-Devices discussed its embedded die packaging for power devices using a laminate structure with a copper base.

Several sessions covered warpage issues. IME A\*Star discussed developments in warpage control for interposers without TSVs. Huawei discussed reflow warpage caused by the interaction gap between the package and PCB and top and bottom packages in a PoP configuration.

**Singulation developments.** An entire session focused on singulation process developments with presentations by ASM for laser full cut for WLP and SPTS Technologies on use of plasma dicing for thin die. IME A\*Star described stealth dicing challenges for MEMS.

**Automotive electronics.** Automotive growth is exciting because of the promise of greater electronics content resulting in revenue growth for the supply chain. A night panel discussion examined automotive electronics applications, developments in powertrain electronics, sensor options, data processing, and wireless communication. A number of papers discussed packages for automotive power modules.

**Emerging technology.** Emerging topics such as medical electronics included a presentation from A\*Star on a conformal patch sensor used to detect swelling that arises in the subcutaneous tissue layer. This condition normally requires expensive hospitalization. The use of the patch created from a TiCuAu thin-film metallization on an elastic polymer layer can alert medical personnel to signs of swelling.

A session was also devoted to 5G, mmWave and beyond. Presentations included a joint paper from Asahi Glass, NGK, and Georgia Tech discussing 28 and 39GHz transmission lines and antennas on glass substrates for 5G modules. ASE discussed a low-cost organic substrate for mmWave communications. TSMC discussed developments in high-performance chip-partitioned mmWave passive devices on their InFO version of FO-WLP.

Many presentations focused on developments in sensors, including medical applications. A NASA presentation discussed a high-temperature capacitive pressure sensor using silicon carbide (SiC) integrated circuit twin ring oscillators.

A night seminar examined 3D printing tools, technologies, and applications. Georgia Tech's overview of the status of the industry in 3D printed electronics underscored the great progress. A presentation from Zuken addressed some of the design questions for printed circuit board applications. Nano Dimension, a startup based in Israel, explained squeezing the development cycle from weeks to hours is one of the key drivers for printing substrates. Circuits with 100µm features have been demonstrated on 5 x 3 x 1.6cm samples fabricated in two hours. A 12-layer PCB has been fabricated. Conductive inks can be used to make patterns on rigid, flex, glass and aluminum substrates. Passives and coils can be printed. Some of the first applications are for the military. Fuji Machine described equipment developed for printed electronics.

Reliability, MEMS, optoelectronics, advances in wire bonding, material developments, and thermal characterization sessions rounded out the program. Special sessions were also held to talk about material and package reliability for harsh environments and flexible hybrid electronics. Interactive poster sessions allowed in-depth, one-on-one discussions with the presenters. The Heterogeneous Integration Roadmap also held a meeting to continue its roadmap development activities. A special women's session discussed emotional intelligence and the link to successful leadership.

Next year, ECTC will be held in San Diego, with one noticeable change. IEEE's society sponsoring the conference has changed its name from the Components Packaging and Manufacturing Technology (CPMT) Society to the Electronics Packaging Society (EPS).

**E. JAN VARDAMAN** is president of TechSearch International (techsearchinc.com); [jan@techsearchinc.com](mailto:jan@techsearchinc.com) (mailto:jan@techsearchinc.com). Her column appears bimonthly.



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