Disruptive Developments for Advanced Die Attach to Tackle the Challenges of Heterogeneous Integration

Hugo Pristauz & Andreas Mayr, Besi Austria
presented by: Stefan Behler, Besi Switzerland
Many predictions of the end of Moore’s Law (last prediction by Gordon Moore -> 2025)
## Enhanced Capabilities Demanded

<table>
<thead>
<tr>
<th>Application</th>
<th>Accuracy</th>
<th>Clean Class</th>
<th>Throughput</th>
<th>Working Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>2D-FCBGA (mass reflow)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WL/PL-FO (organic RDL)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WL-FO (inorganic RDL)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3D-SICs (TC bonding)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Classical 2.5D (mass reflow)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bridge Embedding</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielet Platform (hybrid bonding)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3D-SOCs (hybrid bonding)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transfer Printing (mass transfer)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Introduction

Current Integration Architectures

Future Integration Architectures

Demand for High Capabilities

Disruptive Developments

Conclusions & Take-aways
2D-Side-by-Side Packages

- Conventional 2D Multi Chip Package architectures, typically FC-BGA,
- Either MR-FC bonding or TC-Bonding
- Interconnection of active side-by-side die is accomplished by either (wire bonded) wires and/or substrate traces

Intel’s Knights Landing™

Shinko’s i-THOP™ laminate
Organic RDL Based Packages

- Organic RDL based WL/PL-Fan-out packaging technology
- Interconnection of active side-by-side die is accomplished by an organic redistribution layer (RDL)
Inorganic RDL Based Packages

2.5D silicon interposer package

Xilinx: FPGA
Virtex-7 H580T

Intel EMIB

SLIM™
Silicon-Less Integrated Module

CoWoS

Based on inorganic RDL (silicon oxide, silicon nitride)
- a) 2.5D TSV based or TSV-less silicon or glass interposer packaging
- b) embedded silicon bridges (EMIB™)
- c) CoWoS (Chip on wafer on Substrate): 2.5D Si-interposer on substrate
3D-Stacked IC (3D-SIC)

- Direct interconnected active die which are 3D arranged
- a) 3D TSV based packaging
- b) 3D Face-to-face packaging
Introduction

Current Integration Architectures

Future Integration Architectures

Demand for High Capabilities

Disruptive Developments

Conclusions & Take-aways
## 3D-SOCs

### IMEC 3D-Roadmap

<table>
<thead>
<tr>
<th>Wiring Level</th>
<th>3D-SIC</th>
<th>3D-SOC</th>
<th>3D-SOC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Global</td>
<td>Semi-global</td>
<td>Intermediate</td>
</tr>
<tr>
<td>2-tier stack</td>
<td><img src="image" alt="2-tier stack" /></td>
<td><img src="image" alt="2-tier stack" /></td>
<td><img src="image" alt="2-tier stack" /></td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>40 ⇒ 20 ⇒ 10 ⇒ 5 μm</td>
<td>5 ⇒ 1 μm</td>
<td>2 μm ⇒ 0.5 μm</td>
</tr>
<tr>
<td>Relative density:</td>
<td>1/16 ⇒ 1/4 ⇒ 1 ⇒ 4</td>
<td>4 ⇒ 100</td>
<td>50 ⇒ 400</td>
</tr>
<tr>
<td>Partitioning</td>
<td>Die</td>
<td>blocks of standard cells</td>
<td>Gates</td>
</tr>
</tbody>
</table>

### OPENSPARC T2

3D-SOC Study for OpenSPARC T2 to be 3D-integrated into Logic + Memory

Source: Philipp Absil, “Overview of the 3D Technology Landscape And Challenges”, Semicon Korea 2016:
DARPA’s CHIPS Program [1]
• CHIPS = chiplet (dielet) platform

• Chiplet = functional, verified, re-usable IP block, realized in physical form [2]

Pitch sweet spot between 2 and 10µm for chiplet (dielet) based HI platforms [3]

Source:
[1] D.S. Green, “DARPA’s CHIPS Program, and Making Heterogeneous Integration Common”, 3D-ASIP 2017
Transfer Printing

- Example of transfer-print compatible micro devices
- Devices are undercut and anchored using MEMS-processing technologies
- Throughput proposals beyond 300,000 components/hour
- 1.5µ @ 3σ accuracy required

Introduction

Current Integration Architectures

Future Integration Architectures

Demand for High Capabilities

Disruptive Developments

Conclusions & Take-aways
Drive for Higher Accuracy

Comparison of Heterogeneous Integration architectures according to bump pitch metrics and areal density.

- Areal density = 1 / (bump pitch)$^2$
- Placement accuracy @ 3σ ≈ (bump pitch) / 10

*) Center accuracy for self-centering processes, like MR-FC
Corner accuracy for non self-centering (FO, TC, hybrid bonding)
## Enhanced Capabilities Demanded

<table>
<thead>
<tr>
<th>Application</th>
<th>Accuracy</th>
<th>Clean Class</th>
<th>Throughput</th>
<th>Working Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>2D-FCBGA (mass reflow)</td>
<td>5-10μ@3σ (die center)</td>
<td>ISO-6</td>
<td>15-20 kCPH</td>
<td>300 x 125 mm</td>
</tr>
<tr>
<td>WL/PL-FO (organic RDL)</td>
<td>3-10μ@3σ (die corners)</td>
<td>ISO-5</td>
<td>15-40 kCPH</td>
<td>φ 300 mm 650 x 550 mm</td>
</tr>
<tr>
<td>WL-FO (inorganic RDL)</td>
<td>2-3μ@3σ (die corners)</td>
<td>ISO-5</td>
<td>5-10 kCPH</td>
<td>φ 300 mm</td>
</tr>
<tr>
<td>3D-SICs (TC bonding)</td>
<td>2-3μ@3σ (die corners)</td>
<td>ISO-5</td>
<td>3-5 kCPH (tack &amp; gang)</td>
<td>φ 300 mm</td>
</tr>
<tr>
<td>Classical 2.5D (mass reflow)</td>
<td>3-5μ@3σ (die center)</td>
<td>ISO-5</td>
<td>5-10 kCPH</td>
<td>φ 300 mm</td>
</tr>
<tr>
<td>Bridge Embedding</td>
<td>0.5-2μ@3σ (die corners)</td>
<td>ISO-4</td>
<td>2-5 kCPH</td>
<td>650 x 550 mm</td>
</tr>
<tr>
<td>Dielet Platform (hybrid bonding)</td>
<td>0.2-1μ@3σ (die corners)</td>
<td>ISO-3 (ISO-2)</td>
<td>5-10 kCPH</td>
<td>φ 300 mm</td>
</tr>
<tr>
<td>3D-SOCs (hybrid bonding)</td>
<td>50-500nm@3σ (die corners)</td>
<td>ISO-3 (ISO-2)</td>
<td>1-5 kCPH</td>
<td>φ 300 mm</td>
</tr>
<tr>
<td>Transfer Printing (mass transfer)</td>
<td>0.5-2μ@3σ (die corners)</td>
<td>ISO-5 (ISO-4)</td>
<td>50–300 kCPH</td>
<td>650 x 550 mm (920 x 730 mm)</td>
</tr>
</tbody>
</table>
Introduction

Current Integration Architectures

Future Integration Architectures

Demand for High Capabilities

Disruptive Developments

Conclusions & Take-aways
Advanced Gantry System

• Decoupled metrology
• Water cooled

Strength
• 2µ@3σ global*)
  pick & place accuracy
• Roadmap: 1µ@3σ global*)
  pick & place accuracy

*) ‘global’ means: no local fiducials!
‘Van Gogh Alignment’ Method

To achieve 200nm@3\(\sigma\) placement accuracy (@ 1000 UPH)

**Principle**
1. tool reference marks next to the die
2. upward camera determines position of die fiducial relative to tool reference mark
3. downward camera determines position of substrate fiducial relative to tool reference mark
4. Calculation of resulting misalignment and correction with ‘Nano Actor’
Enhanced Clean Capability

ISO-3 clean concept for Datacon 8800 platform

1. Use of ISO-3 compatible cables & vacuum hoses
2. Covering all energy chains – exhaust dirty air from inside of covers
3. Introducing horizontal, HEPA filter cleaned laminar flow
4. Loading substrate and diced wafers from FOUPs via EFEMs
Parallel Die Processing

Multi-nozzle bond head concept for Datacon 8800 platform

- Common z-axis for 4 nozzles
- Individual mini-stroke per nozzle to move nozzle into working or standby position

1. Sequential picking of dies
2. Concurrent (parallel) transfer of 4 dies
3. Concurrent (parallel) upward vision of 4 dies
4. Sequential bonding of dies

Throughput Target:
- 20,000+ chips/hour
- $\phi300$ or 650x550 mm
Introduction

Current Integration Architectures

Future Integration Architectures

Demand for High Capabilities

Disruptive Developments

Conclusions & Take-aways
Conclusions & Take Aways

- Advanced Die Attach will be in future a key technology for Heterogeneous Integration.
- Roadmaps are proposing 40->10µ pitch for 2.5D/3D SIC, 10-2µ pitch for dielet/chiplet 2.5D platforms, and 5->1µ pitch for 3D-SOCs.
- Hybrid bonding is believed to be the killer technology for sub micron W2W, D2D or D2W 2.5D/3D integration architectures
- Hybrid bonding is driving sub-µm placement accuracy with ultra clean conditions (ISO3->ISO2), while cost down drives throughput beyond 20,000 UPH on GEN-3 panel level (650 x 550 mm)
- 4 disruptive developments for Advanced Die Attach
  - Water cooled Advanced Gantry System based on decoupled metrology
  - ‘Van Gogh Alignment’ method for nanometer scale placement accuracy
  - ISO-3 clean concept for 8800 advanced die attach platform
  - Quattro-nozzle bond head for parallel die transfer and sequential pick/place
Thank You!