Package Advancement to Enable Artificial Intelligence, Autonomous Cars and Wearables in Near Future:
Cost and Implications to Supply Chains

B C Ooi
Sr. Vice President, Global Operations, Broadcom Corporation.
May 30, 2018
Growth Drivers for Semiconductor Industry through 2022

IC End-Use Markets ($B) and Growth Rates

- **Cellphones** $89.7
- **Standard PCs** $69.0

**Growth Drivers**
- Network Infrastructure
- AI
- Storage

**Fueled by Advanced Package Technology**

**Shares of 2017 IC Sales (Est)**

- **2016-2021 CAGR**
  - CAGR > 13%
  - CAGR > Cellphones
  - Automotive $28.0
  - Internet of Things* $20.9
  - Digital TVs $13.8
  - Servers $16.7
  - Wearables $3.5
  - Medical $5.9
  - Gov/Military $2.6
  - Set-Top Boxes $5.8
  - Games $10.5
  - Tablets $11.6

* Covers only the Internet connection portion of systems

Source: IC Insights

# (Ref: https://press.trendforce.com/press/20170907-2954.html)
Implications for 2019-2022

- IP traffic will be ~3X-4.6X (peak hours)
- Wireless and Mobile >63% of total IP traffic
- Pervasive 5G Networks
- Systems and Devices need to be ready
- IC Packaging to be a Key Enabler
## Integration through IC Package for Performance Scaling

### ASIC + High Bandwidth Memory Integration

<table>
<thead>
<tr>
<th>IC Package Need</th>
<th>2018</th>
<th>2022</th>
<th>Challenges</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>56 Gbps</td>
<td>112 Gbps</td>
<td>• Channel Insertion Loss &amp; Return Loss</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Crosstalk</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Power Integrity</td>
</tr>
<tr>
<td>Body Size</td>
<td>67.5mm x 67.5 mm</td>
<td>&gt; 90mm x 90mm</td>
<td>• Package Warpage</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Board Level Reliability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Socket Cost &amp; Performance Penalty</td>
</tr>
<tr>
<td>2.5D Integration</td>
<td>Up to 5 dies</td>
<td>More/Larger dies (incl. Optical)</td>
<td>• Interposer Reticle Size</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Assembly challenges</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• More Memory BW</td>
</tr>
<tr>
<td>Micro-bump Pitch</td>
<td>40um</td>
<td>&lt;=30um</td>
<td>• Assembly challenges</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Routing challenges</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>300 W</td>
<td>&gt; 500 W</td>
<td>• Thermal Interface Material</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Heatsink Solutions</td>
</tr>
</tbody>
</table>

*From ASE’s website*

*Intel Nervana*

*Xilinx/TSMC Virtex-7*
Challenges on IC & Package Engineering

- IC Designs at 7nm, 5nm, full reticle size
- ASICs, Internal designs & Merchant Silicon- Mix
- SerDes data rate 56G to 112 Gbps (PAM4/PAM8)
- 50-100 Tbps Device bandwidth
- ~4Gbps High Bandwidth Memory (HBM) to enable AI
- 8+ High HBM Cube on each 2.5D Package
- Interposers > 65nm to 40 nm
- ABF Package → Core Routing, Transition to 2.1D
Material Cost of Yield Loss is >90%

- Silicon content in Networking device is >90% of total cost
- This will grow larger for 7nm and 5nm
Three Questions to the Supply Chain

1. Is OSAT/Foundry willing to invest Fab like yield tools?

2. Will there be Sufficient capacity/reliability of supply?

3. How will Cost of Excursions & Misprocessing be handled?
Call to Action to Enable the Supply Chain of 2022

- Upgrade assembly yield management to Fab level, Big data
- Develop µ-bump Probe & Test Technologies for improved yield
- Develop substrates for low loss mmWave channels on large packages
- Develop Low-cost Thermal solutions to reduce End-customer’s System Cost
- Need multiple Suppliers for Silicon Content, Packaging Raw Material, Substrates & Assembly, to maintain Business Continuity