

Package Advancement to Enable Artificial Intelligence, Autonomous Cars and Wearables in Near Future: Cost and Implications to Supply Chains

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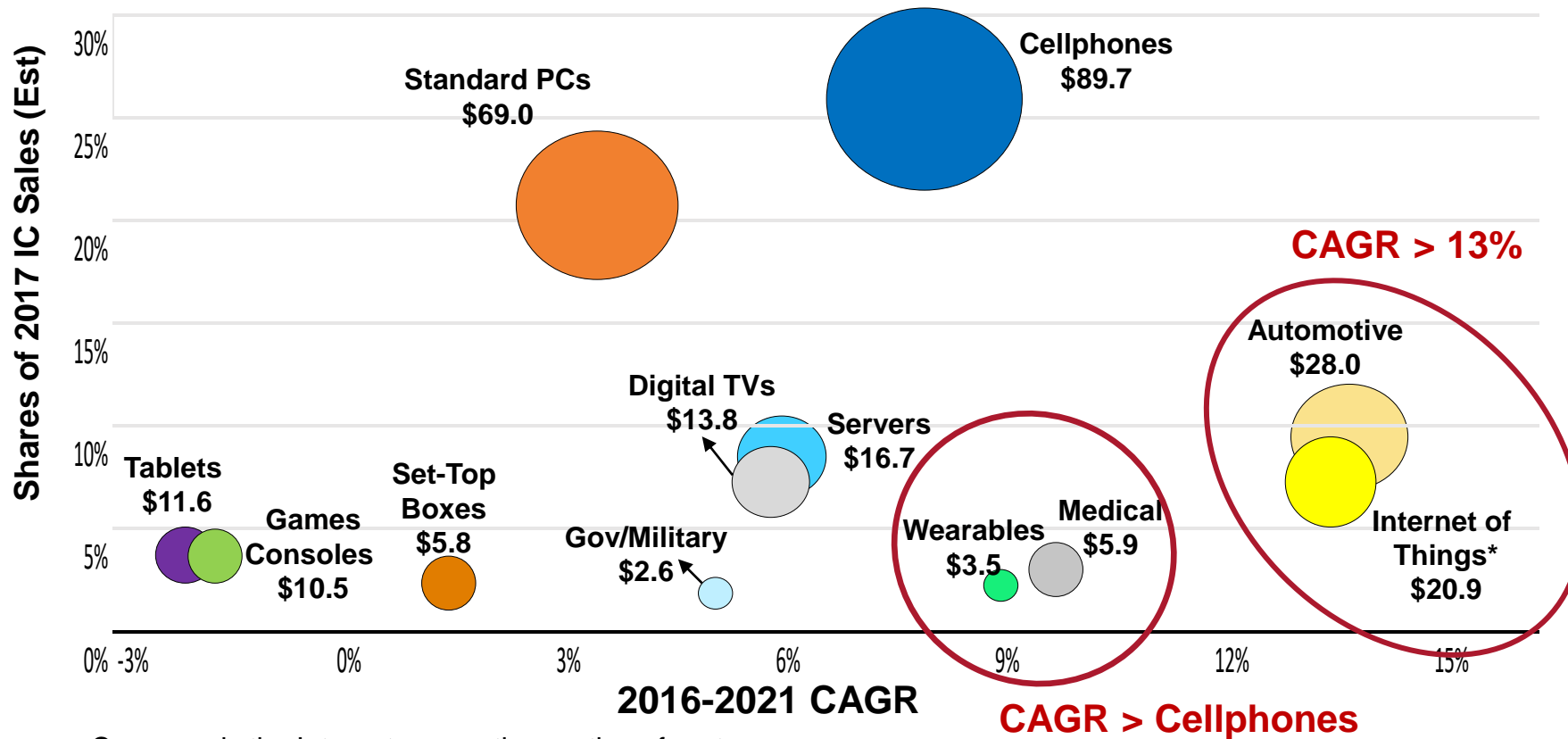
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May 30, 2018



Growth Drivers for Semiconductor Industry through 2022

IC End-Use Markets (\$B) and Growth Rates



• Covers only the Internet connection portion of systems

Source: IC Insights

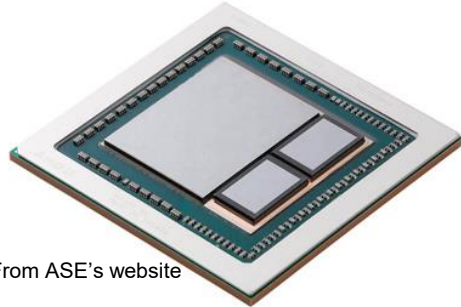
**Network Infrastructure, AI, Storage
Fueled by Advanced Package Technology**

Implications for 2019-2022

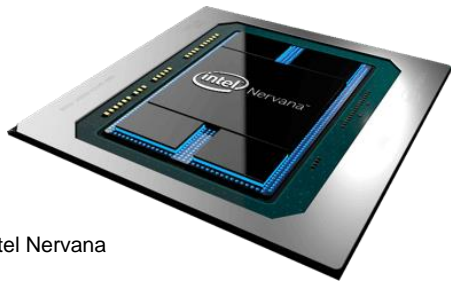
- IP traffic will be ~3X-4.6X (peak hours)
- Wireless and Mobile >63% of total IP traffic
- Pervasive 5G Networks
- Systems and Devices need to be ready
- IC Packaging to be a Key Enabler

Integration through IC Package for Performance Scaling

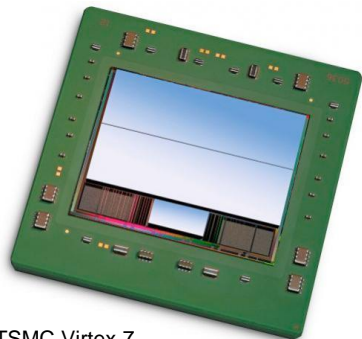
ASIC + High Bandwidth Memory Integration



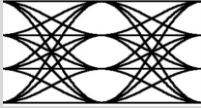


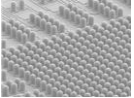

From ASE's website



Intel Nervana



Xilinx/TSMC Virtex-7

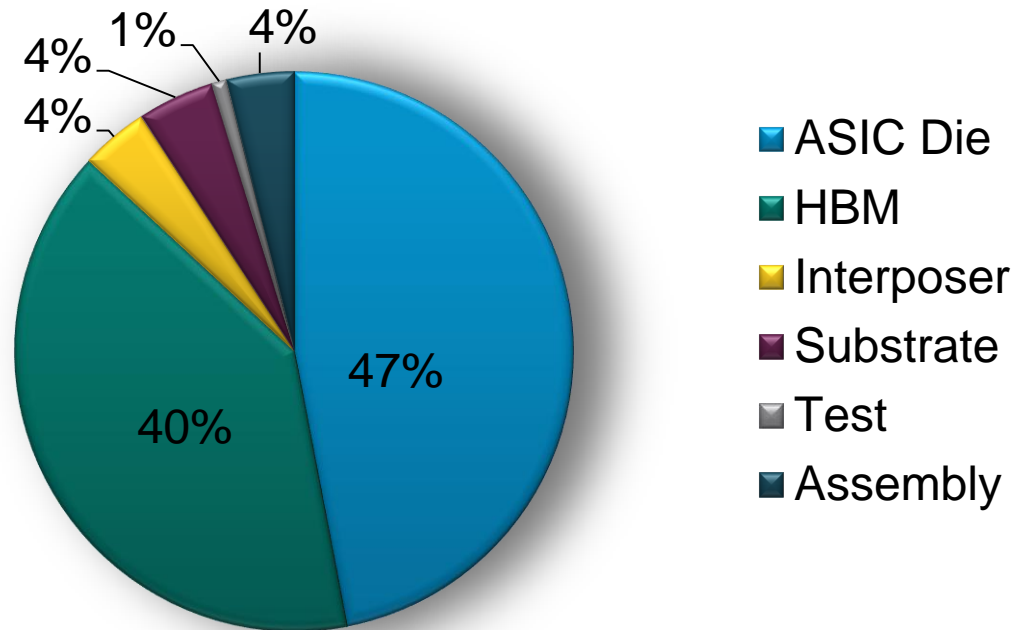
<i>IC Package Need</i>	<i>2018</i>	<i>2022</i>	<i>Challenges</i>
Data Rate 	56 Gbps	112 Gbps	<ul style="list-style-type: none"> • Channel Insertion Loss & Return Loss • Crosstalk • Power Integrity
Body Size 	67.5mm x 67.5 mm	> 90mm x 90mm	<ul style="list-style-type: none"> • Package Warpage • Board Level Reliability • Socket Cost & Performance Penalty
2.5D Integration 	Up to 5 dies	More/Larger dies (incl. Optical)	<ul style="list-style-type: none"> • Interposer Reticule Size • Assembly challenges • More Memory BW
Micro-bump Pitch 	40um	<=30um	<ul style="list-style-type: none"> • Assembly challenges • Routing challenges
Power Dissipation 	300 W	> 500 W	<ul style="list-style-type: none"> • Thermal Interface Material • Heatsink Solutions

Challenges on IC & Package Engineering

- IC Designs at 7nm, 5nm, full reticle size
- ASICs, Internal designs & Merchant Silicon- Mix
- SerDes data rate 56G to 112 Gbps (PAM4/PAM8)
- 50-100 Tbps Device bandwidth
- ~4Gbps High Bandwidth Memory (HBM) to enable AI
- 8+ High HBM Cube on each 2.5D Package
- Interposers > 65nm to 40 nm
- ABF Package → Core Routing, Transition to 2.1D

Material Cost of Yield Loss is >90%

Typical 2.5D Device Cost Breakdown in 2018



- Silicon content in Networking device is >90% of total cost
- This will grow larger for 7nm and 5nm

Three Questions to the Supply Chain

1. Is OSAT/Foundry willing to invest Fab like yield tools?
2. Will there be Sufficient capacity/reliability of supply?
3. How will Cost of Excursions & Misprocessing be handled?

Call to Action to Enable the Supply Chain of 2022

- Upgrade assembly yield management to Fab level, Big data
- Develop μ -bump Probe & Test Technologies for improved yield
- Develop substrates for low loss mmWave channels on large packages
- Develop Low-cost Thermal solutions to reduce End-customer's System Cost
- **Need multiple Suppliers for Silicon Content, Packaging Raw Material, Substrates & Assembly, to maintain Business Continuity**