

Heterogeneous Integration & SiP

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Dr. Harrison Chang

ASE Group

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Convergence of Packaging and System Integration







From Single Building to Metropolitan





SiP – Dual Direction of Design Solutions

Component Counts



* System in Package-intelligent design



SiP Design Flow: Integrating w/IC & System



Targeting for High Density (FOCoS/2.5D) Want fast and optimized RDL

Targeting for Hybrid Integration (SiP, DECA, Embedded aEASI/SESUB) Want to minimize iteration & accurate DRC

* System in Package-intelligent design



Design Challenges

- Tangible Benefit for Integration
 - Performance, Cost, TTM
- System and Component Specs Met when Co-exited in Package
 - Power, PI, Thermo, Wrapage, SI, RF, MEMS, ...

- D4M, Yield
- Test
- Reliability for Applications
- Co-Design Among Designers from IC, Package, and System
- Co-Design with Multi-physics Considerations, Simulations





SiP-id for High Density Design

Advantages of SiP-id for high density package design

- ✓ Import chip netlist
- ✓ Design operations
- ✓ Design rule checking





SiP-id for Hybrid SiP Design





Discussion

- What is the state of the art in co-design?
 - Co-design among designers from IC, package, and system
 - ✓ Co-design with multi-physics considerations, simulations
- What are the key challenges that need to be overcome?
 - Tangible benefit for integration
 - Performance, Cost, TTM
 - ✓ System and component specs met when co-exited in package
 - Power, PI, Thermo, Wrapage, SI, RF, MEMS, ...
 - 🗸 D4M, yield
 - 🗸 Test
 - Reliability for applications
- What needs to happen for these challenges to be overcome?

✓ An Design Flow that integrates these element, and is agreed across the IC, packaging, and system industries



