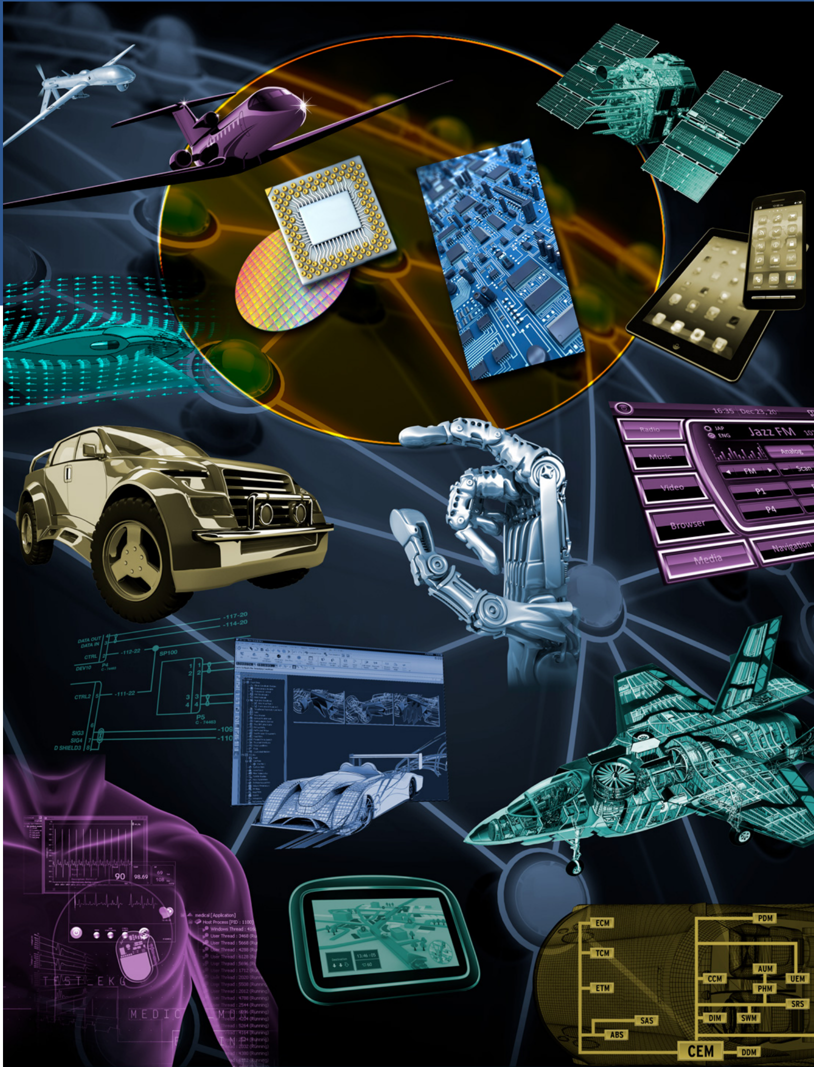

Thermal Sign-Off Analysis for Advanced 3D IC Integration

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Topics

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- Issues with Existing Solutions
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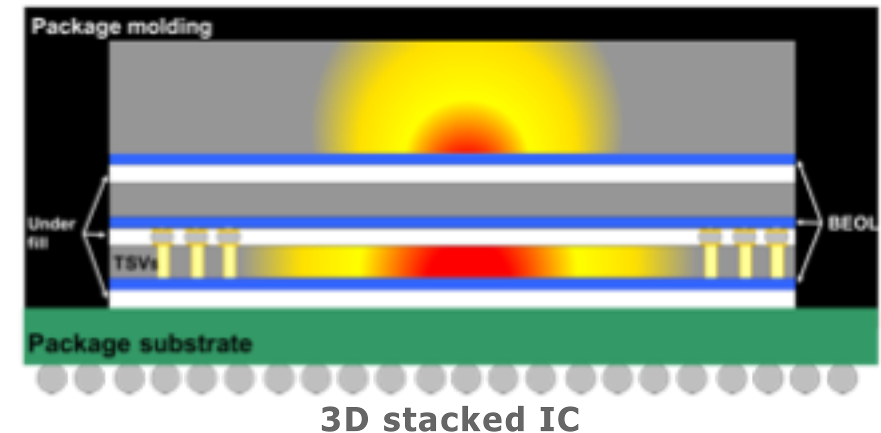
Thermal Challenges

- Thermal issues in 3D ICs:
  - Higher power density
  - Heat removed through stacked dies
  - Die bonding *increases* vertical thermal resistance
  - Thinned dies *increases* lateral thermal resistance
  - Non-homogeneous distribution of 3D connections

Thermal-related issues

- Dies are becoming more non-uniform in temperature; and

- Dies thermally interact: self-heating is augmented by neighbouring die



3D stacked IC

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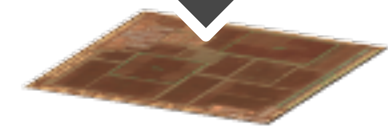
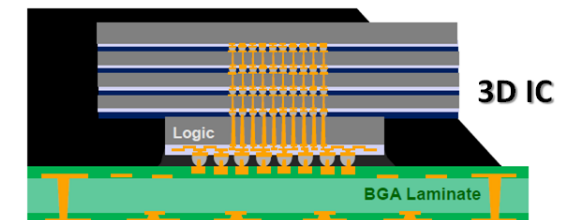
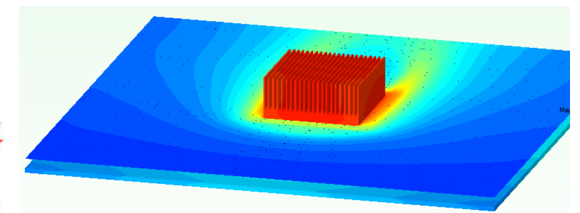
Issues with Existing Solutions (CAE-Leti view)

- "Gaps" in the two main thermal analysis flows:

1. Traditional FEM/CFD/Multiphysics simulation tools
   - Model setup is complex
   - No support for the ASIC design flow
   - Generally unable to handle complexity of analysis:
   - Number of discrete objects, sources etc.
   - Meshing challenges
   - Long solution times

2. ASIC design flow:
   - Poor or no support for 3D integration
   - Limited/simplistic support for package
   - Inaccurate representation of package boundary conditions



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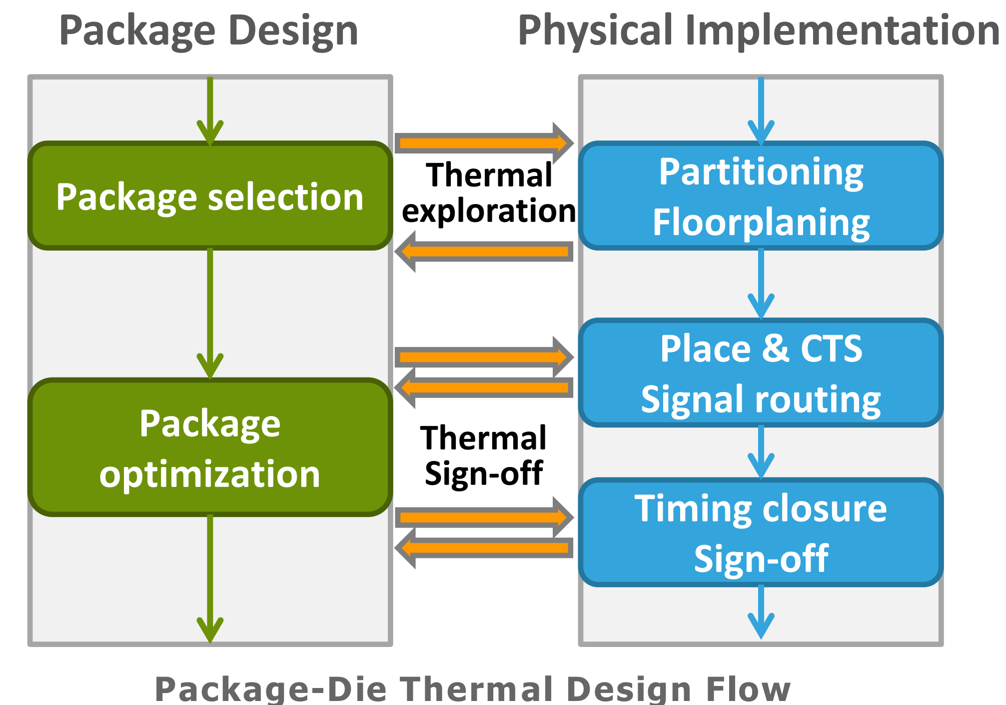
Thermal Analysis Flow Requirements

- Main objective is to support the IC design flow:
  - Aim to get best overall design, or at least a design that works
- Detailed die-level thermal analysis needs an accurate package model and boundary conditions
  - Heat does not respect packaging levels!
- From **Design Exploration** in early design…
  - Requires speed and agility
- … To final **Sign-Off**
  - Requires both high accuracy and automation
- UX: Must be compatible with 3D integration technology and integrated into the ASIC design flow.



Package-Die Thermal Design Flow

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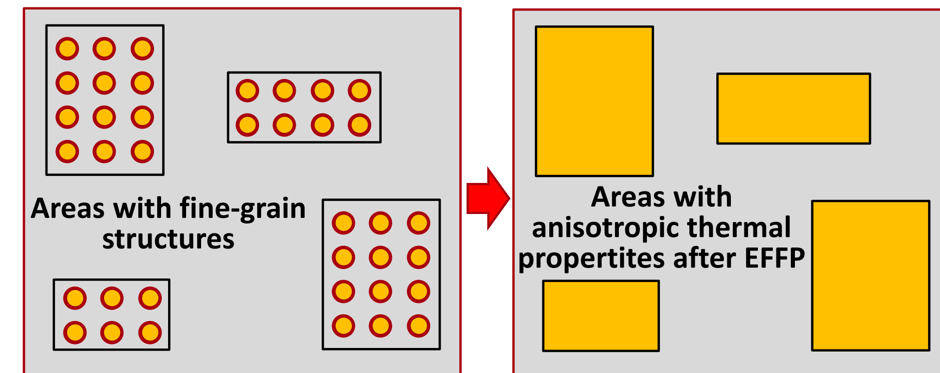
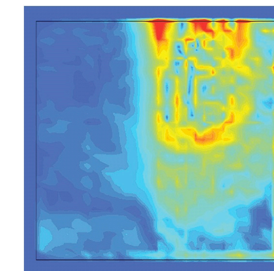
Accuracy and How to Achieve it

- Effective Thermal Property Extraction from layout (EFFP)
  - Compute equivalent anisotropic thermal properties to reduce thermal model complexity
  - Dramatic reduction of geometry count leads to significant simulation speed up
  - Adjustable granularity for accuracy vs. CPU time trade-off
- Support for IPF: from gate-level/device-level power analysis
  - Fine-grain power maps to capture hotspot effects
  - Automatic compression of power sources in very high instance count designs to accelerate simulation
- Automation
  - Automatic constraint checks to avoid error-prone and time-consuming manual verification of thermal constraints
  - Fast, automatic gridding and automatic time step generation for thermal analysis



EFFP: reduces model complexity and accelerates simulations



Hotspots in non-uniform power distribution captured in gate-level thermal analysis

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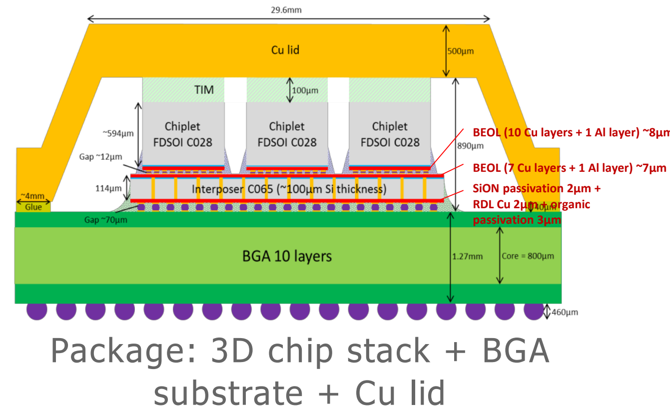
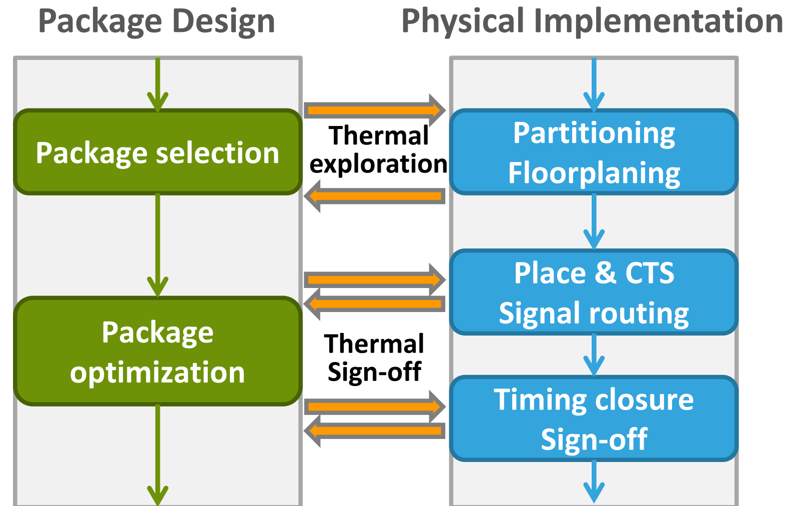
Early Co-Design: Design Space Exploration

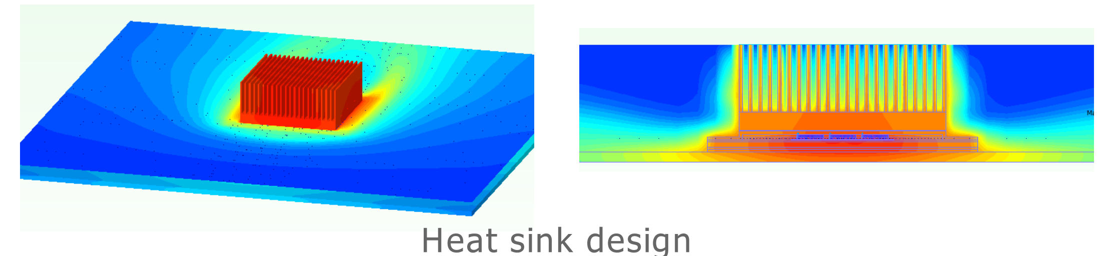
- IC:
  - 3D partitioning,
  - Chiplet placement
  - Die-die interface layer design
  - Block and TSV floorplans,
  - Package selection



Package: 3D chip stack + BGA substrate + Cu lid



- Package/Board/Heatsink:
  - Package I/O connection to board layers
  - Package design exploration (e.g. copper lid)
  - Optimization of TIM layers
  - Heatsink design (e.g. base thickness).



Heat sink design

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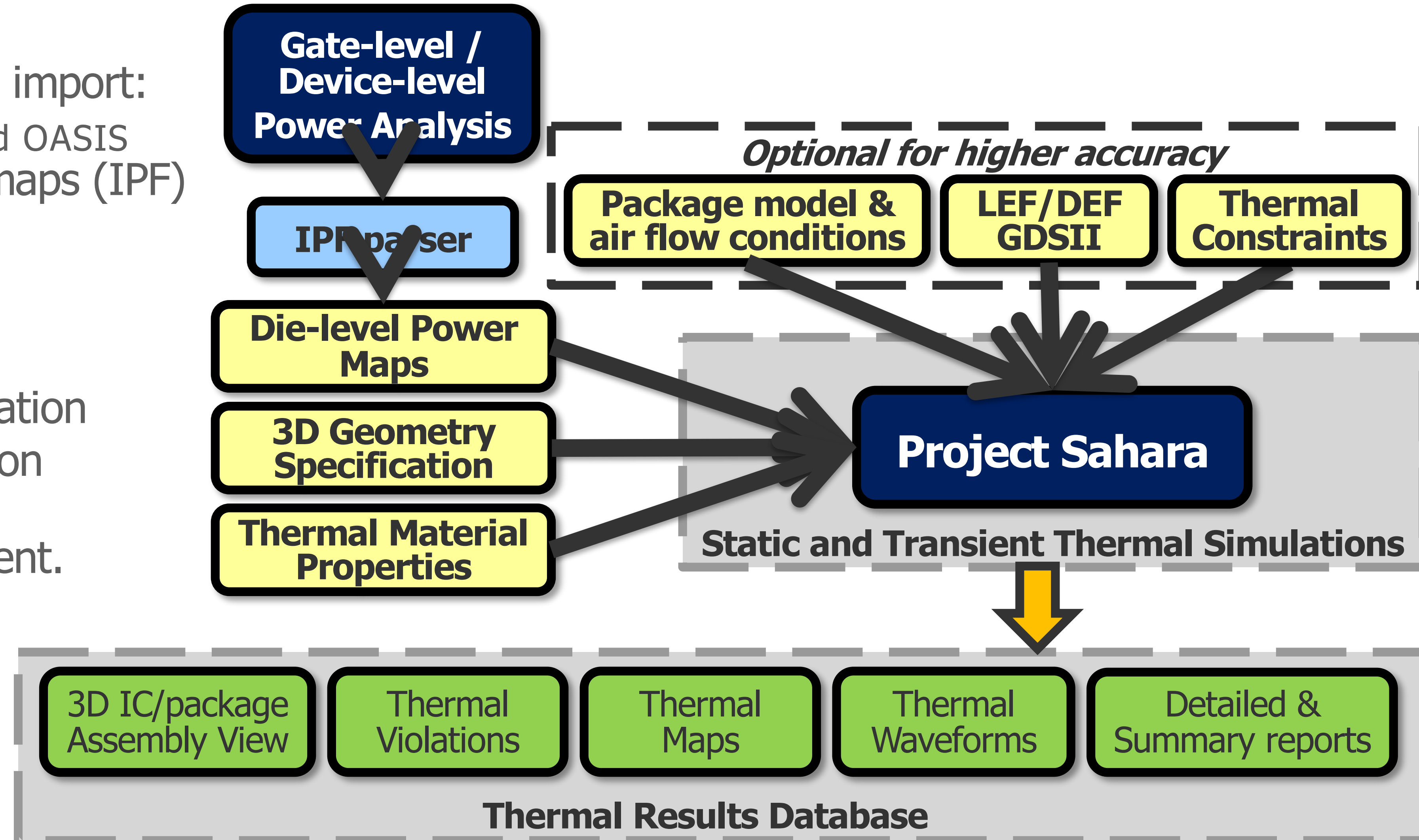
Late Co-Design: Refinement & Design Optimization

- IC:
  - Detailed die layout import:
    - LEF/DEF, GDS and OASIS
  - Fine-grain power maps (IPF)
  - Gate-level thermal simulations
- Package:
  - Detailed representation
  - material optimization
  - Transient analyses
  - Thermal environment.



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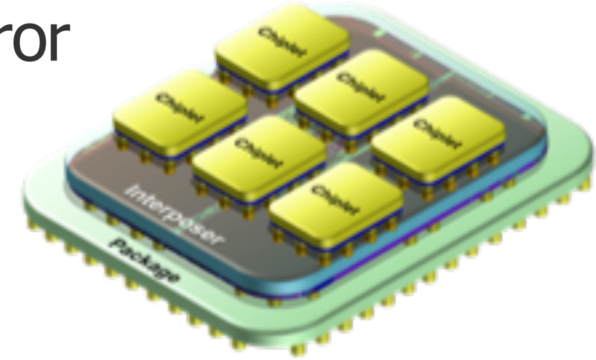
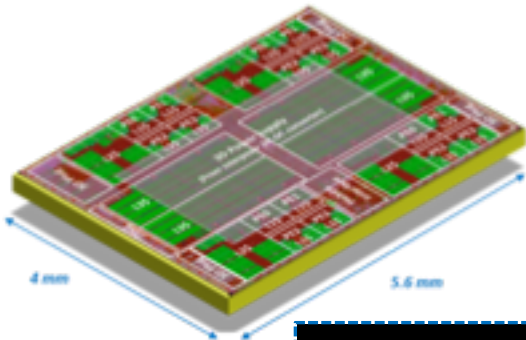
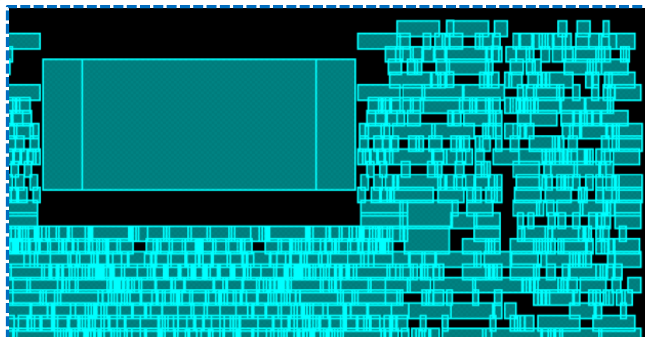
Project Sahara Example from CEA Leti

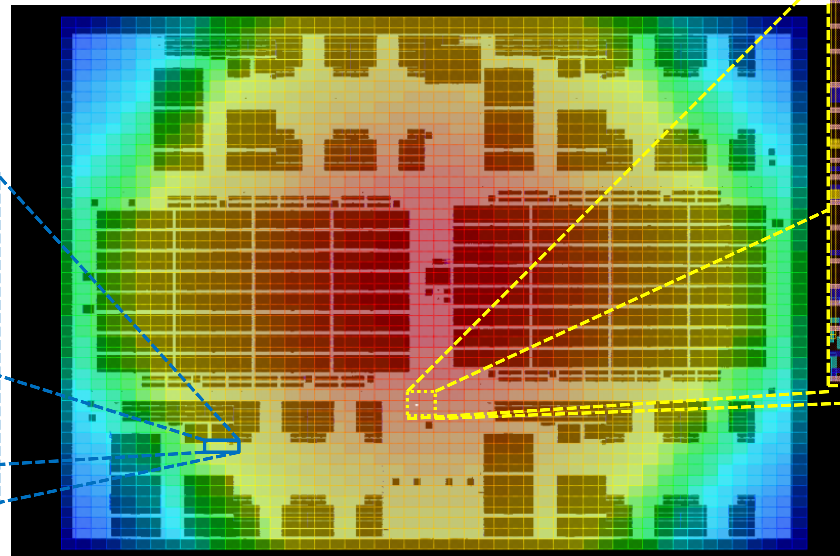
- 3D 4G Telecom network-on-chip example: 4% worst case error
  - 150,000 3D structures (TSVs, µ-bumps) in 9 layer BEOL ~30 mins
  - Convert IPF power maps (20M instances; ~3M per file) <2 mins
  - Thermal simulation of complete packaged 3D IC ~50 mins



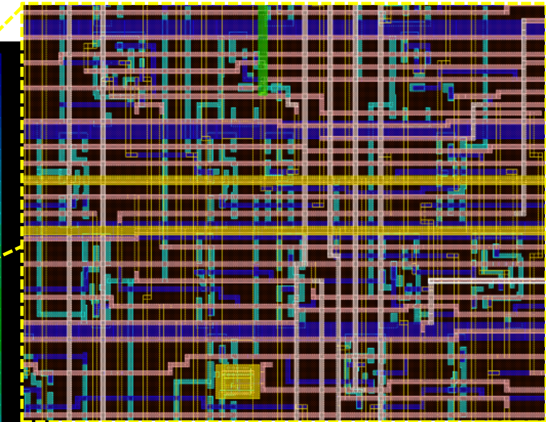




Detailed gate-level power maps



Chiplet: Calibre thermal results database



Original detailed layout (BEOL)

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Questions Answered(?)

1. What is the state-of-the-art in co-design?
   - For IC/package thermal co-design, broadly what has been covered here
   - Thermal IC/package co-design is moving from research into use in design
   - Fast, fine-detail analysis is possible
   - High level of automation can be achieved in both simulation and rule checking
2. What key challenges need to be overcome?
   - Technically, thermal co-design is feasible today
   - Main challenge is awareness raising:
   - Need to do thermal design is often not recognized (until it is too late)
   - After 30 years, people are still using Θ_{JC} in hand calculations for system design
3. What needs to happen for these challenges to be overcome?
   - IEEE Heterogeneous Integration Roadmap will help raise awareness of the challenges, and give pointers to possible solutions.

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