2018 ECTC Panel Session

IC/Package Co-Design of Heterogeneous Integrated Systems

Multi-Physics and Multi-Scale Modeling

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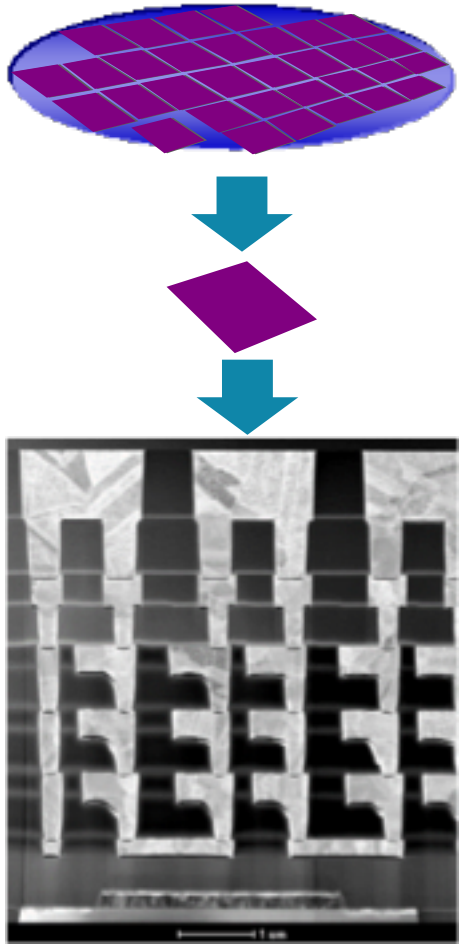
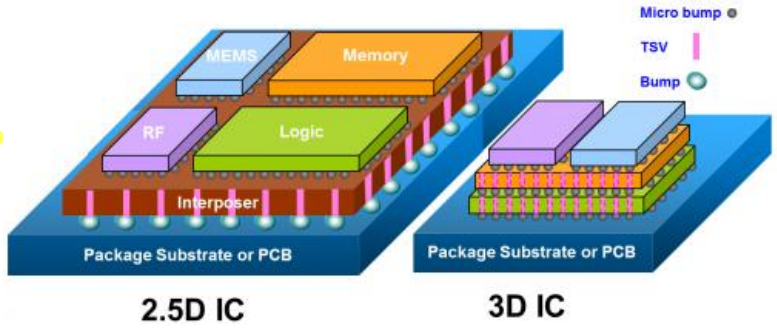
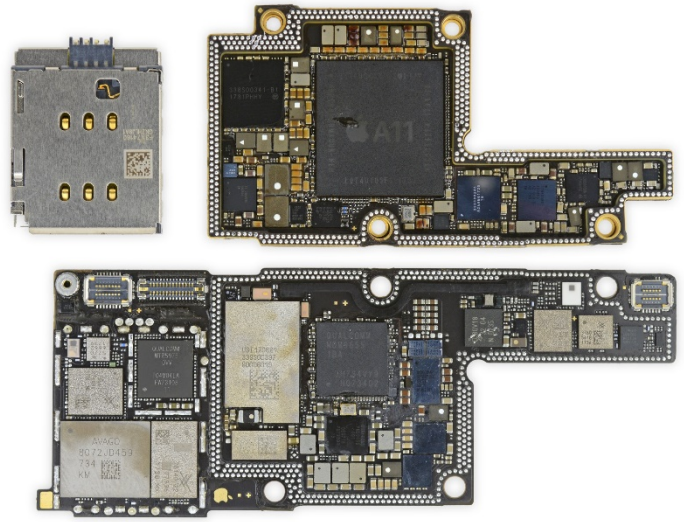
Wafer, Package, Board and System Levels



Wafer Fabrication & Backend Process

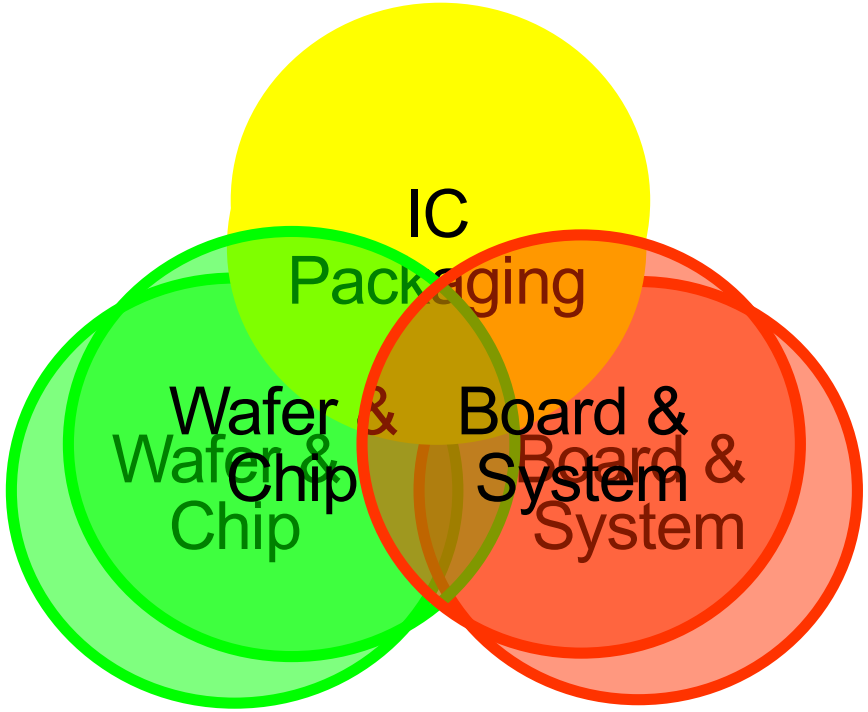


Electronic Packaging



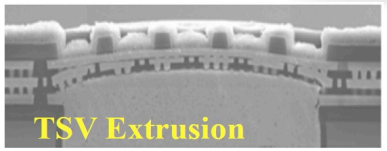
Board and System

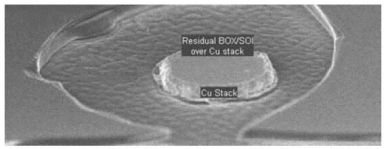
Wafer, Package, Board & System Levels

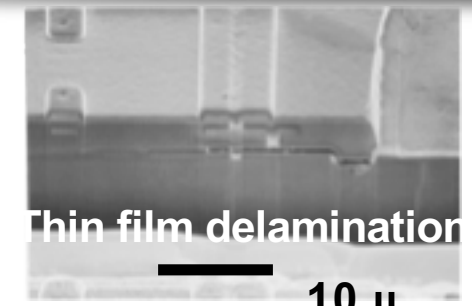


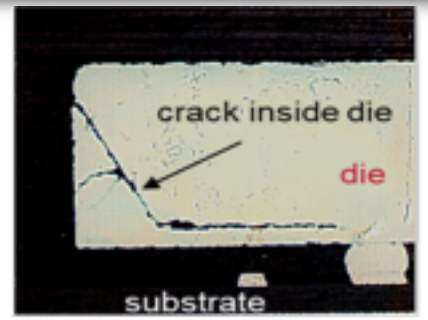
- **Design of a package must consider the interactions among wafer, package, and board (e.g. CPI – chip-package-interaction).**

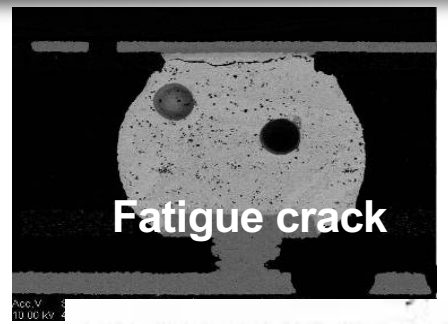
Typical Failures under Various Stresses





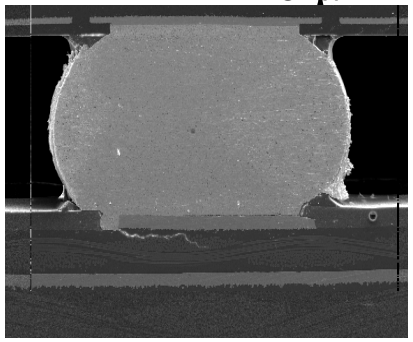


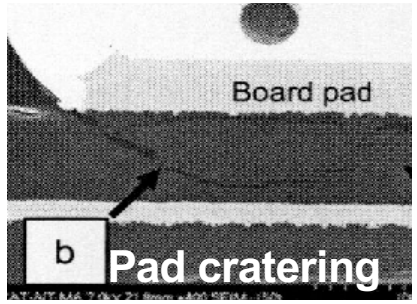


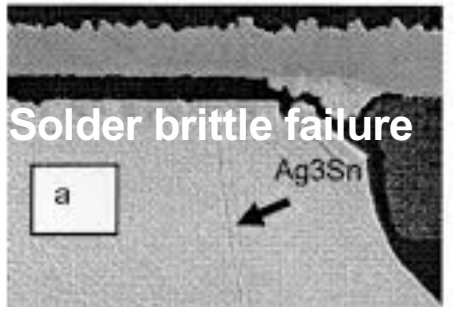


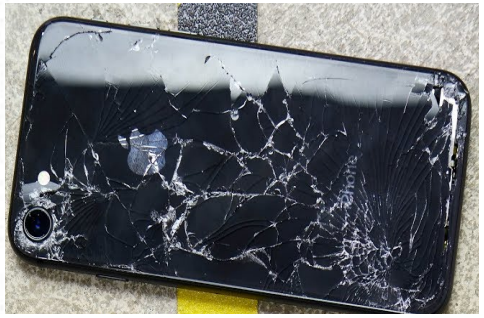
Temperature load

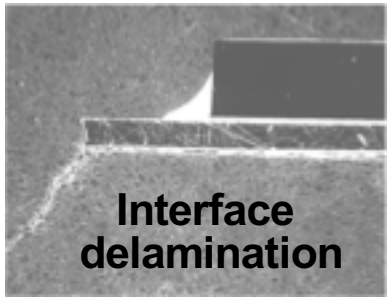
Mechanical load

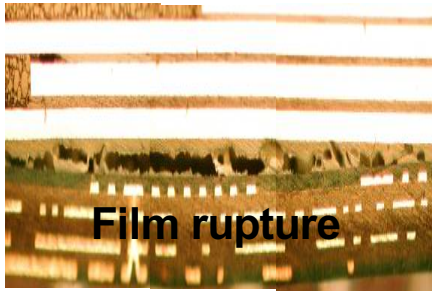


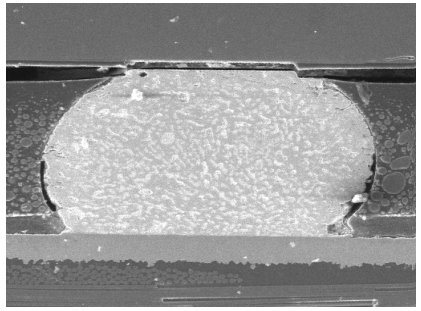


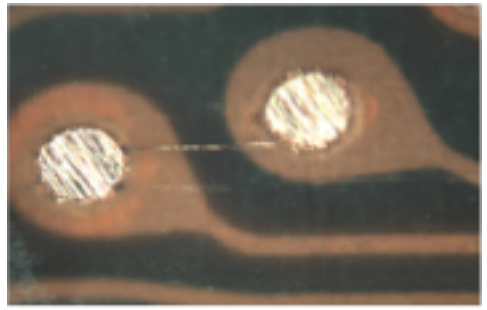






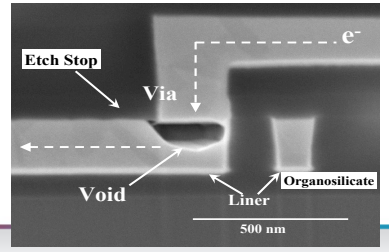


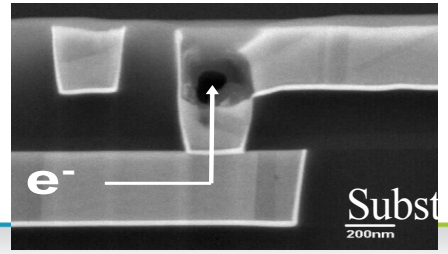


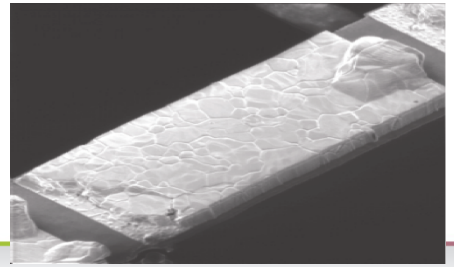


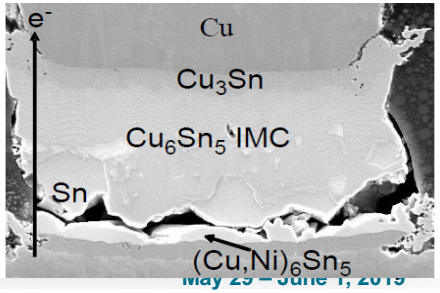
Moisture load

Electrical current

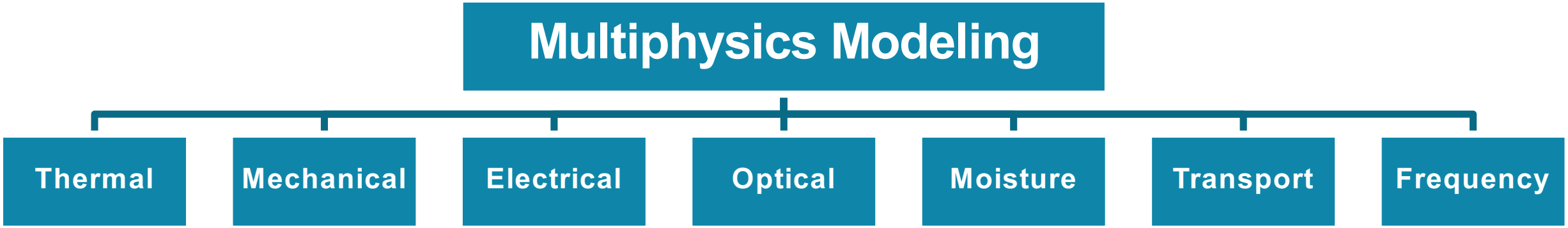








Need for Multiphysics Modeling



An example – electromigration modeling

$$J_v = -D_v \nabla C_v - D_v C_v \frac{Z^* e \rho \vec{j}}{k_B T} - D_v C_v \frac{\Omega}{k_B T} \nabla \sigma - D_v C_v \frac{Q^*}{k_B T} \nabla T$$

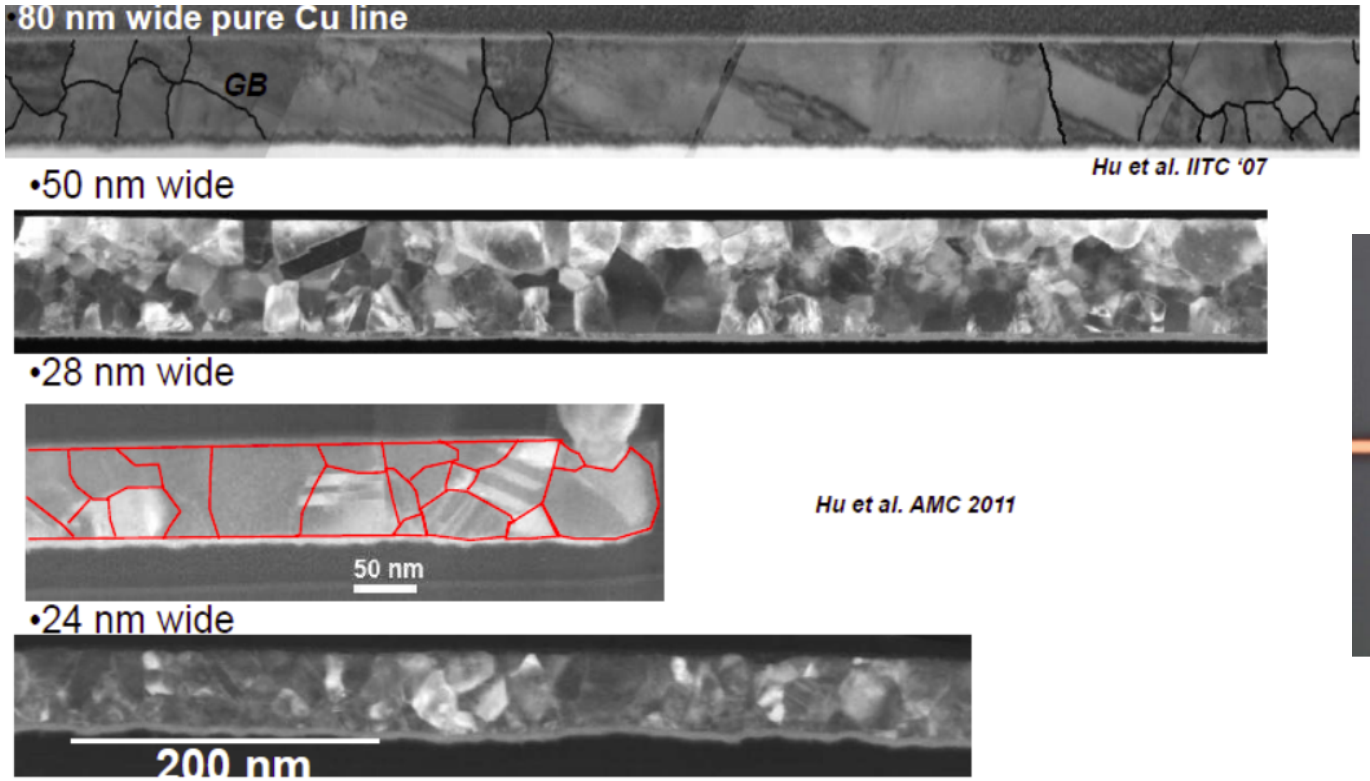
electron wind

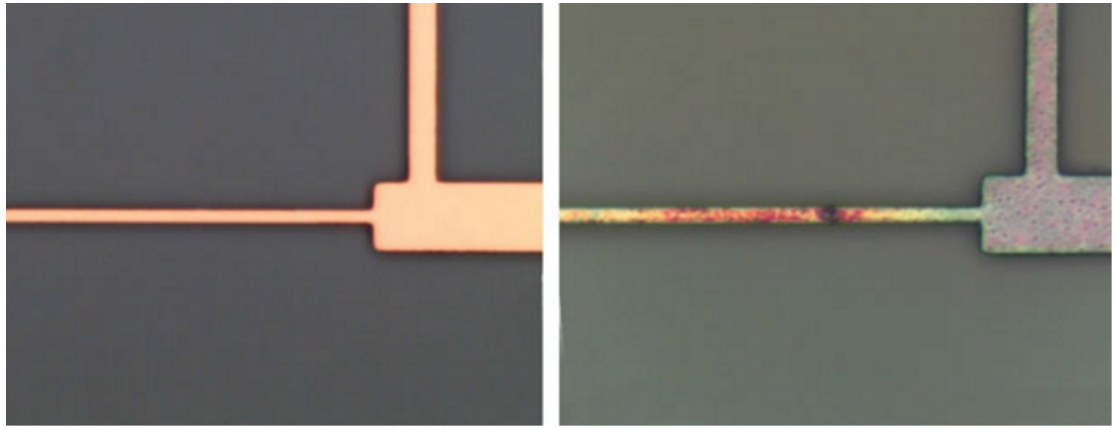
temperature gradient

chemical-potential

stress gradient

Need for Nano-Scale Modeling

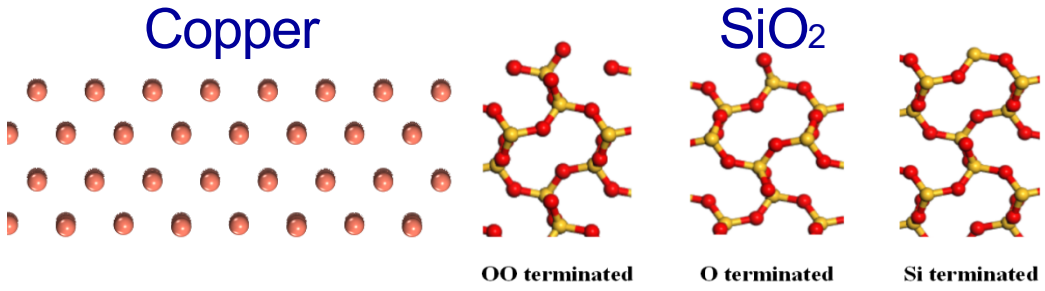


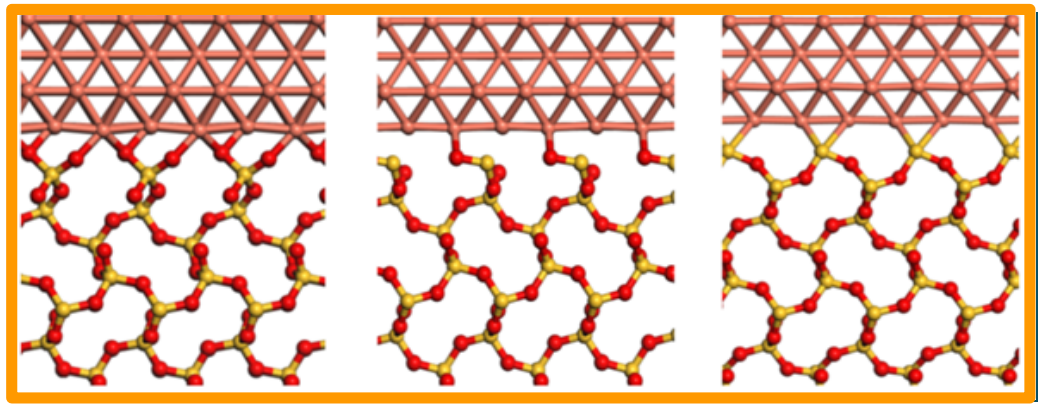


- Today's 14-nanometer-node processors contain more than 10 km in the same area.
- Today's solution is to deposit copper interconnects within trenches lined with 2-nanometer-thick walls of tantalum nitride.
- At 0.3 nm, graphene might be an option.

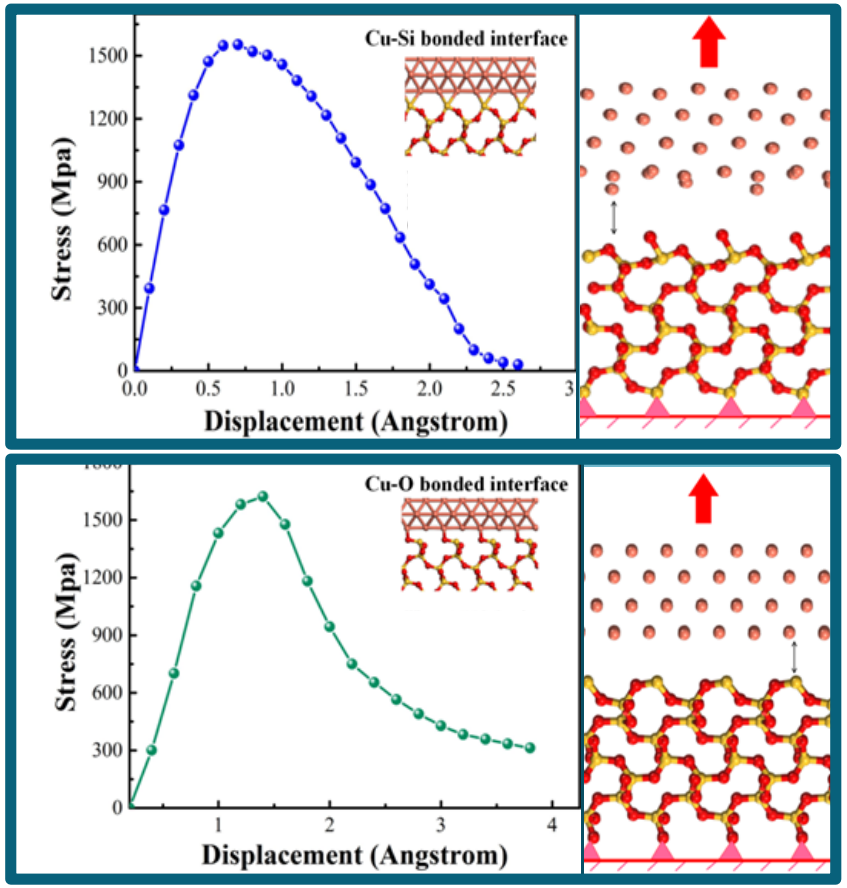
CK Hu, Impact of impurities, liner, Co cap and short length on electromigration in Cu damascene lines, 2014 Stress Workshop, Austin.
SJ Yoon, Improved electromigration-resistance of Cu interconnects by graphene-based capping layer. 2015 VLSI Technology (VLSI Technology)

Multi-Scale Modeling

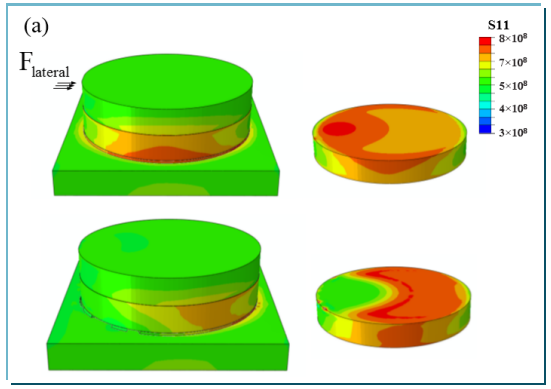




First principles simulation



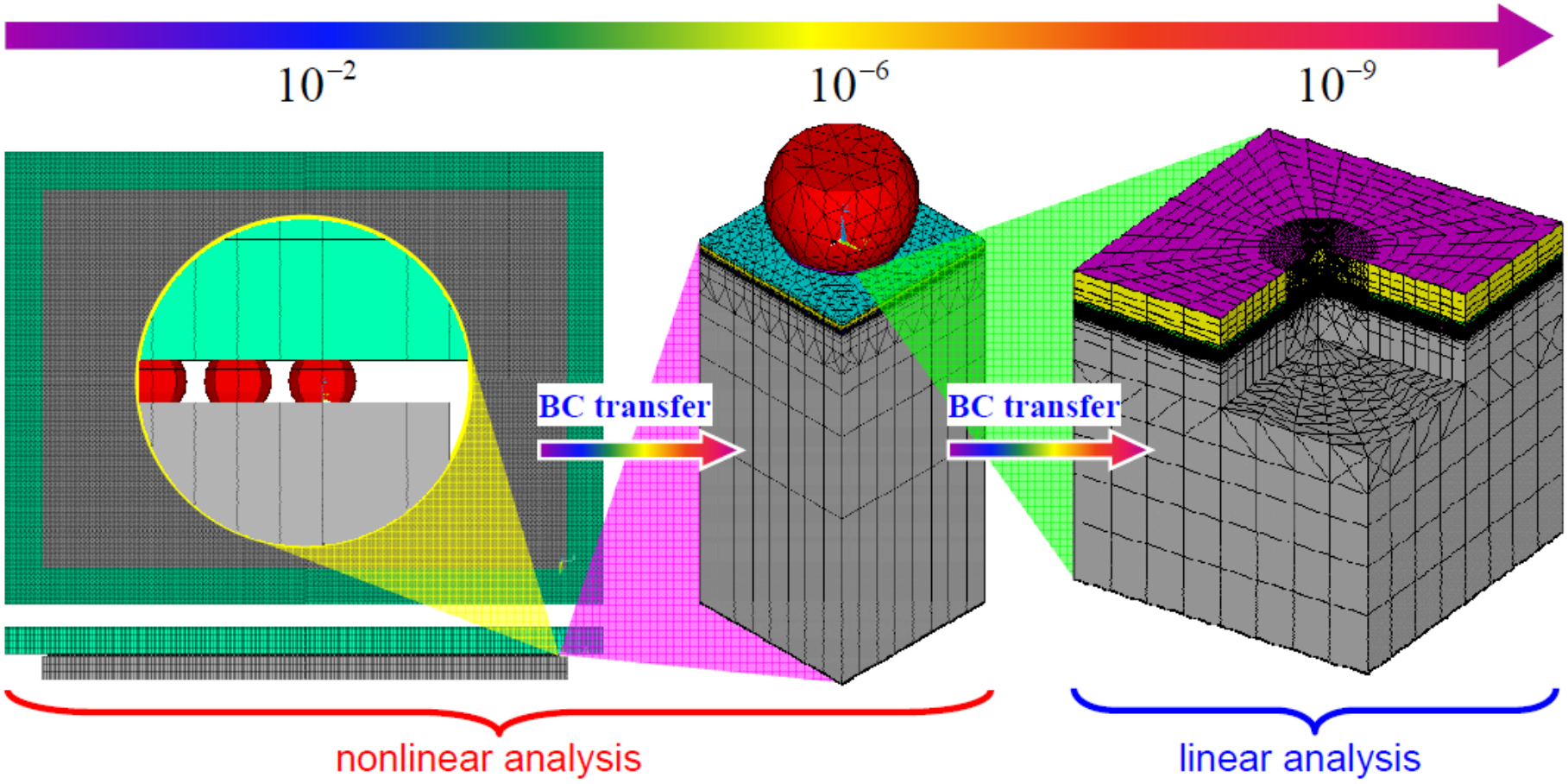
Molecular dynamics simulation



Finite element simulation

Z Cui, X Chen, X Fan, GQ Zhang, Interfacial Properties of Cu/SiO2 using a Multiscale Modelling Approach in Electronic Packages, EuroSimE 2018.

State of the Art: Multilevel Submodeling Technique



- Multilevel models are chained to obtain the driving force for delamination.
- Thousands of lines in ANSYS APDL codes have been written for the model.
- Typical model has one million DOF and takes a few hours to solve.

XH Liu, TM Shaw, G Bonilla - Advanced Metallization Conference, 2010 - sematech.org

Summary

- **The state of the art**
  - Multiphysics modeling software available.
  - Open source code for materials modeling at each scale available.
- **Key challenges that need to be overcome to enable**
  - Fundamental theory on constitutive relationship.
  - Characterization of material properties at different scales.
  - Bridging among different scales.
- **What needs to happen to overcome these challenges?**
  - Develop fundamental constitutive theory for material behavior.
  - Develop theory and implementation for multiscale modeling.
  - Develop micro-/nano-scale material characterization techniques.