Conference Program
& Exhibitor Listings

Don't miss out on electronic packaging's premier conference!

ECTC 2014

The 64th Electronic Components and Technology Conference

May 27-30, 2014

The Walt Disney World Swan & Dolphin Resort
Lake Buena Vista, Florida, USA

Sponsored by:

CPMT
IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

IEEE

For more information,
visit: www.ectc.net

WELCOME FROM THE MAYOR OF ORANGE COUNTY

ORANGE COUNTY MAYOR
TERESA JACOBS

P.O. BOX 1393, 201 SOUTH ROSALIND AVENUE, ORLANDO, FL 32802-1393
PHONE: 407-836-7370 • FAX: 407-836-7360 • Mayor@ocfl.net

May 2014

Dear friends,

As mayor of Orange County, I am pleased to extend a warm welcome to the Electronic Components and Technology Conference!

Orange County has much to offer to help make your event memorable. Most significant, last year we hosted more than 57 million visitors. Aside from our beautiful Florida weather, we are home to more than 90 attractions and exciting theme parks, a world-class convention center, an award winning international airport, more than 150 world-renowned golf courses, a wide variety of sports events, fine museums, great shopping, cultural activities and many natural wonders which makes our region unique.

Additionally, our region is also home to top rated higher education institutions, the second largest convention center in the nation and a burgeoning community of biotech, life sciences and research facilities, which have been recognized around the world for its forward thinking success. We are very proud of being a major international destination.

It is my hope that you enjoy your time with us and wish you much success during your stay!

Sincerely,

Teresa Jacobs

WELCOME FROM ECTC GENERAL AND PROGRAM CHAIRS

On behalf of the Program Committee and Executive Committee, it is our pleasure to welcome you to the 64th Electronic Components and Technology Conference (ECTC), held at the Walt Disney World Swan and Dolphin Resort in Lake Buena Vista, Florida from May 27-30, 2014. This premier international conference is sponsored by the IEEE Components, Packaging, and Manufacturing Technology Society (CPMT).

The ECTC Program Committee has selected more than 300 papers that will be presented in 36 oral sessions and 5 interactive presentation sessions including one student interactive presentation session. The oral sessions will feature selected papers on 3D and TSV technologies, wafer level packaging, electrical and mechanical modeling, RF packaging, system design, and optical interconnects. Session topics will cover advanced packaging technologies, material development and characterization, reliability, assembly and manufacturing, and interposers. Four interactive presentation sessions showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Similarly, the student interactive presentation session will focus on the research being done at academic institutions around the world by emerging scientists and engineers. The Program Committee has created sessions that cover the ongoing technological challenges of established disciplines as well as addressing emerging topics of interest to the industry. Authors from companies, research institutions, and universities from more than 25 countries will present their work at ECTC, illustrating the conference's global focus.

ECTC will also feature panel and special sessions with industry experts covering a number of important and emerging topic areas. On Tuesday, May 27 at 10 a.m., Karlheinz Bock will chair a session entitled "Flexible Electronics - Packaging Technology and Application Trends" where a panel of experts will discuss the recent advancements and market perspectives for this emerging technology area. Tuesday at 2 p.m., Manos Tentzeris will chair a special session sponsored by the Electronic Components & RF technical subcommittee on "Wireless Power Transfer Systems." The ECTC Panel Discussion, "Emerging Technologies and Market Trends of Silicon Photonics," will be chaired by Ricky Lee and Jie Xue and features panelists from various segments of the industry to discuss the growing influence of photonics technologies on microelectronic systems. Nancy Stoffel will chair the ECTC Plenary Session titled "Influence of Packaging on System Integration and Performance" on Wednesday evening at 7:00 p.m. where a panel of experts will discuss system integration and the role that component packaging technologies play. On Thursday evening at 8:00 p.m., the CPMT Seminar titled "Latest Advances in Organic Interposers" will be moderated by Kishio Yokouchi and Venky Sundaram.

Supplementing the technical program, ECTC will also offer several Professional Development Courses (PDCs) and the Technology Corner Exhibits. ECTC will offer 18 PDCs for 2014, covering a wide array of technical areas and organized by the PDC Committee chaired by Kitty Pearsall. The PDCs will take place on Tuesday, May 27 (8:00 a.m. – 5:15 p.m.) and are taught by distinguished experts in their respective fields. The Technology Corner Exhibits will showcase the latest products and technologies offered by leading companies in the electronic components, materials, packaging, and services fields. Technology Corner Exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions. We are pleased to announce that Dr. Peter Bocko of Corning Glass Technologies will give the invited keynote talk at the ECTC Luncheon on Wednesday.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something for everyone in the packaging industry. We would like to take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, program committee members, as well as all the volunteers who have helped to make the 64th ECTC another resounding success. Once again, thank you for being a part of the 64th ECTC.

Wolfgang Sauter
General Chair
IBM Corporation

Alan Huffman
Program Chair
RTI International

WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of CPMT, it is my great pleasure and privilege to welcome you to ECTC 2014 in beautiful Orlando! I'm thrilled to welcome you here, at the award-winning Swan and Dolphin Resort, a heartbeat away from the Walt Disney World Resort – after all, this is the happiest place on earth.

Our magic journey started 64 years ago. Today, ECTC has become the premier international conference where professionals not only get an all-inclusive look at every side of our industry, but also share research and development in technological breakthroughs across a wide range of semiconductor packaging, electronics devices, design, materials, manufacturing, and modeling.

In the Disney spirit of celebrating today and imagining the future, ECTC 2014 opens at a great venue and promises an excellent program.

As the sponsor of ECTC, CPMT presents these program highlights:

- On the evening of Tuesday, May 27, Ricky Lee and I will lead a CPMT panel discussion on "***Emerging Technologies and Market Trends of Silicon Photonics.***" Thought leaders from the entire eco-system in the industry including research academic institutes will discuss opportunities, challenges, and industry readiness on Silicon Photonics, as this hot topic has attracted a lot of attention over the past few years.
- To encourage diversity and networking, CPMT will continue hosting **networking tables for women** during the Wednesday and Thursday luncheons.
- On Thursday, May 29, CPMT will sponsor an **award luncheon session** to present several prestigious IEEE and CPMT awards.
- And during the evening of Thursday, CPMT Technical Committee on High Density Substrates & Boards will continue the tradition by holding a seminar on "**Latest Advances in Organic Interposers.**" This new technology offers a great potential in the advancement of 3D IC packaging.

Finally, I would like to take this opportunity to thank our dedicated volunteers in the ECTC program committee for their hard work over the past year. Also, appreciation goes to the session chairs, authors, speakers, and exhibitors who are instrumental to making the 64th ECTC a great success. I am excited about the impact all these technical events and activities will have on the CPMT society, our industry, and our members.

Here's to four fantastic days of insights, inspiration, and ideas!

Jie Xue
President, IEEE CPMT Society

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, meals, Technology Corner exhibits, and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. Hotel "house" phones have been placed throughout the hotel and conference area for your convenience. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
The hotel does NOT allow smoking and smoking is NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, or seminars as well. Thank you for your consideration and cooperation.

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ECTC Luncheon Keynote Speaker

Wednesday, May 28, 2014
12:00PM
Northern Hemisphere D - E

Glass: The Art, Mythology and Technological Agility of a Material of the Information Age

Presenter: Peter L. Bocko, PhD
Chief Technology Officer – Corning Glass Technologies

Using glass in emerging semiconductor packaging platforms is currently being vigorously researched and debated in the electronics industry. To provide a timely perspective, three aspects of glass will be presented: glass' evolving role since antiquity, technologically in the immersive information environment, and culturally as a vehicle for artistic expression.

"A Day Made of Glass," Corning's futurist video viral hit, portrayed glass as the central medium of an "interconnectivity immersion" future with ubiquitous displays connected by unlimited bandwidth. Suddenly, glass was cool! In parallel, the art world has experienced a thriving period of glass art creativity. Glass as a versatile medium is reflected between the worlds of technology and human artistic expression.

Dr. Peter L. Bocko is chief technology officer for Corning Glass Technologies and is recognized as one of the foremost glass experts in consumer electronics. He is known for his contributions to the flat panel display revolution and is a frequently invited speaker on consumer electronics futures at industry events. As an occasional media commentator, Bocko most recently appeared in a featured role in the PBS Nova Special "Hunting the Elements" with David Pogue.

2015 iNEMI Roadmap North American Workshop

Tuesday, May 27, 2014 • 8:00AM - 5:00PM
Wednesday, May 28, 2014 • 9:30AM - 12:30PM
Oceanic 3, 3rd Floor

Since 1994, iNEMI (the International Electronics Manufacturing Initiative) has been developing a biennial technology roadmap spanning a 10-year horizon. In 2004, iNEMI expanded the initiative to proactively include global input. This year ECTC is hosting one of the several regional meetings intended to solicit input for the 2015 iNEMI Roadmap.

Open to all conference attendees.

ITRS Assembly & Packaging Work Session

Tuesday, 27 May 2014• 8:00 AM-5:00 PM
Europe 4, 3rd Floor

The International Technology Roadmap for Semiconductors (ITRS), is the fifteen-year assessment of the semiconductor industry's future technology requirements. These future needs drive present-day strategies for world-wide research and development among companies, universities, and research institutes and national labs. The ITRS Assembly and Packaging Working Group would like to invite all ECTC conference attendees to join in this work session for future semiconductor technology directions and roadmaps.

Open to all conference attendees.

REGISTRATION, RECEPTIONS AND GENERAL INFORMATION

Registration

ECTC registration will be open at the ECTC Registration Desk located in the Walt Disney World DOLPHIN Resort, conference center, 3rd floor, outside of Australia 3.

Monday, May 26, 2014 – 3:00 p.m. - 5:00 p.m.

Tuesday, May 27, 2014 – 6:45 a.m. - 8:15 a.m.*
(AM PD Courses & Special Session Only)*

Tuesday, May 27, 2014 – 8:15 a.m. - 5:00 p.m.
(All conference attendees)

Wednesday, May 28, 2014 – 6:45 a.m. - 4:00 p.m.

Thursday, May 29, 2014 – 7:30 a.m. - 4:00 p.m.

Friday, May 30, 2014 – 7:30 a.m. - 12:00 p.m.

The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45am start time on Tuesday, May 27 as registration becomes very congested prior to the start of morning Professional Development Courses.

Door Registration Fees

Joint ITHERM & ECTC	$1,100
IEEE Member Full Registration	$795
IEEE Member Speaker / Session Chair	$695
IEEE Member One Day	$525
IEEE Member Speaker One Day	$395
Exhibit Booth Attendant	$0
Non-Member Full Registration	$960
Non-Member Speaker / Session Chair	$695
Non-Member One Day	$525
Non-Member Speaker One Day	$395
Exhibit Booth Attendant	$0
Student	$300
Student Speaker	$300
Exhibits Only	$20
Tuesday Professional Development Courses IEEE Members and Non-Members	
Tuesday AM or PM Course with luncheon	$475
Tuesday All-Day Courses with luncheon	$675
Tuesday Student All-Day Courses with luncheon	$125
Extra Luncheon Tickets for each day	$50
Extra Proceedings with registration	$100

Professional Development Course Instructors' Breakfast

PDC Instructors and Proctors are required to attend a briefing breakfast.

7:00 a.m. Tuesday – PDC Instructors' and Proctors' Briefing
(Room Location: Asia 1, 3rd Floor)

Session Chairs and Speakers Breakfast

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Windows and Microsoft Office.

7:00 a.m. Wednesday thru Friday
(Room Location: Northern Hemisphere Ballroom E 3 & 4, 5th floor)

Speaker Prep Room

Speakers should prepare and review their digital presentations as follows: 7:00 a.m. – 5:00 p.m., Tuesday – Friday (Room Location: Europe 2, 3rd floor)

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

MISCELLANEOUS INFORMATION

Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Message Center
Please use the hotel switchboard or the ECTC Registration Desk located on the 3rd floor, Australia 3 Foyer, WDW DOLPHIN Resort to leave and pickup messages. The hotel number is +1 (407) 934-4000.

Press Room
Press Interviews will be scheduled on an as-requested basis. Check at the ECTC Registration Desk (Australia 3 Foyer, 3rd floor, WDW DOLPHIN Resort) to schedule an interview while onsite. You may also coordinate an interview with conference leadership or presenting technical experts by contacting Eric Perfecto at perfecto@us.ibm.com or +1 (845) 894-4400.

LUNCHEONS

Tuesday, May 27, 2014 12PM (Southern Hemisphere Ballroom I & II, 5th floor)
The Electronic Components and Technology Conference will sponsor a luncheon for all Professional Development Course attendees, proctors and PDC committee members.

Wednesday, May 28, 2014 12PM (Northern Hemisphere D & E, 5th floor)
The Electronic Components and Technology Conference will sponsor a luncheon for conference attendees. Best and Outstanding Papers will be awarded. The guest speaker will be Peter L. Bocko Ph.D. of Corning Glass Technologies.

Thursday, May 29, 2014 12PM (Northern Hemisphere D & E, 5th floor)
The IEEE Components, Packaging and Manufacturing Technology Society will sponsor a luncheon for conference attendees. The CPMT awards will be presented.

Friday, May 30, 2014 12PM (Northern Hemisphere D & E, 5th floor)
The ECTC Program Chair will sponsor a luncheon for conference attendees.

There will be a raffle for attendees.

SPECIAL SESSION, ELECTRONICS & RF SPECIAL SESSION, PANEL SESSION, CPMT SEMINAR, & PLENARY SESSION

2014 ECTC SPECIAL SESSION

Flexible Electronics – Packaging Technology and Application Trends

Tuesday, May 27, 2014
10:00 a.m. – 12:00 p.m.
Northern Hemisphere D, 5th Floor

Chair: Karlheinz Bock – Fraunhofer EMFT & University of Berlin

Speakers:
1. Vivek Subramanian, University of California-Berkeley
2. Jan Vardaman, TechSearch International
3. Christoph Kutter, Fraunhofer EMFT
4. Mitsuru Hiroshima, Panasonic
5. Nancy Stoffel, GE Global Research

2014 ELECTRONIC COMPONENTS & RF SPECIAL SESSION

Wireless Power Transfer Systems

Tuesday May 27, 2014
2:00 p.m. - 4:30 p.m.
Northern Hemisphere D, 5th Floor

Chairs: Manos Tentzeris – Georgia Institute of Technology and Craig Gaw – Freescale

Speakers:
1. Michael de Rooij, EPC
2. Lilly Huang, Intel Corporation
3. Yogesh Ramadass, Texas Instruments
4. Francesco Carobolante, Qualcomm Technologies, Inc.
5. Robert Andosca, Microgen Systems

2014 ECTC PLENARY SESSION

Packaging Influence on System Integration and Performance

Wednesday, May 28, 2014
7:00 p.m. – 9:00 p.m.
Southern Hemisphere II & III, 5th Floor

Chair: Nancy Stoffel – GE Global Research

Speakers:
1. Jon Casey, IBM Corporation
2. Stephane Lessard, Ericsson
3. Raj Master, Microsoft
4. Li Li, Cisco Systems, Inc.
5. Nozad Karim, Amkor

2014 ECTC PANEL SESSION
Emerging Technologies and Market Trends of Silicon Photonics

Tuesday, May 27, 2014
7:30 p.m. – 9:30 p.m.
Southern Hemisphere II & III, 5th Floor

Chairs: Ricky Lee – Hong Kong University of Science and Technology and Jie Xue – Cisco Systems, Inc.

Speakers:
1. Michael Watts, MIT
2. Stéphane Bernabe, CEA-Leti
3. John Cunningham, Oracle
4. Jean Trewhella, IBM Corporation
5. Peter De Dobbelaere, Luxtera
6. Madeleine Glick, APIC Corporation

2014 CPMT SEMINAR

Latest Advances in Organic Interposers

Thursday, May 29, 2014
8:00 p.m. – 10:00 p.m.

Southern Hemisphere II & III, 5th Floor

Chairs: Kishio Yokouchi – Fujitsu and Venky Sundaram – Georgia Tech

Speakers:
1. Yasumitsu Orii, IBM Japan, Ltd.
2. Suresh Ramalingam, Xilinx Inc.
3. Tadashi Kodaira, Shinko Electric Industries Co. Ltd.
4. Mitsuya Ishida, Kyocera SLC Technologies Corp.

These sessions/seminars are open to all conference attendees.

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 27, 2014

Morning Courses 8:00 AM – 12:00 PM	Afternoon Courses 1:15 – 5:15 PM
Northern Hemisphere E-1 **1. Lead-Free Solder Joint Reliability – Material Consideration** *Course Leader:* Ning-Cheng Lee – Indium Corporation	Northern Hemisphere E-1 **9. High-Frequency Modeling and Optimization of Interconnections in Electronic Packaging** *Course Leaders:* Ivan Ndip and Michael Töpper – Fraunhofer IZM
Northern Hemisphere E-2 **2. Wafer Level Packaging** *Course Leader:* Luu Nguyen – Texas Instruments	Northern Hemisphere E-2 **10. Shock - Impact Reliability of Portable Electronics** *Course Leader:* Pradeep Lall – Auburn University
Northern Hemisphere E-3 **3. Package Failure Analysis—Failure Mechanisms and Analytical Tools** *Course Leader:* Rajen Dias – Intel Corporation	Northern Hemisphere E-3 **11. Moisture and Media Influence on Microelectronic Package Reliability** *Course Leaders:* Tanja Braun and Hans Walter – Fraunhofer IZM
Northern Hemisphere E-4 **4. Next Frontier in Electronics: Systems Scaling for Smart Mobile Systems** *Course Leader:* Rao R. Tummala – Georgia Institute of Technology	Northern Hemisphere E-4 **12. 3D IC Packaging and 3D Si Integration** *Course Leader:* John Lau – Industrial Technology Research Institute
Southern Hemisphere III **5. Polymers and Nano-Composites for Electronic and Photonic Packaging: Recent Advances in Materials and Processes** *Course Leaders:* C.P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation	Southern Hemisphere III **13. Polymers in Semiconductor Packaging Including 2.5D and 3D Integration** *Course Leader:* Jeffrey Gotro – InnoCentrix, LLC
Southern Hemisphere IV **6. Power and Electronics Packaging, Reliability, and Thermal Management** *Course Leaders:* Patrick McCluskey and Avram Bar-Cohen – University of Maryland	Southern Hemisphere IV **14. Flip Chip Technology** *Course Leaders:* Eric Perfecto – IBM Corporation; Shengmin Wen – Amkor Technology
Southern Hemisphere V **7. Fundamental Concepts of Reliability and Mechanics in Electronic Packaging** *Course Leaders:* Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation	Southern Hemisphere V **15. Package Failure Mechanisms, Reliability, and Solutions** *Course Leader:* Darvin Edwards – Edwards Enterprises
Americas Seminar **8. Product Qualification and Supply Chain Responsibilities** *Course Leader:* Michael Pecht – University of Maryland	Americas Seminar **16. Statistics for Engineering** *Course Leader:* Patrick Thompson – Texas Instruments
REFRESHMENT BREAKS **10:00 - 10:20 a.m. &** **3:00 - 3:20 p.m.**	Oceanic 1 **17. Thermal Materials and Metrology for Advanced Packaging** *Course Leaders:* Ravi Mahajan – Intel Corporation; Kenneth Goodson – Stanford University
	Asia 2 **18. Thermo-Electrical Co-Design of 3D Chip Stacks** *Course Leaders:* Avram Bar-Cohen and Ankur Srivastava – University of Maryland

ECTC STUDENT RECEPTION
Tuesday, May 27, 2014
5:00 p.m. - 6:00 p.m.
Host: Valerie Oberson – IBM Corporation

Room: Cabana Deck (outside near Cabana Pool & Bar, Dolphin Resort)
(Rain Backup: Asia 1, 3rd floor / Lobby Level)

Students, have you ever wondered what career opportunities exist in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them be successful in their first job search and reach their current positions. You will have the chance to enjoy good food and network with industry leaders and achievers. Don't miss the opportunity to interact with people that you might not have the chance to meet otherwise! Sponsored by the IBM Corporation.

GENERAL CHAIR'S SPEAKERS RECEPTION
Tuesday, May 27, 2014
6:00 p.m. - 7:00 p.m.

Room: Crescent Terrace (outside on Swan Property, to the left, near the Boardwalk)
(Rain Backup: Southern Hemisphere I, 5th floor)

Invited session chairs and speakers are requested to attend this reception.

TECHNOLOGY CORNER RECEPTION
Wednesday, May 28, 2014
5:30 p.m. - 6:30 p.m.

Room: Northern Hemisphere A-C, 5th floor

All attendees and guests are invited to attend this exhibitor sponsored reception. Please use this time to mix and mingle with all exhibitors, learn about their products and services, and pick up a few giveaways.

64th ECTC Gala Reception
Thursday, May 29, 2014
6:30 p.m.

Room: Lake Terrace (outside on Swan Property, to the right)
(Rain Backup: Northern Hemisphere D-E, 5th floor)

All badged attendees and guests are invited to attend our Gala Reception. This is a great way to meet your conference colleagues, speakers, exhibitors, guests, and the ECTC Executive Committee.

CONTINUING EDUCATION UNITS

The IEEE Components, Packaging, and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 64th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops. Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Course CEUs will be underwritten by the conference, i.e. there are no additional costs for Professional Development Courses attendees to obtain CEU credit.

2013 ECTC BEST PAPER AWARDS

BEST OF CONFERENCE PAPERS – 2013

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 63rd ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500 and the authors of the Best Interactive Presentation Paper share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

(Session 16, paper 5)

Grain Structure Evolution and its Impact on the Fatigue Reliability of Lead-Free Solder Joints in BGA Packaging Assembly

Huili Xu, and Choong-Un Kim, University of Texas, Arlington; Tae-Kyu Lee, Cisco Systems, Inc.

Best Interactive Presentation Paper

(Session 37, paper 15)

Bath Chemistry and Copper Overburden as Influencing Factors of the TSV Annealing

P. Saettler, M. Boettcher, Catharina Rudolph, and K. J. Wolter, Technische Universität Dresden

OUTSTANDING PAPERS – 2013

The winning authors for Conference Outstanding Session and Interactive Presentation Papers receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

(Session 28, paper 7)

Effects of Varying Amplitudes on the Fatigue Life of Lead Free Solder Joints

M. Obaidat, S. Hamasha, Y. Jaradat, A. Qasaimeh, P. Borgesen, State University of New York, Binghamton; B. Arfaei, and M. Anselm, Universal Instruments Corporation

Outstanding Interactive Presentation Paper

(Session 38, paper 26)

Fabrication and Characterization of Novel Photodefined Polymer-Enhanced Through-Silicon Vias for Silicon Interposers

Paragkumar A. Thadesar and Muhannad S. Bakir, Georgia Institute of Technology

INTEL BEST STUDENT PAPER – 2013

The winning student receives a personalized plaque and a check for US $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 63rd ECTC:

(Session 10, paper 4)

Low temperature fine pitch Flex-on-Flex (FOF) assembly using nanofiber Sn58Bi solder anisotropic conductive films (ACFs) and ultrasonic bonding method

Tae Wan Kim, Kyung-Lim Suk and Kyung-Wook Paik, Korea Advanced Institute of Science and Technology (KAIST)

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 27, 2014

8:00 a.m. – 5:00 p.m.
iNEMI Meeting
Oceanic 3, 3rd floor (Lobby Level)

8:00 a.m. – 5:00 p.m.
ITRS Assembly & Packaging Technology Committee
Europe 4, 3rd floor (Lobby Level)

6:00 p.m. – 7:00 p.m.
A & MT Committee
Asia 2, 3rd floor (Lobby Level)

9:00 p.m. – 10:00 p.m.
Interconnect Committee
Europe 4, 3rd floor (Lobby Level)

9:00 p.m. – 10:30 p.m.
ECTC OPTO Committee
Americas Seminar, 5th floor

Wednesday, May 28, 2014

7:00 a.m. – 8:00 a.m.
CPMT Materials & Processes TC
Europe 3, 3rd floor (Lobby Level)

7:00 a.m. – 8:00 a.m.
CPMT RF & THz Technology TC
Europe 4, 3rd floor (Lobby Level)

9:30 a.m. – 12:00 p.m.
iNEMI Meeting
Oceanic 3, 3rd floor (Lobby Level)

10:00 a.m. – 12:30 p.m,
CPMT Industry Program Meeting
Asia 1, 3rd floor (Lobby Level)

4:30 p.m. – 5:30 p.m.
CPMT Technical Committee Chairs
Asia 1, 3rd floor (Lobby Level)

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite
(by invitation only)

Thursday, May 29, 2014

7:00 a.m. – 8:00 a.m.
CPMT Photonics TC
Europe 4, 3rd floor (Lobby Level)

7:00 a.m. – 8:00 a.m.
CPMT High Density Substrates & Boards TC
Europe 5, 3rd floor (Lobby Level)

7:00 a.m. – 8:00 a.m.
CPMT Nanotechnology TC
Europe 1, 3rd floor (Lobby Level)

5:30 p.m. – 6:30 p.m.
ECTC 2015 Program Committee Meeting
Southern Hemisphere Ballroom IV, 5th floor

8:00 p.m.
ECTC Governing/Executive Committee Reception
General Chair's Suite

Friday, May 30, 2014

6:45 a.m. – 7:45 a.m.
CPMT Transactions Editors
Northern Hemisphere E – 1

7:00 a.m. – 8:00 a.m.
CPMT Region 8 Meeting
Asia 1, 3rd floor (Lobby Level)

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee Meeting
Europe 3, 3rd floor (Lobby Level)

Program Sessions: Wednesday, May 28, 8:00 a.m. - 11:40 a.m.

Session 1: Interposer Technologies	Session 2: Advances in Copper Pillar & Solder Based Flip Chip Technologies	Session 3: Dynamic Mechanical Characterization
Committee: Advanced Packaging	**Committee: Interconnections**	**Committee: Applied Reliability**
Southern Hemisphere I	**Southern Hemisphere II**	**Southern Hemisphere III**
Session Co-Chairs: Subhash L. Shinde – Sandia National Laboratory John Knickerbocker – IBM Corporation	**Session Co-Chairs: Tom Gregorich – Micron Bernd Ebersberger – Intel Corporation**	**Session Co-Chairs: Darvin R. Edwards – Edwards Enterprises Tim Chaudhry – Broadcom Corporation**
1. ***8:00 a.m. – Integration Study of Die Strength and Various Bumping Volume and Reliability Performance on 2.5D Silicon Interposer Assembly*** Shih-Liang Peng, Chen-Yu Huang, Ming-Hsien Yang, Stephen Tseng, J. Y. Lai, Terren Lu, Hsien-Wen Chen, Steve Chiu, and Stephen Chen – Siliconware Precision Industries Co., Ltd.	1. ***8:00 a.m. – Challenges and Opportunities of Chip Package Interaction with Fine Pitch Cu Pillar for 28nm*** Andy Bao, Lily Zhao, Yangyang Sun, Michael Han, Geoffrey Yeap, Steve Bezuk, Pat Holmes, Cecille Alcira, Xuefeng Zhang, and Kenny Lee – Qualcomm Technologies, Inc.	1. ***8:00 a.m. – Transient Dynamics Model and 3D-DIC Analysis of New-Candidate for JEDEC JESD22-B111 Test Board*** Pradeep Lall, Kalyan Dornala, and Di Zhang – Auburn University; Dongji Xie – Nvidia Corporation; Andy Zhang – Texas Instruments, Inc.
2. ***8:25 a.m. – Process Integration, Improvements, and Testing of TSV Si Interposers for Embedded Computing Applications*** S. Goodwin, J. Lannon, Jr., A. Hilton, A. Huffman, M. Lueck, E. Vick, G. Cunningham, D. Malta, C. Gregory, and D. Temple – RTI International	2. ***8:25 a.m. – Electromigration for Advanced Cu Interconnect and the Challenges with Reduced Pitch Bumps*** Nokibul Islam, Gwang Kim, and KyungOe Kim – STATS ChipPAC, Inc.	2. ***8:25 a.m. – Interconnect Reliability Prediction for Wafer Level Packages (WLP) for Temperature Cycle and Drop Load Conditions*** Tong Cui, Ahmer Syed, Beth Keser, Rey Alvarado, Steven Xu, and Mark Schwarz – Qualcomm Technologies, Inc.
3. ***8:50 a.m. – Mechanically Flexible Interconnects with Highly Scalable Pitch and Large Stand-off Height for Silicon Interposer Tile and Bridge Interconnection*** Chaoqi Zhang, Hyung Suk Yang, and Muhannad S. Bakir – Georgia Institute of Technology	3. ***8:50 a.m. – Electromigration Performance of Cu Pillar Bump for Flip Chip Packaging with Bump on Trace by Using Thermal Compression Bonding*** Kuei Hsiao (Frank) Kuo, Jason Lee, F. L. Chien, Rick Lee, and Cindy Mao – Siliconware Precision Industries Co., Ltd.; John Lau – Industrial Technology Research Institute (ITRI)	3. ***8:50 a.m. – A Novel Drop Test Methodology for Highly Stressed Interconnects in Automotive Electronic Control Units*** M. H. Shirangi, Simo G. Tsebo, and T. Heinrich – Robert Bosch GmbH; Z. Wang – Bosch Automotive Products (Suzhou) Co., Ltd.; R. Unnikrishnan – RWTH Aachen University
Refreshment Break: 9:15 a.m. – 10:00 a.m. (Northern Hemisphere A-C)		
4. ***10:00 a.m. – Advancements in Fabrication of Glass Interposers*** Aric Shorey, John Keech, and Scott Pollard – Corning Incorporated; Philippe Cochet and Klaus Ruhmer – Rudolph Technologies; Alan Huffman and Matt Lueck – RTI International	4. ***10:00 a.m. – Flip-Chip Bonding Alignment Accuracy Enhancement Using Self-Aligned Interconnection Elements to Realize Low-Temperature Construction of Ultrafine-Pitch Copper Bump Interconnections*** Bui Thanh Tung and Masahiro Aoyagi – Nanoelectronics Research Institute; Institute for Photonics-Electronics Convergence System Technology; Naoya Watanabe, Fumiki Kato, and Katsuya Kikuchi – Nanoelectronics Research Institute	4. ***10:00 a.m. – Early-State Crack Detection Method for Heel Cracks in Wire Bond Interconnects*** Michael Krüger, Andreas Middendorf, and Klaus-Dieter Lang – Technical University Berlin; Stefan Trampert and Stefan Schmitz – Fraunhofer IZM
5. ***10:25 a.m. – Large Area Interposer Lithography*** Warren Flack, Robert Hsieh, Gareth Kenyon, and Manish Ranjan – Ultratech, Inc.; John Slabbekoorn, Andy Miller, and Eric Beyne – IMEC; Medhat Toukhy, PingHung Lu, and Chunwei Chen – AZ Electronics Materials USA Corporation	5. ***10:25 a.m. – Development of Second-Level Connection Method for Large-Size CPU Package*** Shunji Baba, Masateru Koide, Manabu Watanabe, Kenji Fukuzono, and Tsuyoshi Yamamoto – Fujitsu Advanced Technologies, Ltd.; Seiki Sakuyama, Kozo Shimizu, Keishiro Okamoto, and Daisuke Mizutani – Fujitsu Laboratories, Ltd.	5. ***10:25 a.m. – Accelerated Vibration Reliability Testing of Electronic Assemblies Using Sine Dwell with Resonance Tracking*** Quang Su, James Pitarresi, Mohammad Gharaibeh, Aaron Stewart, and Gaurang Joshi – Binghamton University; Martin Anselm – Universal Instruments Corporation
6. ***10:50 a.m. – Minimizing Interposer Warpage by Process Control and Design Optimization*** Mikael Detalle, B. Vandevelde, P. Nolmans, J. De Messemaeker, M. Gonzalez, A. Miller, A. La Manna, G. Beyer, and E. Beyne – IMEC	6. ***10:50 a.m. – Development of Fine Pitch Area Array Cu Pillar/Lead Free Solder Bumps for Large 28nm Die in Large Organic Flip Chip Packages*** John Osenbach, Sue Emerich, S. Cate, and D. Crouthamel – LSI Corporation; D. Brady and Seung Min Hwang – Amkor Technology, Inc.; J. Dang – Kyocera America, Inc.	6. ***10:50 a.m. – Crack Monitoring and Life Modeling Technique towards High Thermal Cyclic and Mechanical Reliability of fcBGA Solder Joint*** Dongji Xie, Zhongming Wu, Min Woo, and Tom McMullen – Nvidia Corporation
7. ***11:15 a.m. – High Performance IPDs (Integrated Passive Devices) and TGV (Through Glass Via) Interposer Technology Using the Photosensitive Glass*** Jong-Min Yook, Dongsu Kim, and Jun Chul Kim – Korea Electronics Technology Institute	7. ***11:15 a.m. – ELK Delaminate Improvement Methodology on Cu Pillar Interconnect BOP Structure*** Nistec Chang, Albert Lan, Mark Liao, and Eason Chen – Siliconware Precision Industries Co., Ltd.	7. ***11:15 a.m. – Fatigue Properties of Lead-Free Solder Joints in Electronic Packaging Assembly Investigated by Isothermal Cyclic Shear Fatigue*** Huili Xu – University of Texas, Arlington; Intel Corporation; Tae-Kyu Lee – Cisco Systems, Inc.; Choong-Un Kim – University of Texas, Arlington

Program Sessions: Wednesday, May 28, 8:00 a.m. - 11:40 a.m.

Session 4: Bio & Flexible Electronics	Session 5: Silicon Photonics & LEDs	Session 6: Adhesives, Underfills, and Thermal Interface Materials
Committee: Emerging Technologies	**Committee: Optoelectronics**	**Committee: Materials & Processing**
Southern Hemisphere IV	**Southern Hemisphere V**	**Americas Seminar**
Session Co-Chairs: **Joana Maria – IBM Corporation** **C. S. Premachandran – GLOBALFOUNDRIES**	**Session Co-Chairs:** **Fuad Doany – IBM Corporation** **Stefan Weiss – II-VI Laser Enterprise GmbH**	**Session Co-Chairs:** **Don Frye – ATMI** **C. Robert Kao – National Taiwan University**
1. *8:00 a.m. – MEMS-Based Implantable Heart Monitoring System with Integrated Pacing Function* Fjodors Tjulkins, Anh Tuan Thai Nguyen, Nils Hoivik, Knut Aasmundtveit, Lars Hoff, and Kristin Imenes – Buskerud and Vestfold University College; Erik Andreassen – Buskerud and Vestfold University College; SINTEF Materials and Chemistry; Ole Johannes Grymyr and Per Steinar Halvorsen – Oslo University Hospital Intervention Centre	**1. *8:00 a.m. – Assembly of Mechanically Compliant Interfaces between Optical Fibers and Nanophotonic Chips*** Tymon Barwicz, Yoichi Taira, Hidetoshi Numata, Nicolas Boyer, Stephane Harel, Swetha Kamlapurkar, Simon Laflamme, Sebastian Engelmann, Yurii Vlasov, and Paul Fortier – IBM Corporation; Shotaro Takenobu – Asahi Glass Corporation	**1. *8:00 a.m. – Novel Highly Moisture Resistant Optical Adhesives and Their High Power Resistivity*** Seiko Mitachi – Tokyo University of Technology; Kazushi Kimura – Yokohama Rubber Co. Ltd.
2. *8:25 a.m. – Archipelago Platform for Skin-Mounted Wearable and Stretchable Electronics* Yung-Yu Hsu, Cole Papakyrikos, Milan Raj, Mitul Dalal, Pinghung Wei, Xianyan Wang, Gil Huppert, Briana Morey, and Roozbeh Ghaffari – MC10, Inc.	**2. *8:25 a.m. – Proposal of Integrated-Optic Wavelength-Selective Modulator Based on Coupling-Efficiency Control of Distributed Bragg Reflector in Straight Waveguide*** Shogo Ura, Testunosuke Miura, Satoshi Kawanami, Kosuke Asai, Kenzo Nishio, and Yasuhiro Awatsuji – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology	**2. *8:25 a.m. – Engineered Thermal Interface Material*** Lyndon Larson, Yin Tang, Loren Durfee, Cassandra Hale, and David Plante – Dow Corning Corporation; Sushumna Iruvanti, Rebecca Wagner, Taryn Davis, Hai Longworth, Annique LaVoie, and Richard Langlois – IBM Corporation
3. *8:50 a.m. – Inkjet Printing in Manufacturing of Stretchable Interconnects* Toni Liimatta, Eerik Halonen, Hannu Sillanpää, Juha Niittynen, and Matti Mäntysalo – Tampere University of Technology	**3. *8:50 a.m. – Porous Silicon Technology – A Breakthrough for Silicon Photonics: From Packaging to Monolithic Integration*** M. Balucani, A. Klyshko, K. Kholostov, A. Benedetti, A. Belardini, and C. Sibilia – Sapienza University of Rome; M. Izzi and M. Tucci – Enea Casaccia Research Centre Rome; H. Bandarenka and V. Bondarenko – Belarusian State University of Informatics and Radioelectronics	**3. *8:50 a.m. – Degradation Mechanisms in Electronic Mold Compounds Subjected to High Temperature in Neighborhood of 200°C*** Pradeep Lall, Shantanu Deshpande, Yihua Luo, and Mike Bozack – Auburn University; Luu Nguyen and Masood Murtuza – Texas Instruments
Refreshment Break: 9:15 a.m. – 10:00 a.m. (Northern Hemisphere A-C)		
4. *10:00 a.m. – Ultra Small Hearing Aid Electronic Packaging Enabled by Chip-in-Flex* John Dzarnoski and Susie Johansson – Starkey Hearing Technologies	**4. *10:00 a.m. – High Power Density LED Modules with Silver Sintering Die Attach on Aluminum Nitride Substrates*** Marc Schneider, Benjamin Leyrer, Christian Herbold, and Stefan Maikowske – Karlsruhe Institute of Technology	**4. *10:00 a.m. – Time, Temperature, and Mechanical Fatigue Dependence on Underfill Adhesion*** Joseph Cremaldi and Noshir Pesika – Tulane University; Michael Gaynes, Peter Brofman, and Eric Lewandowski – IBM Corporation
5. *10:25 a.m. – Fabrication of Silicon Based Microfluidics Device for Cell Sorting Application* Bivragh Majeed, Chengxun Liu, Lut Van Acker, Robert Daily, Deniz Sabuncuoglu, and Liesbet Lagae – IMEC; Tomokazu Miyazaki – JSR Micro NV	**5. *10:25 a.m. – Effect of Optical Design on the Thermal Management for SMART TV LED Backlight Systems*** Kivanc Karsli – Vestel AS; Mehmet Arik – Ozyegin University	**5. *10:25 a.m. – Study on Isotropic Electrically Conductive Adhesive for Medical Device Applications*** Shawn Shi, Scott Sleeper, and Chunho Kim – Medtronic, Inc.
6. *10:50 a.m. – A Novel 3D Neural Probe with Integrated Channel and Its Package* Xingming Fu and Sheng Liu – Wuhan University; Yong Xu, Yuefa Li, and Jinshen Zhang – Wayne State University; Xiaobing Luo – Huazhong University of Science & Technology	**6. *10:50 a.m. – Wafer Level LED Packaging with Optimal Light Output and Thermal Dissipation for High-Brightness Lighting*** Liang Wang, Gabe Guevara, Hala Shaba, Roseann Alatorre, Rey Co, and Ron Zhang – Invensas Corporation	**6. *10:50 a.m. – Effect of Aligned Nanofiber in Nanofiber Solder Anisotropic Conductive Films (ACFs) on the Solder Ball Movement for Flex-on-Flex (FOF) Assembly*** Tae-Wan Kim, Sang-Hoon Lee, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST)
7. *11:15 a.m. – CMOS Multiplexer for Portable Biosensing System with Integrated Microfluidic Interface* Tetiana Voitsekhivska, Eike Suthau, and Klaus-Juergen Wolter – Technical University, Dresden	**7. *11:15 a.m. – High Power Laser Packaging Challenges and Standardization*** Eric Zhou and Jeffrey Morris – LDX Optronics, Inc.; Hanguo Wang – UCLA	**7. *11:15 a.m. – Adhesive Enabling Technology for Directly Plating Metal on Molding Resin*** Kwonil Kim, Kenichiroh Mukai, Brian Eastep, Lee Gaherty, Anirudh Kashyap, and Lutz Brandt – Atotech USA, Inc.

Program Sessions: Wednesday, May 28, 1:30 p.m. - 5:10 p.m.

Session 7: Interposers & 3D Integration	Session 8: Flip Chip Packaging & Advanced Substrate	Session 9: Interconnect Reliability
Committee: Interconnections	**Committee: Advanced Packaging**	**Committee: Applied Reliability**
Southern Hemisphere I	**Southern Hemisphere II**	**Southern Hemisphere III**
Session Co-Chairs: Katsuyuki Sakuma – IBM Corporation Lou Nicholls – Amkor Technology, Inc.	**Session Co-Chairs: Young-Gon Kim – IDT Omar Bchir – Qualcomm, Inc.**	**Session Co-Chairs: Tz-Cheng Chiu – National Cheng Kung University Vikas Gupta – Texas Instruments**
1. ***1:30 p.m. – Modeling, Design, and Demonstration of Low-Temperature Cu Interconnections to Ultra-Thin Glass Interposers at 20 µm Pitch*** Tao Wang, Vanessa Smet, Venky Sundaram, P. Markondeya Raj, and Rao Tummala – Georgia Institute of Technology; Makoto Kobayashi – Namics Corporation	1. ***1:30 p.m. – Chip Package Interaction: An Experiment Study on White Bump Mitigation Using Flat Laminates*** Yi Pan, Jeffrey A. Zitz, David L. Questad, and Kamal K. Sikka – IBM Corporation	1. ***1:30 p.m. – Towards a Quantitative Mechanistic Understanding of the Thermal Cycling of SnAgCu Solder Joints*** D. Schmitz, S. Shirazi, L. Wentlent, S. Hamasha, and P. Borgesen – Binghamton University; L. Yin – GE Global Research; A. Qasaimeh – Tennessee Tech University
2. ***1:55 p.m. – Low-Cost TSH (Through-Silicon Hole) Interposers for 3D IC Integration*** J. H. Lau, C. K. Lee, C. J. Zhan, S. T. Wu, Y. L. Chao, M. J. Dai, R. M. Tain, H. C. Chien, C. H. Chien, R. S. Cheng, Y. W. Huang, Y. C. Lee, Z. C. Hsiao, W. L. Tsai, P. C. Chang, H. C. Fu, Y. M. Cheng, L. L. Liao, W. C. Lo, and M. J. Kao – Industrial Technology Research Institute (ITRI)	2. ***1:55 p.m. – Design and Package Technology Development of Face-to-Face Die Stacking as a Low Cost Alternative for 3D IC Integration*** Zhe Li, Yuan Li, and John Xie – Altera Corporation	2. ***1:55 p.m. – Exploration of Aging Induced Evolution of Solder Joints Using Nanoindentation and Microdiffraction*** Mohammad Hasnine, Jeffrey C. Suhling, Barton C. Prorok, Michael J. Bozack, and Pradeep Lall – Auburn University
3. ***2:20 p.m. – Cu Pattern Density Impacts on 2.5D TSI Warpage Using Experimental and FEM Analysis*** C. T. Yeh, C. Y. Wu, C. F. Lin, K. M. Chen, M. J. Lin, Y. C. Lin, and C. L. Kuo – United Microelectronics Corporation	3. ***2:20 p.m. – From C4 to Micro-Bump: Adapting Lead Free Solder Electroplating Processes to Next-Gen Advanced Packaging Applications*** Julia Woertink, Yi Qin, Jonathan Prange, Pedro Lopez-Montesinos, Inho Lee, Yil-Hak Lee, Masaaki Imanari, Jianwei Dong, and Jeffrey Calvert – Dow Electronic Materials	3. ***2:20 p.m. – Accessing Adhesive Induced Risk for BGAs in Temperature Cycling*** Guruprasad Arakere, Milena Vujosevic, and Min Pei – Intel Corporation
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Northern Hemisphere A-C)		
4. ***3:30 p.m. – A Resilient 3-D Stacked Multicore Processor Fabricated Using Die-Level 3-D Integration and Backside TSV Technologies*** K. W. Lee, H. Hashimoto, M. Onishi, Y. Sato, M. Murugesan, J. C. Bae, T. Fukushima, T. Tanaka, and M. Koyanagi – Tohoku University	4. ***3:30 p.m. – Development of New 2.5D Package with Novel Integrated Organic Interposer Substrate with Ultra-Fine Wiring and High Density Bumps*** Kiyoshi Oi, Satoshi Otake, Noriyoshi Shimizu, Shoji Watanabe, Yuji Kunimoto, Takashi Kurihara, Toshinori Koyama, and Masato Tanaka – Shinko Electric Industries Company, Ltd.; Lavanya Aryasomayajula and Zafer Kutlu – GLOBALFOUNDRIES	4. ***3:30 p.m. – Characteristics of Ceramic BGA Using Polymer Core Solder Balls*** Hiroya Ishida and Kiyoto Matsushita – Sekisui Chemical Co., Ltd.
5. ***3:55 p.m. – 3D Stacking Induced Mechanical Stress Effects*** V. Cherman, G. Van der Plas, J. De Vos, M. Lofrano, V. Simons, M. Gonzalez, K. Vanstreels, T. Wang, R. Daily, W. Guo, G. Beyer, A. La Manna, and E. Beyne – IMEC; A. Ivankovic and I. De Wolf – IMEC; KU Leuven	5. ***3:55 p.m. – Package Embedded Decoupling Capacitor Impact on Core Power Delivery Network for ARM SoC Application*** Ga Won Kim, Max (Sungwan) Min, Melinda (Ling) Yang, Anil Gundurao, Eileen You, and Harpreet Gill – Samsung Semiconductor Inc.; Seungyong Cha, Younghoon Kim, Se-Ho You, Seungbae Lee, and Woonghwan Ryuu – Samsung Electronics Corporation	5. ***3:55 p.m. – Lifetime Prediction of Cu-Al Wire Bonded Contacts for Different Mould Compounds*** René Rongen, G. M. O'Halloran, Amar Mavinkurve, Leon Goumans, and Mark-Luke Farrugia – NXP Semiconductors
6. ***4:20 p.m. – Six-Die Stacking: Three-Dimensional Interconnects Using Au and Pillar Bumps*** Fei-Jain Wu, Lung-Hua Ho, Chih-Ming Kuo, Chia-Jung Tu, Chih-Hsien Ni, Shih-Chieh Chang, Chuan-Yu Wu, Kung-An Lin, Wei-Hsin Wu, and Yung Shen Wu – Chipbond Technology Corporation	6. ***4:20 p.m. – Embed Glass Interposer to Substrate for High Density Interconnection*** Dyi-Chung Hu, Yin-Po Hung, Yu-Hua Chen, and Ra-Min Tain – Unimicron Technology Corporation; Wei-Chung Lo – Industrial Technology Research Institute (ITRI)	6. ***4:20 p.m. – The Corrosion Performance of Cu Alloy Wire Bond on Al Pad in Molding Compounds of Various Chlorine Contents under Biased-HAST*** Ying-Ta Chiu, Tzu-Hsing Chiang, Yin-Fa Chen, Ping-Feng Yang, and Louie Huang – ASE Group; Kwang-Lung Lin – National Cheng Kung University
7. ***4:45 p.m. – TSV-Less 3D Stacking of MEMS and CMOS via Low Temperature Al-Au Direct Bonding with Simultaneous Formation of Hermetic Seal*** S. L. Chua, A. Razzaq, K. H. Li, H. Yu, and C. S. Tan – Nanyang Technological University; K. H. Wee – DSO National Laboratory	7. ***4:45 p.m. – First Demonstration of a Surface Mountable, Ultra-Thin Glass BGA Package for Smart Mobile Logic Devices*** Venky Sundaram, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Yoichiro Sato – Asahi Glass Company; Toshitake Seki and Yutaka Takagi – NGK Spark Plug Co., Ltd.; Makoto Kobayashi – Namics Corporation	7. ***4:45 p.m. – The Effect of Nickel Microalloying on Thermal Fatigue Reliability and Microstructure of SAC105 and SAC205 Solders*** Richard Coyle – Alcatel-Lucent; Richard Parker – iNEMI; Babak Arfaei – Universal Instruments; Francis Mutuku – Binghamton University; Keith Sweatman and Keith Howell – Nihon Superior Co., Ltd.; Stuart Longgood – Delphi; Elizabeth Benedetto – Hewlett-Packard Company

Program Sessions: Wednesday, May 28, 1:30 p.m. - 5:10 p.m.

Session 10: Novel Materials & Processes	Session 11: Innovative Packaging Technologies	Session 12: Power Integrity & Passive Component Modeling
Committee: Materials & Processing	**Committee: Assembly & Manufacturing Technology**	**Committee: Modeling & Simulation**
Southern Hemisphere IV	**Southern Hemisphere V**	**Americas Seminar**
Session Co-Chairs: Ivan Shubin – Oracle; Bing Dang – IBM Corporation	**Session Co-Chairs: Paul Tiner – Texas Instruments; Shichun Qu – Fairchild Semiconductor**	**Session Co-Chairs: Wendem Beyene – Rambus Inc.; Daniel de Araujo – Nimbic, Inc.**
1. ***1:30 p.m. – Flexible Non-Volatile Cu/Cu_xO/Ag ReRAM Memory Devices Fabricated Using Ink-Jet Printing Technology*** Simin Zou and Michael C. Hamilton – Auburn University	1. ***1:30 p.m. – A New Era in Manufacturable, Low-Temperature and Ultra-Fine Pitch Cu Interconnections and Assembly without Solders*** Vanessa Smet, Tao Wang, Pulugurtha Markondeya Raj, and Rao Tummala – Georgia Institute of Technology; Makoto Kobayashi – Namics Corporation	1. ***1:30 p.m. – Package Embedded Inductors for Integrated Voltage Regulators*** William J. Lambert, Michael J. Hill, Kaladhar Radhakrishnan, Leigh Wojewoda, and Anne E. Augustine – Intel Corporation
2. ***1:55 p.m. – Ultra-High Refractive Index LED Encapsulant*** Chia-Chi Tuan, Ziyin Lin, Yan Liu, and Kyoung-Sik Moon – Georgia Institute of Technology; Sehoon Yoo – Korea Institute of Industrial Technology; Myong-Gi Jang – EI Lighting Co. Ltd.; Ching-Ping Wong – Georgia Institute of Technology; Chinese University of Hong Kong	2. ***1:55 p.m. – Enabling Fine Pitch Cu & Ag Alloy Wire Bond Assessment for 28nm Ultra Low-k Structure*** John D. Beleran, Ninoy Milanes II, Gaurav Mehta, and Nathapong Suthiwongshunthorn – United Test and Assembly Center, Ltd.; Ranjan Rajoo and Chan Kai Chong – GLOBALFOUNDRIES	2. ***1:55 p.m. – Power Supply Filter for PLL Circuit in Digital Systems*** Nam Pham, Faraydon Pakbaz, Zhenrong Jin, and Lloyd Walls – IBM Corporation
3. ***2:20 p.m. – A Novel Methodology for Wafer-Specific Feed-Forward Management of Backside Silicon Removal by Wafer Grinding for Optimized Through Silicon Via Reveal*** Tyson Alvanos, Yu Iijima, and Frank Wei – Disco Hi Tec America, Inc.; John Garant and Richard Indyk – IBM Corporation; Christopher Rosenthal – Lasertec USA, Inc.; Osamu Sato, Naoki Sugase, and Hideo Takizawa – Lasertec Corporation	3. ***2:20 p.m. – Assembly of Multiple Chips on Flexible Substrate Using Anisotropic Conductive Film for Medical Imaging Applications*** Hoang-Vu Nguyen, Kristin Imenes, and Knut E. Aasmundtveit – Buskerud and Vestfold University College; Trym Eggen and Bjørnar Sten-Nilsen – GE Vingmed Ultrasound AS	3. ***2:20 p.m. – Coaxial Through-Package Vias (TPVs) for Enhancing Power Integrity in 3D Double-Side Glass Interposers*** Gokul Kumar, P. Markondeya Raj, Saumya Gandhi, Parthasarathi Chakraborti, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Jonghyun Cho and Joungho Kim – Korea Advanced Institute of Science and Technology (KAIST)
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Northern Hemisphere A-C)		
4. ***3:30 p.m. – Thermal Characterization of Power Devices Using Graphene-Based Film*** Pengtu Zhang – Chalmers University of Technology; East China University of Science and Technology; Nan Wang, Carl Zandén, and Johan Liu – Chalmers University of Technology; Lilei Ye and Yifeng Fu – Smart High Tech AB	4. ***3:30 p.m. – High Frequency High Current Point of Load Modules with Integrated Planar Inductors*** Wenli Zhang, Yipeng Su, David Gilham, Mingkai Mu, Qiang Li, and Fred C. Lee – Virginia Polytechnic Institute and State University	4. ***3:30 p.m. – Modeling of Switching Noise and Coupling in Multiple Chips of 3D TSV-Based Systems*** Huanyu He and Jian-Qiang Lu – Rensselaer Polytechnic Institute; Xiaoxiong Gu – IBM Corporation
5. ***3:55 p.m. – High Performance Phase Change Thermal Interface Materials Based on Porous Graphitic Carbon Spheres-Paraffin Wax Composite*** Zhihua Cao – Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences; University of Science and Technology of China; Kai Zhang and Matthew M. F. Yuen – Hong Kong University of Science and Technology; Gaugping Zhang, Xianzhu Fu, and Rong Sun – Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences; Ping Gu – University of Science and Technology of China; C. P. Wong – Chinese University of Hong Kong	5. ***3:55 p.m. – Integrated Microprobe Array and CMOS MEMS by TSV Technology for Bio-Signal Recording Application*** Lei-Chun Chou, Shih-Wei Lee, Po-Tsang Huang, Shang-Lin Wu, and Ching-Te Chuang – National Chiao Tung University; Chih-Wei Chang – University of California, Los Angeles; Jin-Chern Chiou – National Chiao Tung University; China Medical University; Wei Hwang and Kuan-Neng Chen – National Chiao Tung University; Advanced Semiconductor Engineering, Inc.; Chung-Hsi Wu, Kuo-Hua Chen, Chi-Tsung Chiu, and Ho-Ming Tong – Advanced Semiconductor Engineering, Inc.	5. ***3:55 p.m. – Characterization of On-Die Power Supply Noise in FCBGA (Flip-Chip Ball Grid Array) Packages*** Hyunho Baek and William R. Eisenstadt – University of Florida
6. ***4:20 p.m. – High Sensitivity In-Plane Strain Measurement Using a Laser Scanning Technique*** Hanshuang Liang, Teng Ma, Cheng Lv, Hoa Nguyen, George Chen, Hao Wu, Rui Tang, Hanqing Jiang, and Hongbin Yu – Arizona State University	6. ***4:20 p.m. – Material Characterization of a Novel Lead-Free Solder Material: SACQ*** Tak-Sang Yeung, Henry Sze, Keith Tan, Javed Sandhu, Chong-Wei Neo, and Edward Law – Broadcom Corporation	6. ***4:20 p.m. – An Enhanced Power Integrity Analysis Flow Based on the Interdependence between Simultaneous Switching Output Noise and Static IR Drop*** Minghui Han, Amir Amirkhany, and Wei Xiong – Samsung Display
7. ***4:45 p.m. – Biophysicochemical Evaluation of Passivation Layers for the Packaging of Silicon Microsystems in Medical Devices*** Jorge Mario Herrera Morales, Jean-Charles Souriau, David Ratel, François Berger, and Gilles Simon – CEA-LETI	7. ***4:45 p.m. – Lithography Challenges for 2.5D Interposer Manufacturing*** Klaus Ruhmer, Philippe Cochet, Roger McCleary, Rich Rogoff, and Rajiv Roy – Rudolph Technologies, Inc.	7. ***4:45 p.m. – Improving the Target Impedance Method for PCB Decoupling of Core Power*** Guang Chen and Dan Oh – Altera Corporation

Program Sessions: Thursday, May 29, 8:00 a.m. - 11:40 a.m.

Session 13: 3D Process Integration & Die Stacking	Session 14: TSV Fabrication & Its Reliability Impact	Session 15: Solder Joint Reliability
Committee: Advanced Packaging	**Committee: Interconnections**	**Committee: Applied Reliability**
Southern Hemisphere I	**Southern Hemisphere II**	**Southern Hemisphere III**
Session Co-Chairs: **Rozalia Beica – Yole Developpement** **Jianwei Dong – Dow Electronic Materials**	**Session Co-Chairs:** **Li Li – Cisco Systems, Inc.** **Wei-Chung Lo – Industrial Technology Research Institute (ITRI)**	**Session Co-Chairs:** **Keith Newman – Hewlett-Packard Company** **Toni Mattila – Aalto University**
1. 8:00 a.m. – Process Development to Enable 3D IC Multi-Tier Die Bond for 20µm Pitch and Beyond Y. H. Hu, C. S. Liu, M. T. Chen, M. D. Cheng, H. J. Kuo, M. J. Lii, and Doug C. H. Yu – TSMC; A. LaManna, K. J. Rebibis, T. Wang, S. V. Huylenbroeck, R. Daily, G. Capuz, D. Velenis, G. Beyer, and E. Beyne – IMEC	***1. 8:00 a.m. – Correlation between Cu Microstructure and TSV Cu Pumping*** Joke De Messemaeker, Olalla Varela Pedreira, Harold Philipsen, Eric Beyne, Ingrid De Wolf, and Kristof Croes – IMEC; Tom Van der Donck – KU Leuven	***1. 8:00 a.m. – Dependence of Solder Joint Reliability on Solder Volume, Composition and Printed Circuit Board Surface Finish*** Babak Arfaei – Universal Instruments Corporation; Francis Mutuku and Eric Cotts – Binghamton University; Keith Sweatman – Nihon-Superior; Ning-Cheng Lee – Indium Corporation; Richard Coyle – Alcatel-Lucent
2. 8:25 a.m. – Factors in Selection of Temporary Wafer Handlers for 3D/2.5 Integration Bing Dang, Bucknell Webb, Cornelia Tsang, Paul Andry, and John Knickerbocker – IBM Corporation	***2. 8:25 a.m. – TSV Reliability Model under Various Stress Tests*** Ben-Je Lwo, Frank M. S. Lin, and Kuo-Hsin Huang – National Defense University	***2. 8:25 a.m. – The Effects of Aging on the Fatigue Life of Lead Free Solders*** Muhannad Mustafa, Jordan C. Roberts, Jeffrey C. Suhling, and Pradeep Lall – Auburn University
3. 8:50 a.m. – Optimization and Challenges on TSV MEOL Integration DoHyeong Kim, DongHun Lee, YoungChul Seo, JungSoo Park, SeungChul Han, BoRa Jang, JooHyun Khim, YoungSuk Chung, SeongMin Seo, and ChoonHeung Lee – Amkor Technology Korea, Inc.	***3. 8:50 a.m. – Development of Process and Design Criteria for Stress Management in Through Silicon Vias*** O. Hölck, M. Nuss, A. Grams, T. Prewitz, P. John, C. Fiedler, M. Böttcher, H. Walter, M. J. Wolf, and O. Wittler – Fraunhofer IZM; K. D. Lang – Technical University Berlin	***3. 8:50 a.m. – Solder Joint Height Impact on Temperature Cycle Reliability of BGA Components with Thermal Enabling Load*** Yun Ge, Jeffery Cook, Min Pei, Milena Vujosevic, Bite Zhou, and Suddhasattwa Nad – Intel Corporation
Refreshment Break: 9:15 a.m. – 10:00 a.m. (Northern Hemisphere A-C)		
4. 10:00 a.m. – TSV Integration on 20nm Logic Si: 3D Assembly and Reliability Results Rahul Agarwal, Sukeshwar Kannan, Sebastian Dej, Dan Smith, Sara Thangaraju, and Jens Paul – GLOBALFOUNDRIES, Inc.; Dave Hiner, KiWook Lee, DoHyeong Kim, JongSik Paek, SungGeun Kang, and Yong Son – Amkor Technology, Inc.	***4. 10:00 a.m. – High-Speed Wet Etching of Through Silicon Vias (TSVs) in Micro- and Nanoscale*** Liyi Li – Georgia Institute of Technology; Ching-Ping Wong – Georgia Institute of Technology; Chinese University of Hong Kong	***4. 10:00 a.m. – Controlling the Sn Grain Morphology of SnAg C4 Solder Bumps*** Gregory Parks and Eric Cotts – Binghamton University; Minhua Lu and Eric Perfecto – IBM Corporation
5. 10:25 a.m. – TSV MEOL (Mid End of Line) and Packaging Technology of Mobile 3D-IC Stacking Duk Ju Na, Kyaw Oo Aung, Won Kyung Choi, Seung Wook Yoon, and Andy Chang Bum Yong – STATS ChipPAC, Ltd.; Tsuyoshi Kida, Toshihiko Ochiai, Tomoaki Hashimoto, Michitaka Kimura, and Keiichirou Kata – Renesas Electronics Company	***5. 10:25 a.m. – Replacing the PECVD-SiO_2 in the Through-Silicon Via of High-Density 3D LSIs with Highly Scalable Low Cost Organic Liner: Merits and Demerits*** Murugesan Mariappan, Takafumi Fukushima, JiChel Beatrix, Hiroyuki Hashimoto, Yutaka Sato, Kangwook Lee, Tetsu Tanaka, and Mitsumasa Koyanagi – Tohoku University	***5. 10:25 a.m. – The Impact of Microstructure Evolution, Localized Recrystallization and Board Thickness on Sn-Ag-Cu Interconnect Board Level Shock Performance*** Tae-Kyu Lee and Weidong Xie – Cisco Systems, Inc.; Thomas R. Bieler – Michigan State University; Choong-Un Kim – University of Texas, Arlington
6. 10:50 a.m. – Thermally Enhanced 3-Dimensional Integrated Circuit (TE3DIC) Packaging S. Snyder, J. Thompson, A. King, E. Walters, P. Tyler, and M. R. Weatherspoon – Harris Corporation GCSD	***6. 10:50 a.m. – Investigation of a TSV-RDL In-Line, Fault-Diagnosis System and Test Methodology for Wafer-Level Commercial Production*** Runiu Fang, Xin Sun, Yunhui Zhu, and Yufeng Jin – Peking University; Min Miao and Minggang Sun – Beijing Information Science and Technology University; Guanjiang Wang and Yichao Xu – Peking University Shenzhen Graduate School	***6. 10:50 a.m. – Thermal Cycle Fatigue Life Prediction for Flip Chip Solder Joints*** Robert Darveaux – Skyworks Solutions, Inc.
7. 11:15 a.m. – Filler Trap and Solder Extrusion in 3D IC Thermo-Compression Bonded Microbumps Yingxia Liu, Menglu Li, and K. N. Tu – University of California, Los Angeles; Dong Wook Kim and Sam Gu – Qualcomm, Inc.; Dilworth Y. Parkinson and Justin Blair – Lawrence Berkeley National Laboratory	***7. 11:15 a.m. – Bonding Technologies for Chip Level and Wafer Level 3D Integration*** Katsuyuki Sakuma, Spyridon Skordas, Jeffrey Zitz, Eric Perfecto, William Guthrie, Luc Guerin, Richard Langlois, Hsichang Liu, Koushik Ramachandran, Wei Lin, Kevin Winstel, Sayuri Kohara, Kuniaki Sueoka, Matthew Angyal, Troy Graves-Abe, Daniel Berger, John Knickerbocker, and Subramanian Iyer – IBM Corporation	***7. 11:15 a.m. – High Thermo-Mechanical Fatigue and Drop Impact Resistant Ni-Bi Doped Lead Free Solder*** Jae Hong Lee, Santosh Kumar, Hui Joong Kim, Young Woo Lee, and Jeong Tak Moon – MK Electron, Ltd.

Program Sessions: Thursday, May 29, 8:00 a.m. - 11:40 a.m.

Session 16: Advances in Signal Integrity & High-Speed System Design

Committee:
Modeling & Simulation

Southern Hemisphere IV

Session Co-Chairs:
Xiaoxiong (Kevin) Gu – IBM Corporation
Bruce Kim – City University of New York

1. ***8:00 a.m. – Optimal Relaxation of I/O Electrical Requirements under Packaging Uncertainty by Stochastic Methods***
   Xu Chen, Juan S. Ochoa, José E. Schutt-Ainé, and Andreas C. Cangellaris – University of Illinois, Urbana-Champaign

2. ***8:25 a.m. – An Accurate and Convenient Lumped/Discrete Port De-Embedding Method for the 3D Integration and Packaging Full-Wave Modeling by Splitting and Absorbing the Error-Cancelling Network***
   Zhaoqing Chen – IBM Corporation

3. ***8:50 a.m. – Design, Modeling, and Characterization of Passive Channels for Data Rates of 50 Gbps and Beyond***
   Wendemagegnehu Beyene, Yeon-Chang Ham, Dave Secker, and Don Mullen – Rambus, Inc.; Yuriy Shlepnev – Simberian Inc.

Session 17: Emerging Wireless Technologies & Design

Committee:
Electronic Components & RF

Southern Hemisphere V

Session Co-Chairs:
Amit P. Agrawal – Cisco Systems, Inc.
Lih-Tyng Hwang – National Sun Yat-Sen University

1. ***8:00 a.m. – Novel Highly-Efficient and Misalignment Insensitive Wireless Power Transfer Systems Utilizing Strongly Coupled Magnetic Resonance Principles***
   Daerhan Daerhan, Olutola Jonah, Hao Hu, and Stavros V. Georgakopoulos – Florida International University; Manos M. Tentzeris – Georgia Institute of Technology

2. ***8:25 a.m. – A Wireless Charging and Near-Field Communication Combination Module for Mobile Applications***
   Hiroki Shibuya, Tatsuaki Tsukuda, Hiroko Suzuki, Tadashi Shimizu, Masahiro Dobashi, Shinji Nishizono, Mikio Baba, Hideki Sasaki, and Katsushi Terajima – Renesas Electronics Corporation

3. ***8:50 a.m. – Enhanced-Performance Wireless Conformal "Smart Skins" Utilizing Inkjet-Printed Carbon-Nanostructures***
   Taoran Le, Ziyin Lin, C. P. Wong, and M. M. Tentzeris – Georgia Institute of Technology

Session 18: WLCSP, Flip Chip, and PoP

Committee:
Assembly & Manufacturing Technology

Americas Seminar

Session Co-Chairs:
Valerie Oberson – IBM Corporation
Sa Huang – Medtronic Corporation

1. ***8:00 a.m. – Wafer-Level Non Conductive Films for Exascale Servers***
   A. Horibe, S. Kohara, H. Mori, and Y. Orii – IBM Corporation; S. Kawamoto, H. Sone, and M. Hoshiyama – Namics Corporation

2. ***8:25 a.m. – Bump Geometric Deviation on the Reliability of BOR WLCSP***
   Yumin Liu, Yong Liu, and Shichun Qu – Fairchild Semiconductor Corporation

3. ***8:50 a.m. – Experimental Identification of Warpage Origination during the Wafer Level Packaging Process***
   Chunsheng Zhu, Wenguo Ning, Heng Lee, Jiaotuo Ye, Gaowei Xu, and Le Luo – Chinese Academy of Sciences

Refreshment Break: 9:15 a.m. – 10:00 a.m. (Northern Hemisphere A-C)

4. ***10:00 a.m. – Low Loss Conductors for CMOS and Through Glass/Silicon Via (TGV/TSV) Structures Using Eddy Current Cancelling Superlattice Structure***
   Arian Rahimi and Yong-Kyu Yoon – University of Florida

5. ***10:25 a.m. – Modeling, Design, Fabrication and Characterization of First Large 2.5D Glass Interposer as a Superior Alternative to Silicon and Organic Interposers at 50 Micron Bump Pitch***
   Brett Sawyer, Hao Lu, Vanessa Smet, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Yuya Suzuki – Zeon Corporation; Yutaka Takagi – NGK Spark Plug Co. Ltd.; Makoto Kobayashi – Namics Corporation; Taiji Sakai – Fujitsu Laboratories Ltd.

6. ***10:50 a.m. – Coupling Impact of Single Ended Signals to LVDS Interface***
   June Feng, Chooi Ian Loh, Edward Lin, Ellen Du, Guang Chen, and Dan Oh – Altera Corporation

7. ***11:15 a.m. – Analysis on Interference between Multi-Giga Bit Display Serial Link and RF Components in Smart Mobile Device***
   Youchul Jeong, Jaemin Kim, and Baegin Sung – Silicon Image Inc.

4. ***10:00 a.m. – Novel THz Imaging Array Using High Resistivity Metasurfaces***
   Kyoung Youl Park and Premjeet Chahal – Michigan State University

5. ***10:25 a.m. – Magneto-Dielectric Characterization and Antenna Design***
   Kyu Han, Madhavan Swaminathan, P. Markondeya Raj, Himani Sharma, and Rao Tummala – Georgia Institute of Technology; Vijay Nair – Intel Corporation

6. ***10:50 a.m. – Flexible Liquid Crystal Polymer Based Complementary Split Ring Resonator Loaded Quarter Mode Substrate Integrated Waveguide Filters for Compact and Wearable Broadband RF Applications***
   David Senior – Universidad Tecnológica de Bolívar, University of Florida; Arian Rahimi, Pitfee Jao, and Yong-Kyu Yoon – University of Florida

7. ***11:15 a.m. – A Dual-Band Power Amplifier Based on Composite Right/Left-Handed Matching Networks***
   Kyriaki Niotaki, Ana Collado, and Apostolos Georgiadis – Centre Tecnologic de Telecomunicacions de Catalunya; John Vardakas – Iquadrat S. L.

4. ***10:00 a.m. – A Stress-Based Effective Film Technique for Wafer Warpage Prediction of Arbitrarily Patterned Films***
   Gregory T. Ostrowicki and Siva P. Gurrum – Texas Instruments, Inc.

5. ***10:25 a.m. – Drop Test and TCT Reliability of Buffer Coating Material for WLCSP***
   Nobuhiro Anzai, Mitsuru Fujita, and Atsushi Fujii – Asahi Kasei E-Materials Corporation

6. ***10:50 a.m. – Optimization of Compression Bonding Processing Temperature for Fine Pitch Cu-Column Flip Chip Devices***
   Yonghyuk Jeong, Joonyoung Choi, Youjoung Choi, Nokibul Islam, and Eric Ouyang – STATS ChipPAC, Inc.

7. ***11:15 a.m. – Reliability Improvement Methods of Solder Anisotropic Conductive Film (ACF) Joints Using Morphology Control of Solder ACF Joints***
   Yoo-Sun Kim, Seung-Ho Kim, Jiwon Shin, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST)

Program Sessions: Thursday, May 29, 1:30 p.m. - 5:10 p.m.

Session 19: Progress in 3D Integration	Session 20: 3D Materials & Processing	Session 21: Wafer-Level & Fan-Out Packages
Committee: Assembly & Manufacturing Technology	**Committee: Materials & Processing**	**Committee: Advanced Packaging**
Southern Hemisphere I	**Southern Hemisphere II**	**Southern Hemisphere III**
Session Co-Chairs: Shawn Shi – Medtronic Corporation Mark Gerber – Texas Instruments	**Session Co-Chairs: Myung Jin Yim – Intel Corporation Daniel D. Lu – Henkel Corporation**	**Session Co-Chairs: Christopher Bower – X-Celeprint Ltd. E. Jan Vardaman – TechSearch International, Inc.**
1. ***1:30 p.m. – Development of the Technology to Control the Spatial Distribution of Plasma Using Double ICP Coil*** T. Sakuishi, T. Murayama, Y. Morikawa, and K. Suu – ULVAC, Inc.; NMEMS Technology Research Organization	1. ***1:30 p.m. – Advanced Wafer Bonding and Laser Debonding*** P. Andry, R. Budd, R. Polastre, C. Tsang, B. Dang, J. Knickerbocker, and M. Glodde – IBM Corporation	1. ***1:30 p.m. – Board Level Reliability and Surface Mount Assembly of 0.35mm and 0.3mm Pitch Wafer Level Packages*** Beth Keser, Rey Alvarado, Alan Choi, Mark Schwarz, and Steve Bezuk – Qualcomm Technologies, Inc.
2. ***1:55 p.m. – Defect Detection in Through Silicon Vias by GHz Scanning Acoustic Microscopy: Key Ultrasonic Characteristics*** Alain Phommahaxay, Harold Philipsen, Gerald Beyer, Herbert Struyf, and Eric Beyne – IMEC; Ingrid De Wolf – IMEC; KU Leuven; Tatjana Djuric, Peter Hoffrogge, and Peter Czurratis – PVA TePla Analytical Systems GmbH; Sebastian Brand – Fraunhofer IWM	2. ***1:55 p.m. – Versatile Thin Wafer Stacking Technology for Monolithic Integration of Temporary Bonded Thin Wafers*** Thomas Uhrmann, Jürgen Burggraf, Julian Bravin, Viorel Dragoi, Markus Wimplinger, Thorsten Matthias, and Paul Lindner – EV Group	2. ***1:55 p.m. – Encapsulated Wafer Level Package Technology (eWLCSP)*** Tom Strothmann, Seung Wook Yoon, and Yaojian Lin – STATS ChipPAC
3. ***2:20 p.m. – Temporary Spin-on Glass Bonding Technologies for Via-Last/ Backside-Via 3D Integration Using Multichip Self-Assembly*** H. Hashiguchi, T. Fukushima, A. Noriki, H. Kino, K. W. Lee, T. Tanaka, and M. Koyanagi – Tohoku University	3. ***2:20 p.m. – Temporary Bonding for High-Topography Applications: Spin-on Material versus Dry Film*** Anne Jourdain, Alain Phommahaxay, Greet Verbinnen, Andy Miller, Kenneth Rebibis, Gerald Beyer, and Eric Beyne – IMEC; Alice Guerrero, Susan Bailey, Mark Privett, and Kim Arnold – Brewer Science, Inc.	3. ***2:20 p.m. – Enabling of Fan-Out WLP for More Demanding Applications by Introduction of Enhanced Dielectric Material for Higher Reliability*** Rodrigo Almeida, Isabel Barros, José Campos, Paulo Cardoso, José Castro, Vitor Henriques, Eoin O'Toole, and Nelson Pinho – Nanium, S.A.
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Northern Hemisphere A-C)		
4. ***3:30 p.m. – TSV Module Optimization for High Performance Silicon Interposer*** Andrew Cao, Thomas Dinan, Zhuowen Sun, Guilian Gao, Cyprian Uzoh, Bong-Sub Lee, Liang Wang, Hong Shen, and Sitaram Arkalgud – Invensas Corporation	4. ***3:30 p.m. – Development of New Concept Thermoplastic Temporary Adhesive for 3D-IC Integration*** A. Kubo, K. Tamura, H. Imai, T. Yoshioka, S. Oya, and S. Otaka – Tokyo Ohka Kogyo Co., Ltd.	4. ***3:30 p.m. – 24" x 18" Fan-Out Panel Level Packaging*** T. Braun, K. F. Becker, J. Bauer, V. Bader, and R. Aschenbrenner – Fraunhofer IZM; S. Voges, R. Kahle, T. Thomas, and K. D. Lang – Technical University Berlin
5. ***3:55 p.m. – Study of TSV Thinning Wafer Strength Enhancement for 3DIC Package*** Jyun-Ling Tsai, Chun-Chieh Chao, Hsiao-Chun Huang, Cheng-Hsiang Liu, Hung-Hsein Chang, Chang-Lun Lu, and Shi-Ching Chen – Siliconware Precision Industries Co., Ltd.	5. ***3:55 p.m. – Underfilling Techniques Comparison in 3D CtW Stacking Approach*** A. Garnier, A. Jouve, R. Franiatte, and S. Chéramy – CEA-LETI	5. ***3:55 p.m. – Development and Characterization of New Generation Panel Fan-Out (P-FO) Packaging Technology*** Hong-Da Chang, David Chang, Kenny Liu, H. S. Hsu, Rui-Feng Tai, Hsiao-Chun Huang, Yi-Che Lai, Chang-Lun Lu, Chun-Tang Lin, and Steve Chiu – Siliconware Precision Industries Co., Ltd.
6. ***4:20 p.m. – Challenges in 3D Die Stacking*** Juergen Grafe, Wieland Wahrmund, Stephan Dobritz, Juergen Wolf, and Klaus-Dieter Lang – Fraunhofer IZM	6. ***4:20 p.m. – High Throughput Thermal Compression NCF Bonding*** Toshihisa Nonaka, Yuta Kobayashi, Noboru Asahi, Shoichi Niizeki, and Koichi Fujimaru – Toray Industries, Inc.; Yoshiyuki Arai, Toshifumi Takegami, Yoshinori Miyamoto, and Masatsugu Nimura – Toray Engineering Co., Ltd.; Hiroyuki Niwa – Toray International America Inc.	6. ***4:20 p.m. – Development of Exposed Die, Large Body to Die Size Ratio Wafer Level Package Technology*** J. Osenbach, S. Emerich, L. Golick, and S. Cate – LSI Corporation; M. Chan, S. W. Yoon, Y. J. Lin, and K. Wong – STATS ChipPac
7. ***4:45 p.m. – Wet Silicon Etch Process for TSV Reveal*** Laura B. Mauer, John Taddei, and Ramey Youssef – Solid State Equipment, LLC; Yongqiang Lu, Sian Collins, Kevin Mclaughlin, and Craig Allen – SACHEM, Inc.	7. ***4:45 p.m. – Through Silicon Underfill Dispensing for 3D Die/Interposer Stacking*** Fuliang Le, S. W. Ricky Lee, KeiMay Lau, C. Patrick Yue, Johnny K. O. Sin, Philip K. T. Mok, and Wing-Hung Ki – Hong Kong University of Science & Technology; Hoi Wai Choi – University of Hong Kong	7. ***4:45 p.m. – 3D Rectangular Waveguide Integrated in Embedded Wafer Level Ball Grid Array (eWLB) Package*** William E. R. Seler, R. Weigel, and A. Hagelauer – University of Erlangen-Nuremberg; M. Wojnowski, W. Hartner, J. Böck, and R. Lachner – Infineon Technologies

Program Sessions: Thursday, May 29, 1:30 p.m. - 5:10 p.m.

Session 22: System-Level Thermal & Mechanical Models I

Committee:
Modeling & Simulation

Southern Hemisphere IV

Session Co-Chairs:
Yong Liu – Fairchild Semiconductor Corporation
Sandeep Sane – Intel Corporation

1. ***1:30 p.m. – Interplay and Influence of Thermomechanical Stress in Copper-Filled TSV Interposers***
   Sheng-Tsai Wu and Heng-Chieh Chien – Industrial Technology Research Institute (ITRI); Cheng-Fu Chen – University of Alaska, Fairbanks

2. ***1:55 p.m. – Does Current Crowding Induce Vacancy Concentration Singularity in Electromigration?***
   Ozgur Taner, Kasemsak Kijkanjanapaiboon, and Xuejun Fan – Lamar University

3. ***2:20 p.m. – Hygro-Thermo-Mechanical Analysis and Failure Prediction in Electronic Packages by Using Peridynamics***
   Selda Oterkus and Erdogan Madenci – University of Arizona; Erkan Oterkus – University of Strathclyde; Yuchul Hwang, Jangyong Bae, and Sungwon Han – Samsung Electronics Company, Ltd.

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Northern Hemisphere A-C)

4. ***3:30 p.m. – Cohesive Zone Experiments for Copper/Mold Compound Delamination***
   William E. R. Krieger, Sathyanarayanan Raghavan, Abhishek Kwatra, and Suresh K. Sitaraman – Georgia Institute of Technology

5. ***3:55 p.m. – Damage Pre-Cursor Based Life Prediction of the Effect of Mean Temperature of Thermal Cycle on the SnAgCu Solder Joint Reliability***
   Pradeep Lall, Kazi Mirza, and Jeff Suhling – Auburn University

6. ***4:20 p.m. – Methodology Development of Warpage Analysis of Polymer Based Packaging Substrate***
   Cheolgyu Kim, Taeik Lee, Hyeseon Choi, and Taek-Soo Kim – Korea Advanced Institute of Science and Technology (KAIST); Min Sung Kim – Samsung Electro-Mechanics

7. ***4:45 p.m. – Simulations for the Impact of Warpage on the Accuracy of Attitude and Heading Reference System***
   Shengzhi Zhang, Qiang Dan, Chaojun Liu, Xing Guo, and Ming Wen – Huazhong University of Science & Technology; Wuhan National Laboratory for Optoelectronics; Yong Xu and Xin Wu – Wayne State University; Sheng Liu – Wuhan University

Session 23: Optical Interconnects

Committee:
Optoelectronics

Southern Hemisphere V

Session Co-Chairs:
Hiren Thacker – Oracle
Ping Zhou – LDX Optronics, Inc.

1. ***1:30 p.m. – Multicore Fiber 4 TX + 4 RX Optical Transceiver Based on Holey SiGe IC***
   Fuad E. Doany, Daniel M. Kuchta, Alexander V. Rylyakov, Christian Baks, Shurong Tian, Mark Schultz, Frank Libsch, and Clint L. Schow – IBM Corporation

2. ***1:55 p.m. – 336-Channel Electro-Optical Interconnect: Underfill Process Improvement, Fiber Bundle and Reliability Results***
   Shuki Benjamin, Kobi Hasharoni, Avi Maman, Stanislav Stepanov, and Michael Mesh – Compass-EOS; Helge Luesebrink, Roland Steffek, Wolfgang Pleyer, and Christian Stömmer – PVA TePla AG

3. ***2:20 p.m. – Development of Optical Multi-Channel Connector for Rigid Waveguide–Fiber Optical Interconnection***
   Kazumi Nakazuru, Masatoshi Tsunoda, and Naoki Takahashi – Kyocera Connector Products Corporation; Satoshi Asai and Takahiro Matsubara – Kyocera Corporation

4. ***3:30 p.m. – Electro-Optical Backplane Demonstrator with Gradient-Index Multimode Glass Waveguides for Board-to-Board Interconnection***
   Lars Brusberg, Henning Schröder, Julia Röder, and Daniel Weber – Fraunhofer Institute IZM; Richard Pitwon and Allen Miller – Xyratex Technology Ltd.; Simon Whalley – ILFA Feinstleitertechnik GmbH; Christian Herbst and Klaus-Dieter Lang – Technical University of Berlin

5. ***3:55 p.m. – Three-Dimensional High-Density Channel Integration of Polymer Optical Waveguide Using the Mosquito Method***
   Takaaki Ishigure, Daisuke Suganuma, and Kazutomo Soma – Keio University

6. ***4:20 p.m. – Novel Trace Design for High Data-Rate, Multi-Channel Optical Transceiver Assembled Using Flip-Chip Bonding***
   Takatoshi Yagisawa, Takashi Shiraishi, Mariko Sugawara, and Kazuhiro Tanaka – Fujitsu Laboratories, Ltd.

7. ***4:45 p.m. – Modeling, Design, and Demonstration of Ultra-Miniaturized and High Efficiency 3D Glass Photonics Modules***
   Bruce C. Chou, Vanessa Smet, Gee-Kung Chang, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Sandeep Razdan, Haipeng Zhang, Jibin Sun, and Terry Bowen – TE Connectivity

Session 24: Innovative Interconnections

Committee:
Interconnections

Americas Seminar

Session Co-Chairs:
James E. Morris – Portland State University
Nathan Lower – Rockwell Collins, Inc.

1. ***1:30 p.m. – A Study on Nanofiber Anisotropic Conductive Films (ACFs) for Fine Pitch Chip-on-Glass (COG) Interconnections***
   Sang Hoon Lee, Tae Wan Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST)

2. ***1:55 p.m. – Study of Fine Pitch Micro-Interconnections Formed by Low Temperature Bonded Copper Nanowires Based Anisotropic Conductive Film***
   Jing Tao, Alan Mathewson, and Kafil M. Razeeb – University College Cork

3. ***2:20 p.m. – Carbon Nanofibers (CNF) for Enhanced Solder-Based Nano-Scale Integration and On-Chip Interconnect Solutions***
   V. Desmaris, A. M. Saleem, S. Shafiee, J. Berg, M. S. Kabir, and A. Johansson – Smoltek AB; Phil Marcoux – PPM Associates

4. ***3:30 p.m. – Pressure-Less Plasma Sintering of Cu Paste for SiC Die-Attach of High-Temperature Power Device Manufacturing***
   S. Nagao, S. Sakamoto, S. W. Park, T. Sugahara, and K. Suganuma – Osaka University; K. Kodani – Nissin, Inc.

5. ***3:55 p.m. – Arrays of Millimeter-Wave Silicon Waveguides for Interchip Communication on Glass Interposer***
   Qidong Wang, Daniel Guidotti, Liqiang Cao, Daquan Yu, Shuling Wang, Xugang Wang, and Tianchun Ye – Institute of Microelectronics, Chinese Academy of Sciences; National Center for Advanced Packaging; Delong Qiu and Lixi Wan – National Center for Advanced Packaging

6. ***4:20 p.m. – Flip Chip Based on Compliant Double Helix Interconnect for High Frequency Applications***
   Pingye Xu, George A. Hernandez, Shiqiang Wang, Jie Zhong, Charles D. Ellis, and Michael C. Hamilton – Auburn University

7. ***4:45 p.m. – Modeling of Crosstalk Effects in Coupled MLGNR Interconnects Based on FDTD Method***
   Vobulapuram Ramesh Kumar, Brajesh Kumar Kaushik, and Amalendu Patnaik – Indian Institute of Technology Roorkee

Program Sessions: Friday, May 30, 8:00 a.m. - 11:40 a.m.

Session 25: Recent Advances in 3D Package Reliability	Session 26: 3D Microbumps	Session 27: Sensors & MEMS Technologies
Committee: Applied Reliability	**Committee: Interconnections**	**Committee: Advanced Packaging**
Southern Hemisphere I	**Southern Hemisphere II**	**Southern Hemisphere III**
Session Co-Chairs: **Deepak Goyal – Intel Corporation** **Jeffrey Suhling – Auburn University**	**Session Co-Chairs:** **Kathy Cook – Ziptronix** **Lei Shan – IBM Corporation**	**Session Co-Chairs:** **Joseph W. Soucy – Draper Laboratory** **Daniel Baldwin – Engent, Inc.**
1. ***8:00 a.m. – First Demonstration of Reliable Copper-Plated 30µm Diameter Through-Package-Vias in Ultra-Thin Bare Glass Interposers*** Kaya Demir, Andac Armutlulu, Jialing Tong, Raghuram Pucha, Venkatesh Sundaram, and Rao Tummala – Georgia Institute of Technology	1. ***8:00 a.m. – Formic Acid Treatment with Pt Catalyst for Cu Direct and Hybrid Bonding at Low Temperature*** Tadatomo Suga, Masakate Akaike, and Wenhua Yang – University of Tokyo	1. ***8:00 a.m. – A Novel 3D Packaging Concept for RF Powered Sensor Grains*** Walther Pachler, Jasmin Grosinger, and Wolfgang Bösch – Graz University of Technology; Klaus Pressel, Gottfried Beer, and Gerald Holweg – Infineon Technologies AG; Christian Zilch – Magna Diagnostics GmbH; Manfred Meindl – Danube Mobile Communications Engineering GmbH & Co. KG
2. ***8:25 a.m. – Through-Glass Interposer Integrated High Quality RF Components*** Cheolbok Kim, Hyup Jong Kim, and Yong-Kyu Yoon – University of Florida; David E. Senior – University of Florida; Universidad Tecnologica de Bolivar; Aric Shorey and Windsor Thomas – Corning, Inc.	2. ***8:25 a.m. – Direct Multichip-to-Wafer 3D Integration Technology Using Flip-Chip Self-Assembly of NCF-Covered Known Good Dies*** Yuka Ito – Tohoku University; Sumitomo Bakelite Co., Ltd.; Mariappan Murugesan, Takafumi Fukushima, Kang-Wook Lee, Tetsu Tanaka, and Mitsumasa Koyanagi – Tohoku University; Koji Choki – Sumitomo Bakelite Co., Ltd.	2. ***8:25 a.m. – A Novel Sound Sensor and Its Package Used in Lung Sound Diagnosis*** Xingming Fu, Chaojun Liu, and Sheng Liu – Wuhan University; Yong Xu – Wuhan University; Wayne State University; Yating Hu and Xin Wu – Wayne State University; Xiaobing Luo – Huazhong University of Science & Technology
3. ***8:50 a.m. – Minimization of Keep-Out Zone (KOZ) in 3D IC by Local Bending Stress Suppression with Low Temperature Curing Adhesive*** Hisashi Kino, Hideto Hashiguchi, Yohei Sugawara, Seiya Tanikawa, Takafumi Fukusima, Kangwook Lee, Mitsumasa Koyanagi, and Tetsu Tanaka – Tohoku University	3. ***8:50 a.m. – Maskless Screen Printing Technology for 20µm-Pitch, 52InSn Solder Interconnections in Display Applications*** Kwang-Seong Choi, Haksun Lee, Hyun-Cheol Bae, and Yong-Sung Eom – ETRI	3. ***8:50 a.m. – Novel System-in-Package Design and Packaging Solution for Solid State Lighting Systems*** Mingzhi Dong, Fabio Santagata, and Jia Wei – Delft University of Technology; State Key Laboratory of Solid State Lighting; Cadmus Yuan – Chinese Academy of Sciences; State Key Laboratory of Solid State Lighting; Guoqi Zhang – Chinese Academy of Sciences; Delft University of Technology
Refreshment Break: 9:15 a.m. - 10:00 a.m. (Southern Hemisphere Foyer)		
4. ***10:00 a.m. – Effect of Thermal Annealing on TSV Cu Protrusion and Local Stress*** Xiangmeng Jing, Hongwen He, Meiying Su, Chongshen Song, Daquan Yu, Liqiang Cao, and Dongkai Shangguan – National Center for Advanced Packaging; Institute of Microelectronics, Chinese Academy of Sciences; Liang Ji, Cheng Xu, Kai Xue, and Wenqi Zhang – National Center for Advanced Packaging	4. ***10:00 a.m. – Accelerated SLID Bonding Using Thin Multi-Layer Copper-Solder Stack for Fine-Pitch Interconnections*** Chinmay Honrao, Ting-Chia Huang, Vanessa Smet, P. Markondeya Raj, and Rao Tummala – Georgia Institute of Technology; Makoto Kobayashi – Namics Corporation	4. ***10:00 a.m. – Implantable Device Including a MEMS Accelerometer and an ASIC Chip Encapsulated in a Hermetic Silicon Box for Measurement of Cardiac Physiological Parameter*** Jean-Charles Souriau, Laetitia Castagné, Guy Parat, and Gilles Simon – CEA-LETI; Karima Amara, Philippe D'hiver, and Renzo Dal Molin – Sorin CRM SAS
5. ***10:25 a.m. – Effect of High Temperature Storage on the Stress and Reliability of 3D Stacked Chips*** Tengfei Jiang, Chenglin Wu, Jay Im, Rui Huang, and Paul S. Ho – University of Texas, Austin; Peng Su, Pierre Chia, and Li Li – Cisco Systems, Inc.; Ho-Young Son, Min-Suk Suh, and Nam-Seog Kim – SK Hynix, Inc.	5. ***10:25 a.m. – Study of Electro-Migration Resistivity of Micro Bump Using SnBi Solder*** Kei Murayama, Mitsuhiro Aizawa, and Mitsutoshi Higashi – Shinko Electric Industries Company, Ltd.	5. ***10:25 a.m. – Capping Technologies for Wafer Level MEMS Packaging Based on Permanent and Temporary Wafer Bonding*** K. Zoschke, M. Wilke, M. Wegner, K. Kaletta, C. A. Manier, and H. Oppermann – Fraunhofer IZM; M. Wietstruck, B. Tillack, and M. Kaynak – IHP GmbH; K.-D. Lang – Technical University Berlin
6. ***10:50 a.m. – A Novel Fine Pitch TSV Interconnection Method Using NCF with Zn Nano-Particles*** Ji-Won Shin, Yong-Won Choi, Young Soon Kim, and Kyoung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST); Un Byung Kang and Sun Kyung Seo – Samsung Electronics Company, Ltd.	6. ***10:50 a.m. – The Impact of Different Under Bump Metallurgies and Redistribution Layers on the Electromigration of Solder Balls for Wafer-Level Packaging*** Christine Hau-Riege, Beth Keser, Rey Alvarado, Ahmer Syed, Youwen Yau, Steve Bezuk, and Kevin Caffey – Qualcomm Technologies, Inc.	6. ***10:50 a.m. – The Novel Assembly Method of a Field Deployable Biosensor Unit*** P. Xu, F. M. Guo, X. Y. Liu, J. H. Shen, L. Ding, W. Wang, Y. Q. Li, Y. P. Ge, S. H. Zhang, M. J. Wang, and H. Z. Zheng – East China Normal University; J. T. Ye and L. Luo – Chinese Academy of Sciences
7. ***11:15 a.m. – Residual Stress Investigations at TSVs in 3D Micro Structures by HR-XRD, Raman Spectroscopy and fibDAC*** U. Zschenderlein, O. Hölck, and H. Rajendran – Technical University Chemnitz; D. Vogel and E. Auerswald – Fraunhofer ENAS; P. Ramm – Fraunhofer EMFT; R. Pufall – Infineon Technologies; B. Wunderle – Technical University Chemnitz; Fraunhofer ENAS	7. ***11:15 a.m. – Low-Pressure Sintering Bonding with Cu and CuO Flake Paste for Power Devices*** S. W. Park, R. Uwataki, S. Nagao, T. Sugahara, and K. Suganuma – Osaka University; Y. Katoh, H. Ishino, K. Sugiura, and K. Tsuruta – Denso Corporation	7. ***11:15 a.m. – SIMEIT-Project: High Precision Inertial Sensor Integration on a Modular 3D-Interposer Platform*** Wolfram Steller, M. Juergen Wolf, and K. Dieter Lang – Fraunhofer IZM; Christoph Meinecke – Technical University Chemnitz; Knut Gottfried – Fraunhofer ENAS; Gregor Woldt – Microelectronic Packaging Dresden GmbH; Wolfgang Günther – GEMAC

Program Sessions: Friday, May 30, 8:00 a.m. - 11:40 a.m.

Session 28: System-Level Thermal & Mechanical Models II	Session 29: Integrated RF & Power Modules	Session 30: Solders & Bonding
Committee: Modeling & Simulation	**Committee: Electronic Components & RF**	**Committee: Materials & Processing**
Southern Hemisphere IV	**Southern Hemisphere V**	**Americas Seminar**
Session Co-Chairs: **Pradeep Lall – Auburn University** **Xuejun Fan – Lamar University**	**Session Co-Chairs:** **Rockwell Hsu – Cisco Systems, Inc.** **P. Markondeya Raj – Georgia Institute of Technology**	**Session Co-Chairs:** **Mikel Miller – Draper Laboratory** **Grace Yi Li – Intel Corporation**
1. *8:00 a.m. – Mechanical Stress Management for Electrical Chip-Package Interaction (e-CPI)* Wei Zhao, Mark Nakamoto, Vidhya Ramachandran, and Riko Radojcic – Qualcomm Technologies, Inc.	**1. *8:00 a.m. – Modeling, Design and Demonstration of Multi-Die Embedded WLAN RF Front-End Module with Ultra-Miniaturized and High-Performance Passives*** Srikrishna Sitaraman, Christopher White, Sung Jin Kim, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Yuya Suzuki – Zeon Corporation; Vijay Nair and Telesphor Kamgaing – Intel Corporation; Frank Juskey – TriQuint Semiconductor	**1. *8:00 a.m. – Wafer IMS (Injection Molded Solder) – A New Fine Pitch Solder Bumping Technology on Wafers with Solder Alloy Composition Flexibility*** Jae-Woong Nah, Jeffrey Gelorme, Peter Sorce, Paul Lauro, Eric Perfecto, Mark McLeod, Kazushige Toriyama, Yasumitsu Orii, and Peter Brofman – IBM Corporation; Takashi Nauchi and Ryoichi Suzuki – Senju Metal Industry Co., Ltd.; Akira Takaguchi and Kazuya Ishiguro – Senju System Technology Co., Ltd.; Tomoyasu Yoshikawa and Derek Daily – Senju Comtek Corp.
2. *8:25 a.m. – Cu Pillar Flip Chip Assembly: Chip Attach Process Failure Mode Study* Shengmin Wen and Bora Baloglu – Amkor Technology; Guangfeng Li – Amkor Assembly and Test (Shanghai) Co., Ltd.	**2. *8:25 a.m. – A Compact 4-Chip Package with 64 Embedded Dual-Polarization Antennas for W-Band Phased-Array Transceivers*** Xiaoxiong Gu, Duixian Liu, Christian Baks, Alberto Valdes-Garcia, Ben Parker, Md. R. Islam, and Scott K. Reynolds – IBM Corporation; Arun Natarajan – IBM Corporation; Oregon State University	**2. *8:25 a.m. – Reliability of Paste Based Transient Liquid Phase Sintered Interconnects*** Hannes Greve, S. Ali Moeini, and F. Patrick McCluskey – University of Maryland
3. *8:50 a.m. – Mechanical and Thermo-Mechanical Stress Considerations in Applying 3D ICs to a Design* Jia-Shen Lan and Mei-Ling Wu – National Sun Yat-Sen University	**3. *8:50 a.m. – Active Die Embedded Small Form Factor RF Packages for Ultrabooks and Smartphones*** Vijay K. Nair, Carlton Hanna, Ronald Spreitzer, and Johanna Swan – Intel Corporation	**3. *8:50 a.m. – A Lead Free Joining Technology for High Temperature Interconnects Using Transient Liquid Phase Soldering (TLPS)*** Christian Ehrhardt and Klaus-Dieter Lang – Technical University Berlin; Matthias Hutter and Hermann Oppermann – Fraunhofer IZM
Refreshment Break: 9:15 a.m. - 10:00 a.m. (Southern Hemisphere Foyer)		
4. *10:00 a.m. – Modeling Microstructure Effects on Electromigration in Lead-Free Solder Joints* Jiamin Ni and Antoinette Maniatty – Rensselaer Polytechnic Institute; Yong Liu, Jifa Hao, and Barry O'Connell – Fairchild Semiconductor	**4. *10:00 a.m. – Design and Material Contributions to Second-Harmonic Nonlinearities in RF Silicon Integrated Passive Devices*** Robert Frye – RF Design Consulting, LLC; Robert Melville – Emecon, LLC; Kai Liu – STATS ChipPAC, Inc.	**4. *10:00 a.m. – Developments of High-Bi Alloys as a High Temperature Pb-Free Solder*** Sandeep Mallampati and Junghyun Cho – Binghamton University; Harry Schoeller – Universal Instruments Corporation; Liang Yin and David Shaddock – GE Global Research
5. *10:25 a.m. – Experimental Demonstration of the Effect of Copper TPVs (Through Package Vias) on Thermal Performance of Glass Interposers* Sangbeom Cho, Venky Sundaram, Yogendra Joshi, and Rao Tummala – Georgia Institute of Technology; Yoichiro Sato – Asahi Glass	**5. *10:25 a.m. – Integration of Magnetic Materials into Package RF and Power Inductors on Organic Substrates for System in Package (SiP) Applications*** Hao Wu, Cheng Lv, and Hongbin Yu – Arizona State University; Donald S. Gardner and Zhihua Zou – Intel Corporation	**5. *10:25 a.m. – The Quantum Theory of Solid-State Atomic Bonding*** Chin C. Lee and Lianxi Cheng – University of California, Irvine
6. *10:50 a.m. – Failure Mechanism Investigation of Stacked Via Cracking in Organic Chip Carrier* Shidong Li, Yi Pan, Sushumna Iruvanti, David L. Questad, and Randall J. Werner – IBM Corporation	**6. *10:50 a.m. – Through Silicon Capacitor Co-Integrated with TSV as an Efficient 3D Decoupling Capacitor Solution for Power Management on Silicon Interposer*** O. Guiller, S. Joblot, and A. Farcy – STMicroelectronics; Y. Lamy and E. Defay – CEA-LETI; K. Dieng – Université de Savoie	**6. *10:50 a.m. – Effective Method to Disperse and Incorporate Carbon Nanotubes in Electroless Ni-P Deposits*** Sha Xu and Yan Cheong Chan – City University of Hong Kong; Xiaoxin Zhu, Hua Lu, and Chris Bailey – University of Greenwich
7. *11:15 a.m. – A Novel Method to Predict Fluid/Structure Interaction in IC Packaging* Chih-Chung Hsu – National Tsing Hua University; Tzu-Chang Wang, Yen-Chi Chen, and Yang-Kai Lin – CoreTech System (Moldex3D) Co., Ltd.	**7. *11:15 a.m. – Design of RF and Thermal Pads of CMOS PAs Using Copper to Copper Bonding Technology*** Lih-Tyng Hwang – National Sun Yat-Sen University; An-Yu Kuo – Cadence Design Systems, Inc.	**7. *11:15 a.m. – Electroless Ni-W-P Alloy as a Barrier Layer between Zn-Based High Temperature Solders and Cu Substrates*** Li Liu and Changqing Liu – Loughborough University; Longzao Zhou – Huazhong University of Science and Technology

Program Sessions: Friday, May 30, 1:30 p.m. - 5:10 p.m.

Session 31: PoP, SiP, and Die Stacking

Committee: Advanced Packaging

Southern Hemisphere I

Session Co-Chairs:
Raj N. Master – Microsoft Corporation
Deborah Patterson – Amkor Technology, Inc.

1. ***1:30 p.m. – Fabrication and Reliability Evaluation of a Novel Package-on-Package (PoP) Structure Based on Organic Substrate***
   Xiaofeng Sun and Yuan Lu – National Center for Advanced Packaging; Institute of Microelectronics, Chinese Academy of Sciences; Lixi Wan – Institute of Microelectronics, Chinese Academy of Sciences

2. ***1:55 p.m. – Strip Grinding Introduction for Thin PoP***
   Jinseong Kim, Yesul Ahn, Gyuwan Han, Byoungwoo Cho, Dongjoo Park, Juhoon Yoon, and Chooheung Lee – Amkor Technology Korea, Inc.; Lou Nicholls and Shengmin Wen – Amkor Technology Inc.

3. ***2:20 p.m. – Cost and Performance Effective Silicon Interposer and Vertical Interconnect for 3D ASIC and Memory Integration***
   Li Li and Jie Xue – Cisco Systems, Inc.; Mitsutoshi Higashi, Akihito Takano, and Gary Ikari – Shinko Electric Industries Company, Ltd.

Session 32: Substrates

Committee: Materials & Processing

Southern Hemisphere II

Session Co-Chairs:
Yu-Hua Chen – Unimicron
Dong Wook Kim – Qualcomm Technologies, Inc.

1. ***1:30 p.m. – Improvement of Substrate and Package Warpage by Copper Plating Process Optimization***
   Omar Bchir, Houssam Jomaa, Chin Kwan Kim, Layal Rouhana, Kuiwon Kang, Milind Shah, and Steve Bezuk – Qualcomm Technologies, Inc.

2. ***1:55 p.m. – Coreless Substrate with Asymmetric Design to Improve Package Warpage***
   Wei Lin, Bora Baloglu, and Ken Stratton – Amkor Technology

3. ***2:20 p.m. – Ultra Low CTE (1.8 ppm/°C) Core Material for Next Generation Thin CSP***
   Tomohiko Kotake, Hikari Murai, Shin Takanezawa, Masato Miyatake, Masaaki Takekoshi, and Masahisa Ose – Hitachi Chemical Co., Ltd.

Session 33: Novel Test Methods

Committee: Applied Reliability

Southern Hemisphere III

Session Co-Chairs:
Lakshmi N. Ramanathan – Microsoft Corporation
Sridhar Canumalla – Microsoft Corporation

1. ***1:30 p.m. – Pad Crater Detection Using Acoustic Waveform Analysis***
   W. Carter Ralph – Southern Research Institute; Elizabeth E. Benedetto, Aileen M. Allen, and Keith Newman – Hewlett Packard

2. ***1:55 p.m. – High Acceleration Board Level Reliability Drop Test Using Dual Mass Shock Amplifier***
   Andy Zhang – Texas Instruments, Inc.

3. ***2:20 p.m. – Non-Destructive Crack and Defect Detection in SAC Solder Interconnects***
   Using Cross-Sectioning and X-Ray Micro-CT
   Pradeep Lall, Shantanu Deshpande, Junchao Wei, and Jeff Suhling – Auburn University

Refreshment Break: 2:45 p.m. - 3:30 p.m. (Southern Hemisphere Foyer)

4. ***3:30 p.m. – Assembly and Packaging of Non-Bumped 3D Chip Stacks on Bumped Substrates***
   Bing Dang, Joana Maria, Qianwen Chen, Jae-Woong Nah, Paul Andry, Cornelia Tsang, Katsuyuki Sakuma, Christy Tyberg, Raphael Robertazzi, Michael Scheuermann, Michael Gaynes, and John Knickerbocker – IBM Corporation

5. ***3:55 p.m. – The Miniaturization of a Micro-Ball Endoscope by SiP Approach***
   Xunxun Zhu, Jian Cai, Yu Chen, Yingke Gu, Xiang Xie, Qian Wang, and Zhihua Wang – Tsinghua University; Xiaofeng Sun and Lixi Wan – Chinese Academy of Sciences

6. ***4:20 p.m. – Design and Demonstration of Paper-Thin and Low-Warpage Single and 3D Organic Packages with Chip-Last Embedding Technology for Smart Mobile Applications***
   Sung Jin Kim, Zihan Wu, Fuhan Liu, Vanessa Smet, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Makoto Kobayashi – Namics Corporation

7. ***4:45 p.m. – Manufacturing Readiness of BVA Technology for Ultra-High Bandwidth Package-on-Package***
   Rajesh Katkar, Rey Co, and Wael Zohni – Invensas Corporation

4. ***3:30 p.m. – A Novel Redistribution Layer Tailored by Nanotwinned Copper Decreases Warpage in Wafer Level Packaging***
   Heng Li, Wenguo Ning, Chunsheng Zhu, Gaowei Xu, and Le Luo – Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences

5. ***3:55 p.m. – Demonstration of 3–5 µm RDL Line Lithography on Panel-Based Glass Interposers***
   Hao Lu, Yuya Suzuki, Brett Sawyer, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Yutaka Takagi – NGK Spark Plug Co., Ltd.; Robin Taylor – Atotech GmbH

6. ***4:20 p.m. – Characterization of Thin Polymer Films with the Focus on Lateral Stress and Mechanical Properties and Their Relevance to Microelectronics***
   Markus Woehrmann and Klaus-Dieter Lang – Technical University Berlin; Thorsten Fischer, Hans Walter, and Michael Toepper – Fraunhofer IZM

7. ***4:45 p.m. – Thin Polymer Dry-Film Dielectric Material and a Process for 10 µm Interlayer Vias in High Density Organic and Glass Interposers***
   Yuya Suzuki – Zeon Corporation; Georgia Institute of Technology; Yutaka Takagi – NGK Spark Plug Co., Ltd.; Venky Sundaram and Rao Tummala – Georgia Institute of Technology

4. ***3:30 p.m. – High Resolution and Fast Throughput-Time X-Ray Computed Tomography for Semiconductor Packaging Applications***
   Yan Li, Mario Pacheco, and Deepak Goyal – Intel Corporation; John W. Elmer and Holly D. Barth – Lawrence Livermore National Laboratory; Dula Parkinson – Lawrence Berkeley National Laboratory

5. ***3:55 p.m. – In-Situ Measurements of the Relative Thermal Resistance: Highly Sensitive Method to Detect Crack Propagation in Solder Joints***
   Gordon Elger and Shri Vishnu Kandaswamy – Technische Hochschule Ingolstadt; Maarten von Kouwen and Robert Derix – Philips Technology GmbH; Fosca Conti – University of Padova

6. ***4:20 p.m. – Reliability Testing of Wire Bonds Using Pad Resistance with van der Pauw Method***
   Michael Mayer and Samuel Kim – University of Waterloo

7. ***4:45 p.m. – Colour Shift in Remote Phosphor-Based LED Products***
   M. Yazdan Mehr – Materials Innovation Institute; Delft University of Technology; W. D. Van Driel – Philips Lighting; Delft University of Technology; G. Q. Zhang – Delft University of Technology

Program Sessions: Friday, May 30, 1:30 p.m. - 5:10 p.m.

Session 34: Novel Packaging	Session 35: Innovations in Wirebond Technology	Session 36: Recent Advancement in Manufacturing Technology
Committee: Emerging Technologies	**Committee: Interconnections**	**Committee: Assembly & Manufacturing Technology**
Southern Hemisphere IV	**Southern Hemisphere V**	**Americas Seminar**
Session Co-Chairs: **Vasudeva P. Atluri – Renavitas Technologies** **Jai Agrawal – Purdue University**	**Session Co-Chairs:** **William Chen – Advanced Semiconductor Engineering, Inc.** **Gilles Poupon – CEA-LETI**	**Session Co-Chairs:** **Paul Houston – Engent** **Hirofumi Nakajima – Consultant**
1. 1:30 p.m. – Multifunctional System Integration in Flexible Substrates K. Bock, E. Yacoub-George, W. Hell, A. Drost, H. Wolf, D. Bollmann, C. Landesberger, G. Klink, H. Gieser, and C. Kutter – Fraunhofer EMFT	***1. 1:30 p.m. – Process Optimization and Reliability Study for Cu Wire Bonding Advanced Nodes*** Ivy Qin, Hui Xu, Basil Milton, Nestor Mendoza, Horst Clauberg, and Bob Chylak – Kulicke and Soffa Industries, Inc.; Hidenori Abe, Dongchul Kang, Yoshinori Endo, Masahiko Osaka, and Shinya Nakamura – Hitachi Chemical Co., Ltd.	***1. 1:30 p.m. – High Uniformity and High Speed Copper Pillar Plating Technique*** Konstantin Kholostov, Aliaksei Klyshko, and Rocco Crescenzi – Sapienza University of Rome; Danilo Ciarniello, Paolo Nenzi, and Roberto Pagliucci – Rise Technology; Dario Bernardi – 2BG; Marco Balucani – Sapienza University of Rome, Rise Technology
2. 1:55 p.m. – Preparation of a Micro Rubidium Vapor Cell and Its Integration in a Chip-Scale Atomic Magnetometer Yu Ji, Jintang Shang, and Youpeng Chen – Southeast University; Ching-Ping Wong – Chinese University of Hong Kong	***2. 1:55 p.m. – Silver-Assisted Copper Wire Bonding Using Solid-State Processes*** Yi-Ling Chen, Yuan-Yun Wu, and Chin C. Lee – University of California, Irvine	***2. 1:55 p.m. – Plasma-Based Die Singulation Processing Technology*** Kenneth D. Mackenzie, David Pays-Volard, Linnell Martinez, Christopher Johnson, Thierry Lazerand, and Russell Westerman – Plasma-Therm LLC
3. 2:20 p.m. – Nanowires-Based, High-Density Capacitors and Thinfilm Power Sources in Ultra-Thin 3D Glass Modules Saumya Gandhi, Liyi Li, Ho-Yee Hui, Parthasarathi Chakraborti, Himani Sharma, P. Markondeya Raj, C. P. Wong, and Rao Tummala – Georgia Institute of Technology	***3. 2:20 p.m. – Ag Alloy Wire Characteristic and Benefits*** Jensen Tsai, Albert Lan, D. S. Jiang, Li Wei Wu, Joseph Huang, and J. B. Hong – Siliconware Precision Industries Co., Ltd.	***3. 2:20 p.m. – Removed Organic Solderability Preservative (OSP) by Ar/O_2 Microwave Plasma to Improve Solder Joint in Thermal Compression Flip Chip Bonding*** Jr-Wei Peng, Yan-Siang Chen, and Yi Chen – ASE Group; Jiang-Long Liang, Kwang-Lung Lin, and Yuh-Lang Lee – National Cheng Kung University
Refreshment Break: 2:45 p.m. - 3:30 p.m. (Southern Hemisphere Foyer)		
4. 3:30 p.m. – Development of a High Density Glass Interposer Based on Wafer Level Packaging Technologies Michael Töpper, Lars Brusberg, Nils Jürgensen, and Ivan Ndip – Fraunhofer IZM; Markus Wöhrmann and Klaus-Dieter Lang – Technical University, Berlin	***4. 3:30 p.m. – Copper versus Palladium Coated Copper Wire Process and Reliability Differences*** Chu-Chung (Stephen) Lee, TuAnh Tran, Dan Boyne, Leo Higgins, and Andrew Mawer – Freescale Semiconductor, Inc.	***4. 3:30 p.m. – A PoP Structure to Support I/O over 2000*** Dyi-Chung Hu, Puru Lin, Yu Hua Chen, and Chun-Ting Lin – Unimicron Technology Corporation
5. 3:55 p.m. – Novel Sealing Technology for Organic EL Display and Lighting by Means of Modified Surface Activated Bonding Method Takashi Matsumae, Masahisa Fujino, and Tadatomo Suga – University of Tokyo	***5. 3:55 p.m. – Improving the Bond Quality of Copper Wire Bonds Using a Friction Model Approach*** Simon Althoff, Jan Neuhaus, Tobias Hemsel, and Walter Sextro – University of Paderborn	***5. 3:55 p.m. – Enabling Eutectic Soldering of 3D Opto-Electronics onto Low Tg Flexible Interposers*** Meriem Ben-Salah Akin, Lutz Rissing, and Wolfgang Heumann – Leibniz University of Hanover
6. 4:20 p.m. – Solder Joint Inspection with Induction Thermography Johannes Bohm, Klaus-Juergen Wolter, and Henning Heuer – Technical University Dresden	***6. 4:20 p.m. – High Aspect Ratio Lithography for Litho-Defined Wire Bonding*** Zahra Kolahdouz Esfahani, Henk van Zeijl, and G. Q. Zhang – Delft University of Technology	***6. 4:20 p.m. – Parameter Optimization in Assembly Manufacturing Process for a Power Module*** Yumin Liu and Yong Liu – Fairchild Semiconductor Corporation
7. 4:45 p.m. – Development of B-Spline X-Ray Diffraction Imaging Techniques for Die Warpage and Stress Monitoring inside Fully Encapsulated Packaged Chips C. S. Wong, A. Cowley, N. S. Bennett, and P. J. McNally – Dublin City University; A. Ivankovic and I. De Wolf – IMEC; KU Leuven; A. N. Danilewsky – Albert-Ludwigs-Universität; M. Gonzalez, V. Cherman, and B. Vandevelde – IMEC	***7. 4:45 p.m. – Comprehensive Intermetallic Compound Phase Analysis and Its Thermal Evolution at Cu Wirebond Interface*** In-Tae Bae and Dae Young Jung – Binghamton University; Jenny Chang and Scott Chen – Advanced Semiconductor Engineering, Inc.	***7. 4:45 p.m. – Automated Inspection and Metrology for 2.5D and 3D/TSV Process Assurance*** James Wood, Vilmarie Soler, and Eric Perfecto – IBM Corporation; Thomas Luckenbach and Aki Shoukrun – Camtek

Interactive Presentations: Wednesday, May 28 and Thursday, May 29, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

Wednesday, May 28
Session 37: Interactive Presentations 1
9:00 a.m. – 11:00 a.m.
Committee:
Interactive Presentations
Northern Hemisphere A-C

Session Co-Chairs:
Mark Poliks – i3 Electronics, Inc.
Ibrahim Guven – University of Arizona

1. ***Investigation of a Photodefinable Glass Substrate for Millimeter-Wave Radios on Package***
   Telesphor Kamgaing, Adel A. Elsherbini, Torrey W. Frank, Sasha N. Oster, and Valluri R. Rao – Intel Corporation
2. ***Design and Fabrication of Low-Pressure Piezoresistive MEMS Sensor for Fuel Cell Electric Vehicles***
   Minkyu Lee, Kiyoung Nam, Seungyong Lee, Hakgu Kim, Chimyung Kim, Yongsun Park, and Byungki Ahn – Hyundai Motor Company; Taewan Kim and Hochul Seo – Sejong Industrial Company, Ltd.
3. ***Demonstration of TCNCP Flip Chip Reliability with 30µm Pitch Cu Bump and Substrate with Thin Ni and Thick Au Surface Finish***
   Weihong Zhang, Shengping Hong, Xiaolong Yan, Feng Zhou, and Tonglong Zhang – Nantong Fujitsu Microelectronics Co., Ltd.
4. ***Integrated Process Characterization and Fabrication Challenges for 2.5D IC Packaging Utilizing Silicon Interposer with Backside Via Reveal Process***
   Cheng-Hsiang Liu, Jyun-Ling Tsai, Hung-Hsien Chang, Chang-Lun Lu, and Shih-Ching Chen – Siliconware Precision Industries Co., Ltd.
5. ***Structure Effects on the Electrical Reliability of Fine-Pitch Cu Micro-Bumps for 3D Integration***
   Byeong-Rok Lee, June-Bum Kim, Seung-Hyun Kim, Byeong-Hyun Bae, and Young-Bae Park – Andong National University; Ho-Young Son, Tac-Keun Oh, Min-Suk Suh, and Nam-Seog Kim – SK Hynix Inc.
6. ***Demonstration of Low Cost TSV Fabrication in Thick Silicon Wafers***
   E. Vick, D. S. Temple, R. Anderson, and J. Lannon – RTI International; C. Li, K. Peterson, G. Skidmore, and C. J. Han – DRS RSTA, Inc.
7. ***X-Ray Micro-Beam Diffraction Measurement of the Effect of Thermal Cycling on Stress in Cu TSV: A Comparative Study***
   Chukwudi Okoro, Lyle E. Levine, and Yaw Obeng – NIST; Ruqing Xu – Argonne National Laboratory; Klaus Hummler – SEMATECH
8. ***Adhesive Enabling Technology for Directly Plating Copper onto Glass/Ceramic Substrates***
   Hailuo Fu, Sara Hunegnaw, Zhiming Liu, Lutz Brandt, and Tafadzwa Magaya – Atotech USA Inc.
9. ***Very Thin POP and SIP Packaging Approaches to Achieve Functionality Integration Prior to TSV Implementation***
   Fernando Roa – Amkor Technology, Inc.
10. ***A Study on the Fine Pitch Chip Interconnection Using Cu/SnAg Bumps and B-Stage Non-Conductive Films (NCFs) for 3D-TSV Vertical Interconnection***
    Yongwon Choi, Jiwon Shin, Young Soon Kim, Kyung-Lim Suk, Il Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST)
11. ***Pathfinding Methodology for Optimal Design and Integration of 2.5D/3D Interconnects***
    Farhang Yazdani – BroadPak Corporation; John Park – Mentor Graphics Corporation
12. ***Cost Effective Interposer for Advanced Electronic Packages***
    Satoru Kuramochi, Sumio Koiwa, and Kousuke Suzuki – Dai Nippon Printing Co., Ltd.; Yoshitaka Fukuoka – WEISTI
13. ***Thermal Management for Wafer Level Packaging (WLP)***
    Tiao Zhou and Arkadii Samoilov – Maxim Integrated
14. ***Inkjet Printed Nano-Particle Cu Process for Fabrication of Re-Distribution Layers on Silicon Wafer***
    Ayat Soltani, Tero Kumpulainen, and Matti Mäntysalo – Tampere University of Technology
15. ***Design of Multi-Sensor for Safety Monitoring of Heavy Machinery***
    Long Li, Zhang Luo, Shengzhi Zhang, and Qiang Dan – Huazhong University of Science & Technology; Fei Hou – Dongfeng Automobile Electronics Co., Ltd.; Jinghao Qiu – Nanjing University of Aeronautics and Astronautics; Sheng Liu – Wuhan University
16. ***Novel TSV Process Technologies for 2.5D/3D Packaging***
    Y. Morikawa, T. Murayama, T. Sakuishi, and K. Suu – ULVAC, Inc.; NMEMS Technology Research Organization; A. Suzuki and Y. Nakamuta – ULVAC, Inc.
17. ***Increasing the Lifetime of Electronic Packaging by Higher Temperatures: Solders vs. Silver Sintering***
    Aaron Hutzler, Adam Tokarski, Silke Kraft, Sigrid Zischler, and Andreas Schletz – Fraunhofer IISB
18. ***Comparison of New Die-Attachment Technologies for Power Electronic Assemblies***
    Eike Möller, Adeel Ahmad Bajwa, and Jürgen Wilde – University of Freiburg; Eugen Rastjagaev – Infineon Technologies AG
19. ***High Vacuum Wafer Level Packaging for High-Value MEMS Applications***
    S. Nicolas, F. Greco, S. Caplet, C. Coutier, C. Dressler, M. Audoin, X. Baillin, G. Dehag, F. Souchon, and S. Fanget – CEA-LETI
20. ***Thermal and Electrical Tests of Air-Gap TSV***
    Cui Huang, Dong Wu, and Zheyao Wang – Tsinghua University
21. ***Heterogeneous System Integration Pseudo-SoC Technology for Smart-Health-Care Intelligent Life Monitor Engine and Eco-System (SILMEE)***
    Hiroshi Yamada, Yasuhiro Sato, Nobuhiro Ooshima, Hiroyuki Hirai, Takuji Suzuki, and Shigenobu Minami – Toshiba
22. ***Effects of Various Environmental Conditions on the Electrical Properties and Interfacial Reliability of Printed Ag/Polyimide System***
    Byung-Hyun Bae, Min-Su Jeong, Byeong-Rok Lee, and Young-Bae Park – Andong National University; Joung-Hoon Choo, Eun-Kuk Choi, and Jong-Sun Yoon – HICEL
23. ***Wafer Level Warpage Characterization for Backside Manufacturing Processes of TSV Interposers***
    Feng Jiang – National Center for Advanced Packaging; Qibin Wang, Kai Xue, Xiangmeng Jing, Daquan Yu, and Dongkai Shangguan – National Center for Advanced Packaging; Chinese Academy of Sciences
24. ***Stretchable and Transparent Silicone/Zinc Oxide Nanocomposite for Advanced LED Packaging***
    Xueying Zhao, Liyi Li, and Zhuo Li – Georgia Institute of Technology; Ching-Ping Wong – Georgia Institute of Technology; Chinese University of Hong Kong
25. ***Warpage Characterization of Panel Fan-Out (P-FO) Package***
    Hung Wen Liu, Yi Wei Liu, Jason Ji, Jash Liao, Agassi Chen, Yan-Heng Chen, Nicholas Kao, and Yi-Che Lai – Siliconware Precision Industries Co., Ltd.

Wednesday, May 28
Session 38: Interactive Presentations 2
2:00 p.m. – 4:00 p.m.
Committee:
Interactive Presentations
Northern Hemisphere A-C

Session Co-Chairs:
Mark Eblen – Kyocera America, Inc.
Michael Mayer – University of Waterloo

1. ***A Novel Double Layer NCF for Highly Reliable Micro-Bump Interconnection***
   Ji-Won Shin, Yong-Won Choi, Young Soon Kim, and Kyoung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST); Un Byung Kang and Sun Kyung Seo – Samsung Electronics Company, Ltd.
2. ***CO_2-Laser Drilling of TGVs for Glass Interposer Applications***
   Lars Brusberg and Henning Schröder – Fraunhofer IZM; Marco Queisser, Marcel Neitz, and Klaus-Dieter Lang – Technical University Berlin
3. ***Effects of Pad Surface Finish on Interfacial Reliabilities of Cu-Pillar/Sn-Ag Bumps of 2.5D TSV-Interposer on PCB Applications***
   Youngsoon Kim – Samsung Electro-Mechanics Company, Ltd.; Ji-Won Shin, Young-Won Choi, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST)
4. ***Effect of Variation in the Reflow Profile on the Microstructure of Near Eutectic SnAgCu Alloys***
   Francis Mutuku and Eric J. Cotts – Binghamton University; Babak Arfaei – Binghamton University; Universal Instruments Corporation
5. ***Development of the Thin Film with High Thermal Conductivity for Power Devices***
   Hiroshi Takasugi, Shin Teraki, Tsuyoshi Kurokawa, and Issei Aoki – Namics Corporation
6. ***Development of Electroless Nickel-Iron Plating Process for Microelectronic Applications***
   Yu Luo, Sung K. Kang, Oblesh Jinka, Maurice Mason, Steven A. Cordes, and Lubomyr T. Romankiw – IBM Corporation
7. ***Novel Conductive Paste Using Hybrid Silver Sintering Technology for High Reliability Power Semiconductor Packaging***
   Howard (Hwa Il) Jin, Senthil Kanagavel, and Wai Foo Chin – Alpha Advanced Materials
8. ***Novel Low Temperature Curable Photo-Sensitive Insulator***
   Kenji Okamoto, Hikaru Mizuno, Tomohiko Sakurai, and Katsumi Inomata – JSR Corporation
9. ***3D and 2.5D Packaging Assembly with Highly Silica Filled One Step Chip Attach Materials for Both Thermal Compression Bonding and Mass Reflow Processes***
   Christopher Breach, Daniel Duffy, and David Eichstadt – Kester Inc.
10. ***Process Compatibility of Conventional and Low-Temperature Curable Organic Insulation Materials for 2.5D and 3D IC Packaging – A User's Perspective***
    Guilian Gao, Bong-Sub Lee, Andrew Cao, and Ellis Chau – Invensas Corporation
11. ***Optimization of CMP Process for TSV Reveal in Consideration of Critical Defect***
    D. H. Lee – Amkor Technology Korea, Inc.; Sungkyunkwan University; D. H. Kim, S. C. Han, J. H. Kim, J. S. Park, B. R. Jang, Y. S. Chung, S. M. Seo, and C. H. Lee – Amkor Technology Korea, Inc.; Y. S. Kim – Sungkyunkwan University
12. ***High Throughput Roller Type Nano-Pattern Transfer Technique on Both Rigid Flexible Substrates and Mold Deformation Analysis under Atmospheric Imprint Environment***
    Yinsheng Zhong and Matthew M. F. Yuen – Hong Kong University of Science & Technology
13. ***Capacitive Deionization of Water Coolant Using Hybrid Carbon Electrodes for High Power Electronic Applications***
    Ziyin Lin, Zhuo Li, and Kyoung-Sik Moon – Georgia Institute of Technology; Ching-Ping Wong – Georgia Institute of Technology; Chinese University of Hong Kong
14. ***A Microfluidic Chip Integrated with a Sono-Transducer Using Combined Resonance between Oscillations of Hemispherical Micro Glass Shell and Enclosed Microfluid***
    Jiafeng Xu and Jintang Shang – Southeast University; Ching-Ping Wong – Chinese University of Hong Kong
15. ***RF Energy Harvesting***
    Parvizso Aminov and Jai P. Agrawal – Purdue University
16. ***Localized Metal Plating on Aluminum Back Side PV Cells***
    M. Balucani – Sapienza University of Rome; Rise Technology; K. Kholostov – Sapienza University of Rome; L. Serenelli, M. Izzi, and M. Tucci – ENEA Casaccia Research Centre; D. Bernardi – 2BG
17. ***Wet Etching of Deep Trenches on Silicon with Three-Dimensional (3D) Controllability***
    Liyi Li – Georgia Institute of Technology; Ching-Ping Wong – Georgia Institute of Technology; Chinese University of Hong Kong
18. ***An Innovative Bumpless Stacking with Through Silicon Via for 3D Wafer-On-Wafer (WOW) Integration***
    S. C. Liao, E. H. Chen, C. C. Chen, S. C. Chen, J. C. Chen, P. C. Chang, Y. H. Chang, C. H. Lin, T. K. Ku, and M. J. Kao – Industrial Technology Research Institute (ITRI); Y. S. Kim, N. Maeda, S. Kodama, H. Kitada, K. Fujimoto, and T. Ohba – Tokyo Institute of Technology
19. ***3D Integration and Assembly of Wireless Sensor Nodes for "Green" Sensor Networks***
    Jian Lu, Hironao Okada, Toshihiro Itoh, and Ryutaro Maeda – National Institute of AIST; NMEMS Technology Research Organization; Takeshi Harada – NMEMS Technology Research Organization
20. ***New Demultiplexer Component for Optical Polymer Fiber Communication Systems***
    S. Höll, M. Haupt, and U. H. P. Fischer – Harz University of Applied Sciences
21. ***Nanofiller Based Spin-on Materials for Negligible Reflection of Silicon Photonic External Coupling***
    Yoichi Taira, Kuniaki Suaoke, and Hidetoshi Numata – IBM Corporation; Rie Matsumoto and Ryuma Mizusawa – Tokyo Ohka Kogyo Co., Ltd.
22. ***Effect of Patterned Substrate on Light Extraction Efficiency of Chip-on-Board Packaging LEDs***
    Huai Zheng, Zhili Zhao, Yiman Wang, Lang Li, Sheng Liu, and Xiaobing Luo – Huazhong University of Science & Technology

Thursday, May 29
Session 39: Interactive Presentations 3
9:00 a.m. – 11:00 a.m.
Committee:
Interactive Presentations
Northern Hemisphere A-C

Session Co-Chairs:
Patrick Thompson – Texas Instruments, Inc.
Rao Bonda – Amkor Technology

1. ***Transferrable Fine Pitch Probe Technology***
   Y. Liu, S. L. Wright, B. Dang, P. Andry, R. Polastre, and J. Knickerbocker – IBM Corporation
2. ***Improvement of the Crystallinity of Electroplated Copper Thin Films for Highly Reliable 3D Interconnections***
   Chuanhong Fan, Osamu Asai, Ryosuke Furuya, Ken Suzuki, and Hideo Miura – Tohoku University
3. ***Process, Assembly and Electromigration Characteristics of Glass Interposer for 3D Integration***
   C. H. Chien, C. K. Lee, C. T. Lin, Y. M. Lin, C. J. Zhan, H. H. Chang, C. K. Hsu, H. C. Fu, W. W. Shen, Y. W. Huang, C. T. Ko, and W. C. Lo – Industrial Technology Research Institute (ITRI); Y. J. Lu – Corning, Inc.
4. ***Improved PCB Via Pattern to Reduce Crosstalk at Package BGA Region for High Speed Serial Interface***
   Yujeong Shim and Dan Oh – Altera Corporation
5. ***A Wafer Level Through-Stack-Via Integration Process with One-Time Bottom-up Copper Filling***
   Yunhui Zhu, Xin Sun, Runiu Fang, Xiao Zhong, Yuan Bian, Yong Guan, Jing Chen, and Yufeng Jin – Peking University; Shenglin Ma – Xiamen University, Peking University; Min Miao – Peking University, Beijing Information Science and Technology University
6. ***Effect of Joint Shape Controlled by Thermocompression Bonding on the Reliability Performance of 60µm-Pitch Solder Micro Bump Interconnections***
   Y. W. Huang, C. J. Zhan, J. Y. Juang, Y. M. Lin, S. Y. Huang, S. M. Chen, C. W. Fan, R. S. Cheng, and J. H. Lau – Industrial Technology Research Institute (ITRI); S. H. Chao, W. L. Hsieh, and C. Chen – National Chiao Tung University
7. ***Development of Microbump Joints Fabrication Process Using Cone Shape Au Bumps for 3D LSI Chip Stacking***
   Fumito Imura, Naoya Watanabe, Shunsuke Nemoto, Wei Feng, Katsuya Kikuchi, Hiroshi Nakagawa, and Masahiro Aoyagi – National Institute of AIST
8. ***Effect of Polymer Liners in CNT Based Through Silicon Vias***
   Archana Kumari, M. K. Majumder, B. K. Kaushik, and S. K. Manhas – Indian Institute of Technology Roorkee
9. ***Investigation of Low-Temperature Deposition High-Uniformity Coverage Parylene-HT as a Dielectric Layer for 3D Interconnection***
   Bui Thanh Tung, Naoya Watanabe, Fumiki Kato, Katsuya Kikuchi, and Masahiro Aoyagi – National Institute of AIST; Xiaojin Cheng – National Institute of AIST; Loughborough University
10. ***Effect of Ag and Cu Content in Sn Based Pb-Free Solder on Electromigration***
    Minhua Lu, Charles Goldsmith, Thomas Wassick, Eric Perfecto, and Charles Arvin – IBM Corporation

Wednesday & Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 10-17 for location.

11. ***FBEOL No-Aluminum Pad Integration in Pb-Free C4 Products for Environmental, Cost and Reliability Benefits***
E. Misra, T. Daubenspeck, T. Wassick, K. Tunga, and D. Questad – IBM Corporation

12. ***Low Loss Transmission Lines on Flexible COP Substrate by Standard Lamination Process***
Chang-Ho Liou, Wen-Ching Ko, and Je-Ping Hu – Industrial Technology Research Institute (ITRI); Hsin-Chia Lu, Yi-Fan Lin, and Shih-Keng Chuang – National Taiwan University

13. ***Preparing 25Gbps Electrical I/O for Exascale Computing Systems***
Lei Shan, Young Kwark, Renato Rimolo-Donadio, Christian Baks, Michael Gaynes, and Timothy Chainer – IBM Corporation; Manabu Hoshino, Masakazu Hashimoto, Toshihiko Jimbo, Junji Kodemura, and Ikkei Matsuura – Zeon Corporation

14. ***Large Low-CTE Glass Package-to-PCB Interconnections with Solder Strain-Relief Using Polymer Collars***
Gary Menezes, Vanessa Smet, Venky Sundaram, Pulugurtha Markondeya Raj, and Rao Tummala – Georgia Institute of Technology; Makoto Kobayashi – Namics Corporation

15. ***The Study of Bare Die FCBGA Die Damage in Response to Applied Mechanical Stress during Heat Sink Assembly***
Heidi S. Y. Ho and Daijiao Wang – Broadcom Corporation; Michael Johnson and C. J. Berry – Amkor Technology, Inc.

16. ***Prognostication of Copper-Aluminum Wirebond Reliability under High Temperature Storage and Temperature-Humidity***
Pradeep Lall and Shantanu Deshpande – Auburn University; Luu Nguyen and Masood Murtuza – Texas Instruments

17. ***Low-Frequency Testing of Through Silicon Vias for Defect Diagnosis in Three-Dimensional Integration Circuit Stacking Technology***
Yichao Xu, Runiu Fang, Xin Sun, Yunhui Zhu, Guanjiang Wang, and Yufeng Jin – Peking University; Min Miao – Beijing Information Science & Technology University; Peking University; Minggang Sun – Beijing Information Science & Technology University

18. ***Fast Estimation of LED's Accelerated Lifetime by Online Test Method***
Qi Chen, Quan Chen, and Xiaobing Luo – Huazhong University of Science & Technology

19. ***Methodology and Apparatus for Rapid Power Cycle Accumulation and In-Situ Incipient Failure Monitoring for Power Electronic Modules***
Roy I. Davis and Daniel J. Sprenger – Fairchild Semiconductor Corporation

20. ***Fine-Pitch Probing on TSVs and Microbumps Using a Chip Prober Having a Transparent Membrane Probe Card***
Naoya Watanabe and Masahiro Aoyagi – National Institute of AIST; Michiyuki Eto and Kenji Kawano – STK Technology Co., Ltd.

Thursday, May 29
Session 40: Interactive Presentations 4
2:00 p.m. – 4:00 p.m.
Committee:
Interactive Presentations
Northern Hemisphere A-C

Session Co-Chairs:
Nam Pham – IBM Corporation
Rabindra N. Das – MIT Lincoln Labs

1. ***Thermal Management of 3D RF PoP Based on Ceramic Substrate***
Fengze Hou, Fengman Liu, Xia Zhang, Liqiang Cao, Yuan Lu, and Dongkai Shangguan – National Center for Advanced Packaging; Institute of Microelectronics, Chinese Academy of Sciences; Yi He and Xiaomeng Wu – Institute of Microelectronics, Chinese Academy of Sciences

2. ***Bump Pattern Optimization and Stress Comparison Study for DCA Packages***
Akash Agrawal, Owen Fay, and Mark Johnson – Micron Technology Inc.

3. ***Characterization of In-Plane Stress in TSV Array-A Unit Model Approach***
Cheng-Fu Chen – University of Alaska, Fairbanks

4. ***Electrical-Thermal Characterization of Wires in Packages***
Kai Liu, Robert Frye, HyunTai Kim, YongTaek Lee, Gwang Kim, Susan Park, and Billy Ahn – STATS ChipPAC, Inc.

5. ***Computational Investigation of Failure in Anodized Aluminum***
Sabrina Ball and Ibrahim Guven – The University of Arizona; Pankaj Sinha, Rajiv Rastogi, and Brian McCarson – Intel Corporation

6. ***Study on Prediction about Residual Position of Void Generated by Resin Flow***
Masayuki Mino and Tsutomu Kono – Hitachi, Ltd.; Naoya Suzuki and Hiroshi Takahashi – Hitachi Chemical Co., Ltd.

7. ***Modeling and Analysis of Temperature Effect on MEMS Gyroscope***
Ming Wen, Weihui Wang, and Zhang Luo – Huazhong University of Science & Technology; Yong Xu – Wuhan University; Wayne State University; Xin Wu – Wayne State University; Fei Hou – Dongfeng Automobile Electronics Co., Ltd.; Sheng Liu – Wuhan University

8. ***Life Prediction and Classification of Failure Modes in Solid State Luminaires Using Bayesian Probabilistic Models***
Pradeep Lall, Junchao Wei, and Peter Sakalaukus – Auburn University

9. ***Modeling for Reliability of Ultra Thin Chips in a System in Package***
Richard Qian and Yong Liu – Fairchild Semiconductor Corporation

10. ***Development of Effective Thermal Characterization on Handheld Devices by Matrix Method***
Tai-Yu Chen and Chung-Fa Lee – Media Tek Inc.

11. ***Comprehensive Design Optimization for 2.133 Gbps LPDDR3 Extension for Mobile Platform System***
Chanmin Jo, Jaemin Shin, Baekkyu Choi, Sangmin Lee, Seongjae Moon, Sungjoo Kim, and Woong Hwan Ryu – Samsung Electronics

12. ***Estimation of Mode Conversion and Crosstalk Impact from a Single-Ended Aggressor to a Differential Victim Using Statistical BER Analysis***
Arun Reddy Chada, Jun Fan, and James L. Drewniak – Missouri S&T EMC Laboratory; Bhyrav Mutnury – Dell, Inc.

13. ***Power Distribution Network Worst-Case Power Noise and an Efficient Estimation Method***
Jiangyuan Qian – Broadcom Corporation; Shiji Pan – University of California, Irvine

14. ***Fast Calculation of Electromagnetic Interference by Through-Silicon Vias***
Aosheng Rong and Andreas C. Cangellaris – University of Illinois, Urbana-Champaign; Feng Ling – Nanjing University of Science and Technology

15. ***Electrical Simulation and Analysis of Si Interposer for 3D IC Integration***
Xin Sun, Yunhui Zhu, Runiu Fang, Guanjiang Wang, Wengao Lu, Jing Chen, and Yufeng Jin – Peking University; Min Miao – Beijing Information Science & Technology University

16. ***A SPICE Model of Multi-Mode Optical Fiber in Mid-Channel Link for Package System SI Transient Simulations***
Zhaoqing Chen – IBM Corporation

17. ***Next Generation Package-on-Package Solution to Support Wide IO and High Bandwidth Interface***
Hung-Hsiang Cheng, Chang-Chi Lee, Ming-Feng Chung, Po-Chih Pan, Ping-Feng Yang, Chi-Tsung Chiu, Chih-Pin Hung, and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

18. ***Package-Level Electromagnetic Interference Analysis***
Namhoon Kim, Leo Hongyu Li, Sam Karikalan, Reza Sharifi, and Henry Kim – Broadcom Corporation

19. ***A Path Finding Based SI Design Methodology for 3D Integration***
Bill Martin – E-System Design; Kijin Han – UNIST; Madhavan Swaminathan – Georgia Institute of Technology

20. ***Design and Implementation of a 700-2600 MHz RF SiP for Micro Base Station***
Yi He, Fengman Liu, Anmou Liao, Jun Li, Peng Wu, and Liqiang Cao – National Center for Advanced Packaging; Institute of Microelectronics, Chinese Academy of Sciences; Xiaomeng Wu and Dongkai Shangguan – National Center for Advanced Packaging

21. ***Dielectric Lens Optimization for Conical Helix THz Antennas***
Paolo Nenzi – ENEA Frascati Research Center; Volha Varlamava, Frank Silvio Marzano, Fabrizio Palma, and Marco Balucani – Sapienza University of Rome

22. ***Embedded Diodes for Microwave and Millimeter Wave Circuits***
Xianbo Yang, Amanpreet Kaur, and Premjeet Chahal – Michigan State University

23. ***PCIe Gen3 Link Design and Tuning in Server Systems with End Devices from Multiple IP Suppliers***
Si T. Win, Daniel Rodriguez, and Nanju Na – IBM Corporation

24. ***A Low-Cost PCB Fabrication Process***
Jack Ou, Alberto Maldonado, Chio Saephan, and Farid Farahmand – Sonoma State University; Michael Caggiano – Rutgers University

25. ***Novel Band-Pass Filters on Thin Glass Substrate with Through Glass Vias (TGVs)***
Cheng Pang, Wenya Shang, Zheng Qin, Huijuan Wang, Daquan Yu, and Dongkai Shangguan – National Center for Advanced Packaging; Institute of Microelectronics, Chinese Academy of Sciences; Mingchuan Zhang and Jie Pan – Institute of Microelectronics, Chinese Academy of Sciences; Xiaoli Ren – National Center for Advanced Packaging

26. ***Study of Microwave Circuits Based on Metal-Insulator-Metal (MIM) Diodes on Flex Substrates***
Amanpreet Kaur, Xianbo Yang, and Premjeet Chahal – Michigan State University

Friday, May 30
Session 41: Student Interactive Presentations
8:30 a.m. – 10:30 a.m.
Committee:
Interactive Presentations
Southern Hemisphere Foyer

Session Co-Chairs:
Mark Poliks – i3 Electronics, Inc.
Ibrahim Guven – University of Arizona

1. ***Nanocomposite Pastes for Thermal and Mechanical Bonding***
Tingting Zhang, Bahgat Sammakia, and Howard Wang – Binghamton University

2. ***Assembly and Packaging Technologies for High-Temperature and High-Power GaN HEMTs***
A. A. Bajwa, Y. Qin, and J. Wilde – University of Freiburg; R. Reiner, P. Waltereit, and R. Quay – Fraunhofer Institute IAF

3. ***Flip-Chip on Glass (FCOG) Package for Low Warpage***
Scott R. McCann, Venkatesh Sundaram, Rao R. Tummala, and Suresh K. Sitaraman – Georgia Institute of Technology

4. ***Laser-Based Conductive Film Forming with Gold Nanoparticles for Electrical Contacts***
Mitsugu Yamaguchi, Kazuhiko Yamasaki, and Katsuhiro Maekawa – Ibaraki University; Shinji Araga – Ibaraki Giken Ltd.; Mamoru Mita – M&M Research Laboratory

5. ***Analysis of Modes Effect on Signal/Power Integrity in Finite Cavity for Chip and Die Level Packaging Based on a Hybrid Full Wave Method***
Xin Chang and Leung Tsang – University of Washington

6. ***Directed Self-Assembly of Mesoscopic Dies Using Magnetic Force and Shape Recognition***
Anton Tkachenko, Robert F. Karlicek, Jr., and James J.-Q. Lu – Rensselaer Polytechnic Institute

7. ***Controlled Silicon IC Thinning on Individual Die Level for Active Implant Integration Using a Purely Mechanical Process***
Vasiliki Giagka, Nooshin Saeidi, Andreas Demosthenous, and Nick Donaldson – University College London

8. ***Connectors and Vibrations: Damages in Different Electrical Environments***
A. Berghuvud, T. Björnängen, and T. Gissila – Blekinge Institute of Technology

9. ***Study of Extreme Low Temperature and Load Solid-Phase Sn-Ag System Bonding Mechanism for 3D ICs***
Kiyoto Yoneta, Ryohei Sato, Yoshiharu Iwata, Koichiro Atsumi, Kazuya Okamoto, Yukihiro Satio, and Takumi Shigemoto – Osaka University

10. ***Self-Patterning, Pre-Applied Underfilling Technology for Stack-Die Packaging***
Chia-Chi Tuan, Ziyin Lin, Yan Liu, and Kyoung-Sik Moon – Georgia Institute of Technology; Ching-Ping Wong – Georgia Institute of Technology; Chinese University of Hong Kong

11. ***Study of High CRI White Light-Emitting Diode Devices with Multi-Chromatic Phosphor***
Min Zheng, Wen Ding, Feng Yun, Deyang Xia, Yaping Huang, Yukun Zhao, Weihan Zhang, Minyan Zhang, Maofeng Guo, and Ye Zhang – Xi'an Jiaotong University

12. ***The Effects of Self-Fluxing Additives in Solder Anisotropic Conductive Films (ACFs) on Solder Wettability and Joint Reliability of Flex-on-Board (FOB) Assemblies***
Seung-Ho Kim, Yongwon Choi, Yoosun Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST)

13. ***Modeling and Analysis of Frequency Shift of MEMS Gyroscope Subjected to Temperature Change***
Weihui Wang, Zhang Luo, Ming Wen, Qiang Dan, and Man Yu – Huazhong University of Science & Technology; Sheng Liu – Wuhan University; Yong Xu – Wuhan University, Wayne State University; Xin Wu – Wayne State University

14. ***Interaction Effect between Electromigration and Microstructure Evolution in Cu/Sn-58Bi/Cu Solder Interconnect***
Hong-Bo Qin, Wu Yue, Chang-Bo Ke, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology; Bin Li – Southern Methodist University

15. ***Effects of Alignment of Graphene Flakes on Water Permeability of Graphene-Epoxy Composite Film***
Seong-Yoon Jung and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology (KAIST)

16. ***Characterization of Alternate Power Distribution Methods for 3D Integration***
David C. Zhang, Madhavan Swaminathan, David Keezer, and Satyanarayana Telikepalli – Georgia Institute of Technology

17. ***Adhesion and Reliability of Direct Cu Metallization of Through-Package Vias in Glass Interposers***
Timothy Huang, Venky Sundaram, P. Markondeya Raj, Himani Sharma, and Rao Tummala – Georgia Institute of Technology

18. ***High-Frequency Characterization of Through-Package Vias Formed by Focused Electrical Discharge in Thin Glass Interposers***
Jialing Tong, Andrew F. Peterson, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Yoichiro Sato, Shintaro Takahashi, and Nobuhiko Imajyo – Asahi Glass Company

19. ***Interfacial Reactions between Cu and Sn, Sn-Ag, Sn-Bi, Sn-Zn Solder under Space Confinement for 3D IC Micro Joint Applications***
T. L. Yang, W. L. Shih, J. J. Yu, and C. R. Kao – National Taiwan University

20. ***Simulation and Optimization of a Micro Flow Sensor***
Xing Guo, Chunlin Xu, and Shengzhi Zhang – Huazhong University of Science & Technology; Yong Xu and Xin Wu – Wayne State University; Sheng Liu – Wuhan University

21. ***Minimizing Coupling of Power Supply Noise between Digital and RF Circuit Blocks in Mixed Signal Systems***
Satyanarayana Telikepalli, Madhavan Swaminathan, and David Keezer – Georgia Institute of Technology

22. ***A Feasibility Study of Flip-Chip Packaged Gallium Nitride HEMTs on Organic Substrates for Wideband RF Amplifier Applications***
Spyridon Pavlidis, A. Cagri Ulusoy, Wasif T. Khan, Outmane Lemtiri Chlieh, and John Papapolymerou – Georgia Institute of Technology; Edward Gebara – I2R Nanowave Inc.

23. ***A Novel Molding Process for Wafer Level LED Packaging Using Uniform Micro Glass Bubble Arrays***
Yu Zou, Jintang Shang, and Yu Ji – Southeast University; Li Zhang, Chiming Lai, Dong Chen, and Kim-Hui Chen – Jiangyin Changdian Advanced Packaging Co. Ltd.; Ching-Ping Wong – Chinese University of Hong Kong

24. ***Analysis of Room-Temperature Bonded Compliant Bump with Ultrasonic Bonding***
Keiichiro Iwanabe, Takanori Shuto, and Tanemasa Asano – Kyushu University

2014 TECHNOLOGY CORNER EXHIBITS AND INTERACTIVE PRESENTATIONS

Technology Corner Exhibits

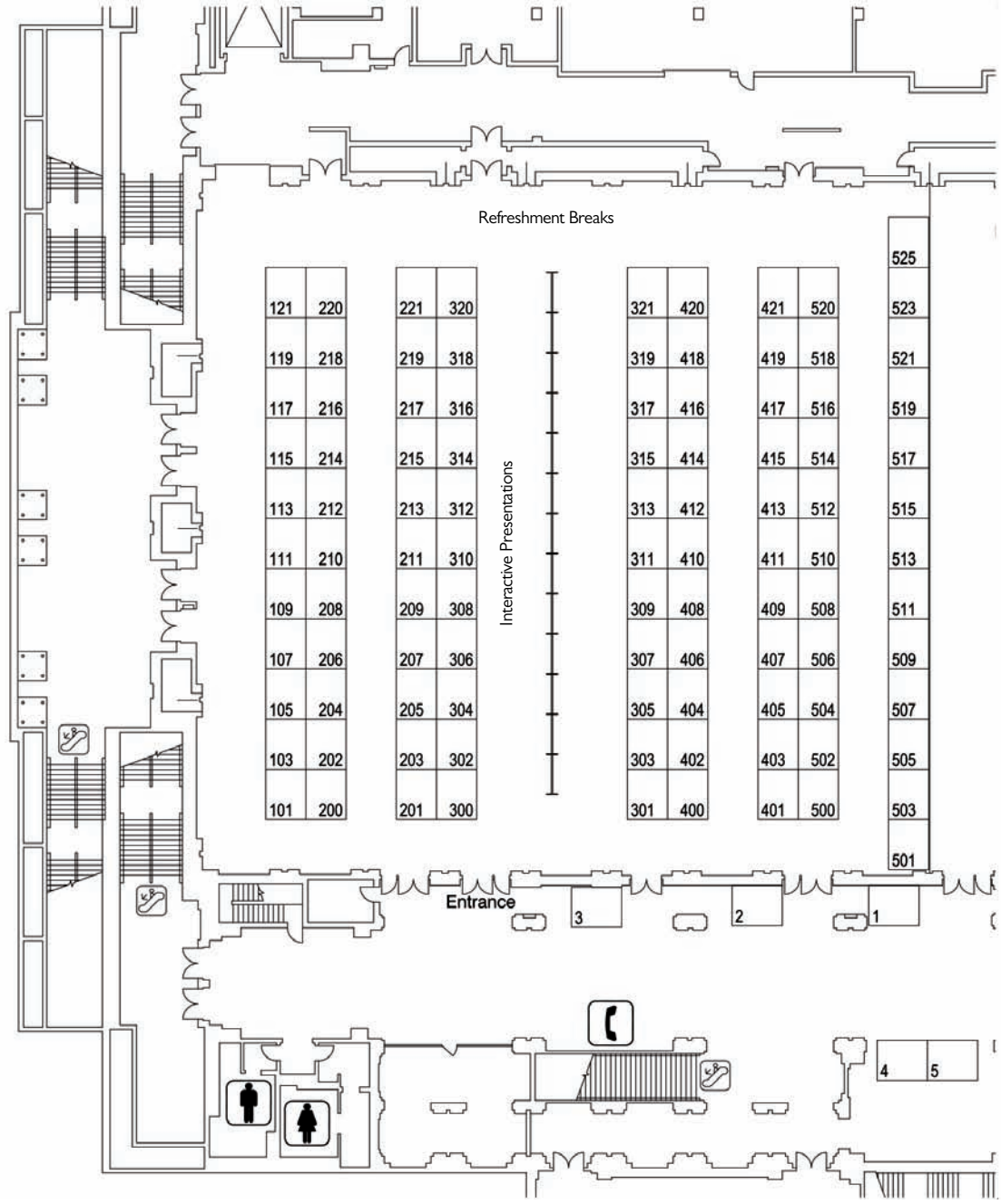
Wednesday, May 28: 9:00 a.m. - Noon & 1:30 p.m. - 6:30 p.m.
Thursday, May 29: 9:00 a.m. - Noon & 1:30 p.m. - 4:00 p.m.

Interactive Presentation Sessions

Wednesday, May 28
Session 37: 9:00 a.m. - 11:00 a.m.
Session 38: 2:00 p.m. - 4:00 p.m.

Thursday, May 29
Session 39: 9:00 a.m. - 11:00 a.m.
Session 40: 2:00 p.m. - 4:00 p.m.

Northern Hemisphere A-C, 5th floor



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65th ECTC Call for Papers

First Call For Papers

IEEE 65th Electronic Components and Technology Conference

www.ectc.net

To be held May 26 - May 29, 2015

at the Sheraton San Diego Hotel & Marina in San Diego, California, USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education, in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to, as given below under each technical program subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:
3D integration, embedded, and wafer level packaging, flip chip, advanced substrates, novel assembly technologies, interposers, TSVs, MEMS & sensors, electronic (digital, analog, & RF), and optoelectronic & photovoltaic device packaging.

Applied Reliability:
Package reliability, characterization and test methods, interconnection reliability; solder and material characterization, and next generation/novel packaging reliability.

Assembly and Manufacturing Technology:
Assembly challenges and solutions, manufacturing aspects of 3D/TSV, manufacturing challenges of wafer thinning and flip chip processing.

Electronic Components & RF:
Components (including embedded components) and modules for RF/THz systems and bio applications, metamaterials, wireless sensors, RFID, RF MEMS, flexible & printed electronics, "green" RF electronics, wireless power transmission, power scavenging components, nano-based RF structures, and low-power RF designs.

Emerging Technologies:
Emerging packaging concepts and technologies, novel approaches to packaging, organic IC & TFT, microfluidics and MEMS, anti-counterfeiting packaging, and packaging for biosensing.

Interconnections:
First- and second-level interconnections: designs, structures, processes, performance, reliability, test including TSV, Si interposer, and interconnections for 3D integration, flip chip, solder bumping and Cu-pillar, wafer-level packaging, advanced wirebonds, non-traditional interconnections (e.g. ECA, CNT, graphene, optical, etc.), electromigration for 2.5D and 3D, substrates and PCB solutions for the next generation systems, system packaging and heterogeneous integration.

Materials & Processing:
Adhesives and adhesion, lead free solder, novel materials and processing; underfills, mold compounds, and dielectrics, emerging materials and processing for 2D and 3D.

Modeling & Simulation:
Thermal, mechanical, electrical modeling and related measurements, 3D/TSV design and modeling, signal and power integrity, fracture and warpage in packages, material and fabrication modeling, first-level and second-level interconnects, high-speed interconnects.

Optoelectronics:
Fiber optical interconnects, active optical cables, parallel optical transceivers, silicon and III-V photonics devices, optical chip-scale and heterogeneous integration, micro-optical system integration and photonic system-in-package, optoelectronic assembly and reliability, materials and manufacturing technology, high-efficiency LEDs and high power lasers, and integrated optical sensors.

Interactive Presentations:
Papers may be submitted on any of the listed major topics; presentation of papers in an interactive format is highly encouraged at ECTC. Interactive presentations allow significant interaction between the presenter and attendees, and are especially suited for material that benefits from more explanation than is practical for oral presentations. Highly rated abstracts not fitting the theme of an oral session or submitted specifically for interactive presentation, and abstracts that are selected at the discretion of the program chair are included in the Interactive Presentation sessions.

You are invited to submit an abstract of no more than 750 words that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have any questions, contact:

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Abstracts must be received by October 13, 2014. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number, and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 13, 2014. If you have any questions, contact:

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65th Electronic Components & Technology Conference

Sheraton San Diego Hotel & Marina • San Diego, CA, USA • May 26 - 29, 2015

ECTC will be 65 years old next year and we will be celebrating in San Diego, CA! The Sheraton San Diego Hotel & Marina is a tried and true venue for ECTC as we have been using this property for quite some time! It touts panoramic views of the bay and the city skyline, yet is just 10 minutes from renowned attractions including the San Diego Zoo, Old Town, and Balboa Park.

Dubbed by many as "the only area in the US with perfect weather," San Diego is the oldest port on the West Coast and the sixth-largest city in the nation. Long known as a naval base, the military, along with tourism, still dominates the economy. In addition to rolling mountains, beautiful deserts, and seventy miles of coastline featuring some of the world's best beaches, San Diego offers a wealth of attractions. Art lovers can choose from many fine museums or catch a Shakespearean play at the Old Globe Theater. With more championship golf courses, over 85, than any other US city, you won't have a problem teeing off. The city also hosts the NFL's Chargers and Major League Baseball's Padres. And one last thing, don't forget to bring your passports as Tijuana, Mexico is only an hour away from sunny San Diego!

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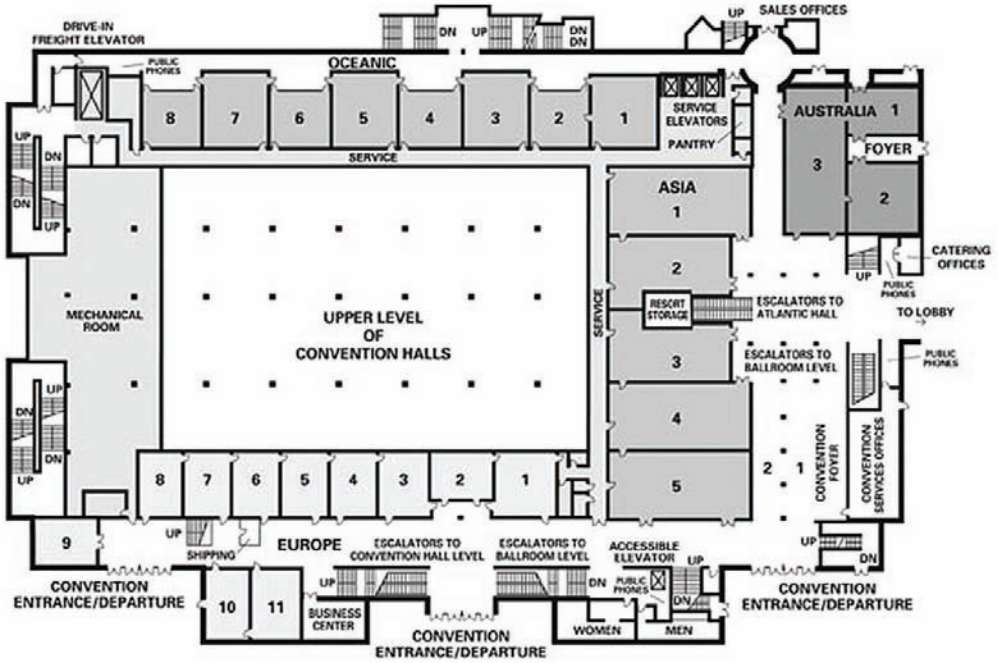

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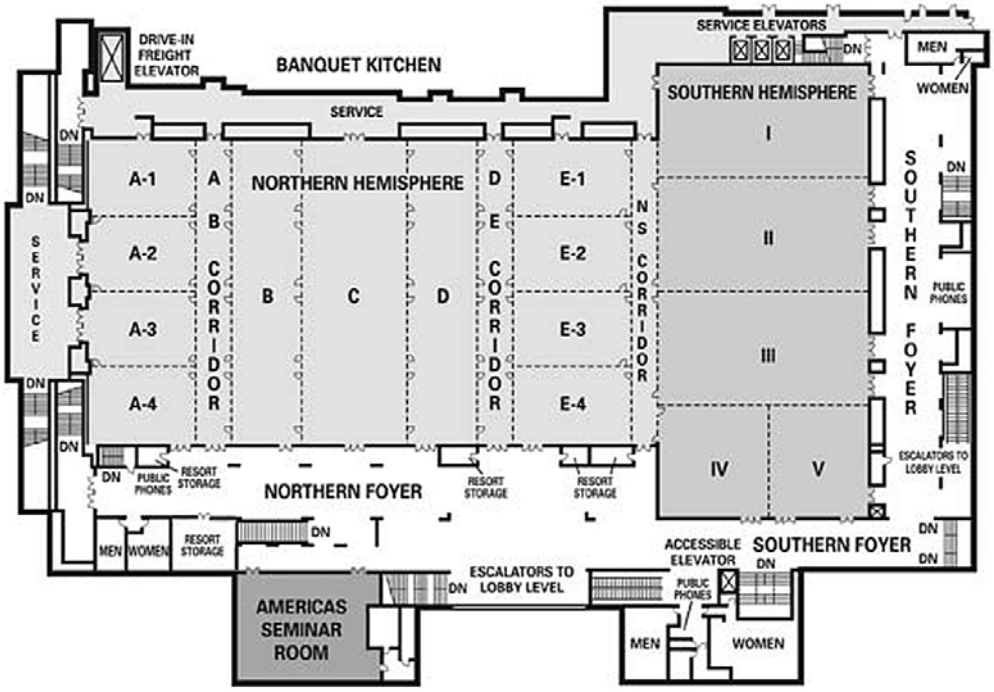

Conference At A Glance • The 3rd floor is lobby level.

Monday, May 26, 2014

3:00 p.m. – 5:00 p.m.
Registration – Australia 3 Foyer, 3rd floor

Tuesday, May 27, 2014

6:45 a.m. – 5:00 p.m.
Registration – Australia 3 Foyer, 3rd floor

6:45 a.m. – 8:45 a.m.
AM PD Courses Registration Only
11:00 a.m. – 1:15 p.m.
PM PD Course Registration Only

7:00 a.m. – 7:45 a.m.
PD Courses Instructors and Proctors Briefing & Breakfast
Asia 1, 3rd floor

7:00 a.m. – 5:00 p.m.
Speakers Prep
Europe 2, 3rd floor

8:00 a.m. – Noon
AM PD Courses
See page 8 for locations

8:00 a.m. – 5:00 p.m.
ITRS Assembly & Packaging Technology Committee Meeting
Europe 4, 3rd floor

8:00 a.m. – 5:00 p.m.
iNEMI Roadmap Meeting
Oceanic 3, 3rd floor

10:00 a.m. – Noon
Special Session
Northern Hemisphere D

10:00 a.m. – 10:20 a.m.
AM PD Course Break
Southern Hemisphere Foyer

Noon
PD Courses Luncheon
Southern Hemisphere I & II

1:00 p.m. – 5:00 p.m.
Technology Corner Set-up
Northern Hemisphere A - C

1:15 p.m. – 5:15 p.m.
PD PM Courses
See page 8 for locations

2:00 p.m. – 4:30 p.m.
Special Electronic Components & RF Session
Northern Hemisphere D

3:00 p.m. – 3:20 p.m.
PM PD Course Break
Southern Hemisphere Foyer

5:00 p.m. – 6:00 p.m.
ECTC Student Reception
Cabana Deck, outside
(rain backup: Asia 1)

6:00 p.m. – 7:00 p.m.
General Chair's Speakers Reception (by Invitation)
Crescent Terrace, outside on Swan Property
(Rain backup: Southern Hemisphere I)

7:30 p.m. – 9:30 p.m.
Panel Session
Southern Hemisphere III

Wednesday, May 28, 2014

6:45 a.m. – 4:00 p.m.
Conference Registration
Australia 3 Foyer, 3rd floor

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Northern Hemisphere E 3 & 4

7:00 a.m. – 5:00 p.m.
Speakers Prep
Europe 2

8:00 a.m. – 11:40 a.m.
Sessions 1, 2, 3, 4, 5, 6
See pages 10 thru 11 for Locations

9:00 a.m. – 11:00 a.m.
Session 37: Interactive Presentations 1
Northern Hemisphere A - C

9:00 a.m. – Noon
Technology Corner Exhibits
Northern Hemisphere A - C

9:15 a.m. – 10:00 a.m.
Refreshment Break
Northern Hemisphere A - C

9:30 a.m. – 12:30 a.m.
NEMI Roadmap Meeting
Oceanic 3, 3rd floor

Noon
ECTC Luncheon
Northern Hemisphere D - E

1:30 p.m. – 6:30 p.m.
Technology Corner Exhibits
Northern Hemisphere A - C

1:30 p.m. – 5:10 p.m.
Sessions 7, 8, 9, 10, 11, 12
See pages 12 thru 13 for Locations

2:00 p.m. – 4:00 p.m.
Session 38: Interactive Presentations 2
Northern Hemisphere A - C

2:45 p.m. – 3:30 p.m.
Refreshment Break
Northern Hemisphere A - C

5:30 p.m. – 6:30 p.m.
Technology Corner Reception
Northern Hemisphere A - C

7:00 p.m. – 9:00 p.m.
Plenary Session
Southern Hemisphere II & III

Thursday, May 29, 2014

7:00 a.m. – 5:00 p.m.
Speakers Prep
Europe 2

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Northern Hemisphere E 3 & 4

7:30 a.m. – 4:00 p.m.
Conference Registration
Australia 3 Foyer, 3rd floor

8:00 a.m. – 11:40 a.m.
Sessions 13, 14, 15, 16, 17, 18
See pages 14 thru 15 for Locations

9:00 a.m. – 11:00 a.m.
Session 39: Interactive Presentations 3
Northern Hemisphere A - C

9:00 a.m. – Noon
Technology Corner Exhibits
Northern Hemisphere A - C

9:15 a.m. – 10:00 a.m.
Refreshment Break
Northern Hemisphere A - C

Noon
CPMT Luncheon
Northern Hemisphere D - E

1:30 p.m. – 4:00 p.m.
Technology Corner Exhibits
Northern Hemisphere A - C

1:30 p.m. – 5:10 p.m.
Sessions 19, 20, 21, 22, 23, 24
See pages 16 thru 17 for Locations

2:00 p.m. – 4:00 p.m.
Session 40: Interactive Presentations 4

Northern Hemisphere A - C**2:45 p.m. – 3:30 p.m.**
Refreshment Break
Northern Hemisphere A - C

6:30 p.m. – 7:30 p.m.
Gala Reception
Lake Terrace, outside on Swan Property
(rain backup: Northern Hemisphere D – E)

8:00 p.m. – 10:00 p.m.
CPMT Seminar
Southern Hemisphere II & III

Friday, May 30, 2014

7:00 a.m. – 5:00 p.m.
Speakers Prep
Europe 2

7:00 a.m. – 7:45 a.m.
Today's Speaker's Breakfast
Northern Hemisphere E 3 & 4

7:30 a.m. – Noon
Conference Registration
Australia 3 Foyer

8:00 a.m. – 11:40 a.m.
Sessions 25, 26, 27, 28, 29, 30
See pages 18 thru 19 for Locations

8:30 a.m. – 10:30 a.m.
Student Poster Session
Southern Hemisphere Foyer

9:15 a.m. – 10:00 a.m.
Refreshment Break
Southern Hemisphere Foyer

Noon
Program Chair Luncheon
Northern Hemisphere D - E

1:30 p.m. – 5:10 p.m.
Sessions 31, 32, 33, 34, 35, 36
See pages 20 thru 21 for Locations

2:45 p.m. – 3:30 p.m.
Refreshment Break
Southern Hemisphere Foyer

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May 26-29, 2015

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