Conference Program
and Exhibitor Listings

Don't miss out on
electronic packaging's
premier conference!

ECTC 2016

The 66th Electronic Components and Technology Conference

May 31- June 3, 2016

The Cosmopolitan of Las Vegas • Las Vegas, Nevada

For more information,
visit: www.ectc.net

Sponsored by:

CPMT
IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

IEEE

WELCOME FROM THE MAYOR OF LAS VEGAS

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ECTC 2016

ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE

MAY 31- JUNE 3, 2016
LAS VEGAS, NEVADA

Dear Attendees,

Welcome to America's most dynamic City – Las Vegas! You could not have chosen a better City to hold your conference in, and I am convinced that once you get a taste of what Las Vegas has to offer, you will definitely be back. As the Mayor of this great City, I am delighted to tell you why Las Vegas is *the* place to live, work and play!

Las Vegas continues to capture the world's imagination as the City where anything is possible. With world-class hotels, award-winning restaurants, luxurious spas, fantastic shopping, the finest golf courses and spectacular entertainment, Las Vegas remains one of the most electrifying destinations in the world.

While attending the conference, is my hope that you will have a chance to explore Downtown Las Vegas, an area of our City that is undergoing a dramatic renaissance. It is evolving into a vibrant place for living, working, entertainment and the arts. Downtown Las Vegas is comprised of an enticing mix that includes:

- The neon-drenched excitement of the Fremont Street Experience, visited by over 21 million people each year.
- Multi-million dollar casino and hotel renovations and expansions.
- Fremont East Entertainment District featuring trendy new gathering places for dining, dancing, cocktails and enjoyment.
- An emerging eclectic mix of live-in artists and galleries known as the 18b Arts District.
- The World Market Center, a state-of-the-art home furnishings trade show complex with over 5 million square feet, has merged with another furniture complex in North Carolina and will now be called the International Market Center. The facilities in Las Vegas and North Carolina encompass 13 buildings, with 10.6 million square feet of furniture showrooms.
- Symphony Park, a phenomenal 61-acre planned development anchored by two key projects, the Cleveland Clinic Lou Ruvo Center for Brain Health, designed by renowned architect Frank Gehry, and The Smith Center for the Performing Arts, Las Vegas' first world-class performing arts facility. Symphony Park will also be the planned future home of The Charlie Palmer, a luxury boutique business hotel; a first-class casino/hotel with significant retail space; abundant street-side retail offerings; a two-acre park; and an estimated 1000 urban style residences.
- A collection of world-class museums including the Neon Museum Boneyard, which houses over 100 donated and rescued Las Vegas signs that date from the late 1930s through the early 1990s; The Mob Museum, which provides a fascinating glimpse into our City's history and Discovery Children's Museum in Symphony Park, among others.

Again, welcome to fabulous Las Vegas! Best wishes for an enjoyable stay in our fine City.

Sincerely,

Carolyn Goodman

Carolyn G. Goodman
Mayor, City of Las Vegas

WELCOME FROM ECTC GENERAL AND PROGRAM CHAIRS

On behalf of the Program Committee and Executive Committee, it is our pleasure to welcome you to the IEEE 66th Electronic Components and Technology Conference (ECTC), held at The Cosmopolitan of Las Vegas, Las Vegas, Nevada, USA, from May 31 – June 3, 2016. This premier international conference of the global microelectronic packaging industry is sponsored by the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society.

The ECTC Program Committee has selected 391 papers which will be presented in 36 oral sessions and five interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as flip chip packaging, 3D/TSV technologies, wafer level packaging, design for RF performance and signal/power integrity, thermal and mechanical modeling, optoelectronics packaging, materials, and reliability. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from 22 countries will be presenting their work at the 66th ECTC, covering ongoing technological challenges with established disciplines or emerging topics of interest for our industry such as the Internet of Things, wearables, etc.

ECTC will also feature panel and special sessions with industry experts covering a number of important and emerging topic areas. On Tuesday, May 31 at 10 a.m., Nanju Na will chair a session entitled "Memory Technology Advances and Prospects for Packaging" where a panel of experts will discuss how packaging is enabling the advances in memory technologies. On the same day at 2 p.m., Kannan Raj and Fuad Doany will chair a special session sponsored by the Optoelectronics Subcommittee on "Emerging Optical Interconnect Packaging for the Cloud". Tuesday evening will also have the ECTC Panel Session at 7:30 p.m., on "Power Module Integration", chaired by Patrick McCluskey and Yoshikazu Takahashi from the Energy Electronics Technical Committee of the CPMT Society.

Jordan P. Evans, Manager of the Mechanical Systems Division of NASA's Jet Propulsion Laboratory will be giving the invited keynote talk on "Dare Mighty Things: Landing a Car on Mars" at the ECTC Luncheon on Wednesday, June 1. On the same day at 6:30 p.m., we will have the CPMT Women's Panel and Reception chaired by Beth Keser, with participation from distinguished women leaders and technologists in our industry. This will be followed by the ECTC Plenary Session titled "Life after Moore's Law", chaired by Rozalia Beica at 7:30 p.m., where executives from leading research institutions across the globe will be presenting on their ground-breaking and game-changing research work to help our industry to stay on course with the performance and cost scaling curves. On Thursday, June 2 at 8 p.m. the CPMT Seminar titled "Systems, Devices, and Packaging Technologies for the IoT and Hyper-Connected Society" will be moderated by Venky Sundaram and Yasumitsu Orii from the High Density Substrates & Boards Technical Committee of the CPMT Society.

Supplementing the technical program, ECTC also offers several Professional Development Courses (PDCs) and the Technology Corner exhibits. Co-located with the IEEE iTHERM conference this year, the 66th ECTC will offer 18 PDCs, organized by the PDC Committee chaired by Kitty Pearsall. The PDCs will take place on Tuesday morning and afternoon and are taught by distinguished experts in their respective fields. The Technology Corner will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than 100 Technology Corner exhibits will be open starting at 9 a.m. on Wednesday and Thursday. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a scientist, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. We would like to take this opportunity to thank all our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, program committee members, as well as all the volunteers who have helped to make the 66th ECTC another resounding success. Once again, thank you for being a part of the 66th ECTC.

Alan Huffman
General Chair
RTI International

Sam Karikalan
Program Chair
Broadcom Limited

WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of CPMT, it is my great pleasure and privilege to welcome you to ECTC 2016 in vibrant Las Vegas at the spectacular Cosmopolitan Hotel!

The ECTC held its opening night 65 years ago and it hasn't missed a single year yet! Today, ECTC has become the premier international conference where professionals not only get a close-up look at every side of our industry, but also share research and development in technological breakthroughs across a wide range of semiconductor packaging, electronics devices, design, materials, manufacturing, and modeling.

The CPMT Society is proud to be a sponsor of ECTC and present these program highlights:

- Opening Day: Tuesday, May 31, in addition to the ever popular Professional Development Courses there will be two special sessions: Memory Technology Advances chaired by Dr. Nanju Na and Emerging Optical Interconnect Packaging for the Cloud chaired by Kannan Raj and Fuad Duany. Tuesday's program highlights the breadth and depth that ECTC delivers!
- To encourage diversity, networking, and professional development CPMT will host a Women's Panel "Maximize Your Career Potential" chaired by Beth Keser and CPMT will continue the women's **networking tables** during the Wednesday and Thursday luncheons.
- On Thursday, June 2nd, CPMT will sponsor an **award luncheon session** to present several prestigious IEEE and CPMT awards.
- After the traditional Gala reception Thursday CPMT will turn the **focus to IoT** hosting the seminar "Systems, Devices, and Packaging Technologies for the IoT and Hyper-Connected Society" chaired by Venkatesh Sundaram and Yasumitsu Orii.

Friday will be capped with a FO-WLP session showing the cutting edge advances in this disruptive technology.

Lastly I would like to take this opportunity to thank our dedicated volunteers on the ECTC program committee for their hard work over the past year. Also, appreciation goes to the session chairs, authors, speakers, and exhibitors who are instrumental to making the 66th ECTC a great success. As always I look forward to the impact all these technical and networking events will make on the CPMT Society, our industry, and our members.

Here's to four fast and furious days of in-depth analysis, peer debate, and network expansion!

Jean Trewhella, President, IEEE CPMT Society

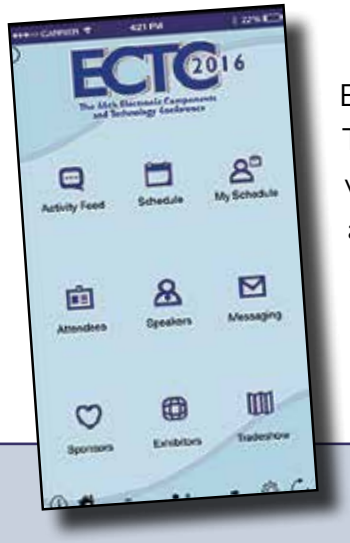
CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, meals, Technology Corner exhibits, and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. Hotel "house" phones have been placed throughout the hotel and conference area for your convenience. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
The hotel only allows smoking in designated smoking areas near and around the casino. Please follow hotel policies and signs regarding this. Smoking is NOT permitted, however, at any ECTC activities including, but not limited to, functions, events, sessions, and / or seminars. Thank you for your consideration and cooperation.



ECTC Mobile App

ECTC is pleased to announce that a **free mobile app** is available again this year. The app provides information on schedules for our technical program and PDCs as well as exhibitors, sponsors, and general conference information and venue maps. The app also features tools to set your schedule so you don't miss presentations important to you, social interaction functions, and the ability to provide ratings on presentations that are used in selecting candidates for best paper awards. The app is available for iOS and Android devices from their respective app stores by searching "2016 ECTC". Look for login and password information on signage at ECTC!

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Conference organizers reserve the right to cancel or change this program without prior notice.

ECTC Luncheon Keynote Speaker

Wednesday, June 1, 2016
12:00 Noon
Belmont 3& 4

Dare Mighty Things: Landing a Car on Mars

Presenter: Jordan P. Evans, Manager of the Mechanical Systems Division, Jet Propulsion Laboratory

How does a team tackle the task of sending a 2,000 pound rover on a 350 million mile journey and land it on three nylon ropes within a football field's length from its intended target? In this talk, Jordan Evans will share how the "crazy" idea of the skycrane landing came to be and some of the many challenges associated with sending a robotic geologist, like the Curiosity Rover, to another planet.

Jordan Evans manages the Mechanical Systems Division of NASA's Jet Propulsion Laboratory, responsible for leading 800 engineers and scientists in the development of advanced robotic systems for the exploration of our universe. For 7 years, in roles as both the Engineering Development and Operations Manager and Deputy Flight System Manager for the Mars Science Laboratory (MSL) "Curiosity" rover project, Mr. Evans led the MSL team through the challenges of design, assembly, testing, and ultimately through early operations on the surface of Mars.

Prior to and since landing, Jordan has shared those challenges with the national and international media and as a speaker at numerous conferences. Additionally, Mr. Evans serves as a science consultant for major motion pictures and television shows. An accomplished jazz musician, Mr. Evans regularly performs with big bands and small jazz ensembles in the Southern California area.

IEEE CPMT Heterogeneous Integration Technology Roadmap Workshop

Tuesday, May 31, 2016 • 8:00 a.m. - 5:00 p.m.
Condesa 2, 2nd Floor

Our Industry has reinvented itself through multiple disruptive changes in technologies, products and markets. We now face new challenges with the slowing of Moore's Law, the rapid migration of logic, memory and applications to the Cloud and the emerging Internet of Things (IoT). The pace of innovation is increasing to meet these challenges. What will be the winning directions going forward?

The CPMT Heterogeneous Integration Technology Roadmap, organized under the auspices of the IEEE CPMT Society, will follow directly the purpose, process and format of the ITRS Heterogeneous Integration Roadmap (activity ended as of Spring 2016) for the 15-year assessment of future requirements. This Heterogeneous Integration Roadmap workshop at the 2016 ECTC conference will continue the ITRS Heterogeneous Integration and Assembly and Packaging roadmapping workshops held in previous years at ECTC Conferences.

We invite all the ECTC participants to attend this important working session for our profession and for our industry.

iNEMI Technical & Research Committee Meetings

Tuesday, May 31 and Wednesday, June 1, 2016
9:00 a.m. - 5:00 p.m. • Castellana 1, 3rd Floor

By Invitation Only

REGISTRATION, RECEPTIONS AND GENERAL INFORMATION

Registration

ECTC registration will be open at the ECTC Registration Desk located in The Cosmopolitan of Las Vegas, 4th floor, Belmont Commons Area.

Monday, May 30, 2016 • 3:00 p.m. – 5:00 p.m.

Tuesday, May 31, 2016 • 6:45 a.m. – 8:15 a.m.*
(AM PD Courses & Special Session only)*

Tuesday, May 31, 2016 • 8:15 a.m. – 5:00 p.m.
(All conference attendees)

Wednesday, June 1, 2016 • 6:45 a.m. – 4:00 p.m.

Thursday, June 2, 2016 • 7:30 a.m. – 4:00 p.m.

Friday, June 3, 2016 • 7:30 a.m. – Noon

The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45 a.m. start time on Tuesday, May 31, as registration becomes very congested prior to the start of the morning Professional Development Courses.

Door Registration Fees

Door Registration with Proceedings on USB drive
IEEE Member JOINT Registration
(full ECTC + ITHERM conference) $1050
IEEE Member Full Registration $795
IEEE Member Speaker / Session Chair $695
IEEE Member One Day $525
IEEE Member Speaker One Day $395
Exhibit Booth Attendant $0
Non-Member JOINT Registration
(full ECTC + ITHERM conference) $1250
Non-Member Full Registration $975
Non-Member Speaker / Session Chair $695
Non-Member One Day $525
Non-Member Speaker One Day $395
Exhibit Booth Attendant $0

Student $300
Student Speaker $300

Exhibits Only $25

Tuesday Professional Development Courses
IEEE Members and Non-Members
Tuesday AM or PM Course with Luncheon $475
Tuesday All-Day Courses with Luncheon $675
Tuesday Student All-Day Courses with Luncheon $125

Extra Luncheon Tickets for Each Day $65
Extra Proceedings with Registration $100

Professional Development Course Instructors Breakfast

PDC Instructors and Proctors are required to attend a briefing breakfast.

7:00 a.m. Tuesday – PDC Instructors and Proctor Briefing
(Room Location: Belmont 3, 4th floor)

Session Chairs and Speakers Breakfast

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Microsoft Windows and Microsoft Office.

7:00 a.m. Wednesday thru Friday
(Room Location: Belmont 3, 4th floor)

Speaker Prep Room

Speakers should prepare and review their digital presentations within the allotted times below:

7:00 a.m. – 5:00 p.m., Tuesday – Friday
(Room Location: Yaletown 3, 4th floor)

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

MISCELLANEOUS INFORMATION

Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Message Center
Please use the hotel switchboard or the ECTC Registration Desk, located on the 4th floor in the Belmont Commons, to leave and pickup messages. The hotel phone number is +1 (702) 698-7000

Press Room
Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eric.perfecto@globalfoundries.com or (845) 475-1290.

LUNCHEONS

Tuesday, May 31, 2016
12 Noon
(Belmont 3, 4th floor)
The Electronic Components and Technology Conference will sponsor a luncheon for all Professional Development Courses attendees, proctors and PDC committee members.

Wednesday, June 1, 2016
12 Noon
(Belmont 3 & 4, 4th floor)
The Electronic Components and Technology Conference will sponsor a luncheon for conference attendees. Best and Outstanding Papers will be awarded. The guest speaker will be Jordan P. Evans, Manager of the Mechanical Systems Division, Jet Propulsion Laboratory.

Thursday, June 2, 2016
12 Noon
(Belmont 3 & 4, 4th floor)
The IEEE Components, Packaging and Manufacturing Technology Society will sponsor a luncheon for conference attendees. The CPMT awards will be presented.

Friday, June 3, 2016
12 Noon
(Belmont 3 & 4, 4th floor)
The ECTC Program Chair will sponsor a luncheon for conference attendees. You won't want to miss it!
There will be a raffle for attendees.

2016 ECTC SESSIONS & SEMINARS – Open to all conference attendees

2016 ECTC SPECIAL SESSION

Memory Technology Advances and Prospects for Packaging

Tuesday, May 31, 2016
10:00 a.m. – 11:30 a.m.
Condesa 3

Chair: Nanju Na – Xilinx, Inc.

Speakers:

1. Bryan Black – Advanced Micro Devices, Inc.
2. Sandeep Bharathi – Xilinx, Inc.
3. Nick Kim – SK Hynix, Inc.
4. Craig Hampel – Rambus, Inc.
5. Ravi Mahajan – Intel Corporation

2016 OPTOELECTRONICS SPECIAL SESSION

Emerging Optical Interconnect Packaging for the Cloud

Tuesday, May 31, 2016
2:00 p.m. - 3:30 p.m.
Condesa 3

Chairs: Kannan Raj – Oracle and Fuad Doany – IBM Corporation

Speakers:

1. Frank Flens – Finisar Corporation
2. Peter De Dobbeleare – Luxtera, Inc.
3. Wilfried Haensch – IBM Corporation
4. Ashok Krishnamoorthy – Oracle
5. Erin Byrne – TE Connectivity, Ltd.

2016 ECTC PANEL SESSION

Power Module Integration

Tuesday, May 31, 2016
7:30 p.m. – 9:00 p.m.
Mont Royal Ballroom

Chairs: Yoshikazu Takahashi – Fuji Electric Co. Ltd. and Patrick McCluskey – University of Maryland, College Park

Speakers:

1. Klaus-Dieter Lang, Fraunhofer IZM
2. Bernd Roemer - Infineon Technologies AG
3. Hiroshi Hozoji, Hitachi, Ltd.
4. Yoshiyuki Nagatomo, Mitsubishi Materials Corporation
5. Jared Hornberger, Wolfspeed
6. Avi Bar-Cohen - University of Maryland, College Park

2016 CPMT WOMEN'S PANEL AND RECEPTION

Maximize Your Career Potential

Wednesday, June 1, 2016
6:30 p.m. – 7:30 p.m.
Nolita 1

Chair: Beth Keser – Qualcomm Technologies, Inc.

Speakers:

1. Maryam Rofougaran – Seasoned Entrepreneur, Fmr. SVP of Engineering
2. Jan Vardaman – President, TechSearch International, Inc.
3. Rebeca Jimenez – Sr. Vice President, Amkor Technology, Inc.

2016 ECTC PLENARY SESSION

Life after Moore's Law

Wednesday, June 1, 2016
7:30 p.m. – 9:00 p.m.
Mont Royal Ballroom

Chair: Rozalia Beica – Dow Electronic Materials

Speakers:

1. Subramanian Iyer – University of California, Los Angeles
2. Luc Van den hove – IMEC
3. Dim Lee Kwong – IME, Singapore
4. Liqiang Cao – NCAP, China
5. Marie-Noelle Semeria – CEA-LETI

2016 CPMT SEMINAR

Systems, Devices, and Packaging Technologies for the IoT and Hyper-Connected Society

Thursday, June 2, 2016
8:00 p.m. – 9:30 p.m.
Mont Royal Ballroom

Chairs: Venkatesh Sundaram – Georgia Institute of Technology and Yasumitsu Orii – IBM Corporation

Speakers:

1. Mudasir Ahmad – Cisco Systems, Inc.
2. Kohji Hosokawa – IBM Corporation
3. Christian Hoffmann – TDK-Epcos
4. Eita Horiki – Sekisui America Corporation

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 31, 2016

Morning Courses 8:00 a.m. – Noon	Afternoon Courses 1:30 p.m. – 5:30 p.m.
Yaletown 4 **1. Achieving High Reliability of Lead-Free Solder Joints – Material Considerations** *Course Leader: Ning-Cheng Lee – Indium Corporation*	**Yaletown 4** **10. Flip Chip Fabrication and Interconnection** *Course Leaders: Eric Perfecto – GlobalFoundries; Shengmin Wen – Synaptics Inc.*
Nolita 3 **2. Wafer Level Chip Scale Packaging** *Course Leader: Luu Nguyen – Texas Instruments*	**Nolita 3** **11. Fan-Out Wafer Level Packaging** *Course Leader: Beth Keser – Qualcomm Technologies, Inc.*
Nolita 2 **3. LED Packaging, System, and Reliability Considerations** *Course Leader: Xuejun Fan – Lamar University*	**Nolita 2** **12. Operation, Design, Characteristics, and Key Parameters of Integrated Silicon Analog Components** *Course Leader: Badih El-Kareh – Consultant*
Nolita 1 **4. System Scaling for New Era of Self-Driving, Infotaining and Electric Cars** *Course Leaders: Rao Tummala, Vanessa Smet, and Venky Sundaram – Georgia Institute of Technology*	**Nolita 1** **13. Design and Analysis of High-Performance Memory Systems** *Course Leader: Wendem Beyene – Rambus*
Mont-Royal 1 **5. Polymers and Nano-Composites for Electronic and Photonic Packaging** *Course Leaders: C. P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation*	**Mont-Royal 1** **14. Polymers for Electronic Packaging** *Course Leader: Jeffrey Gotro – InnoCentrix, LLC*
Mont-Royal 2 **6. Integrated Thermal Packaging and Reliability of Power Electronics** *Course Leaders: Patrick McCluskey and Avram Bar-Cohen – University of Maryland*	**Mont-Royal 2** **15. Novel Interconnect and System Integration Technologies** *Course Leader: Muhannad Bakir – Georgia Institute of Technology*
Belmont 4 **7. Fundamentals of Electrical Design and Fabrication Processes of Interposers, Including Their RDLs** *Course Leaders: Ivan Ndip and Michael Töpper – Fraunhofer IZM*	**Belmont 4** **16. Package Failure Mechanisms, Reliability, and Solutions** *Course Leader: Darvin Edwards – Edwards Enterprises*
Belmont 8 **8. Introduction to Mechanics Based Quality and Reliability Assessment Methodology** *Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation*	**Belmont 8** **17. 3D IC Integration and 3D IC Packaging** *Course Leader: John Lau – ASM Pacific Technology Ltd.*
Condesa 4, 2nd Floor **9. Thermo-Electric Coolers: Characterization, Reliability, and Modeling** *Course Leader: Jaime Sanchez – Intel Corporation*	**Condesa 4, 2nd Floor** **18. Thermo-Electrical Co-Design of 3D Chip Stacks** *Course Leader: Ankur Srivastava and Avram Bar-Cohen – University of Maryland*

Refreshment Breaks – 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Mont-Royal Commons & Belmont Commons South

ECTC STUDENT RECEPTION
Tuesday, May 31, 2016
5:00 p.m. - 6:00 p.m.
Host: Texas Instruments, Inc.
Location: Condesa 5 & 6, 2nd Floor

ECTC welcomes our student attendees and student presenters who bring their research results to our audience. The Student Reception is an event where we provide guidance to students for their job search from industry leaders. In addition to the Student Reception, in the Student Interactive Presentation Session, we provide one-on-one access to students and their research to our audience. We encourage you to attend the Student Interactive Presentation Session on Friday. We also welcome Texas Instruments as the sponsor for these activities.

GENERAL CHAIR'S SPEAKERS RECEPTION
Tuesday, May 31, 2016
6:00 p.m. - 7:00 p.m.
Location: Blvd. Pool North, Center Bar (outside on 4th Floor)
(Backup Location: Belmont 3 & 7, 4th Floor)

Invited session chairs and speakers are requested to attend the reception.

TECHNOLOGY CORNER RECEPTION
Wednesday, June 1, 2016
5:30 p.m. - 6:30 p.m.
Location: Belmont 1 & 5, 4th Floor

An Exhibitor Sponsored Reception will be held in Belmont 1 & 5, 4th floor. All attendees and guests are invited.

66th ECTC GALA RECEPTION
Thursday, June 2, 2016
6:30 p.m.
Location: Belmont 3 & 4, 4th Floor

All badged attendees and guests are invited to attend our Gala Reception. This is a great way to meet your conference colleagues, speakers, exhibitors, guests, and the ECTC Executive Committee.

CONTINUING EDUCATION UNITS
The IEEE Components, Packaging, and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 66th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops. Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Course CEUs will be underwritten by the conference, i.e., there are no additional costs for Professional Development Course attendees to obtain CEU credit.

2015 ECTC BEST PAPER AWARDS

BEST OF CONFERENCE PAPERS – 2015

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 65th ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500 and the authors of the Best Interactive Presentation share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

Session 18, Paper 3

Automated, Self-Aligned Assembly of 12 Fibers per Nanophotonic Chip with Standard Microelectronics Assembly Tooling

Tymon Barwicz, Nicolas Boyer, Stephane Harel, Alexander Janta-Polczynski, Swetha Kamlapurkar, Sebastian Engelmann, Yurii A. Vlasov, and Paul Fortier – IBM Corporation; Ted W. Lichoulas and Eddie L. Kimbrell – AFL Telecommunications

Best Interactive Presentation

Session 38, Paper 20

Modeling, Design and Demonstration of Low-Temperature, Low-Pressure and High-Throughput Thermocompression Bonding of Copper Interconnections without Solders

Ninad Shahane, Scott McCann, Venky Sundaram, Pulugurtha Markondeya Raj, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Gustavo Ramos, Arnd Killian, and Robin Taylor – Atotech GmbH

OUTSTANDING PAPERS – 2015

The winning authors for Conference Outstanding Session Paper and Interactive Presentation receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

Session 6, Paper 6

Noise Coupling between TSVs and Active Devices: Planar nMOSFETs vs. nFinFETs

Xiao Sun, W. Guo, C. Roda Neve, I. De Wolf, G. Van der Plas, E. Beyne, and P. Absil – IMEC; A. Rouhu Najaf Abadi – Katholieke Universiteit Leuven; K. Ben Ali, M. Rack, and J. P. Raskin – Université Catholique de Louvain; M. Choi and V. Moroz – Synopsys, Inc.

Outstanding Interactive Presentation

Session 40, Paper 6

On the Failure Mechanism in Lead-Free Flip-Chip Interconnects Comprising ENIG Finish during Electromigration

Marek Gorywoda – Hochschule für Angewandte Wissenschaften Hof; Rainer Dohle, Andreas Wirth, Bernd Burger, and Jörg Goßler – Micro Systems Engineering GmbH

INTEL BEST STUDENT PAPER – 2015

The winning student receives a personalized plaque and a check for $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 65th ECTC:

Session 15, Paper 1

Size Effect on Ductile-to-Brittle Transition in Cu-Solder-Cu Micro-Joints

Yaodong Wang, Igor M. De Rosa, and K. N. Tu – University of California, Los Angeles

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 31, 2016

8:00 a.m. – 5:00 p.m.
CPMT Heterogeneous Integration Technology Roadmap Workshop
Condesa 2, 2nd Floor

9:00 a.m. – 5:00 p.m.
iNEMI Meeting
Castellana 1, 3rd Floor

5:00 p.m. – 6:00 p.m.
CPMT Industry Roundtable
Bellavista Boardroom, 2nd Floor

8:00 p.m. – 10:30 p.m.
ECTC Interconnections Sub-Committee
Jardins Boardroom, 2nd Floor

9:00 p.m. – 10:30 p.m.
ECTC Optoelectronics Sub-Committee
Bellavista Boardroom, 2nd Floor

Wednesday, June 1, 2016

7:00 a.m. – 8:00 a.m.
CPMT Materials & Processes TC
Jardins Boardroom, 2nd Floor

7:00 a.m. – 8:00 a.m.
CPMT Energy Electronics TC
Bellavista Boardroom, 2nd Floor

9:00 a.m. – 5:00 p.m.
iNEMI Meeting
Castellana 1, 3rd Floor

5:00 p.m. – 6:00 p.m.
CPMT Technical Committee Chairs
Bellavista Boardroom, 2nd Floor

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite
(by invitation only)

Thursday, June 2, 2016

7:00 a.m. – 8:00 a.m.
CPMT Region 8 Meeting
Praga, 3rd Floor

7:00 a.m. – 8:00 a.m.
CPMT Nanotechnology TC
Bellavista Boardroom, 2nd Floor

7:00 a.m. – 8:00 a.m.
CPMT High Density Substrates & Boards TC
Jardins Boardroom, 2nd Floor

7:00 a.m. – 8:00 a.m.
CPMT Photonics TC
Belmont 4, 4th Floor

4:30 p.m. – 6:00 p.m.
CPMT Officers and Directors Meeting
Bellavista Boardroom, 2nd Floor

5:30 p.m. – 6:30 p.m.
2017 Program Committee Meeting
Nolita 1, 4th Floor

5:30 p.m. – 6:30 p.m.
CPMT RF & THz Technology
Praga, 3rd Floor

8:00 p.m.
66th ECTC Governing/Executive Committee Reception
General Chair's Suite

Friday, June 3, 2016

7:00 a.m. – 8:00 a.m.
CPMT Thermal and Mechanical TC
Bellavista Boardroom, 2nd Floor

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee
Jardins Boardroom, 2nd Floor

4:45 p.m. – 5:45 p.m.
ECTC Steering Committee
Jardins Boardroom, 2nd Floor

Program Sessions: Wednesday, June 1, 8:00 a.m. - 11:40 a.m.

Session 1: Advances in Fan-Out Packaging	Session 2: TSV Fabrication, Characterization and Reliability	Session 3: Enhancement in Thermal Compression Bonding Processes
Committee: Advanced Packaging	**Committee: Interconnections**	**Committee: Assembly & Manufacturing Technology**
Room: Nolita 1	**Room: Nolita 2**	**Room: Nolita 3**
Session Co-Chairs: Young-Gon Kim – Integrated Device Technology, Inc. Beth Keser – Qualcomm Technologies, Inc.	**Session Co-Chairs: Katsuyuki Sakuma – IBM Corporation Chuan Seng Tan – Nanyang Technological University**	**Session Co-Chairs: Paul Houston – Engent Shichun Qu – Lumileds**
1. 8:00 AM - InFO (Wafer Level Integrated Fan-Out) Technology Chien-Fu Tseng, Chung-Shi Liu, Chi-Hsi Wu, and Douglas Yu – Taiwan Semiconductor Manufacturing Company	***1. 8:00 AM - Small Pitch High Aspect Ratio Via-Last TSV Module*** Stefaan Van Huylenbroeck, Michele Stucchi, Yunlong Li, John Slabbekoorn, Nina Tutunjyan, Stefano Sardo, Nicolas Jourdan, Lieve Bogaerts, Filip Beirnaert, Gerald Beyer, and Eric Beyne – IMEC	***1. 8:00 AM - Development of Next Generation Flip Chip Interconnection Technology Using Homogenized LASER Assisted Bonding*** YangGyoo Jung, DongSu Ryu, Minho Gim, ChoongHoe Kim, Byonglin Kim, JinYoung Kim, and JuHoon Yoon – Amkor Technology Korea, Inc.; ChoonHeung Lee – Amkor Technology, Inc.
2. 8:25 AM - Adaptive Patterning Design Methodologies Craig Bishop, Boyd Rogers, Chris Scanlan, and Tim Olson – Deca Technologies	***2. 8:25 AM - Impact of Interconnections on Vertically Stacked 20 µm-thick DRAM Chips*** Murugesan Mariappan, JiChel Bea, Hiroyuki Hashmoto, KangWook Lee, and Mitsumasa Koyanagi – GINTI; Seiya Tanikawa and Tetsu Tanaka – Tohoku University	***2. 8:25 AM - Photonic Flash Soldering on Flex Foils for Flexible Electronic Systems: From Thin Bare Die Chips to LED Packages*** Gari Arutinov and Jeroen van den Brand – Holst Centre; Rob Hendriks – NovaCentrix
3. 8:50 AM - Wafer Warpage Experiments and Simulation for Fan-Out Chip on Substrate Yuan-Ting Lin, Wei-Hong Lai, Jian-Wen Lou, Chin-Li Kao, Ping-Feng Yang, Chi-Yu Wang, and Chueh-An Hsieh – Advanced Semiconductor Engineering, Inc.	***3. 8:50 AM - Analysis and Remedy of the Discolor on Back-side Revealing TSV*** Ming-Hung Chen, Ting-Chun Lin, Yu-Hsiang Hsiao, Yuan-Feng Chiang, Po-Wei Lu, Zhe-Hao Huang, and PingFeng Yang – Advanced Semiconductor Engineering, Inc.	***3. 8:50 AM - Thermocompression Bonding Process Design and Optimization for Warpage Mitigation of Ultra-Thin Glass Package Assemblies*** Vidya Jayaram, Scott McCann, Ting-Chia Huang, Venky Sundaram, Raj Pulugurtha, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall – Belmont 1 & 5		
4. 10:00 AM - Foldable Fan-Out Wafer Level Packaging Tanja Braun, Karl-Friedrich Becker, Stefan Raatz, Mathias Minkus, V. Bader, J. Bauer, and Rolf Aschenbrenner – Fraunhofer IZM; Ruben Kahle, Leopold Georgi, Steve Voges, M. Wöhrmann, and Klaus-Dieter Lang – Technical University Berlin	***4. 10:00 AM - Electroless and Electrolytic Copper Plating of Glass Interposer Combined with Metal Oxide Adhesion Layer for Manufacturing 3D RF Devices*** Zhiming Liu, Hailuo Fu, Sara Hunegnaw, Jun Wang, Michael Merschky, and Tafadzwa Magaya – Atotech USA, Inc.; Akira Mieno - Atotech Japan K. K.; Hobie Yun – Qualcomm Technologies, Inc.; Satoru Kuramochi and Miyuki Akazawa – Dai Nippon Printing Co., Ltd.; Aric Shorey – Corning, Inc.	***4. 10:00 AM - High-Throughput Thermal Compression Bonding of 20um Pitch Cu Pillar for 3D IC Stacking*** Ling Xie, Sunil Wickramanayaka, Ser Choong Chong, Vasarla Nagendra Sekhar, and Daniel Ismael Cereno – Institute of Microelectronics, A*STAR
5. 10:25 AM - Panel Level Advanced Packaging Roger McCleary, Philippe Cochet, Tom Swarbrick, ChinTiong Sim, and Gurvinder Singh – Rudolph Technologies, Inc.; Yong Chang Bum and Andy KyawOo Aung - STATS ChipPAC	***5. 10:25 AM - High-Frequency Analysis of Embedded Microfluidic Cooling Within 3-D ICs Using a TSV Testbed*** Hanju Oh, Xucheng Zhang, Gary S. May, and Muhannad S. Bakir – Georgia Institute of Technology	***5. 10:25 AM - Chip Rework on Ceramic and Organic Modules*** Richard Langlois and Christian Bergeron – IBM Corporation
6. 10:50 AM - Development of Non-TSV Interposer (NTI) for High Electrical Performance Package Fang-Yu Liang, Hung-Hsien Chang, Wen-Tsung Tseng, J.Y. Lai, Stephen Cheng, Mike Ma - Siliconware Precision Industries Co., Ltd.; Suresh Ramalingam, Xin Wu, Jaspreet Gandhi - Xilinx Inc.	***6. 10:50 AM - Electrical Model of Different Architectures of Through Silicon Capacitors for High Frequency Power Distribution Network (PDN) Decoupling Operations*** Khadim Dieng, Cédric Bermond, Philippe Artillan, Thierry Lacrevaz, Gregory Houzet, and Bernard Fléchet – Université Savoie Mont Blanc; Olivier Guiller, Sylvain Joblot, and Alexis Farcy – STMicroelectronics; Yann Lamy – CEA-LETI	***6. 10:50 AM - Wafer Level Multi-Chip Gang Bonding Using TCNCF*** SeokGeun Ahn, HwanKyu Kim, Dave Hiner, MinJae Lee, DaeByoung Kang, KeunSoo Kim, TaeKyeong Hwang, and JuHoon Yoon – Amkor Technology, Inc.; DongWook Kim – Qualcomm Technologies, Inc.
7. 11:15 AM - Fan-Out Packaging of Microdevices Assembled Using Micro-Transfer-Printing Matthew Lueck, Alan Huffman, Paul Hines, and John Lannon – RTI International; Sal Bonafede, A. J. Trindade, and Chris Bower – X-Celeprint	***7. 11:15 AM - Gold TSVs (Through Silicon Vias) for High-Frequency III-V Semiconductor Applications*** Kevin Kröhnert, Veronika Glaw, Gunter Engelmann, Rafael Jordan, K. Samulewicz, and Karin Hauck – Fraunhofer IZM; Michael Robertson and Richard Cronin – CIP Ipswich; Oswin Ehrmann and Klaus-Dieter Lang – Technical University Berlin	***7. 11:15 AM - 3D Stacking Using Bump-Less Process for Sub-10um Pitches*** Jaber Derakhshandeh, Inge De Preter, Carine Gerets, Lin Hou, Nancy Heylen, Eric Beyne, Gerald Beyer, John Slabbekoorn, Vikas Dubey, Anne Jourdain, Goedele Potoms, Fumihiro Inoue, Geraldine Jamieson, Kevin Vandersmissen, Samuel Suhard, TomasWebers, Giovanni Capuz, Teng Wang, Kenneth June Rebibis, and Andy Miller – IMEC

Program Sessions: Wednesday, June 1, 8:00 a.m. - 11:40 a.m.

Session 4: Next Generation Substrates for Package Integration	Session 5: Novel Materials, Devices and 3D Interconnects	Session 6: Solder Joint Reliability Characterization and Modeling
Committee: Materials & Processing	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Room: Mont-Royal 1	**Room: Mont-Royal 2**	**Room: Yaletown 4**
Session Co-Chairs: **Yi Li – Intel Corporation** **Bing Dang – IBM Corporation**	**Session Co-Chairs:** **Karlheinz Bock – Technische Universität Dresden** **Vasudeva P. Atluri – Renavitas Technologies**	**Session Co-Chairs:** **Przemyslaw Gromala – Robert Bosch GmbH** **Sandeep Sane – Intel Corporation**
1. 8:00 AM - Large Panel Level Fan Out Package Built Up Study With Film Type Encapsulation Material Hiroshi Takahashi, Hirokazu Noma, Naoya Suzuki, Yutaka Nomura, Kasahara Aya, Nozomu Takano, and Toshihisa Nonaka – Hitachi Chemical Co., Ltd.	***1. 8:00 AM - Tunable Curvature of Large Visible CMOS Image Sensors: Towards New Optical Functions and System Miniaturization*** Bertrand Chambion, Stephane Getin, Gaid Moulin, Aurelie Vandeneynde, Liubov Nikitushkina, and David Henry – CEA-LETI; Emmanuel Hugot – University of Aix-Marseille	***1. 8:00 AM - Solder Joint Fatigue Life Prediction of Electronic Packages Using Combined FEA and Peridynamics*** Forrest Baber and Ibrahim Guven – Virginia Commonwealth University
2. 8:25 AM - Studying The Effect of Stackup Structure of Large Die Size Fan-in Wafer Level Package at 0.35 mm Pitch With Varying Ball Alloy to Enhance Board Level Reliability Performance Kuei Hsiao Kuo, Jerry Chiang, Kui Chang, Jack Hsu, F.L. Chien, Katch Wang, and Rick Lee – Siliconware Precision Industries Co., Ltd.	***2. 8:25 AM - Packaging Architecture for Fluidic Components in Microfluidic PCBs*** Sarkis Babikian, G. P. Li, and Mark Bachman – University of California, Irvine	***2. 8:25 AM - Life Prediction and RUL Assessment of Fine Pitch Solder Joint Fuze Electronics Under Mechanical Shock Loads up to 50,000g*** Pradeep Lall, Kalyan Dornala, and Jeff Suhling – Auburn University; Ryan Lowe – ARA Associates; Jason Foley – Air Force Research Labs
3. 8:50 AM - 2/2 µm Embedded Fine Line Technology for Organic Interposer Applications Dyi-Chung Hu, Wen-Liang Yeh, Yu-Hua Chen, and Ray Tain – Unimicron Technology Corp.	***3. 8:50 AM - Biopackaging of Intracranial Pressure Microsystem for Multimodality Neuro monitoring of Severe Head Injury Patients*** Ramona Damalerio, Kwan Ling Tan, Ruiqi Lim, Weiguo Chen, Yuan Gao, Ning Xue, and Ming-Yuan Cheng – Institute of Microelectronics, A-STAR; Jai Prashanth Rao – National Neuroscience Institute	***3. 8:50 AM - Solder Joint Reliability Investigation of Chip Scale Package With Plastic Core Solder Balls on Thermomechanically Loaded PCBs*** Fama Ghaffari Ashtiani, Allen Jose George, Thomas Heinrich, Simon Wolfangel, Shirangi Hossein, and Christian Klein – Robert Bosch GmbH
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall – Belmont 1 & 5		
4. 10:00 AM - Full-Sized Panel Photodesmear for Via Residue Cleaning Masahito Namai, Akira Aiba, Hiroko Suzuki, Hiroki Horibe, Hajime Kikuiri, Masaki Miura, Kazuki Arikawa, Noritaka Takezoe, Shinichi Endo, Shintaro Yabu, and Tomoyuki Habu – Ushio, Inc.	***4. 10:00 AM - Integration of Micro-Fabricated Scalar Atomic Magnetometer with the Combination of MX and MZ Techniques*** Qi Gan, Jintang Shang, Lei Wu, and Yu Ji – Key Lab of MEMS of Education Ministry, Southeast University	***4. 10:00 AM - Characterization of Thermal Cycling Ramp Rate and Dwell Time Effects on AF (Acceleration Factor) Estimation*** Kai-Chiang Wu, Chih-Hsuan Lee, and Kuo-Ning Chiang – National Tsing Hua University
5. 10:25 AM - A Novel Photosensitive Dry-Film Dielectric Material for High Density Package Substrate and Interposer Xiaozhu Wei and Yoko Shibasaki – Taiyo Ink Mfg. Co., Ltd.	***5. 10:25 AM - Highly-Effective Integrated EMI Shields with Graphene and Nanomagnetic Multilayered Composites*** Atom Watanabe, Junki Min, Markondeya Pulugurtha, and Rao Tummala – Georgia Institute of Technology; Seungtaek Jeong, Subin Kim, Youngwoo Kim, and Joungho Kim – KAIST; Denny Wong and Ravi Mullapudi – Tango Systems	***5. 10:25 AM - Board-Level Reliability Performance of Discrete Power Packages*** Yong Liu, Yumin Liu, Erwin Ian Almagro, OS Jeon, and Jerome Teysseyre – Fairchild Semiconductor Corporation
6. 10:50 AM - The Study on Parameters Affecting Depth-Wise Photo-Curing Process Based on Interaction Between Light and Metal Surface Giho Jeong, Choonhee Lee, Jinil Kang, Okseon Lee, and Anseop Shin – Samsung Electro-Mechanics Company, Ltd.	***6. 10:50 AM - Double-Densified Vertically-Aligned Carbon Nanotube Bundles for Application in 3D Integration High Aspect Ratio TSV Interconnects*** Wei Mu, Josef Hansson, Shuangxi Sun, Michael Edwards, Yifeng Fu, Kjell Jeppson, and Johan Liu – Chalmers University of Technology	***6. 10:50 AM - Phase Field Simulation of Segregation of Bi-Rich Phase in Sn-Bi/Cu Solder Interconnects Under Electric Current Stressing*** Shui-Bao Liang, Chang-Bo Ke, Wen-Jing Ma, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology
7. 11:15 AM - Demonstration of 20 µm I/O pitch RDL Using a Novel, Ultra-Thin Dry Film Photosensitive Dielectric for Panel-Based Glass Interposers Atsushi Kubo and Tomoyuki Ando – Tokyo Ohka Kogyo Co., Ltd.; Chandrasekharan Nair, Hao Lu, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Ryuta Furuya – Ushio, Inc.	***7. 11:15 AM - Metallic Nanoparticle Based Interconnect for Heterogeneous 3D Integration*** H. W. van Zeijl and Y. Carisey – Delft University of Technology / EKL; A. Damien – NXP Semiconductors; R. H. Poelma and C.Q. Zhang – Delft University of Technology / ECTM; A. A. Zinn – Lockheed Martin Corporation	***7. 11:15 AM - Finite Element Modeling of C4 Cracking in a Large Die Large Laminate Coreless Flip Chip Package*** Shidong Li, Tuhin Sinha, Thomas Wassick, Thomas Lombardi, Charles Reynolds, Brian Quinlan, and Sushumna Iruvanti – IBM Corporation

Program Sessions: Wednesday, June 1, 1:30 p.m. - 5:10 p.m.

Session 7: 2.5 & 3D Process and Integration Technologies	Session 8: Innovations in TSV Interconnect and Bonding Technologies	Session 9: Design and Analysis of Power Delivery Systems
Committee: **Advanced Packaging**	**Committee:** **Interconnections**	**Committee:** **High-Speed, Wireless & Components**
Room: Nolita 1	**Room: Nolita 2**	**Room: Nolita 3**
Session Co-Chairs: **Dean Malta – RTI International** **Luke England – GLOBALFOUNDRIES**	**Session Co-Chairs:** **Tom Gregorich – Micron Technology, Inc.** **William Chen – Advanced Semiconductor Engineering, Inc.**	**Session Co-Chairs:** **Kemal Aygun – Intel Corporation** **Zhaoqing Chen – IBM Corporation**
1. 1:30 PM - A Cost-Effective, CMP-Less Via-Last TSV Process for High Density, Fine RDL Applications King-Jien Chui, Woon Leng Loh, Chunmei Wang, Ka-Fai Chang, Qin Ren, Gilho Hwang, Hung-Ming Chua, Mingbin Yu – Institute of Microelectronics, A*STAR	***1. 1:30 PM - 2.5D Stacked Die Microbump Materials Characterization and IMC Evolution Under Reliability Stress*** Michael Su and Bryan Black – Advanced Micro Devices, Inc.; Yu-Hsiang Hsiao, Chien-Lin ChangChien, Chang-Chi Lee, and Hung-Jen Chang – Advanced Semiconductor Engineering, Inc.	***1. 1:30 PM - Power Delivery Design and Correlation of 14nm Multicore Server CPUs with Fully Integrated Voltage Regulators*** Krishna Bharath and Srikrishnan Venkataraman – Intel Corporation
2. 1:55 PM - End-to-End Integration of a Multi-Die Glass Interposer Brittany Hedrick, Vijay Sukumaran, Benjamin Fasano, Christopher Tessler, John Garant, Jorge Lubguban, Sarah Knickerbocker, Michael Cranmer, Koushik Ramachandran, Ian Melville, and Daniel Berger – GLOBALFOUNDRIES; Matthew Angyal, Richard Indyk, David Lewison, Charles Arvin, Luc Guerin, Maryse Cournoyer, Marc Phaneuf Luc Ouellet, Jean Audet, Franklin Baez, and Shidong Li – IBM Corporation	***2. 1:55 PM - Fluxless Thermo-Compression Bonding Process Using Micro-Scrub for 61µm-Pitch SnAg Solder 3-D Interconnections*** Katsuyuki Sakuma, Buck Webb, Xiao Hu Liu, John Knickerbocker, Thomas Weiss, Shidong Li, Hongqing Zhang, and Conor R. Thomas – IBM Corporation; Eric Perfecto – GLOBALFOUNDRIES; Tingge Xu and Hongbing Lu – University of Texas at Dallas	***2. 1:55 PM - Magnetic Materials and Design Trade-Offs for High Inductance Density, High-Q and Low-Cost Power and EMI Filter Inductors*** Teng Sun, Pulugurtha Markondeya, Minsuk Kim, Junki Min, Zihan Wu, Himani Sharma, and Rao Tummala – Georgia Institute of Technology; Tadashi Takahashi and Keiji Takemura – Nitto Denko Corporation; Hobie Yun – Qualcomm Corporation
3. 2:20 PM - Transfer and Non-Transfer 3D Stacking Technologies Based on Chip-to-Wafer Self-Assembly and Direct Bonding Takafumi Fukushima, Hideto Hashiguchi, Murugesan Mariappan, Jicheol Bea, Hiroyuki Hashimoto, Hisashi Kino, Tetsu Tanaka, Kangwook Lee, and Mitsumasa Koyanagi – Tohoku University	***3. 2:20 PM - The Development and Technological Comparison of Various Die Stacking and Integration Options with TSV Si Interposer*** Mike Ma, Stephen Chen, J. Y. Lai, Terrence Lu, Alex Chen, G. T. Lin, C. H. Lu, Cheng-Hsiang Liu, and Shih-Liang Peng – Siliconware Precision Industries Co., Ltd.	***3. 2:20 PM - Signal and Power Integrity Analysis on Integrated Fan-Out PoP (InFO_PoP) Technology for Next Generation Mobile Applications*** Chuei-Tang Wang and Douglas Yu – Taiwan Semiconductor Manufacturing Company, Ltd.
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall – Belmont 1 & 5		
4. 3:30 PM - Cost Comparison of Different TSV Implementation Options Dimitrios Velenis, Stefaan Van Hulenbroeck, Nancy Heylen, Kevin Vandersmissen, Anne Jourdain, Andy Miller, and Eric Beyne – IMEC	***4. 3:30 PM - All-Copper Flip Chip Interconnects by Pressureless and Low Temperature Nanoparticle Sintering*** Jonas Zürcher, Luca Del Carro, Gerd Schlottig, and Thomas Brunschwiler – IBM Corporation; Daniel Nilsen Wright, Astrid-Sofie Vardøy, and Maaike M. Visser Taklo – SINTEF ICT; Tobias Mills – Intrinsiq Materials Ltd.; Sridhar G. Kumar and Bernhard Wunderle –Technische Universität Chemnitz	***4. 3:30 PM - Analysis and Measurement of Power Integrity and Jitter Impacts on Thin-Core and Coreless Packages*** Yeon-Chang Hahm, Ming Li, John Yan, Yuri Tretiakov, and Hai Lan – Rambus, Inc.; Scott Chen and Simon Wang – Advanced Semiconductor Engineering, Inc.
5. 3:55 PM - Development of 3D Thin WLCSP Using Vertical Via Last TSV Technology with Various Temporary Bonding Materials and Low Temperature PECVD Process Zhiyi Xiao, Jun Fan, Jinqian Huo, Yulong Ren, Yang Li, Xiaohua Huang, and Daquan Yu – Huatian Technology (Kunshan) Electronics Co., Ltd.	***5. 3:55 PM - Novel W2W/C2W Hybrid Bonding Technology with High Stacking Yield Using Ultra-Fine, Ultra-High Density Cu Nano-Pillar (CNP) for Exascale 2.5D/3D Integration*** Kangwook Lee, Chisato Nagai, Jichel Bea, Takafumi Fukushima, Tetsu Tanaka, and Mitsumasa Koyanagi – Tohoku University; Suresh Ramalingam and Xin Wu – Xilinx, Inc.	***5. 3:55 PM - Measurement Based Method for Decomposing PDN Matrix*** Javid Mohamed, Varin Sriboonlue, Tim Michalka, and Larry Smith – Qualcomm Technologies, Inc.
6. 4:20 PM - Silicon Interposer Warpage Study for 2.5D IC Without TSV Utilizing Glass Carrier Properties Tuning Chieh-Lung Lai, Harry Li, Allen Chen, and Terren Lu – Siliconware Precision Industries Co., Ltd.	***6. 4:20 PM - Mechanical and Thermal Characterization of TSV Multi-Chip Stacked Packages for Reliable 3D IC Applications*** Ho-Young Son, Tackeun Oh, Joo-Whan Hong, Byeong-Do Lee, Ji-Huyk Shin, Sung-Ho Kim, and Nam-Seog Kim – SK Hynix	***6. 4:20 PM - Impact of Channel Loading to Power Distribution Network Designs*** Changwook Yoon and Dan Oh – Altera Corporation
7. 4:45 PM - Robust and Low Cost TSV Backside Reveal for 2.5D Multi-Die Integration Chongshen Song, Lei Wang, Yue Yang, Zhun Wang, Wenqi Zhang, and Liqiang Cao – National Center for Advanced Packaging	***7. 4:45 PM - Understanding the Behavior of SnAg Bumps at 10 Micron Pitch and Below for Imaging and Micro-Display Application*** Divya Taneja, Marion Volpert, Gilles Lasfargues, Thibault Catelain, and David Henry – CEA-LETI; Fiqiri Hodaj – University Grenoble Alpes	***7. 4:45 PM - Design and Analysis of Power Distribution Network (PDN) for High Bandwidth Memory (HBM) Interposer in 2.5D Terabyte/s Bandwidth Graphics Module*** Kyungjun Cho, Youngwoo Kim, Hyungsuk Lee, Heegon Kim, Sumin Choi, Subin Kim, and Joungho Kim – KAIST

Program Sessions: Wednesday, June 1, 1:30 p.m. - 5:10 p.m.

Session 10: Novel Interconnect Materials	Session 11: Optical Interconnects & 3D Photonics	Session 12: Electromigration, Warpage, and Material Characterization
Committee: Materials & Processing	**Committee: Optoelectronics**	**Committee: Thermal/Mechanical Simulation & Characterization**
Room: Mont-Royal 1	**Room: Mont-Royal 2**	**Room: Yaletown 4**
Session Co-Chairs: **Ivan Shubin – Oracle** **Dong Wook Kim – Qualcomm Technologies, Inc.**	**Session Co-Chairs:** **Hiren Thacker – Oracle** **Stephane Bernabe – CEA LETI**	**Session Co-Chairs:** **Pradeep Lall – Auburn University** **Gamal Refai-Ahmed – PreQual Technologies Corp.**
1. 1:30 PM - Novel Low Cost Bumping Process with Non-strip Type Photosensitive Resin and Injection Molded Solder (IMS) for Fine Pitch Flip Chip Joining Toyohiro Aoki, Takashi Hisada, Eiji Nakamura, Hiroyuki Mori, Yasumitsu Orii, and Yasuharu Yamada – IBM Corporation; Seiichirou Takahashi, Jun Mukawa, Chihiro Kobata, Kenzou Ohkita, and Kouichi Hasegawa – JSR Corporation	***1. 1:30 PM - Scalable Optical Coupling Between Silicon Photonics Waveguides and Polymer Waveguides*** Antonio La Porta, Roger Dangel, Daniel Jubin, Norbert Meier, Daniel Chelladurai, Folkert Horst, and Bert Jan Offrein – IBM Corporation	***1. 1:30 PM - The Nonlinearity of Stress Evolution in Polymer-Metal Composite Thin Films During Thermal Treatment*** Heng Li, Le Luo, and Gaowei Xu – Chinese Academy of Sciences
2. 1:55 PM - Design and Fabrication of Silver Solid Solution Layer on Silicon and Its Solid-State Bonding Applications Yi-Ling Chen, Yongjun Huo, and Chin C. Lee – University of California, Irvine	***2. 1:55 PM - Multi-layer Electro-Optical Circuit Board Fabrication on Large Panel*** Henning Schröder and Christopher Frey – Fraunhofer IZM; Marcel Neitz, Christian Herbst, and Klaus-Dieter Lang – Technical University of Berlin; Simon Whalley – ILFA Industrieelektronik und Leiterplattenfertigung GmbH	***2. 1:55 PM - Substrate Trace Modeling for Package Warpage Simulation*** Mingji Wang and Brendan Wells – Amkor Technology, Inc.
3. 2:20 PM - Die Attach Material Having Nano-Level Sn-Cu Diffusion Control for Power Semiconductor Devices Hiroaki Ikeda, Shigenobu Sekine, Ryuji Kimura, Koichi Shimokawa, Keiji Okada, Hiroaki Shindo, Tatsuya Ooi, and Rei Tamaki – Napra Co., Ltd.; Makoto Nagata – Kobe University	***3. 2:20 PM - Low-Loss Characteristics of a Multimode Polymer Optical Waveguide on an Electrical Hybrid LSI Package Substrate at 1.3 um Wavelength*** Takeru Amano, Akihiro Noriki, and Yoichi Sakakibara – AIST; Shigenari Ukita, Yoshiyuki Egashira, Mikiko Sasaki, and Kazuhiko Kurata – PETRA	***3. 2:20 PM - Wafer Warpage Characterization of Multi-Layer Structure Composed of Diverse Passivation Layers and Re-Distribution Layers for Cost-Effective 2.5D IC Packaging Alternatives*** Cheng-Hsiang Liu, Chen-Hong Chiu, Hsiao-Chun Huang, Lu-Yi Chen, Chang-Lun Lu, and Shih-Ching Chen – Siliconware Precision Industries Co., Ltd.
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall – Belmont 1 & 5		
4. 3:30 PM - Exploring Bismuth as a New Pb-Free Alternative for High Temperature Electronics Junghyun Cho, Sandeep Mallampati, and Russell Tobias – Binghamton University; Harry Schoeller – Universal Instruments Corporation; Liang Yin and David Shaddock – GE Global Research	***4. 3:30 PM - 3D Silicon Photonics Packaging Based on TSV Interposer for High Density On-Board Optics Module*** Yan Yang and Rusli – Nanyang Technological University; Mingbin Yu, Qing Fang, Junfeng Song, Xiaoguang Tu, and Guo-Qiang Lo – IME, A*STAR	***4. 3:30 PM - Measurement of the Comprehensive Viscoelastic Properties of an Advanced EMC Using a FBG Sensor*** Yong Sun, Hyun-Seop Lee, and Bongtae Han – University of Maryland, College Park
5. 3:55 PM - Porous Cu3Sn Formation in Cu-Sn IMC-Based Micro-Joints Yaodong Wang, David T. Chu, and King-Ning Tu – University of California, Los Angeles	***5. 3:55 PM - Graded-Index Multimode Polymer Optical Waveguide Enabling Low Loss and High Density 3D On-Board Integration*** Akira Yamauchi, Kyuta Suzuki, Yoshie Morimoto, Hikaru Masuda, and Takaaki Ishigure – Keio University	***5. 3:55 PM - Electromigration Induced Stress in Lead-Free Solder Joints*** Jiamin Ni and Antoinette Maniatty – Rensselaer Polytechnic Institute; Yong Liu, Jifa Hao, and Matt Ring – Fairchild Semiconductor Corporation
6. 4:20 PM - Solder Process for Fluxfree Solder Paste Applications Alexander Hanss and Gordon Elger – Technische Hochschule Ingolstadt; Matthias Hutter – Fraunhofer IZM; Jörg Trodler – Heraeus Deutschland GmbH & Co. KG	***6. 4:20 PM - Design and Demonstration of Micro-Mirror and Lens for Low-loss and Low-Cost Single-Mode Fiber Coupling in 3D Glass Photonic Interposers*** Bruce Chou, William Vis, Fuhan Liu, Venkatesh Sundaram, and Rao Tummala – Georgia Institute of Technology; Ryuta Furuya – Ushio, Inc.	***6. 4:20 PM - Peridynamic Direct Concentration Approach by Using ANSYS*** Sungwon Han, Y. Hwang, and H. Seol – Samsung Electronics Company, Ltd.; C. Diyaroglu, S. Oterkus, and E. Oterkus – University of Strathclyde, Glasgow; Erdogan Madenci – University of Arizona
7. 4:45 PM - Improved Joint Strength with Sintering Bonding Using Microscale Cu Particles by an Oxidation-Reduction Process Xiangdong Liu and Hiroshi Nishikawa – Osaka University	***7. 4:45 PM - Wet Etched Silicon Interposer for the 2.5D Stacking of CMOS and Optoelectronic Dies*** Chenhui Li, Barry Smalbrugge, Tjibbe de Vries, Teng Li, Patty Stabile, and Oded Raz – Eindhoven University of Technology	***7. 4:45 PM - Electromigration Induced Voiding and Resistance Change in Three-Dimensional Copper Through Silicon Vias*** Marco Rovitto and Hajdin Ceric – Technische Universität Wien

Program Sessions: Thursday, June 2, 8:00 a.m. - 11:40 a.m.

Session 13: Substrate Embedding & Advanced Flip-Chip Packaging	Session 14: Advancement on Wirebond Process & Reliability	Session 15: Advanced Assembly Technology Solutions
Committee: Advanced Packaging	**Committee: Interconnections**	**Committee: Assembly & Manufacturing Technology**
Room: Nolita 1	**Room: Nolita 2**	**Room: Nolita 3**
Session Co-Chairs: Steffen Kroehnert – Nanium S.A. Markus Leitgeb – AT&S	**Session Co-Chairs: Matthew Yao – GE Energy Management Gilles Poupon – CEA-LETI**	**Session Co-Chairs: Wei Koh – Pacrim Technology Paul Tiner – Texas Instruments**
1. 8:00 AM - Embedded Multi-Die Interconnect Bridge (EMIB) – A High Density, High Bandwidth Packaging Interconnect Ravi Mahajan, Robert Sankman, Neha Patel, Dae-Woo Kim, Kemal Aygun, Zhiguo Qian, Yidnekachew Mekonnen, Islam Salama, Sujit Sharan, Deepti Iyengar, and Debendra Mallik – Intel Corporation	***1. 8:00 AM - Copper Ball Voids for Pd-Cu Wires: Affecting Factors and Methods of Controlling*** Chuchung (Stephen) Lee, Tu Anh Tran, Varughese Mathew, Rusli Ibrahim, and Poh-Leng Eu – Freescale Semiconductor	***1. 8:00 AM - Two-Phase Flow Simulation of Molded Underfill Process to Mitigate Void and Assure Reliability at Product Level*** Kwang Won Choi, In Hak Baick, Eunmi Kwon, Sangwoo Pae, and Jongwoo Park – Samsung Electronics Company, Ltd.; Donghwan Lee and Eunjung Lee – Samsung SDI Company, Ltd.
2. 8:25 AM - Design of High Efficiency Integrated Voltage Regulators with Embedded Magnetic Core Inductors Sebastian Mueller, Khondker Zakir Ahmed, Arvind Singh, Saibal Mukhopadyay, and Madhavan Swaminathan – Georgia Institute of Technology; Yong Wang, Jennifer Wong, and Sandeep Bharathi – Xilinx, Inc.; Yasuhiko Mano – IBIDEN Co., Ltd.; Hesam Fathi Moghadam and Don Draper – Oracle	***2. 8:25 AM - Wire Bonding Looping Solutions for Advanced High Pin Count Devices*** Ivy Qin, Basil Milton, Gary Schulze, Cuong Huynh, Bob Chylak, and Nelson Wong – Kulicke and Soffa, Inc.	***2. 8:25 AM - Effect of High Tg Mold Compound on MEMS Sensor Package Performance*** Yeonsung Kim, Dipak Sengupta, Benoit Dufort, and Michael Zylinski – Analog Devices, Inc.; Dapeng Liu – Binghamton University
3. 8:50 AM - Fluxless Chip Join Process Using Formic Acid Atmosphere in a Continuous Mass Reflow Furnace Maud Samson, Valérie Oberson, Isabelle Paquin, Clément Fortin, Jean-Claude Raymond, and Charles Bureau – IBM Corporation; Michael Barnes, Xike Zhao, and David Wright – Heller Industries	***3. 8:50 AM - Reliable Manufacturing of Heavy Copper Wire Bonds Using Online Parameter Adaptation*** Tobias Meyer, Andreas Unger, and Walter Sextro – University of Paderborn; Michael Brökelmann – Hesse GmbH; Karsten Guth – Infineon Technologies	***3. 8:50 AM - BOP Substrate Design to Decrease the Overall Cost of FC Packaging*** Fletcher (Cheng Piao) Tung, Albert (Chang Yi) Lan, Max (Chin Yu) Lu, Wen Zhi Zhang, Angel Chen, and Roger Lo – Siliconware Precision Industries Co., Ltd.; Vincent (Wen-Hsien) Huang, Raymond (Kwok Cheung) Tsang, and Edward Law – Broadcom Limited
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall – Belmont 1 & 5		
4. 10:00 AM - Eternal Packages: Liquid Metal Flip Chip Devices Assane Ndieguene, Pierre Albert, and Julien Sylvestre – Université de Sherbrooke; Clément Fortin and Valérie Oberson – IBM Corporation	***4. 10:00 AM - Corrosion Behavior of Cu-Al Intermetallic Compounds in Copper Wire Bonding in Chloride-Containing Accelerated Humidity Testing*** Dong Liu and Edward Then – NXP Semicondutors Guangdong Ltd.; Haibin Chen and Jingshen Wu – Hong Kong University of Science & Technology; Fei Wong – NXP Semiconductors Hong Kong Ltd.	***4. 10:00 AM - Process Capability and Elastomer Stamp Lifetime in Micro Transfer Printing*** David Gomez, Kanchan Ghosal, Matthew Meitl, Salvatore Bonafede, Carl Prevatte, David Kneeburg, Brook Raymond, and Christopher Bower – X-Celeprint Inc.; Alin Fecioru and Antonio Trinidade – X-Celeprint Ltd.
5. 10:25 AM - Toward High-Yield 3D Self-Alignment of Flip-Chip Assemblies via Solder Surface Tension Yves Martin, Jae-Woong Nah, Swetha Kamlapurkar, Sebastian Engelmann, and Tymon Barwicz – IBM Corporation	***5. 10:25 AM - Principal Components Regression Model for Prediction of Acceleration Factor of Copper-Aluminum Wirebond Subjected to Harsh Environment.*** Pradeep Lall and Shantanu Deshpande – Auburn University; Luu Nguyen – Texas Instruments, Inc.	***5. 10:25 AM - Solving ILD Cracking with Copper Wire: A Silicon – Package Co-Design Approach*** Ernesto Rafael, Joel Raposas, and Mark Gerald Pinlac – Texas Instruments, Inc.
6. 10:50 AM - Ultra Fine Pitch / Low Cost FCCSP Package and Chip Package Interaction (CPI) for Advanced CMOS Nodes Yen-Liang Lin, Chung-Shi Liu, and Douglas Yu – Taiwan Semiconductor Manufacturing Company	***6. 10:50 AM - Solid-State Reactions of Silver and Aluminum Associated with Silver Wire Bonds*** Shao-Wei Fu and Chin Lee – University of California Irvine	***6. 10:50 AM - Dynamic Warpage Characterization and Reflow Soldering Defects for BGA Packages*** Kaiqiang Peng, Weihua Yang, Wei Xu, Linlin Lai, and Lei Feng – Huawei Technologies Co. Ltd.
7. 11:15 AM - Chip-to-Chip and Chip-to-Wafer Thermocompression Flip Chip Bonding Horst Clauberg, Alireza Rezvani, Vinod Venkatesan, Guy Frick, Bob Chylak, and Tom Strothmann – Kulicke and Soffa, Inc.	***7. 11:15 AM - The Electrical Reliability of Silver Wire Bonds Under High Temperature Storage*** Michael Mayer, Di Xu, and Kieran Ratcliffe – University of Waterloo	***7. 11:15 AM - In-Situ Measurement of Stress Development in ECA for Die-Attachment of Electronic Devices*** Eike Möller, Alexander Schiffmacher, Andi Wijaya, and Jürgen Wilde – University of Freiburg, IMTEK

Program Sessions: Thursday, June 2, 8:00 a.m. - 11:40 a.m.

Session 16: Performance Enhanced Adhesives, Underfills, and TIMs	Session 17: Advancements in Characterization and Reliability Methods	Session 18: Additive Fabrication Technologies for Packaging
Committee: Materials & Processing	**Committee:** Applied Reliability	**Committee:** Emerging Technologies
Room: Mont-Royal 1	**Room: Mont-Royal 2**	**Room: Yaletown 4**
Session Co-Chairs: Kwang-Lung Lin – National Cheng Kung University; Kimberly Yess – Brewer Science	**Session Co-Chairs:** Scott Savage – Medtronic Microelectronics Center; Babak Arfaei – Ford Motor Company	**Session Co-Chairs:** Florian Herrault – HRL Laboratories, LLC; Mark Bachman – University of California, Irvine
1. 8:00 AM - Heat Dissipation Enhancement of 2.5D Package with 3D Graphene & 3D Boron Nitride Networks as Thermal Interface Material (TIM) Manuela Loeblein and Edwin Teo – Nanyang Technological University; Siu Hon Tsang – Temasek Laboratories@NTU; Xiaowu Zhang and Yong Han – Institute of Microelectronics - A*Star	***1. 8:00 AM - Innovations in Fault Isolation Methods for 3D Packages with 10X Improvement in Accuracy*** Mayue Xie, Tom Begala, and Deepak Goyal – Intel Corporation; Kasemsak Kijkanjanapaiboon – Lamar University	***1. 8:00 AM - Conductive and Stretchable Silver-Polymer Blend for Emerging Electronic Applications*** Todd Houghton, Jignesh Vanjaria, and Hongbin Yu – Arizona State University
2. 8:25 AM - Inline Monitoring of Epoxy Molding Compound in Transfer Molding Process for Smart Power Modules Burcu Kaya and Jan-Martin Kaiser – Robert Bosch GmbH; Karl-Friedrich Becker and Tanja Braun – Fraunhofer IZM; Klaus-Dieter Lang – Technical University Berlin	***2. 8:25 AM - Global and Local Characterization of Passivated Aluminum Metallization Film for Extracting Elastoplastic Constitutive Model*** Hung-Yun Lin and Siva Gurrum – Texas Instruments, Inc.	***2. 8:25 AM - Fabrication of Terahertz Components Using 3D Printed Templates*** Jennifer Byford, Zachary Purtill, and Premjeet Chahal – Michigan State University
3. 8:50 AM - Development of High Thermal Conductive Adhesive Film for High Performance Power Modules Fumikazu Komatsu, Issei Aoki, Junya Sato, Hiroshi Takasugi, and Shin Teraki – NAMICS Corporation	***3. 8:50 AM - Crevice Corrosion of Ball Bond Intermetallics of Cu and Ag Wire*** Michiel van Soestbergen, Amar Mavinkurve, Jeroen Zaal, Mark Luke Farrugia, Rene Rongen, and Orla O'Halloran – NXP Semiconductors	***3. 8:50 AM - 3-D Inkjet Printed Ultra-Wideband Equi-Angular Spiral Antennas*** Xing Lan, Wesley Chan, Neal Yamamoto, and May Tan – Northrop Grumman; Maggie Yihong Chen and Jun Yu – Texas State University, San Marcos; Xuejun Lu – University of Massachusetts, Lowell
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall – Belmont 1 & 5		
4. 10:00 AM - Effect of Underfill Formulation on Large-Die, Flip-Chip Organic Package Reliability: A Systematic Study on Compositional and Assembly Process Variations Marie-Claude Paquet, Catherine Dufort, Thomas E. Lombardi, and Tuhin Sinha – IBM Corporation; Masahiro Hasegawa, Kodai Okoshi, and Kazuyuki Kohara - NAMICS Corporation	***4. 10:00 AM - In-Situ Warpage Characterization of BGA Packages with Solder Balls Attached During Reflow with 3D Digital Image Correlation (DIC)*** Yuling Niu, Huayan Wang, Shuai Shao, and S.B. Park – Binghamton University	***4. 10:00 AM - Novel High-Temperature, High-Power All-Cu Interconnections Through Low-Temperature Sintering of Nanocopper Foams*** Ninad Shahane, Kashyap Mohan, Antonia Antoniou, Pulugurtha Markondeya Raj, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology
5. 10:25 AM - Effects of Cooling Process and Silica Filler Content of Polymer Resin on Removing Solder ACF (Anisotropic Conductive Films) Joint Crack for Higher Reliability Shuye Zhang and Kyung-Wook Paik – KAIST	***5. 10:25 AM - Characterization of Moisture Induced Die Stresses in Flip Chip Packaging*** Quang Nguyen, Jordan Roberts, Jeffrey Suhling, Richard Jaeger, and Pradeep Lall – Auburn University	***5. 10:25 AM - Additively Manufactured Ceramic Substrate Technology for High-Temperature Electronics Through Selective Laser Melting*** Aarief Syed Khaja and Joerg Franke – Friedrich-Alexander University
6. 10:50 AM - Ceramic-Metal Composite Filler for Highly Thermally Conductive Underfill Chia-Chi Tuan, Gang Lian, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology	***6. 10:50 AM - Copper-Plated Through-Package-Via (TPV) Reliability in Glass Packages with In-Situ Stress Measurements using Raman Spectroscopy*** Kaya Demir, Venky Sundaram, P.Markondeya Raj, and Rao Tummala – Georgia Institute of Technology; Abdellah Benali – UIR	***6. 10:50 AM - Low Warpage Wafer Level Transfer Molding Post 3D Die-to-Wafer Assembly*** Francisco Cadacio Jr., Teng Wang, Abdellah Salahouelhadj, Giovanni Capuz, Goedele Potoms, Kenneth June Rebibis, Gerald Beyer, Andy Miller, and Eric Beyne – IMEC; Wilfred Gal, Jurrian Zijl, Sebastiaan Kersjes, and Henk Wensink – Besi
7. 11:15 AM - Development of Encapsulant Material for Molded Underfill for Fine Pitch Flip-Chip Packages Takayuki Tsuji, Takahiro Akashi, Naoki Watanabe, Kyoko Nishidono, and Masashi Nakamura – Panasonic Corporation	***7. 11:15 AM - Use of Digital Signal Characteristics for Solder Joint Failure Precursors*** Jinwoo Lee, Jeongah Yoon, and Daeil Kwon – UNIST	***7. 11:15 AM - Enabling Rapid Production and Mass Customization of Electronics Using Digitally Driven Hybrid Additive Manufacturing Techniques*** Thomas Wasley, Ji Li, and Robert Kay – Loughborough University; Duong Ta and Jonathan Shepard – Heriot-Watt University; Patrick Smith and Jonathan Stringer – University of Sheffield; Emre Esenturk and Colm Connaughton – University of Warwick

Program Sessions: Thursday, June 2, 1:30 p.m. - 5:10 p.m.

Session 19: MEMS & Sensor Technologies	Session 20: Flip-Chip: Bonding, Materials, and Reliability	Session 21: High-Speed Systems: Design & Analysis
Committee: Advanced Packaging	**Committee: Interconnections**	**Committee: High-Speed, Wireless & Components**
Room: Nolita 1	**Room: Nolita 2**	**Room: Nolita 3**
Session Co-Chairs: **Joseph W. Soucy – Draper Laboratory** **Daniel Baldwin – H.B. Fuller Company**	**Session Co-Chairs:** **Li Li – Cisco Systems, Inc.** **Lou Nicholls – Amkor Technology, Inc.**	**Session Co-Chairs:** **Xiaoxiong (Kevin) Gu – IBM Corporation** **Rockwell Hsu – Cisco Systems, Inc.**
1. 1:30 PM - Hermetic Wafer Level Thin Film Packaging for MEMS Bo Woon Soon and Navab Singh – Institute of Microelectronics - A*Star; Enes Calayir, Gianluca Piazza, and Gary K. Fedder – Carnegie Mellon University	***1. 1:30 PM - Study of Crystal Orientation and Microstructure in Sn-Bi and Sn-Ag-Cu Solder with Thermal Compression Bonding and Mass Reflow*** Kei Murayama, Mitsuhiro Aizawa, and Takashi Kurihara – Shinko Electric Industries Company, Ltd.	***1. 1:30 PM - A Feasibility Study on 100 Gbps/ Channel Die-to-Die Signal Transmission on Silicon Interposer-Based 2.5-D LSI with a Passive Digital Equalizer*** Ryuichi Oikawa – Renesas Electronics Corporation
2. 1:55 PM - Chip-Scale Integration of a SERF-Regime Optical Magnetometer Lei Wu, Jintang Shang, Qi Gan, and Yu Ji – Key Lab of MEMS of Education Ministry, Southeast University	***2. 1:55 PM - A Study on the Double Layer Non Conductive Films (NCFs) for Fine-Pitch Cu-Pillar/Sn-Ag Micro-Bump Interconnection*** SeYong Lee, Ji-Won Shin, Hyeong Gi Lee, Young Soon Kim, and Kyung-Wook Paik – KAIST	***2. 1:55 PM - Fast and Accurate Electrical Modeling of Large TSV Arrays in 3D-ICs Using a 3D Circuit Model Validated Against Full-Wave FEM Simulations and RF Measurements*** Martin Rack and Jean-Pierre Raskin – Université Catholique de Louvain; Xiao Sun, Geert Van der Plas, Philipe Absil, and Eric Beyne – IMEC
3. 2:20 PM - Reliable 300 mm Wafer Level Hybrid Bonding for 3D Stacked CMOS Image Sensors S. Lhostis, A. Farcy, E. Deloffre, F. Lorut, S. Mermoz, Y. Henrion, L. Berthier, F. Bailly, D. Scevola, F. Guyader, F. Gigon, C. Besset, S. Pellissier, L. Gay, N. Hotellier, and M. Arnoux – STMicroelectronics; A.-L. Le Berrigo, S. Moreau, V. Balan, F. Fournel, A. Jouve, and S. Chéramy – CEA, LETI, MINATEC Campus-Univ. Grenoble Alpes; B. Rebhan - EV Group; G. A.Maier and L. Chitu - Materials Center Leoben Forschung GmbH	***3. 2:20 PM - Use of Non-Conductive Film (NCF) with Nano-sized Filler Particles for Solder Interconnect: Investigations on Material and Process Characterization*** Tatsuo Nagamatsu – Dexerials America Corporation; Tomoyuki Ishimatsu, Hidekazu Yagi, Takayuki Saito, Daichi Mori, Keiji Honjo, and Katsuyuki Ebisawa – Dexerials Corporation	***3. 2:20 PM - Design and Demonstration of 2.5D Glass Interposers as a Superior Alternative to Silicon Interposers for 28 Gbps Signal Transmission*** Brett Sawyer, Bruce Chou, Jialing Tong, William Vis, Kadappan Panayappan, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Hugues Tournier – Ciena Corporation
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall – Belmont 1 & 5		
4. 3:30 PM - Demonstration of a Packaged Capacitive Pressure Sensor System Suitable for Wireless Jet Engine Health Monitoring Maximilian C. Scardelletti, Jennifer L. Jordan, Roger D. Meredith, Glenn M. Beheim, and Gary W. Hunter - NASA Glenn Research Center; Kevin Harsh, Evan Pilant, and Michael W. Ursey - Sporian Microsystems; Christian A Zorman - Case Western Reserve University	***4. 3:30 PM - A Room Temperature Flip-Chip Technology for High Pixel Count Micro-Displays and 4 Megapixel Imaging Arrays*** Francois Marion, Sylvette Bisotto, Frederic Berger, Alain Gueugnot, Lydie Mathieu, David Henry, Francois Templier, and Thibault Catelain – CEA LETI	***4. 3:30 PM - Investigation of Package Crosstalk and Impact to 28-32 Gbps Transceiver Jitter Margin*** Hong Shi, Siow Chek Tan, and Sarajuddin Niazi – Xilinx, Inc.
5. 3:55 PM - LiTaO3 Capping Technology for Wafer Level Chip Size Packaging of SAW Filters Kai Zoschke, Matthias Wegner, and Christina Lopper – Fraunhofer IZM; Matthias Klein, Richard Gruenwald, and Clemens Schoenbein – Vectron International GmbH; Klaus-Dieter Lang – Technical University of Berlin	***5. 3:55 PM - Thermal Compression Bonding of 30 Micron Pitch Cu Pillar Microbump*** K.Y. Au, Jong-Kai Lin, Jie Li Aw, F.X. Che, Hsiang-Yao Hsiao, Xiaowu Zhang, and Sharon Seow Huang Lim – Institute of Microelectronics, A*STAR; Alvin Chow – United Test And Assembly Center, Ltd.	***5. 3:55 PM - Improved Package Modeling and Correlation Methodology for High Speed I/O Design*** Cemil Geyik, Zhichao Zhang, and Kemal Aygün – Intel Corporation
6. 4:20 PM - Organic Chip-Scale Physics Packages for MEMS Atomic Clocks Jongchelp Park, Tae Hyun Kim, Chung-Mo Yang, and Hee Yeoun Kim – National NanoFab Center; Taeg Yong Kwon – Korea Research Institute of Standards and Science	***6. 4:20 PM - Improving Copper Pillar Interconnection on Embedded Trace Substrates*** Brendan Wells – Amkor Technology, Inc.	***6. 4:20 PM - Co-Design of a High Performance 12-bit 8GHz DDR4 Switch on a Laminate-Based CSP (Chip Scale Package) Technology*** Ming Li, Oscar Moreira-Tamayo, and Rajen Murugan – Texas Instruments, Inc.
7. 4:45 PM - Microfluidic Cooling for Distributed Hot-Spots Yudan Pi – Institute of Microelectronics, Peking University; Wei Wang, Jing Chen, and Yufeng Jin – National Key Laboratory of Science and Technology on Micro/Nano Fabrication	***7. 4:45 PM - Low Temperature Cu Nanorod and Sn-Cu Nanorod Bonding Technology for 3D Integration*** Li Du, Tielin Shi, Zirong Tang, Junjie Shen, and Guanglan Liao – Huazhong University of Science & Technology	***7. 4:45 PM - Behavioral Circuit Models of Data Clocked and Reference Clock Driven Retimers for Signal Integrity Transient Simulation*** Zhaoqing Chen – IBM Corporation

Program Sessions: Thursday, June 2, 1:30 p.m. - 5:10 p.m.

Session 22: Mechanical Modeling and Characterization of Interposer & Wirebonds	Session 23: Transceivers and Silicon Photonic Modules	Session 24: Reliability of Interconnects
Committee: Thermal/Mechanical Simulation & Characterization	**Committee: Optoelectronics**	**Committee: Applied Reliability**
Room: Mont-Royal 1	**Room: Mont-Royal 2**	**Room: Yaletown 4**
Session Co-Chairs: **Kuo-Ning Chiang – National Tsinghua University** **Jiantao Zheng – Qualcomm Technologies, Inc.**	**Session Co-Chairs:** **Ping Zhou – LDX Optronics, Inc.** **Alex Rosiewicz – A2E Partners**	**Session Co-Chairs:** **Tz-Cheng Chiu – National Cheng Kung University** **Darvin R. Edwards – Edwards Enterprises**
1. 1:30 PM - Effect of Silicone Gel on the Reliability of Heavy Aluminum Wire Bond for Power Module During Thermal Cycling Test Ling Xu, Miaocao Wang, and Yang Zhou – Huazhong University of Science & Technology; Sheng Liu and Zhengfang Qian – Wuhan University	***1. 1:30 PM - A Four-Channel Silicon Photonic Carrier With Flip-Chip Integrated Semiconductor Optical Amplifier (SOA) Array Providing >10-dB Gain*** Fuad E. Doany, Russell A. Budd, Laurent Schares, Tam N. Huynh, Michael G. Wood, Daniel M. Kuchta, Nicolas Dupuis, Clint L. Schow, and Benjamin G. Lee – IBM Corporation; M. Moehrle, A. Sigmund, and W. Rehbein – Fraunhofer HHI; T. Y. Liow, L. W. Luo, and G. Q. Lo - Institute of Microelectronics - A*STAR	***1. 1:30 PM - Effect of Environmental and Testing Condition on BL Vibration*** R. Roucou, J. J. M. Zaal, J. Jalink, R. Rongen, and R. de Heus – NXP Semiconductors
2. 1:55 PM - Cohesive Zone Parameters for a Cyclically Pre-Loaded Copper-Epoxy Interface David Samet, Abhishek Kwatra, and Suresh Sitaraman – Georgia Institute of Technology	***2. 1:55 PM - Hybrid III-V/SOI Optoelectronic Module*** I. Shubin, J. Yao, J.-H. Lee, S. S. Djordjevic, J. Bovington, C. Zhang, H. Thacker, S. Lin, D. Lee, Y. Luo, K. Raj, J. E. Cunningham, A. V. Krishnamoorthy, and X. Zheng – Oracle	***2. 1:55 PM - Impact of Lead Free Solder Joint Orientation on Multi-Terminal Passive Components during FCBGA Board Level Reliability*** Jaimal Williamson, Gregory Ostrowicki, Vikas Gupta, Siva Gurrum, and Andy Zhang – Texas Instruments, Inc.
3. 2:20 PM - Contact Pressure and Load Measurement Techniques for Applications in Semiconductor Packaging Sivakumar Yagnamurthy, Steven Klein, Nicholas Haehn, Seth Reynolds, Tannaz Harirchian, Chia-Pin Chiu, Haowen Liu, Shaw Fong Wong, Shankar Devasenathipathy, and Pramod Malatkar – Intel Corporation	***3. 2:20 PM - Compactly Packaged High-Speed Optical Transceiver Using Silicon Photonics ICs on Ceramic Submount*** Do-Won Kim, Andy Eu Jin Lim, Raja Muthusamy Kumarasamy, Vishal Vinayak Kulkarni, Leong Ching Wei, Jason Liow Tsung Yang, and Patrick Lo Guo Qiang – Institute of Microelectronics - A*STAR	***3. 2:20 PM - Cyclic Stress-Strain Behavior of SAC305 Lead Free Solder: Effects of Aging, Temperature, Strain Rate, and Plastic Strain Range*** Nianjun Fu, Jeffrey Suhling, and Pradeep Lall – Auburn University
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall – Belmont 1 & 5		
4. 3:30 PM - Multiphysics Life-Prediction Model Based on Measurements of Polarization Curves for Copper-Aluminum Intermetallics Pradeep Lall and Yihua Luo – Auburn University; Luu Nguyen – Texas Instruments, Inc.	***4. 3:30 PM - Packaging of Photonic Integrated Circuit Based High-Speed Coherent Transmitter Module*** Stéphane Bernabé, Benjamin Blampey, André Myko, and Benoît Charbonnier – CEA-LETI Univ. Grenoble Alpes; Alexandre Mottet, Jérôme Hauden, Steve Jillard – iXBlue; Karim Frigui, Samuel Ngoho, and Stéphane Bila – XLIM UMR 7252, University of Limoges/CNRS; Bouchra Frigui – CISTEME; Guanghua Duan and Xavier Pommarède – III-V Lab; Gabriel Charlet - Nokia Bell Labs	***4. 3:30 PM - The Mechanism of Dense Interfacial Voids and its Impact on Solder Joint Reliability*** Pilin Liu, Balu Pathangey, and Deepak Goyal – Intel Corporation
5. 3:55 PM - Simulation Methods for Crack Initiation and Propagation in Bulk Mold Material of Electro Mechanical Components Fabian Welschinger and Przemyslaw Jakub Gromala – Robert Bosch GmbH	***5. 3:55 PM - Polymer Waveguide-Coupled Solderable Optical Modules for High-Density Optical Interconnects*** Hideyuki Nasu, Naoya Nishimura, Yoshinobu Nekado, and Toshinori Uemura – Furukawa Electric Co., Ltd.	***5. 3:55 PM - Choice of Intermetallics for Structural Applications in Micro Joints of Three-Dimensional Integrated Circuits (3D ICs)*** Jen-Jui Yu, Jui-Yang Wu, Li-Jen Yu, and C. Robert Kao – National Taiwan University
6. 4:20 PM - Stress Concentration and Profile Under Thermal Cycling Test in Power Device Heat Dissipation Structures Using Double-Side Chip Bonding with Ag Sintered Layer on a Cu Plate Kensuke Osonoe, Masaaki Aoki, Takahiro Asai, and Nobuhiko Nakano – Keio University; Yoshio Murakami, Hitoshi Kida, and Goro Yoshinari – Alent Japan Company	***6. 4:20 PM - Wide Temperature Operation of 25.8 Gbit/s Uncooled DFB-LD TOSA with Extremely High Eye-Mask Margin*** Daisuke Noguchi, Hiroshi Yamamoto, Takayuki Nakajima, Noriko Sasada, Kazuhiko Naoe, Sachiko Mizuzeki, Norimichi Shibuya, and Masanobu Okayasu – Oclaro Japan, Inc.	***6. 4:20 PM - Reliability Assessment and Microstructure Characterization of the Cu Pillars Assembled on Si and Glass Substrates*** Babak Arfaei – Universal Instruments; Mohammed Genanu, Francis Mutuku, and Eric J. Cotts – Binghamton University; Scott Pollard and Aric Shorey - Corning, Incorporated; Eric Perfecto - GLOBALFOUNDRIES
7. 4:45 PM - Determination of Adhesion Strength of EMC/PSR Interface in Thin Packages Using Modified Offset Single Cantilever Adhesion Test Kenneth Mahan and Bongtae Han – University of Maryland	***7. 4:45 PM - Structure of 25-Gb/s Optical Engine for QSFP Enabling Passive Alignment of Optical Assembly*** Takatoshi Yagisawa, Tatsuhiro Mori, Rie Gappa, Kazuhiro Tanaka, Osamu Daikuhara, Takeshi Komiyama, and Satoshi Ide – Fujitsu Component Ltd.	***7. 4:45 PM - Cu Bump Flip Chip Package Reliability on 28nm Technology*** Pei-Haw Tsao, Steven Hsu, Y. L. Kuo, J. H. Chen, Abel Chang, H. P. Pu, L. H. Chu, and M. J. Lii – Taiwan Semiconductor Manufacturing Company

Program Sessions: Friday, June 3, 8:00 a.m. - 11:40 a.m.

Session 25: Wafer-Level CSP & Heterogeneous Integration	Session 26: Innovative Interconnects	Session 27: Advancement in 3D Handling & Packages
Committee: Advanced Packaging	**Committee:** Interconnections	**Committee:** Assembly & Manufacturing Technology
Room: Nolita 1	**Room: Nolita 2**	**Room: Nolita 3**
Session Co-Chairs: Jianwei Dong – Dow Electronic Materials; Omar Bchir – Qualcomm Technologies, Inc.	**Session Co-Chairs:** James E. Morris – Portland State University; Nathan Lower – Rockwell Collins, Inc.	**Session Co-Chairs:** Valerie Oberson – IBM Canada Ltee; Yang Liu – IBM TJ Watson Research Center
1. 8:00 AM - UFI (UBM-Free Integration) Fan-In WLCSP Technology Enables Large Die Fine Pitch Package Max (K.C.) Wu, Chung Shi Liu, and Douglas Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 8:00 AM - Low Cost, High Density Interposers in Aluminum Oxide Films*** Hsiang Yu Chan, Dogukan Yildirim, Guann Pyng Li, and Mark Bachman – University of California, Irvine; Chisa Fukuda – OM Sangyo Co., Ltd.	***1. 8:00 AM - Novel Dicing Technologies for WLCSP Using Stealth Dicing-Through-Dicing Tape and Back Side Protection-Film*** Shinya Takyu, Daisuke Yamamoto, Shigeyuki Yamashita, and Yusuke Fumita – Lintec Corporation; Kenji Furuta, Yohei Yamashita, and Kei Tanaka – Disco Corporation; Naoki Uchiyama, Takafumi Ogiwara, and Yuta Kondo – Hamamatsu Photonics K. K.
2. 8:25 AM - Implementation of Keep-Out-Zones to Protect Sensitive Sensor Areas During Back-End Processing in Wafer Level Packaging Technology André Cardoso, Raquel Pinto, Elisabete Fernandes, and Isabel Barros – NANIUM S.A.; Heikki Kuisma and Sami Nurmi – Murata Electronics Oy	***2. 8:25 AM - Micro-Scale Solder Joints between Cu-Cu Wires Formed by Nanoparticle Enabled Lead-free Solder Pastes*** Evan Wernicki, Edward Fratto, Yang Shu, Fan Gao, and Zhiyong Gu – University of Massachusetts Lowell	***2. 8:25 AM - Investigation of Advanced Dicing Technologies for Ultra Low-k and 3D Integration*** Arnita Podpod, Fumihiro Inoue, Kenneth Rebibis, Robert Andy Miller, Eric Beyne, and Ingrid De Wolf – IMEC
3. 8:50 AM - Challenges of Ultra-Thin 5 Sides Molded WLCSP Tom Tang, Albert Lan, Jason Wu, Joe Huang, Jensen Tsai, and Terry Yu – Siliconware Precision Industries Co., Ltd.; Arthur Ho, Jerry Chang, and W.H. Lin – NXP Semiconductors Taiwan Ltd.	***3. 8:50 AM - Pressure-Activated Electrical Interconnection during Micro-Transfer-Printing*** Carl Prevatte, Matthew Meitl, David Gomez, Kanchan Ghosal, Salvatore Bonafede, Brook Raymond, Tanya Moore, and Christopher A. Bower – X-Celeprint Inc.; António Jose Trindade - X-Celeprint Ltd.; Paul Hines – RTI International; Ibrahim Guven – Virginia Commonwealth University	***3. 8:50 AM - Improvement of a TSV Reveal Process Comprising Direct Si/Cu Grinding and Residual Metal Removal*** Naoya Watanabe and Masahiro Aoyagi – Advanced Industrial Science and Technology; Tsubasa Bandoh, Takahiko Mitsui, and Eiichi Yamamoto – Okamoto Machine Tool Works, Ltd.
Refreshment Break: 9:15 a.m. - 10:00 a.m. Mont-Royal Commons		
4. 10:00 AM - Stacking of Insulating Substrates and a Field Plate to Increase the PDIV for High Voltage Power Modules Christoph Friedrich Bayer, Uwe Waltrich, Amal Soueidan, Eberhard Baer, and Andreas Schletz – Fraunhofer IISB	***4. 10:00 AM - Novel Growth of Whole Preferred Orientation Intermetallic Compound Interconnects for 3D IC Packaging*** M.L. Huang, Z.J. Zhang, F. Yang, and N. Zhao – Dalian University of Technology	***4. 10:00 AM - No Pumping at 450C with Electrodeposited Copper*** Kazuo Kondo – Osaka Prefecture University
5. 10:25 AM - Ultra-Fine Pitch 3D Integration Using Face-to-Face Hybrid Wafer Bonding Combined with a Via-Middle Through-Silicon-Via Process Soon-Wook Kim, Mikael Detalle, Lan Peng, Philip Nolmans, Nancy Heylen, Dimitrios Velenis, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC	***5. 10:25 AM - Ultrasonic-Assisted Soldering of Sn-Based Solder Alloys to form Intermetallic Interconnects for High Temperature Application*** Hongjun Ji, Mingyu Li, and Yunfei Qiao – Harbin Institute of Technology Shenzhen Graduate School	***5. 10:25 AM - Integration and Packaging of Embedded Radial Micro-Channels for 3D-Chip Cooling*** Bing Dang, Evan Colgan, Fanghao Yang, Mark Schultz, Yang Liu, Qianwen Chen, Jae-Woong Nah, Robert Polastre, Michael Gaynes, Gerard McVicker, Pritish Parida, Cornelia Tsang, John Knickerbocker, and Timothy Chainer – IBM Corporation
6. 10:50 AM - Heterogeneous Integration of Microscale Gallium Nitride Transistors by Micro-Transfer-Printing Ralf Lerner and Stefan Eisenbrandt – X-FAB; Christopher A. Bower, Matthew A. Meitl, and Salvatore Bonafede – X-Celeprint Inc.; Alin Fecioru and António Jose Trindade - X-Celeprint Ltd.; Richard Reiner and Patrick Waltereit – Fraunhofer Institute for Applied Solid State Physics	***6. 10:50 AM - Characterization and Optimization of Sn-Cu TLPS Interconnects for High Temperature Power Electronics Through In-Situ X-Ray Investigations*** Aarief Syed Khaja and Joerg Franke – Friedrich-Alexander-University Erlangen-Nuremberg, FAPS; Alexander Klemm and Thomas Zerna – Technische Universitat Dresden	***6. 10:50 AM - Hemispherical Glass Shell Resonators with Integrated Silicon-in-Glass Electrodes for Electrostatic Transduction*** Bin Luo, Ming-ai Zhang, Chenyue Lu and Jintang Shang – Southeast University
7. 11:15 AM - Miniaturized Double Side Cooling Packaging for High Power Three Phase SiC Inverter Module with Junction Temperature over 220C Daniel Rhee Min Woo, Hwang How Yuan, Jerry Aw Jie Li, Lee Jong Bum, and Zhang Hengyun – Institute of Microelectronics, A*STAR	***7. 11:15 AM - Design of Mechanical Properties of Transient Liquid Phase Bonds with Tertiary Metal Particles*** Masao Noguchi – Toyota Motor Corporation; Shailesh Joshi and Ercan Dede – Toyota Research Institute of North America	***7. 11:15 AM - Room Temperature Bonding and Debonding of Ultra-Thin Glass Substrates for Fabrication of LCD*** Kai Takeuchi, Masahisa Fujino, and Tadatomo Suga – University of Tokyo

Program Sessions: Friday, June 3, 8:00 a.m. - 11:40 a.m.

Session 28: RF, Microwave and Millimeter Wave	Session 29: Advanced Reliability Applications	Session 30: Thermo-Mechanical and Thermal Characterization
Committee: Advanced Packaging joint with High-Speed, Wireless & Components	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Room: Mont-Royal 1	**Room: Mont-Royal 2**	**Room: Yaletown 4**
Session Co-Chairs: **Deborah S. Patterson – Principal, Patterson Group** **Amit P. Agrawal – Keyssa Inc.**	**Session Co-Chairs:** **Keith Newman – Hewlett Packard Enterprise** **Tim Chaudhry – Amkor Technology, Inc.**	**Session Co-Chairs:** **Yong Liu – Fairchild Semiconductor Corporation** **Suresh K. Sitaraman – Georgia Institute of Technology**
1. 8:00 AM - Breakthrough Packaging Level Shielding Techniques and EMI Effectiveness Modeling and Characterization Jimmy-Dinhphuoc Hoang, Robert Darveaux, Tony LoBianco, Yi Liu, and Wayne Nguyen – Skyworks Solutions, Inc.	***1. 8:00 AM - Combination of Experimental and Simulation Methods for Analysis of Sintered Ag Joints for High Temperature Applications*** Hans Walter, Constanze Weber, Matthias Hutter, Marius von Dijk, and Olaf Wittler – Fraunhofer IZM; Klaus-Dieter Lang – Fraunhofer IZM/Technical University Berlin	***1. 8:00 AM - Simulation Driven Design of Novel Integrated Circuits – Part 3: Physics of Failure Simulation of the Electronic Control Modules for Harsh Environment Application*** Alicja Palczynska, Arun Sasi, Matthias Werner, Alexandru Prisacaru, and Przemyslaw Gromala – Robert Bosch GmbH; Bongtae Han – University of Maryland; Dirk Mayer and Tobias Melz -- Fraunhofer Institut für Betriebsfestigkeit und Systemzuverlässigkeit LBF
2. 8:25 AM - Modeling, Design, Fabrication and Demonstration of RF Front-End Module with Ultra-Thin Glass Substrate for LTE Applications Junki Min, Zihan Wu, Markondeya Raj Pulugurtha, Vanessa Smet, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Arjun Ravindran and Christian Hoffmann – TDK-EPCOS, Inc.	***2. 8:25 AM - Improvements to the IES TM-28-14 Lumen Maintenance Standard: A Generalized Acceleration Factor Approach for Solid-State Lighting*** Pradeep Lall and Peter Sakalaukus – Auburn University; Lynn Davis – RTI International	***2. 8:25 AM - Non-Linear Finite Element Analysis on Stacked Die Package Subjected to Integrated Vapor-Hygro-Thermal-Mechanical Stress During Solder Reflow*** Jing Wang and Seungbae Park – Binghamton University
3. 8:50 AM - Chip Last Fan-Out Packaging for Millimeter Wave Application Hsin-Chia Lu and Yuan-Hong Wang – National Taiwan University; Jeng-Long Leou, Harrison Chan, and Scott Chen – Advanced Semiconductor Engineering, Inc.	***3. 8:50 AM - An Advanced Study on Ion Impurities on Solder Resist and the Solutions for High-Temperature Reliability Performance*** Lei Zhang and Hideaki Kojima – Taiyo Ink Mfg. Co., Ltd.	***3. 8:50 AM - Electronic PCB & Package Thermal Stress Analysis*** Gamal Refai-Ahmed and Hong Shi – Xilinx, Inc.; Madhu Keshavamurthy, Siddharth Shah, Dale Ostergaard, Bryan Boots, Tim Pawlak, Yasharth Bhartiya, and Steven Pytel – ANSYS, Inc.
Refreshment Break: 9:15 a.m. - 10:00 a.m. Mont-Royal Commons		
4. 10:00 AM - A Highly Integrated RFSoC Design for 3G Smart Phone Application Nan-Cheng Chen, Wen-Chou Wu, Sheng-Mou Lin, Wan-Ju Kuo, Kun-Ting Hung, and Ya-Ling Tseng – Mediatek Inc.	***4. 10:00 AM - Joule Heating Enhanced Electromigration Failure in Redistribution Layer in 2.5D IC*** Yingxia Liu, Menglu Li, Mengjie Jiang, and K. N. Tu – University of California, Los Angeles; Dong-Wook Kim and Sam Gu – Qualcomm Technologies, Inc.	***4. 10:00 AM - Ultra-High Performance of Thermal Interface Material via Capillary Attraction*** Hongye Sun and Matthew Yuen – Hong Kong University of Science and Technology
5. 10:25 AM - TGV (Through-Glass-Via) Metallization of Direct Cu on Glass Shigeo Onitake, Kotoku Inoue, Masatoshi Takayama, and Takashi Kozuka – Koto Electric Co., Ltd.; Satoru Kuramochi - Dai Nippon Printing Co. Ltd.; Hobie Yun - Qualcomm Technologies, Inc.	***5. 10:25 AM - Electromigration Analysis (Experimental & Simulation) on 6 um Solid Cu TSV (via last) in 32nm SOI Technology*** Prakash Periasamy, Michael Iwatake, Joyce Liu, Troy Graves-Abe, and Thuy Tran Quinn – GLOBALFOUNDRIES; Menglu Liu and Subramanian Iyer – University of California, Los Angeles	***5. 10:25 AM - Thermal Simulations and Experimental Verification on Power Modules Designed for Double Sided Cooling*** Klas Brinkfeldt, Alexander Mann, and Dag Andersson – Swerea IVF; Jonas Ottosson – Volvo GTT; Alexander Otto – Fraunhofer ENAS; Olaf Zschieschang – Fairchild Semiconductor Corporation; Sophia Frankeser – Technical University of Chemnitz
6. 10:50 AM - In-Substrate Resonators and Bandpass Filters with Improved Insertion Loss in K-Band Utilizing Low Loss Glass Interposer Technology and Superlattice Conductors Arian Rahimi and Yong-Kyu Yoon – University of Florida; David Senior – State University of New York at Oswego; Aric Shorey – Corning, Inc.	***6. 10:50 AM - Enhancing Thermal Fatigue Reliability of Large CLCC Package*** Ketan Shah, Sridhar Canumalla, Tung Nguyen, Mohan Kirloskar, and Xiangdong Qiu – Microsoft Corporation	***6. 10:50 AM - Investigation of Geometry, Frequency and Material's Effects in Lock-In Thermography Applications in Semiconductor Packages*** Xuejun Fan and Kasemsak Kijkanjanapaiboon – Lamar University; Mayue Xie - Intel Corporation
7. 11:15 AM - Analysis and Estimation on EMI Effects in AP-DRAM Interface for a Mobile Platform Sungwook Moon, Sae-il Kim, Dong-Chul Kim, Donny Yi, Seung-Bae Lee, and Jaemin Shin – Samsung Electronics Co., Ltd.	***7. 11:15 AM - Demonstration of Enhanced System Level Reliability of Ultra-Thin Glass BGA Packages with Circumferential Polymer Collars and Doped Solder Alloys*** Bhupender Singh, Ting-Chia Huang, Venky Sundaram, Raj Pulugurtha, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Satomi Kawamoto – Namics Corporation	***7. 11:15 AM - Analysis of Thermal Performance of Advanced Packaging Technologies for State-of-the-Art Mobile Applications*** Cheng-Chieh Hsieh, Chi-Hsi Wu, and Douglas Yu – Taiwan Semiconductor Manufacturing Company

Program Sessions: Friday, June 3, 1:30 p.m. - 5:10 p.m.

Session 31: 3D Applications and Wafer Processing

Committee: Advanced Packaging

Room: Nolita 1

Session Co-Chairs:
Rozalia Beica – Dow Electronic Materials
John Knickerbocker – IBM Corporation

1. 1:30 PM - An Overview of the Development of a GPU with Integrated HBM on Silicon Interposer
Chang-Chi Lee, C.P. Hung, Calvin Cheung, PingFeng Yang, Chin-Li Kao, Dao-Long Chen, MengKai Shih, Chien-Lin Chang Chien, Yu-Hsiang Hsiao, and Li-Chieh Chen – Advanced Semiconductor Engieering, Inc.; Michael Su, Michael Alfano, Joe Siegel, Julius Din, and Bryan Black - Advanced Micro Devices, Inc.

2. 1:55 PM - 3D SiP with Organic Interposer for ASIC and Memory Integration
Li Li, Pierre Chia, Paul Ton, Mohan Nagar, Sada Patil, and Jie Xue – Cisco Systems, Inc; Javier DeLaCruz, Marius Voicu, Jack Hellings, Bill Isaacson, Mark Coor, and Ross Havens – eSilicon Corporation

3. 2:20 PM - 3Di DC-DC Buck Micro Converter With TSVs, Using Grind Side Inductors and Deep Trench Decoupling Capacitors in 32nm SOI CMOS
John Safran, Shahid Butt, Alberto Cestero, Thuy Tran-Quinn, Norman Robson, Troy Graves-Abe, Daniel Berger, and James Pape - GLOBALFOUNDRIES; Giri N.K. Rangan and Vikram Chaturvedi - IBM STG Bangalore; Venkata Nr Vanukuru, Sandeep Torgal, and Sarath Lal K.P. - GLOBALFOUNDRIES, Bangalore; Gary Maier, Matthew Angyal, Joyeeta Nag, and Sami Rosenblatt - IBM Corporation; Subramanian Iyer - University of California, Los Angeles

4. 3:30 PM - TSV-last, Heterogeneous 3D Integration of a SiGe BiCMOS Beamformer and Patch Antenna for a W-Band Phased Array Radar
Dean Malta, Erik Vick, Matthew Lueck, and Alan Huffman – RTI International; Sharon Woodruff, Parrish Ralston, Jeffrey Hartman, Nathan Bushyager, G. David Ebner, and Stuart Quade – Northrop Grumman Electronic Systems; Adam Young, Christopher Hillman, and Jonathan Hacker – Teledyne Scientific Company

5. 3:55 PM - Design, Demonstration and Characterization of Ultra-Thin Low-Warpage Glass BGA Packages for Smart Mobile Application Processors
Tailong Shi, Bruce Chou, Ting-Chia Huang, Venky Sundaram, Kadappan Panayappan, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Tomonori Ogawa and Yoichiro Sato – Asahi Glass Company; Hiroyuku Matsuura – NGK Spark Plug Co., Ltd; Satomi Kawamoto – NAMICS Corporation

6. 4:20 PM - Warpage-Free Ultra-Thinning Ranged from 2 to 5 Micron for DRAM Wafers and Evaluation of Devices Characteristics
Young Suk Kim, S. Kodama, Y. Mizushima, T. Nakamura, N. Maeda, K. Fujimoto, and T. Ohba – Tokyo Institute of Technology; A. Kawai – DISCO Corporation

7. 4:45 PM - Scalable Modeling and Measurement of TSV Applied for Efficiency Improvement of a RF PA
Ming Fong Jhong, Cheng Yu Ho, Po Chih Pan, Hung Hsiang Cheng, Sheng Chi Hsieh, and Chen Chao Wang – Advanced Semiconductor Engineering, Inc.; Lih Tyng Hwang – National Sun Yat-Sen University

Session 32: Novel Fan-Out Interconnections

Committee: Assembly & Manufacturing Technology joint with Interconnections

Room: Nolita 2

Session Co-Chairs:
Jae-Woong Nah – IBM Corporation
Rajen Dias – Intel Corporation

1. 1:30 PM - A Comparative Study of a Fan Out Packaged Product: Chip-First and Chip-Last
Scott Chen, Leander Liang, Simon Wang, Golden Kao, William Chen, John Hunt, and Abner Peng – Advanced Semiconductor Engineering, Inc.

2. 1:55 PM - Versatile Metrology Platform for FOWLP PoP Manufacturing Process Control
Francy Abraham – Koh Young America Inc.; Jeong Yul Jeon - Koh Young Technology Inc.

3. 2:20 PM - A Novel System in Package with Fan-Out WLP for High Speed SERDES Application
Tung-Hsien Hsieh, Jimmy Jinn, P.H. Chang, Fandy Huang, J.W. Xiao, Alan Chou, Benson Lin, and Nan-Cheng Chen – Mediatek Inc.

4. 3:30 PM - Effect of Local Grain Distribution and Enhancement on Edgebond Applied Wafer-Level Chip-Scale Package (WLCSP) Thermal Cycling Performance
Weidong Xie and Steven Perng – Cisco Systems, Inc.; Edward Ibe and Karl Loh – Zymet; Tae-Kyu Lee – Portland State University

5. 3:55 PM - The Development and the Integration of the 1 to 5 Micron Half Pitches Wafer Level Cu Redistribution Layers (RDL)
Mike Ma, Stephen Chen, P. I. Wu, Ann Huang, C. H. Lu, Alex Chen, Cheng-Hsiang Liu, and Shih-Liang Peng – Siliconware Precision Industries Co., Ltd.

6. 4:20 PM - Next Generation Panel-Scale RDL with Ultra Small Photo Vias and Ultra-Fine Embedded Trenches for Low Cost 2.5D Interposers and High Density Fan-Out WLPs
Fuhan Liu, Chandrasekharan Nair, Shreya Dwarakanath, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Atushi Kubo – Tokyo Ohka Kogyo Co., Ltd.; Tomoyuki Ando – Tokyo Ohka Kogyo Co. Ltd; Ryuta Furuya – Ushio Inc.

7. 4:45 PM - Development of High Density Fan Out Wafer Level Package (HD FOWLP) with Multi-Layer Fine Pitch RDL for Mobile Applications
Vempati Srinivasa Rao, Chai Tai Chong, David Ho, Ding Mian Zhi, Chong Ser Choong, Sharon Lim PS, Daniel Ismael, and Ye Yong Liang – Institute of Microelectronics, A*STAR

Session 33: Advances in RF Materials & Components

Committee: High-Speed, Wireless & Components joint with Materials & Processing

Room: Nolita 3

Session Co-Chairs:
Craig Gaw – NXP Semiconductor
Praveen Pandojirao – Johnson & Johnson

1. 1:30 PM - A New Reliable Adhesion Enhancement Process for Directly Plating on Molding Compounds for Package Level EMI Shielding
Kenichiroh Mukai, Brian Eastep, Kwonil Kim, Lee Gaherty, and Anirudh Kashyap – Atotech USA Inc.

2. 1:55 PM - Silver Hybrid Paste for Improvement of Radio Frequency Characteristics
Kwang-Ho Jung, Sang-Woo Kim, and Seung-Boo Jung – Sungkyunkwan University; Dong Gun Kam - Ajou University

3. 2:20 PM - High-Frequency Characterization of Silicon Substrates and Through Silicon Vias
Xiaomin Duan, Christian Tschoban, Ivan Ndip, and Klaus-Dieter Lang – Fraunhofer IZM; Mathias Böttcher – Fraunhofer IZM-ASSID; David Dahl and Christian Schuster – Technical University Hamburg

4. 3:30 PM - A Novel Integration of 3D Printing and Stretchable Conductive Adhesive Technologies for High Frequency Packaging Applications
Taoran Le, Ryan A. Bahr, Ryan Bhar, C.P. Wong, and Manos Tentzeris – Georgia Institute of Technology

5. 3:55 PM - A Metamaterial-Inspired Sensor for Detection of Volatile Molecules
Nophadon Wiwatcharagoses – King Mongkut's University of Technology North Bangkok; Kyoung Y. Park - Agency for Defense Development (Daejeon); Premjeet Chahal – Michigan State University

6. 4:20 PM - MEMS-Based Tunable TSV Inductors
Bruce Kim and Saikat Mondal – City University of New York; Sang-Bock Cho – University of Ulsan

7. 4:45 PM - Fabrication and Modeling of Nitride Thin-film Encapsulation Based on Anti-Adhesion Assisted Transfer Technique and Nitride/BCB Bi-layer Wrinkling
Seonho Seok – IEF-University Paris-Sud

Refreshment Break: 2:45 p.m. - 3:30 p.m. Mont-Royal Commons

Program Sessions: Friday, June 3, 1:30 p.m. - 5:10 p.m.

Session 34: 3D, TSV, and TGV Reliability & Characterization

Committee: Thermal/Mechanical Simulation & Characterization joint with Applied Reliability

Room: Mont-Royal 1

Session Co-Chairs:
Xuejun Fan – Lamar University
Lakshmi N. Ramanathan – Microsoft Corporation

1. 1:30 PM - Board-Level Reliability of 3D TGV Filters During Thermal Cycling
Scott McCann, Venkatesh Sundaram, M. Raj Pulugurtha, Rao R. Tummala, and Suresh K. Sitaraman – Georgia Institute of Technology; Hobie Yun – Qualcomm Technologies Inc.; Satoru Kuramochi – Dai Nippon Printing Co., Ltd.

2. 1:55 PM - Remaining Useful Life Assessment of Field Deployed Electronics Using X-ray Micro-CT Based Digital Volume Correlation
Pradeep Lall and Junchao Wei – Auburn University

3. 2:20 PM - Impact of 3D Via Middle TSV process on 20nm Wafer Level FEOL and BEOL Reliability
C. S. Premachandran, Rakesh Ranjan, Jing Tan, Kong Boon Yeap, Walter Teo, Sukeshwar Kannan, Salavatore Cimino, Haojun Zhang, Daniel Smith, Luke England, Patrick Justison, Biju Parameshwaran, and Natarajan Mahadeva Iyer – GLOBALFOUNDRIES

4. 3:30 PM - Effect of Electroplating Parameter on the TSV-Cu Protrusion during Annealing
Si Chen, Fei Qin, Tong An, and Pei Chen – Beijing University of Technology

5. 3:55 PM - Comprehensive Investigation of Die Shift in Compression Molding Process for 12 Inch Fan-Out Wafer Level Packaging
Yong Han, Mian Zhi Ding, Lin Bu, and Ser Choong Chong – Institute of Microelectronics, A*STAR

6. 4:20 PM - Low Residual Stress in Si Substrate of Annular-Trench-Isolated TSV
Wei Feng, Tung Thanh Bui, Naoya Watanabe, Masahiro Aoyagi, and Katsuya Kikuchi – AIST

7. 4:45 PM - Mechanical Effects of the Volmer-Weber Growth in the TSV Sidewall
Santo Papaleo, Marco Rovitto and Hajdin Ceric – Technische Universität Wien

Session 35: Wearable, Flexible, and Stretchable Electronics

Committee: Emerging Technologies

Room: Mont-Royal 2

Session Co-Chairs:
C. S. Premachandran – GLOBALFOUNDRIES
Bharat Penmecha – Intel Corporation

1. 1:30 PM - A Wearable Flexible Hybrid Electronics ECG Monitor
Mark Poliks, James Turner, Kanad Ghose, Zhanpeng Jin, Mohit Garg, and Qiong Gui – Binghamton University; Ana Arias and Yasser Kahn – University of California, Berkeley; Mark Schadt and Frank Egitto – i3 Electronics, Inc.

2. 1:55 PM - Wearable Sensor Patch for Early Extravasation Detection
Ming-Yuan Cheng, Ramona Damalerio, Ruiqi Lim, Weiguo Chen, NS Kwan Ling Tan – Institute of Microelectronics, A*STAR; Choon Looi Bong and Swee Kim Tan - K. K. Women's & Children's Hospital (Singapore)

3. 2:20 PM - An Implantable, Stretchable Microflow Sensor Integrated with a Thin-Film Nitinol Stent
Connor Howe, Yongkuk Lee, and Woon-Hong Yeo – Virginia Commonwealth University; Yanfei Chen and Youngjae Chun – University of Pittsburgh

4. 3:30 PM - A Flexible and Stretchable Resistive Epidermal Pressure Sensor for Health Monitoring
Zhibo Chen, Wei Huang, Xinfeng Zhang, Matthew Ming, and Fai Yuen – Hong Kong University of Science & Technology

5. 3:55 PM - Screen-Printed Stretchable Interconnections
Jari Suikkola, Pekka Iso-Ketola, Timo Kankkunen, Jukka Vanhala, and Matti Mäntysalo – Tampere University of Technology

6. 4:20 PM - Flexible Wire-Component for Weaving Electronic Textiles
Jussi Mikkonen – Aalto University; Emmi Pouta – Leeluu Labs Inc.

7. 4:45 PM - Mechanical Reliability Analysis of Ultra-Thin Chip-on-Foil Assemblies under Different Types of Recurrent Bending
Nagarajan Palavesam, Detlef Bonfert, Waltraud Hell, Christof Landesberger, Horst Gieser, and Christoph Kutter – Fraunhofer EMFT; Karlheinz Bock – Technical University Dresden

Session 36: 3D Materials & Processing

Committee: Materials & Processing

Room: Yaletown 4

Session Co-Chairs:
Mikel Miller – Draper Laboratory
Myung Jin Yim – Intel Corporation

1. 1:30 PM - Feasibility Study of Si Handler Debonding by Laser Release
Bing Dang, Thomas Wassick, Paul Andry, Li-Wen Hung, Jeffery Gelorme, Qianwen Chen, John Knickerbocker, Yang Liu, and Hongqing Zhang – IBM Corporation

2. 1:55 PM - High Throughput Air Jetting Wafer Debonding For 3D IC and MEMS Manufacturing
Hao Tang and Chris Luo – Micro Materials Inc.; Ming Yin, Yushen Zeng, and Wei Zhang – Zhejiang -Microtech Material Company

3. 2:20 PM - Extremely Low Force Debonding of Thinned CMOS Substrate by Laser Release of a Temporary Bonding Material
Alain Phommahaxay, Goedele Potoms, Greet Verbinnen, Erik Sleeckx, Gerald Beyer, and Eric Beyne – IMEC; Alice Guerrero, Dongshun Bai, Xiao Liu, Kim Yess, and Kim Arnold – Brewer Science Inc.; Walter Spiess, Tim Griesbach, Thomas Rapps, and Stefan Lutter – SÜSS MicroTec Lithography GmbH

4. 3:30 PM - In-Plane Collective CoSA Assembly by NCF-TCB Enabled using the Newly Developed Bonding Force Leveling Film
Hitoshi Onozeki, Hiroshi Takahashi, Naoya Suzuki, Kumpei Yamada, and Yuta Koseki – Hitachi chemical Co.,Ltd.

5. 3:55 PM - Rapid Scan In-Situ FT-IR Curing Studies of Low-Temperature Cure Thin Film Polymer Dielectrics in the Solid State
Frank Windrich – Fraunhofer IZM; Mikhail Malanin and Klaus-Jochen Eichhorn – Leibniz-Institut für Polymerforschung Dresden e.V.; Brigitte Voit – Technische Universität Dresden

6. 4:20 PM - Development of Novel Low-Temperature Curable Positive-Tone Photosensitive Dielectric Materials with High Elongation
Yu Shoji, Yuki Masuda, Keika Hashimoto, Kimio Isobe, Yutaro Koyama, and Ryoji Okuda – Toray Industries Inc.

7. 4:45 PM - Formation of Polymer Insulation Layer (Liner) on Through Silicon Vias (TSV) with High Aspect Ratio over 5:1 by Direct Spin Coating
Liyi Li, Chia-Chi Tuan, and Kyoung-Sik Moon – Georgia Institute of Technology; Guoping Zhang and Rong Sun – Shenzhen Institutes of Advanced Technology, CAS

Refreshment Break: 2:45 p.m. - 3:30 p.m. Mont-Royal Commons

Wednesday, June 1, 2016
Session 37: Interactive Presentations 1
9:00 AM - 11:00 AM
Committee: Interactive Presentations
Belmont Commons

Session Co-Chairs:
Patrick Thompson – Texas Instruments, Inc.
Rao Bonda – Amkor Technology
Tom Poulin – Aerie Engineering
Subhash L. Shinde – Sandia National Laboratory

A Wirebond-Less Package for High-Voltage Cascode Gallium Nitride Devices
Wenli Zhang, Zhengyang Liu, and Fred Lee – Virginia Tech; Shuojie She – Beijing University of Technology

Constitutive Relations for FEM of SnAgCu in Thermal Cycling – How Wrong We Were!
Peter Borgesen, Thaer Alghoul, Farhan Batieha, Nardeeka Adams, Saif Khasawneh, Dustin Watson, and Chris Greene – Binghamton University

Novel Process of RDL formation for Advanced Packaging by Excimer Laser Ablation
Habib Hichri, Markus Arendt, and Matthew Gingerella – SUSS MicroTec Photonic Systems, Inc.

Ultra-Precise Low-Cost Surface Planarization Process for Advanced Packaging Fabrications and Die Assembly: A Survey of Recent Investigations on Unit Process Applications and Integrations
Frank Wei – Disco Corporation; Vanessa Smet, Ninad Shahane, Hao Lu, Venky Sundaram, and Rao Tummala - Georgia Institute of Technology

Formation of High-Aspect-Ratio Through Silicon Vias (TSV) with A Broad Range of Diameter from 1 to 100 um by Uniform Metal-assisted Chemical Etching (MaCE)
Liyi Li and C. P. Wong – Georgia Institute of Technology

Effective Post-TSV-DRIE Wet Clean Process for Through Silicon Via Applications
Laura Mauer, John Taddei, John Clark, and Kenji Nulman – Veeco PSP; Stephen Olson, Victor Vartanian, and Michael Hatzistergos – SUNY Polytechnic Institute

Fabrication and Characterization of Low Stress Si Interposer with Air-gapped Si Interconnection for Hermetical System-in-Package
Rongfeng Luo, Kuili Ren, Shenglin Ma, Jun Yan, and Yanming Xia – Xiamen University; Yufeng Jin and Jing Chen – Peking University; Tianzhun Wu, Hangao Yang, and Lifang Yuan – Shenzhen Institutes of Advanced Technology

Study on Ar(5H2) Plasma Pretreatment for Cu/Sn/Cu Solid-State-Diffusion (SSD) Bonding in 3D Interconnection
Junqiang Wang and Dejun Wang – Dalian University of Technology; Qian Wang and Jian Cai – Tsinghua University

Advanced 3D eWLB-PoP (Embedded Wafer Level Ball Grid Array - Package on Package) Technology
Yaojian Lin, Chen Kang, Linda Chua, Won Kyung Choi, and Seung Wook Yoon – STATS ChipPAC Ltd.

Impact of Via Density on the Mechanical Integrity of Advanced Back-End-Of-Line During Packaging
Luka Kljucar, Mario Gonzalez, Kristof Croes, Ingrid De Wolf, Gayle Murdoch, Joeri De Vos, Juergen Boemmels, Eric Beyne, and Zsolt Tokei – IMEC

Die Bonding with Non-Clean Flux in Fine Pitch Copper Pillar Bump Study and Reliability Performance for 2.5D IC Package
J.C Liao, Ally Liao, Sam Peng, G.T Lin, Terrence Lu, and Stephen Chen – Siliconware Precision Industries Co., Ltd.

High Quality Fine-Pitch Cu-Cu Wafer-on-Wafer Bonding with Optimized Ti Passivation at 160 deg C
Asisa Kumar Panigrahi, Satish Bonam, Tamal Ghosh, Siva Rama Krishna Vanjari, and Shiv Govind Singh – Indian Institute of Technology, Hyderabad

Evaluation and Optimization of Thermo-Mechanical Reliability of a TSV-based 3D MEMS
Qinghua Zeng, Wei Meng, Yong Guan, Jing Chen, and Yufeng Jin – Peking University

Low Cost Wafer Level Packaging of MEMS Devices by Vertical Via-Last Process
Xiangmeng Jing, Fengwei Dai, Chunyan Zhang, Wenqi Zhang, and Liqiang Cao – National Center for Advanced Packaging

Thermo-Compression Bonding Using Non-Conductive Films (NCFs) for Cu Pillar/Sn-Ag Micro-Bump Interconnection
Hyeong Gi Lee, Se-Yong Lee, Yong-Won Choi, and Kyung-Wook Paik – KAIST

3D WL MEMS with Various TSV Technologies – Thermo-Mechanical Analysis
Ying-Te Ou, Hung-Hsiang Cheng, Dao-Long Chen, Hsiao-Yen Lee, Ying-Chih Lee, Meng-Kai Shih, Chin-Cheng Kuo, Ping-Feng Yang, and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

Joint Properties and Thermomechanical Reliability of Nanoparticle-Added Sn-Ag-Cu Solder Paste
Kyoung-Ho Kim and Sehoon Yoo – Korea Institute of Industrial Technology; Jonghyuk Yoon, Songhee Yim, Bum-Gyu Baek, and Jong Hyun Yoon – KD One; Jae Pil Jung and Dohyun Jung – University of Seoul

Study of Chip Stacking Process and Electrical Characteristic Evaluation of Cu Pillar Joints Between the Chips Including TSV
Toshiya Akamatsu, Shinji Tadaki, Kazutoshi Yamazaki, Hideki Kitada, and Seiki Sakuyama – Fujitsu, Ltd.

Reliability Demonstration of an Ultra-Thin Core (UTC) Large Die Laminate Package
Tomoyuki Yamada – Kyocera America; Hiroyuki Fukushima, Fumio Kumokawa, and Micho Ohori – Kyocera Circuit Solutions; Sushumna Iruvanti, Shidong Li, Tuhin Sinha, Jeff Coffin, Hai Longworth, and Charlie Reynolds – IBM Corporation

Challenges in Assembly and Reliability of Thin NAND Memory Die
Ning Ye, Qing Li, Huirong Zhang, Zhongli Ji, Xiaoyu Yang, Chin-Tien Chiu, and Hem Takiar – SanDisk

Thermal Isolation within High-Power 2.5D Heterogeneously Integrated Electronic Packages
Michael Fish, Patrick McCluskey, and Avram Bar-Cohen – University of Maryland

Electromagnetic Bandgap Design for Power Distribution Network Noise Isolation in the Glass Interposer
Youngwoo Kim, Jinwook Song, Jihye Kim, and Joungho Kim – KAIST; Jonghyun Cho – MST; Venky Sundaram and Rao Tummala – Georgia Institute of Technology

On Chip RF Passives using an SU-8 Composite with Magnetic Nanoparticles
Hüseyin Sagkol, Mamady Kebe, Zilhicce Mehmedi, and Erdal Korkmaz – Fatih University

Wednesday, June 1, 2016
Session 38: Interactive Presentations 2
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Belmont Commons

Session Co-Chairs:
Mark Poliks – Binghamton University
Nancy Stoffel – GE Global Research
René Rongen – NXP Semiconductors
Pradeep Lall – Auburn University

Proposal of Package Structure Requirements for Effective Cooling from the Bottom (Substrate) Side of Chips, Aiming for a 3D Chip Stack
Keiji Matsumoto and Hiroyuki Mori – IBM Corporation

Innovative Temperature and Heat Distribution Measurement Protocol Applied to 3D TSV Technology
Denis Mercier, Thomas Portanier, David Bouchu, and Stephane MOREAU – CEA-LETI; Chirstophe Aumont – STMicroelectronics

Study on Process Induced Wafer Level Warpage of Fan-Out Wafer Level Packaging
Faxing Che, David Ho, Mianzhi Ding, and Daniel MinWoo Rhee – Institute of Microelectronics, A*STAR

Simulation Model to Predict Failure Cycles in Board Level Drop Test
Wei Wang, Daniel Robbins, and Christopher Glancey – Micron Technology, Inc.

Assembly Process and Warpage Management of Large Size Through Silicon Interposer (38.7mm × 26.7mm) Package
Zhaohui Chen, Jong-Kai Lin, Mian Zhi Ding, Sharon Pei Siang Lim, and Xiaowu Zhang – Institute of Microelectronics, A*STAR

Characterization of Warpages and Layout-Dependent Local-Deformations for Large Die 3D Stacking
Aki Dote, Hideki Kitada, Yoriko Mizushima, Tomoji Nakamura, and Seiki Sakuyama – Fujitsu Ltd.

Comparison of Thermal Measurement Methods of Die Attach Materials used in Power Electronic Modules
Thomas Krebs, Susanne Duch, and Wolfgang Schmitt – Heraeus Deutschland GmbH & Co. KG

Sub-100 nm Patterning Process and Adhesion Force Simulation in UV-Nanoimprint Lithography
Yinsheng Zhong and Matthew. M. F. Yuen – Hong Kong University of Science & Technology

Deep, High Aspect Ratio Etches in Alumina Films for MEMS and Advanced Packages
Dogukan Yildirim, Guann-Pyng Li, and Mark Bachman – University of California, Irvine

Effect of Storage on the High Strain Rate Properties of SAC Leadfree Alloys at Temperatures up to 200°C
Pradeep Lall, Di Zhang, Vikas Yadav, and Jeff Suhling – Auburn University; David Locker – US Army AMRDEC

A Fast and Low Computation Consumption Model for System-Level Thermal Management in 3D IC
Yudan Pi, Wenhua Xu, Jiaxi Zhang, Guojie Luo, Yufeng Jin, Ningyu Wang, and Wei Wang – Peking University; Min Miao – Beijing Information Science and Technology University

Mass Transport-Induced Failure of Hybrid Bonding-Based integration for Advanced Image Sensor Applications
Stéphane Moreau, David Bouchu, Viorel Balan, Anne-Lise Le Berrigo, and Amandine Jouve – CEA-LETI; Yann Henrion, Carine Besset, Daniel Scevola, Sandrine Lhostis, François Guyader, Sébastien Mermoz, Julien Pruvost, and Emilie Deloffre – STMicroelectronics

In Vehicle Infotainment and Advanced Driver Assistance Systems: Advantages of Knowledge-Based Qualification Over Standard-Based Qualification for Solder Joint Reliability
Ru Han, Min Pei, Sibasish Mukherjee, Milena Vujosevic, Kenneth Darschewski, and Robert Kwasnick – Intel Corporation

Demonstration of Novel Adhesive Technology Enabling Low-Temperature Polymeric Bonding for Use in Microelectronics Applications
Lyndon Larson and Kate Johnson – Dow Corning

Fabrication and Integration of Ultrathin, High Density, High-Frequency Ta Capacitors on Silicon for Power Modules
Parthasarathi Chakraborti, Nathan Neuhart, Himani Sharma, P. Markondeya Raj, and Rao Tummala – Georgia Institute of Technology; Kamil-Paul Rataj - H. C. Starck GmbH; Saumya Gandhi, Frank Stepniak, and Matt Romig - Texas Instruments; Naomi Lollis - A.V.X. Corporation

Optimization Design of 2.5D TSV Package Using Thermo-Electrical Coupled Analysis Method
Fengze Hou, Yunyan Zhou, Fengman Liu, Jun Li, Cheng Chen, Delong Qiu, and Liqiang Cao – Chinese Academy of Sciences; Tingyu Lin – National Center for Advanced Packaging

A Novel Experimental System for Characterizing Interface Delamination Under Mixed-Mode Fatigue Loading
Tz-Cheng Chiu, Wei Lu, Chi-An Hua, and Chia-Kuei Hsu – National Cheng Kung University

Simulative and Experimental Investigation of the Mechanical Reliability of the Flexible Optoelectronic Packaging Using Optodic Bonding
Yixiao Wang, Xiaoxu Yang, and Ludger Overmeyer – Leibniz Universitaet Hannover

Effect of Die Size and Die Tilt on Solder Reliability Under Thermal Cycling
Miaocao Wang, Yang Zhou, and Ling Xu – Huazhong University of Science & Technology; Sheng Liu – Wuhan University

Deformation of Display for Hand-Held Devices During Drop Impact
Charandeep Singh and Seungbae Park – Binghamton University; Satish Chaparala, Chunfeng Zhou, and Zhang Bin – Corning, Inc.

Reliability Assessment of QFN Components for Aerospace Applications
Stoyan Stoyanov, Chunyan Yin, and Christopher Bailey – University of Greenwich; Paul Stewart and Steve McCallum - Finmeccanica, Airborne & Space Systems Division

Impact of Die Pin Capacitance and Package Crosstalk on DDR4 Channel Jitter
Janani Chandrasekhar, Changwook Yoon, Dan Oh, Alan Liu, and Hui Liu – Altera Corporation

A Novel Programmable On-chip Voltage Droop Detector for FPGA Applications
Hing Yan "Thomas" To, Changyi Su, Sean Long, Juan Wang, Nanju Na, Dima Klokotov, and Yong Wang – Xilinx, Inc.

Reliability Assessment of Die-on-Board Packages Using High Resolution Moiré Interferometry and Synchrotron X-Ray Microdiffraction
Laura Spinella, Jang-Hi Im, and Paul Ho – University of Texas, Austin

Crosstalk-Induced Jitter Simulation Methodology for High-Density I/O Designs
Shen Dong and Hong Shi – Xilinx, Inc.

Detection of Noise Coupling between Power Domains on Package
Suzanne Huh and Hong Shi – Xilinx, Inc.

An Image-Based Effective Property Method for Strip Warpage Modeling
Siva Gurrum, Guangxu Li, Hung-Yun Lin, and Yong Lin – Texas Instruments, Inc.

Impact of PCB Layer Orientation on the Drop Reliability of WCSP
Anik Mahmood, Trina Barua, A. R. Nazmus Sakib, and Dereje Agonafer – University of Texas, Arlington

Thursday, June 2, 2016
Session 39: Interactive Presentations 3
9:00 AM - 11:00 AM
Committee: Interactive Presentations
Belmont Commons

Session Co-Chairs:
Mark Eblen – Kyocera America, Inc.
Swapan Bhattacharya – Engent Inc.
Takafumi Fukushima – Tohoku University
Wei Frank – Disco Japan

Miniaturized Integrated Array of Micro-Supercapacitors as Efficient Power Sources for Biocompatible and Wearable Electronic Devices
Bo Song, Liyi Li, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology

Development of RF 3D Module Based on Si Interposers with Redundnat TSVs
Kwang-Seong Choi, Seok Hwan Moon, Yong-Sung Eom, Hyun-Cheol Bae, and Jin Ho Lee – ETRI

Low-Stress Design for SiC Power Modules with Sintered Porous Ag Interconnection
Chuantong Chen, Shijo Nagao, Hao Zhang, Tohru Sugahara, and Katsuaki Suganuma – Osaka University; Tomohito Iwashige, Kazuhiko Sugiura, and Kazuhiro Tsuruta – Denso Corporation

A Characterized Redistribution Layer Architecture for Advanced Packaging Technologies
Hiroshi Kudo, Takamasa Takano, Masaya Tanaka, Ryohhei Kasai, Jyunichi Suyama, Miyuki Akazawa, Mitsuhiro Takeda, Hiroshi Mawatari, Toshio Sasao, Yumi Okazaki, Naoki Oota, Susumu Tashiro, Haruo Iida, Kouji Sakamoto, Hiroyuki Sato, Daisuke Kitayama, Shouhei Yamada, and Satoru Kuramochi – Dai Nippon Printing Co., Ltd.

Binder Chemistry for Ultra-Conductive Pastes by Low Temperature Sintering of Ag Micro-Fillers
Masahiro Inoue, Yoshiaki Sakaniwa, and Yasunori Tada – Gunma University

Effects of Reflow Cooling Rate on the Growth of Ag3Sn Platelets and Deformation of Solder Balls
Chi-Pu Lin, Tommy Sun, Katch Wan, and Rick Lee – Siliconware Precision Industries Co., Ltd.; Chih-Ming Chen – National Chung Hsing University

Interconnection of Flexible Thin Film Batteries for Systems-In-Foil
Messaoud Bedjaoui, Steve Martin, and Raphael Salot – CEA-Leti

Development and Reliability Evaluation of Large Scale Thin TSV Die Stacking on Wafer
Jong Bum Lee, Ser Choong Chong, Keng Yuen Au, and Min Woo Rhee – Institute of Microelectronics, A*STAR

Characterization of Extreme Si Thinning Process for Wafer-to-Wafer Stacking
Fumihiro Inoue, Anne Jourdain, Joeri De Vos, Eric Beyne, and Erik Sleeckx – IMEC; Jash Patel, Oliver Ansell, Huma Ashraf, Janet Hopkins, and Dave Thomas – SPTS Technologies; Akira Uedono – Tsukuba University

Shape-Dependent Transmittable Tangential Force of Wire Bond Tools
Simon Althoff, Tobias Meyer, Andreas Unger, Walter Sextro, and Florian Eacock – University of Paderborn

Effect of Different Oxide Layers on the Ultrasonic Copper Wire Bond Process
Florian Eacock, Andreas Unger, Paul Eichwald, Olexandr Grydin, Florian Hengsbach, Simon Althoff, and Mirko Schaper – University of Paderborn; Karsten Guth – Infineon Technologies AG

Electrophoretic Deposition of Ni/Au Coated Particles for Ultra-fine Pitch Interconnection
Junlei Tao, David C. Whalley, and Changqing Liu – Loughborough University;

Six Micron Pitch High Density Cu-Cu Bonding for 3D IC Stacking
Ling Xie, Sunil Wickramanayaka, Ser Choong Chong, Vasarla Nagendra Sekhar, Daniel Ismeal, and Yong Liang Ye – Institute of Microelectronics, A*STAR

Mesoporous Silica Nanoparticles: a Potential Inorganic Filler to Prepare Polymer Composites with Low CTE and Modulus for Electronic Packaging Applications
Gang Li, Pengli Zhu, Tao Zhao, Rong Sun, Daoqiang Lu, Guoping Zhang, and Xiaoliang Zeng – Chinese Academy of Sciences; Chingping Wong – Georgia Institute of Technology

Conductive Microfluidic Interconnects to Enable Scalable 3D Manufacturing of Wearable Electronics
Jonathan Flowers, Changqing Liu, Sean Mitchell, Dale Esliger, and Andy Harland – Loughborough University

20" x 20" Panel Size Glass IPD Interposer Manufacturing
Yu-Hua Chen, Chun-Hsien Chien, Yu-Chung Hsieh, Wei-Ti Lin, Wen-Liang Yeh, Chien-Chou Chen, and Tzvy-Jang Tseng – Unimicron Technology Corp.; Hobie Yune – Qualcomm Technologies, Inc.

Enabling Low-Temperature Bonding in Advanced Packaging Using Electrodeposited Indium
Yi Qin, Kristen Flajslik, Brandon Sherzer, Emily Banelis, Inho Lee, Regina Cho, Louis Grippo, Masaaki Imanari, Mark Lefebvre, Lingyun Wei, Wataru Tachikawa, Jianwei Dong, and Jeffrey Calvert – Dow Chemical Company

Failure Analysis and Material Characterization in Power Electronics Packaging
Bianca Boettge, M. Schak, R. Klengel, J. Schischka, and Sandy Klengel – Fraunhofer IMWS

Comparative Reliability Study of Au Wire Bond Contacts on Al Metallization vs. Over Pad Metallization
Robert Klengel, Jan Schischka, Sandy Klengel, and Lutz Berthold – Fraunhofer IMWS

Effect of Epoxy Flux Underfill on Thermal Cycling Reliability of Sn-8Zn-3Bi Lead-Free Solder in Sensor Applications
Milad Mostofizadeh, Masoud Najari, and Laura Frisk – Tampere University of Technology; Diganta Das and Michael Pecht – University of Maryland

Solder Injected Through Via for Multi Stacked Wafers
Akihiro Horibe, Kuniaki Sueoka, Risa Miyazawa, Toyohiro Aoki, Sayuri Kohara, Keishi Okamoto, Hiroyuki Mori, and Yasumitsu Orii – IBM Corporation

A Prospective Low-k Insulator for Via-Last Through-Silicon-Vias (TSVs) in 3D Integration
Tung Thanh Bui, Xiaojin Cheng, Naoya Watanabe, Fumiki Kato, Katsuya Kikuchi, and Masahiro Aoyagi – National Institute of AIST

Effects of the Deposition Process Variation on the Performance of Open TSVs
Lado Filipovic and Siegfried Selberherr – Technical University Wien

Investigation of Ni as Magnetic Micro-Seed in SAC 305 Solder For Inductive Heating Applicability
R. Gopala Krishnan, Xu Ke, S. Arun Kumar, and Eng Soon Tok – National University of Singapore; G. Yaadhav Raaj and G. Srayes – Advanced Integrated Analytical Test Services; Michael Pecht - University of Maryland

Moisture Diffusion and Hygroscopic Swelling of Adhesives in Electronics Packaging
Ruiyang Liu, Huayan Wang, HoHyung Lee, Jing Wang, and S. B. Park – Binghamton University; Xiaojie Xue, Yeonsung Kim, Shafi Saiyed, and Dipak Sengupta – Analog Devices, Inc.

Advances in Panel Scalable Planarization and High Throughput Differential Seed Layer Etching Processes for Multilayer RDL on 2.5D Glass Interposers at 20 micron I/O Pitch
Hao Lu, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Frank Wei – Disco Corporation; Ryuta Furuya – USHIO, Inc.; Atsushi Kubo – Tokyo Ohka Kogyo Co., Ltd.

Process Design of Fine Pitch Ball Bonding by Volume Conservation Modelling
Michael Mayer – University of Waterloo

2D Grating Pitch Mapping of a Through-Silicon Vias (TSV) and Solder Ball Interconnect Region using Laser Diffraction
Todd Houghton, Michael Saxon, Zeming Song, Hoa Nguyen, Hanqing Jiang, and Hongbin Yu – Arizona State University

Copper Ball Bond Over Probe Marks in Two Pad Aluminum Thicknesses
Jacob Marsh, Austin Doutre I, Kyle Syndergaard, Priscila Brown, Kok Inn Hoo, Edsel De Jesus, and Stevan Hunter – ON Semiconductor

Thursday, June 2, 2016
Session 40: Interactive Presentations 4
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Belmont Commons

Session Co-Chairs:
Nam Pham – IBM Corporation
John Hunt – ASE US Inc.
P. Markondeya Raj – Georgia Institute of Technology
Isaac Robin Abothu – Siemens Medical Solutions USA Inc.

Forward Tactile Sensing Device Development and Biopackaging for Endovasular Guidewire Intervention Application
Ruiqi Lim, Ee Lim Tan, Kwan Ling Tan, Weiguo Chen, Ramona Damalerio, and Ming-Yuan Cheng – Institute of Microelectronics, A*STAR; Benjamin Soo Yeng Chua, Melvin Wee Chuan Loh, and Rachel Tsui Ying Hong - National University of Singapore

Ultra-Miniaturized Planar Absorbing Metamaterial Structures for Millimeter Wave and Terahertz Imaging Array
Kyoung Youl Park – Agency for Defense Development; Premjeet Chahal – Michigan State University; Nophadon Wiwatcharagoses - Mongkut's University of Technology at North Bangkok

A Study on Cu-Rod Anisotropic Conductive Films (ACFs) for Flex-on-Fabric (FOF) Interconnections by Using an Ultrasonic Bonding Method
Seung-Yoon Jung, Hye Eun Hong, and Kyung-Wook Paik – KAIST

Novel Periodic Aperiodic Routing to Mitigate Floquet Mode Resonances in Crosstalk Transfer Function due to Periodically Routed Structures
Arun Chada and Bhyrav Mutnury – Dell; Jun Fan and James L. Drewniak – Missouri University of Science and Technology

Sub-Micron Bondline-Shape Control in Automated Assembly of Photonic Devices
Nicolas Boyer, Alexander Janta-Polczynski, Swetha Kamlapurkar, Sebastian U. Engelmann, Yoichi Taira, Hidetochi Numata, Paul Fortier, and Tymon Barwicz – IBM Corporation; Jean-Francois Morissette – Université de Sherbrooke; Shotaro Takenobu – AGC Corporation

A Novel Modular Design and Modeling Methodology for High Speed High Density Die Package PCB Co-Design and Model Library Creation
Xiaohong Jiang, Chit Zhung Tan, Yee Huan Yew, Xinyun Guo, Lei Hua, Nathaniel Unger, Hui Liu, and Pheak Ti Teh – Altera Corporation

Narrowband-Stop Reflector Using Guided-Mode Resonance in Waveguide Cavity for WDM Optical Interconnects
Shogo Ura, Masahiro Nakata, Kenichi Yanagida, and Junichi Inoue – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology

Behavioral Circuit Models of Jitter Modulator and Single-Ended-Mode to Mixed-Mode Transformer for Signal Integrity Transient Simulation
Zhaoqing Chen – IBM Corporation

Simulation, Modeling and Analysis of Dynamic Power Delivery Network and its Impact on Jitter
Sheng-Feng Lee, Chia-Yu Chan, and Shang-Pin Chen – Mediatek

Performance Improvement in Side Contact Multilayer Graphene Nanoribbon Interconnects Using Intercalated Doping
Atul Kumar Nishad and Rohit Sharma – Indian Institute of Technology, Ropar

Stochastic LIM for Transient Simulation of Transmission Lines and Power Delivery Networks with Uncertainties
Xu Chen, Jose Schutt-Aine, and Andreas Cangellaris – University of Illinois, Urbana-Champaign

High Speed Data Acquisition and Pre-Processing System of the Photodetector Linear Array with Through-Silicon Vias (TSVs) 2.5D/3D integration
H. D. Lu, B. Zhang, S. H. Zhang, F. M. Guo, M. J. Wang, W. Wang, and J. H. Shen – East China Normal University

An Ultra Low Loss SerDes Signal Design on a FC Package Applied on 56 Gbps Networks
Yuan-Hsi Chou – University of Texas, Austin; Tsun-Lung Hsieh, Cheng-Yu Tsai, and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.; Lih-Tyng Hwang – National Sun Yat-Sen University

High Density Micro-Lens Array Connector for Optical Multi-chip Module
Koji Masuda, Hsiang-Han Hsu, Masao Tokunari, and Shigeru Nakagawa – IBM Corporation

Large-Scale, High-Speed and High-Precision Simulation Method for the Multi-Domain/Multi-Scale Electronic System
Hideki Asai, Yuta Ioue, and Shingo Okada – Shizuoka University

Synthesis and Characterization of One-dimensional Cu-Sn Nanowire Diffusion Couples for Nanowire Assembly and Interconnection
Fan Gao, Jirui Wang, and Zhiyong Gu – University of Massachusetts, Lowell; Qiyue Yin and Guangwen Zhou – Binghamton University

Novel Power Delivery Noise Mitigation Scheme Using Negatively Coupled Inductors
Amit Jain and Sameer Shekhar – Intel Corporation

System Co-Design for Low Power, High Performance Multicore DSP Systems
Tapobrata Bandyopadhyay, Anita Pratti, Bill Taboada, Thomas Krause, Tom Johnson, and Snehamay Sinha – Texas Instruments, Inc.

Design and Demonstration of Ultra-Thin Glass 3D IPD Diplexers
Zihan Wu, Junki Min, Minsuk Kim, Markondeya Raj Pulugurtha, Venky Sundaram, and Rao R. Tummala – Georgia Institute of Technology

Room-Temperature Wafer Bonding Using Al/Ti/Au Layers for Integrated Reflectors in the Ultraviolet Spectral Region
Eiji Higurashi, Yutaka Kunimune, and Tadatomo Suga – The University of Tokyo

Slot Waveguide Enhanced Field Confinement by CMOS-Compatible Hybrid Plasmonic Structures
Jing Xiao and Qiqin Wei – Guilin University of Electronic Technology

Ultra-Thin Wireless Power Module with Doubleside Integration of Wireless Inductive Link and Supercapacitors
Chintan Buch, P. Markondeya Raj, Billyde Brown, Himani Sharma, Teng Sun, Kyoung-Sik Moon, Klaus-Jürgen Wolter, Mirbozorgi Seyedabdollah, Maysam Ghovanloo, and Rao Tummala - Georgia Institute of Technology; Hobie Yun and Francesco Carobolante - Qualcomm Technologies, Inc.; Keiji Takemura and Tadashi Takahashi – Nitto Denko Corporation

Optoelectronic Integration with Improved Sensitivity for Microfabricated Optical Magnetometers
Yu Ji, Jintang Shang, Lei Wu, and Qi Gan – Southeast University

Investigation of Differential Twisted-Pairs Implemented on Silicon IPD and High Performance Multilayer Organic Platforms
Hsiao-Wei Chin, Pei-Shuo Lee, Chung-Yi Hsu, Lih-Tyng Hwang, and Tzyy-Sheng Horng – National Sun Yat-Sen University; Cheng-Yu Ho and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

Innovative Electrical-Thermal Co-Design of Ultra High-Q TPV-Based 3D Inductors in Glass Package
Min Suk Kim, Markondeya Raj Pulugurtha, Zihan Wu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology

Electrical and Optical TSVs for High Frequency Photonic Applications
Jochen Kraft, Gerald Meinhardt, Kund Molnar, Thomas Bodner, and Franz Schrank – ams AG

Performance Methodology and Characterization of a Multi-Fiber Expanded Beam Lensed Optical Interconnect
Dirk Schoellner, Jillcha Wakjira, Steven Chuang, and Sharon Lutz – US Conec, Ltd.

RFID Coupled Sensors for Remote Liquid Sample Measurements
Saranraj Karuppuswami, Amanpreet Kaur, Mohd Ifwat Mohd Ghazali, and Premjeet Chahal – Michigan State University

The Effect of Ultra-Fine Pitch RDL Process Variations on Electrical Performance of 2.5D Glass Interposers up to 110 GHz
Chandrasekharan Nair, Hao Lu, Kadappan Panayappan, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology

Fabrication of Freeform Lens Based on Ionic Wind for Chip-on-Board Light-Emitting Diodes
Zefeng Zhang, Jiading Wu, Xing Guo, and Xiang Lei - Huazhong University of Science & Technology; Sheng Liu and Huai Zheng - Wuhan University

Friday, June 3, 2016
Session 41: Student Interactive Presentations
Sponsored by Texas Instruments, Inc.
8:30 AM - 10:30 AM
Committee: Interactive Presentations
Belmont Commons

Session Co-Chairs:
Ibrahim Guven – Virginia Commonwealth University
Michael Mayer – University of Waterloo

Determination of Tracer Diffusivites of Cu atoms and Sn atoms in Cu3Sn Intermetallic Compound by Considering Chemical Effect
Yi-Ting Henry Chen and King-Ning Tu – University of California, Los Angeles; Andriy Gusak – Cherkasy National University

Highly Conductive, Stretchable, Polyurethane/Polyaniline - Based Adhesives for Wearable Electronic Applications
Bo Song, Liyi Li, Chia-Chi Tuan, Yuntong Zhu, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology

Fabrication and Traceable Quality Evaluation of Fine Pitch TSV with Self-Integrated Micro Heater and Thermocouple
Yong Guan, Qinghua Zeng, Jing Chen, Yuan Bian, Xiao Zhong, and Yufeng Jin – Peking University; Yunhui Zhu – Smart Grid Research Institute, State Grid; Shenglin Ma – Xiamen University

Surface Treatment to Enable Low Temperature and Pressure Copper Direct Bonding
Vikas Dubey – KU Leuven; Jaber Derakhshandeh, Carine Gerets, Patrick Laermans, Koen De Leersnijder, Kim Baumans, Kenneth June Rebibis, Andy Miller, Ingrid De Wolf, and Eric Beyne – IMEC

Probe Card Design with Signal and Power Integrity for Wafer-Level Application Processor Test in LPDDR4 Channel
Jinwook Song, Eunjung Lee, Jonghoon Kim, Shinyoung Park, and Joungho Kim – KAIST; Jung Keun Park, Jong Hyun Park, Yoon Hee Bang, Hyun Min Kim, and Young Bu Kim - Will-Technology Co., Ltd.; Seungki Nam - Samsung Electronics Co., Ltd.

Optimized Power Delivery for 3D IC Technology Using Grind Side Redistribution Layers
Menglu Li, King-Ning Tu, and Subramanian Iyer – University of California, Los Angeles; Prakash Periasamy – GLOBALFOUNDRIES

Light Extraction Efficiency Enhancement of Deep-Ultraviolet Light-Emitting Diodes With Nanostructured Silica Glass
Yang Peng, Hao Cheng, Si Min Wang, and Ming Xiang Chen – Huazhong University of Science & Technology

Adhesion Properties of Anisotropic Conductive Films (ACFs) Assembled Chip-In-Flex (CIF) Packages for Wearable Electronics Applications
Ji-Hye Kim, Tae-Ik Lee, Taek-Soo Kim, and Kyung-Wook Paik – KAIST

Study of Sintered Nano-Silver Die Attachment Materials Doped with Indium
Chun-An Yang and C. Robert Kao – National Taiwan University

Design of an on-Interposer Passive Equalizer for High Bandwidth Memory (HBM) with 30 Gbps Data Transmission
Yeseul Jeon, Heegon Kim, Sumin Choi, Youngwoo Kim, and Joungho Kim – KAIST

Measurement of High-Bandwidth and High-Density Silicone Rubber Socket up to 110 GHz
Junyong Park, Hyesoo Kim, Jonghoon J. Kim, and Joungho Kim – KAIST; Dongho Ha and Michael Bae – SRC; Bumhee Bae - Samsung Electronics

Process Development and Characterization for Integrating Microchannel Into TSV Interposer
Yanming Xia, Kuili Ren, Shenglin Ma, Rongfeng Luo, and Jun Yan – Xiamen University; Yufeng Jin and Jing Chen – Peking University

Controlling the Conduction Mechanisms in Isotropic Conductive Adhesives With Silver-Coated Polymer Spheres
Sigurd Rolland Pettersen, Zhiliang Zhang, and Jianying He – Norwegian University of Science and Technology; Keith Redford and Helge Kristiansen – Conpart AS; Susanne Helland and Erik Kalland – Mosaic Solutions AS

Development of New Low Melting Solder Alloys
Chih-Hao Chen and Albert T. Wu – National Central University; Hsiang-Chuan Chen, Boon-Ho Lee, and Chang-Meng Wang – Shenmao Technology, Inc.

Millimeter-Wave Wireless Intra/Inter-Chip Communications in 3D Integrated Circuits Using Through Glass Via (TGV) Disk-Loaded Antennas
Seahee Hwangbo and Yong-Kyu Yoon – University of Florida; Aric Shorey – Corning, Inc.

A Novel Package Feasibility Study Tool for Power Delivery Network Design and Optimization
Lei Zheng, Kevin Cai, Julia Cline, and Arun Vaidyanath – Rambus, Inc.

Signal Integrity Analysis of Bumpless High-Speed Through Silicon Via (TSV) Channel for 2.5D High Bandwidth Memory (HBM)-Based System
Hyunsuk Lee, Heegon Kim, Sumin Choi, Jaemin Lim, Kyungjun Cho, Yeseul Jeon, and Joungho Kim – KAIST

Analysis of Bending Effects for Optical-Bus-Couplers
Lukas Lorenz, Krzysztof Niewegłowski, Klaus-Jürgen Wolter, and Karlheinz Bock – Technical University Dresden

Size-Controllable Copper Nanomaterials for Flexible Printed Electronics
Yu Zhang, Pengli Zhu, Gang Li, Tao Zhao, and Rong Sun – Chinese Academy of Sciences; Chingping Wong – Georgia Institute of Technology

RFID Compatible Wireless Magnetoelastic Sensors for Liquid Sample Measurements
Saranraj Karuppuswami and Premjeet Chahal – Michigan State University; Harikrishnan Arangali – Indian Institute of Technology, Madras

Low Temperature Bonding Between Polyether Ether Ketone (PEEK) and Pt Through Vapor Assisted VUV Surface Modification
Weixin Fu, Shuichi Shoji, and Jun Mizuno – Waseda University; Akitsu Shigetou – National Institute for Material Science

Study of a Novel Amorphous Silicon Temporary Bonding and Corresponding Laser Assisted De-Bonding Technology
Yu-Hsiang Huang, Hao-Wen Liang, Chuan-An Cheng, and Kuan-Neng Chen - National Chiao Tung University; Chien-Hung Lin, Chia-Lin Lee, and Shan-Chun Yang - Kingyoup Optronics Co., Ltd.

Demonstration of Next-generation Au-Pd Surface Finish with Solder-capped Cu Pillars for Ultra-fine Pitch Applications
Ting-Chia Huang, Pulugurtha Markondeya Raj, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Gustavo Ramos, Arnd Kilian, Rick Nichols, and Robin Taylor – Atotech Deutschland GmbH

Microstructural Evolution of Transient Liquid Phase Sinter Joints in High Temperature Environmental Conditions
Hannes Greve, S. Ali Moeini, and F. Patrick McCluskey – University of Maryland; Shailesh Joshi – Toyota Research Institute of North America

Polysiloxane-Based Surface Modification of Nanosilica Fillers for Low Stress Underfill
Chia-Chi Tuan, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology

Embedded Passive RF Tags towards Intrinsically Locatable Buried Plastic Materials
Mohd Ifwat Mohd Ghazali, Saranraj Karuppuswami, and Premjeet Chahal – Michigan State University

Electrical Comparison between TSV in Silicon and TPV in Glass for Interposer and Package Applications
Jialing Tong, Kadppan Panayappan, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology

High Performance 3D Glass-Embedded Inductors Fabricated by a Glass Reflow Process
Mingai Zhang, Jintang Shang, and Bin Luo – Southeast University

Self-Actuating 3D Printed Packaging for Shape-Changing Antenna Arrays
Ryan Bahr, Taoran Le, Bo Song, Ching-Ping Wong, and Manos Tentzeris – Georgia Institute of Technology

Technology Corner Exhibits

Wednesday, June 1: 9:00 a.m. - Noon & 1:30 p.m. - 6:30 p.m.
Thursday, June 2: 9:00 a.m. - Noon & 1:30 p.m. - 4:00 p.m.

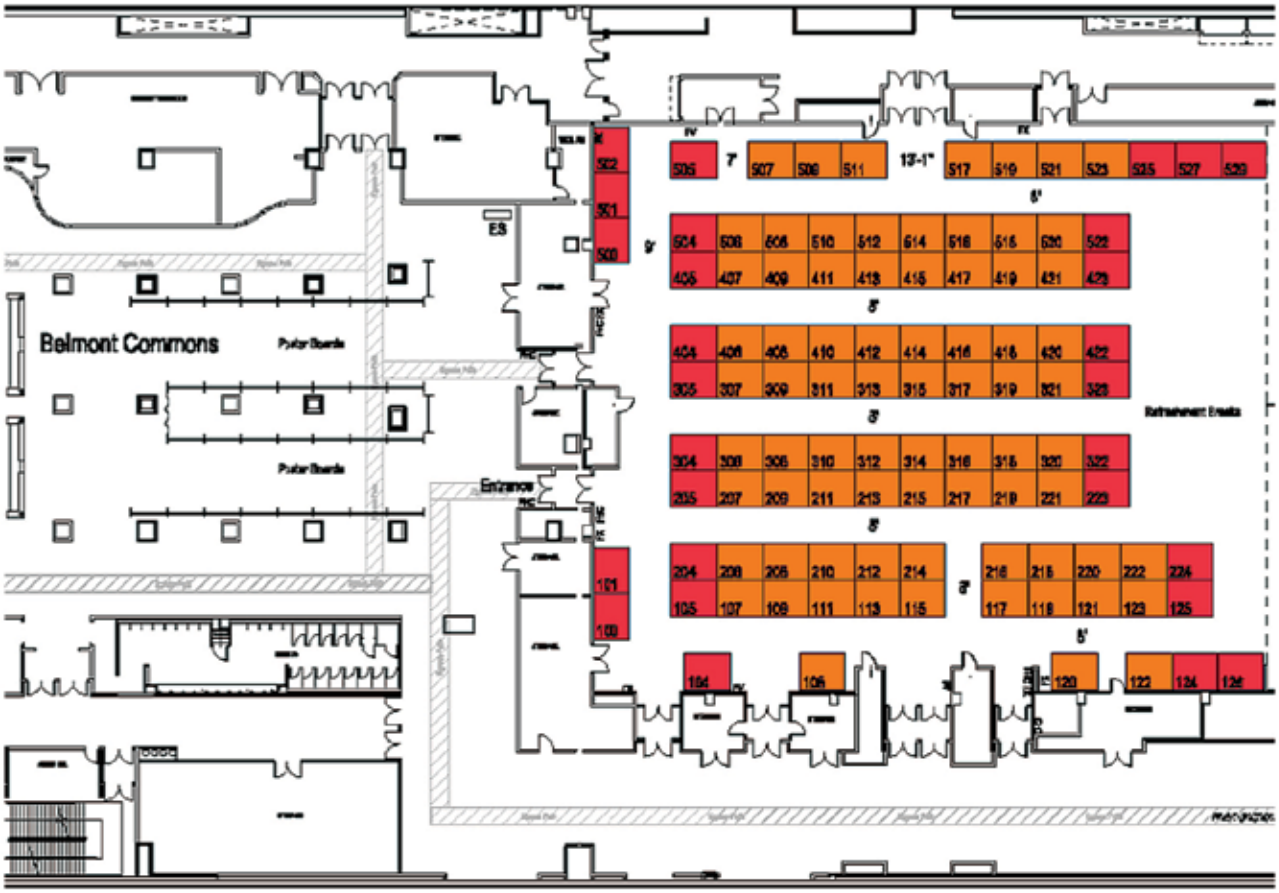
Interactive Presentation Sessions

Location: Belmont Commons

Wednesday, June 1
Session 37: 9:00 a.m. - 11:00 a.m.
Session 38: 2:00 p.m. - 4:00 p.m.

Thursday, June 2
Session 39: 9:00 a.m. - 11:00 a.m.
Session 40: 2:00 p.m. - 4:00 p.m.

Friday, June 3
Session 41: 8:30 a.m. - 10:30 a.m.



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Invensas Corporation a wholly owned subsidiary of Tessera Technologies, Inc. (TSRA) is a provider of world-leading integrated Circuit interconnect and bonding solutions for the global electronics industry. Our technologies and solutions can be found in high-volume production at leading original equipment makers (OEMs), original design manufacturers (ODMs), and integrated device manufacturers (IDMs). Invensas BVA provides advanced package-on-Package (PoP) solutions targeting mobile computing and communications applications, while the Invensas xFD technology is at the heart of advanced memory stacking solutions for data center and storage markets. Following the acquisition last year of Ziptronix, Invensas now also offer industry leading Invensas ZiBond® direct bonding and Invensas DBI® hybrid bonding technologies. These wafer-to-wafer and die-to-wafer bonding processes are in high volume production today, and are set to further accelerate broad adoption of 2.5D/3D IC architectures in high performance, Image Sensor, MEMS, Sensors, RF, System-in-Package devices for computing and consumer electronics products.

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Kingyoup Optronics (KYO) and IBM have a JDA to develop innovative 2.5D/3D IC Temporary Bonding and De-bonding systems. The system with IBM IP coverage is much faster throughput and higher yield with competitive CoO and compatible with various qualified materials. Currently 355nm glass carrier laser de-bonding system has been successful to be applied in High Density Fan out process in industry. It also can be applied in panel fan out process. The innovative Si carrier laser de-bonding system is in development with IBM. The result looks very promising. Besides semiconductor equipment, KYO provides turnkey solutions for in-line and roll to roll sputtering equipment for FPD, TP (Touch Panel), graphene applications etc. Please contact us for further information.

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Lasertec Corporation, founded in 1960, has grown into a world leading innovator of inspection and metrology equipment serving the global semiconductor and related industries. Guided by its corporate philosophy, "Create unique solutions; Create new value," Lasertec has created several new tools to help companies developing and manufacturing the next generation of semiconductors – 3DICs with TSV technology. Tools being highlighted at ECTC 2016 are the BGM300, BIM300, and the EZ300. The BGM300 is an IR based metrology tool capable of measuring all the critical depths/thicknesses needed for wafer specific grind, polish and etch process optimizing to enable the highest yielding TSV wafers. The BIM300 is based on Lasertec's proprietary confocal optics and is an ideal solution for measuring and inspecting revealed vias, bumps and other critical elements found throughout the TSV wafer finishing. The EZ300, an edge inspection and analysis system, is the latest addition to Lasertec's product portfolio and provides unmatched analysis capability on wafer edge issues.

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Nitto, Inc. is a global supplier of materials and equipment for semiconductor manufacturing, represented by the following products: ELEP holder tapes for back-grinding and dicing; high temperature resistant masking tape; NEL machines (Taper/Detaper/ Wafer Mounter with or without peeling function/ UV machine) for thin wafer application; ELEPMOUNT (2-in-1: DAF+Dicing Tape conductive/non-conductive) for thin stacked chip package; REVALPHA thermal-release tape for various applications, such as dicing, grinding and MLCC production process; clear molding compound and sheet encapsulating resin.

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Nordson DAGE is the market leading provider of award winning wire pull, ball and die shear test systems along with X-Ray and AOI inspection systems. They are recognized as the industry standard. The recently released 4800 bond tester brings the latest developments in automated wafer testing technology to users testing wafers from 100mm to 450mm in diameter. When combined with an integrated wafer handling device the system can test multiple wafers consecutively. Additionally, the multi-function cartridge (MFC) can be used for automated application changing within a test pattern or simply very quick cartridge changes in manual operation. Automation on non-wafer samples can also be conducted on the 2nd Generation 4000Plus which performs shear tests up to 200kg, pull tests up to 100kg and push tests up to 50kg. The all-purpose 4000 and 4000 Optima systems are capable of manual pull testing up to 50kg and shear tests to 200kg with accuracies up to 0.1% as standard. Paragon software offers ease of use and intelligent automated testing with a focus on user experience. The 4000HS high speed bond tester is used for pull and shear testing of solder spheres to identify brittle fractures at speeds up to 4m/sec in shear and 1.3m/sec pull.

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SavanSys is the industry standard choice for electronics manufacturing cost modeling. The company began in the mid-nineties with a focus on multi-chip module and PCB fabrication and assembly before expanding into electronics packaging. SavanSys provides both cost modeling services and software products and maintains an extensive library of manufacturing activity costs. Projects range from multi-year ventures focused on detailed supply chain modeling to one-time projects comparing a new technology to the current industry standard. All SavanSys projects and products use activity based cost modeling, which is a bottom-up approach to cost that aggregates individual cost contributors (labor, material, throughput, equipment cost, etc.) for every step in a process flow.

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Senju Comtek Corp. is an American subsidiary of Senju Metal Industry Co. (SMIC) of Tokyo, Japan. Senju is a global leader in solder materials and related processing equipment with over two dozen manufacturing, technical, and sales support facilities located around the world. Senju Comtek has two solder paste manufacturing locations in USA (San Jose, CA and Chicago, IL) supporting a wide range of products for the semiconductor and PCBA industries.

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Abstracts may be submitted related to any of the nine major program committee topics listed above. Interactive presentations of technical papers are highly encouraged at ECTC as it allows significant interaction between the presenter and attendees. It is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to submit an abstract of no more than 750 words that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net.

If you have any questions, contact:
Mark Poliks, 67th ECTC Program Chair
Binghamton University, Watson School of Engineering & Applied Science,
PO Box 6000, Binghamton, NY 13902-6000, USA
Phone: +1-607-777-5361
E-mail: mpoliks@binghamton.edu

Abstracts must be received by October 10, 2016. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number, and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses
In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 10, 2016.

If you have any questions, contact:
Kitty Pearsall
67th ECTC Professional Development Courses Chair
Boss Precision, Inc.
1806 W. Howard Lane, Austin, TX 78728, USA
Phone: +1-512-845-3287
E-mail: kitty.pearsall@gmail.com

IEEE 67th Electronic Components & Technology Conference

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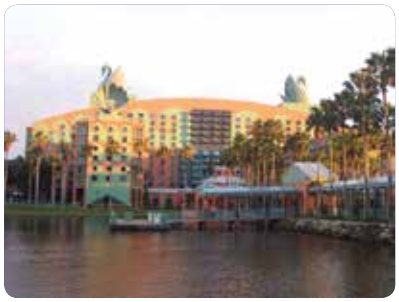

The fun and splendor of Walt Disney World and the greater Orlando area awaits you in 2017. In the heart of the Walt Disney World® Resort, the award-winning Walt Disney World Swan and Dolphin Resort is your gateway to Central Florida's greatest theme parks and attractions. The resort is located in between Epcot® and Disney's Hollywood Studios™, and nearby Disney's Animal Kingdom® Theme Park and Magic Kingdom® Park. Come discover our 17 world-class restaurants and lounges, sophisticated guest rooms with Westin Heavenly Beds® and the luxurious Mandara Spa. Enjoy five pools, two health clubs, tennis, nearby golf, and many special Disney benefits, including complimentary transportation to Walt Disney World Theme Parks and Attractions, and the Extra Magic Hours benefit.

Just minutes from the Walt Disney World Swan and Dolphin Resort is Downtown Disney's West Side and Marketplace. Downtown Disney's West Side showcases top-notch restaurants, a 24-screen AMC Pleasure Island movie theater, and other uncommon shops. Here you'll also find the exquisite Cirque du Soleil La Nouba live entertainment show and the DisneyQuest Indoor Interactive theme park.

Downtown Disney Marketplace provides an appealing place to take a break from Disney Theme Parks and Water Parks. Check out the largest Disney character store in the world. Or, for more of a respite, relax and dine at a lakeside restaurant.

Should you decide to explore outside the Greater Lake Buena Vista area, Orlando boasts other parks and recreation areas tailor made for whatever your pleasure. Favorites include Universal Orlando, SeaWorld, Gatorland, and Winter Park.

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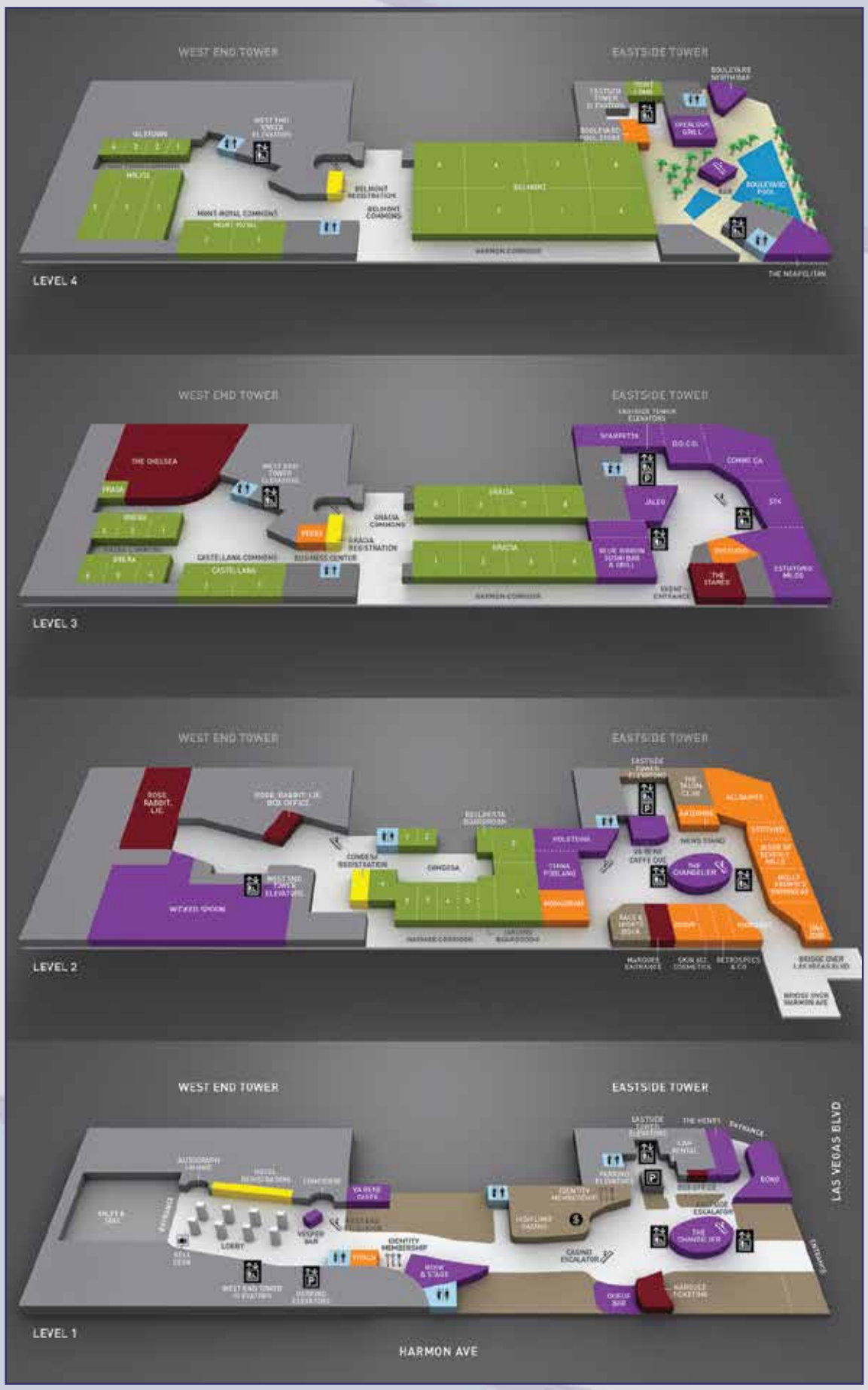

Conference At A Glance

MONDAY
May 30, 2016

3:00 p.m. – 5:00 p.m.
Registration
Belmont Commons, 4th Floor

TUESDAY
May 31, 2016

6:45 a.m. – 5:00 p.m.
Registration
Belmont Commons, 4th Floor
6:45 a.m. – 8:15 a.m.
Morning PDC Registration Only

7:00 a.m. – 7:45 a.m.
PDC Instructors and Proctors
Briefing & Breakfast
Belmont 3

7:00 a.m. – 5:00 p.m.
Speaker Preparation
Yaletown 3

8:00 a.m. – Noon
Morning PDCs
See page 8 for locations

8:00 a.m. – 5:00 p.m.
CPMT Heterogeneous Integration Technology Roadmap Workshop
Condesa 2

9:00 a.m. – 5:00 p.m.
iNEMI Meeting
Castellanna 1, 3rd Floor
By invitation only

10:00 a.m. – 11:30 a.m.
ECTC Special Session
Condesa 3

10:00 a.m. – 10:20 a.m.
Morning PDC Break
Mont-Royal Commons and Outside Belmont 4 & 8

Noon
PDC Luncheon
Belmont 3 & 7

1:00 p.m. – 5:00 p.m.
Technology Corner Setup
Belmont 1, 2, 5 & 6

1:15 p.m. – 5:15 p.m.
Afternoon PDCs
See page 8 for locations

2:00 p.m. – 3:30 p.m.
Optoelectronics Special Session
Condesa 3

3:00 p.m. – 3:20 p.m.
Afternoon PDC Break
Mont-Royal Commons and Outside Belmont 4 & 8

5:00 p.m. – 6:00 p.m.
ECTC Student Reception
Condesa 5 & 6

6:00 p.m. – 7:00 p.m.
General Chair's Speakers Reception
Blvd. Pool North Center Bar
Backup: Belmont 3 & 7
By invitation only

7:30 p.m. – 9:00 p.m.
ECTC Panel Session
Mont-Royal 1 & 2

WEDNESDAY
June 1, 2016

6:45 a.m. – 4:00 p.m.
Conference Registration
Belmont Commons, 4th Floor

7:00 a.m. – 7:45 a.m.
Today's Speakers Breakfast
Belmont 3

7:00 a.m. – 5:00 p.m.
Speaker Preparation
Yaletown 3

8:00 a.m. – 11:40 a.m.
Sessions 1, 2, 3, 4, 5, 6
See pages 10–11 for Locations

9:00 a.m. – 11:00 a.m.
Session 37: Interactive Presentations 1
Belmont Commons

9:00 a.m. – Noon
Technology Corner Exhibits
Belmont 1, 2, 5 & 6

9:15 a.m. – 10:00 a.m.
Refreshment Break
Belmont 1, 2, 5 & 6

Noon
ECTC Luncheon
Belmont 3 & 4

1:30 p.m. – 6:30 p.m.
Technology Corner Exhibits
Belmont 1, 2, 5 & 6

1:30 p.m. – 5:10 p.m.
Sessions 7, 8, 9, 10, 11, 12
See pages 12–13 for Locations

2:00 p.m. – 4:00 p.m.
Session 38: Interactive Presentations 2
Belmont Commons

2:45 p.m. – 3:30 p.m.
Refreshment Break
Belmont 1, 2, 5 & 6

5:30 p.m. – 6:30 p.m.
Technology Corner Reception
Belmont 1, 2, 5 & 6

6:30 p.m. – 7:30 p.m.
CPMT Women's Panel & Reception
Nolita 1

7:30 p.m. – 9:00 p.m.
ECTC Plenary Session
Mont-Royal 1 & 2

THURSDAY
June 2, 2016

7:00 a.m. – 5:00 p.m.
Speaker Preparation
Yaletown 3

7:00 a.m. – 7:45 a.m.
Today's Speakers Breakfast
Belmont 3

7:30 a.m. – 4:00 p.m.
Conference Registration
Belmont Commons, 4th floor

8:00 a.m. – 11:40 a.m.
Sessions 13, 14, 15, 16, 17, 18
See pages 14–15 for Locations

9:00 a.m. – 11:00 a.m.
Session 39: Interactive Presentations 3
Belmont Commons

9:00 a.m. – Noon
Technology Corner Exhibits
Belmont 1, 2, 5 & 6

9:15 a.m. – 10:00 a.m.
Refreshment Break
Belmont 1, 2, 5 & 6

Noon
CPMT Luncheon
Belmont 3, 4, 7 & 8

1:30 p.m. – 4:00 p.m.
Technology Corner Exhibits
Belmont 1, 2, 5 & 6

1:30 p.m. – 5:10 p.m.
Sessions 19, 20, 21, 22, 23, 24
See pages 16–17 for Locations

2:00 p.m. – 4:00 p.m.
Session 40: Interactive Presentations 4
Belmont Commons

2:45 p.m. – 3:30 p.m.
Refreshment Break
Belmont 1, 2, 5 & 6

6:30 p.m. – 7:30 p.m.
66th ECTC Gala Reception
Belmont 3, 4, 7 & 8

8:00 p.m. – 9:30 p.m.
CPMT Seminar
Mont-Royal 1 & 2

FRIDAY
June 3, 2016

7:00 a.m. – 5:00 p.m.
Speaker Preparation
Yaletown 3

7:00 a.m. – 7:45 a.m.
Today's Speakers Breakfast
Belmont 3

7:30 a.m. – Noon
Conference Registration
Belmont Commons, 4th Floor

8:00 a.m. – 11:40 a.m.
Sessions 25, 26, 27, 28, 29, 30
See pages 18–19 for Locations

8:30 a.m. – 10:30 a.m.
Student Interactive Presentation Session
Belmont Commons

9:15 a.m. – 10:00 a.m.
Refreshment Break
Mont-Royal Commons

Noon
ECTC Program Chair Luncheon
Belmont 3 & 4

1:30 p.m. – 5:10 p.m.
Sessions 31, 32, 33, 34, 35, 36
See pages 20–21 for Locations

2:45 p.m. – 3:30 p.m.
Refreshment Break
Mont-Royal Commons

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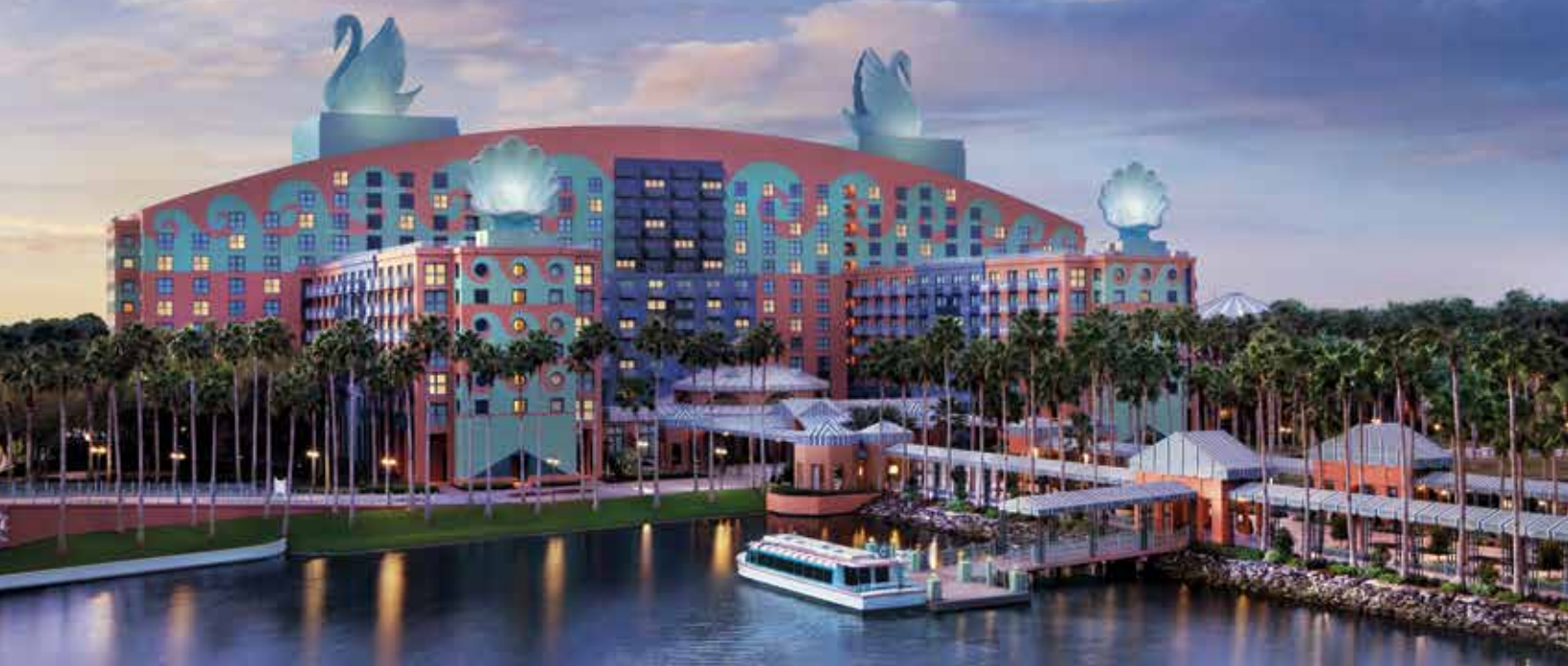

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