Conference Program & Exhibitor Listings

Don't miss out on electronic packaging's premier conference!

ECTC 2017

The 67th Electronic Components and Technology Conference

May 30 - June 2, 2017

Walt Disney World Swan & Dolphin Resort
Lake Buena Vista, Florida, USA

For more information, visit: www.ectc.net

Program Supported by:

ASE GROUP

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CPMT IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

IEEE

WELCOME FROM THE MAYOR OF ORANGE COUNTY

Orange County Mayor
Teresa Jacobs

P.O. Box 1393
201 South Rosalind Ave, 5th Floor
Orlando, FL 32802-1393
Phone: 407-836-7370
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Mayor@ocfl.net

May 2017

Greetings!

As Mayor of Orange County, it is my pleasure to welcome you to IEEE Electronic Components and Technology Conference 2017. We are honored that you chose the beautiful Walt Disney World Swan & Dolphin Hotel to host you event.

As you enjoy your time in Central Florida, I encourage you to see everything that our region has to offer. You will quickly discover why we continue to be the number one vacation destination in the nation with more than 66 million visitors in 2015. With our beautiful "Florida sunshine" providing the backdrop, you can discover our exciting theme parks, great cities and towns, excellent shopping opportunities, and relaxing parks and recreational amenities while experiencing superior hospitality and welcoming residents. These reasons, among many more, make Orange County a great place to live, work, and raise a family.

Our region is also home to top rated higher education institutions, the second largest convention center in the nation, and a burgeoning community of biotech, life sciences and research facilities, which have been recognized around the world for its forward thinking success. We are very proud of being a major international destination.

I wish you much success for your annual conference and hope that you enjoy your time here!

Sincerely,

Teresa Jacobs

WELCOME FROM 67th ECTC GENERAL AND PROGRAM CHAIRS

On behalf of the Program Committee and Executive Committee, it is our pleasure to welcome you to the IEEE 67th Electronic Components and Technology Conference (ECTC), held at the beautiful Walt Disney World Swan & Dolphin Resort, Lake Buena Vista, Florida, from May 30 to June 2, 2017. All ECTC meetings and events will be taking place in the Dolphin building of the resort. This premier international conference of the global microelectronic packaging industry is sponsored by the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society.

The ECTC Program Committee has selected 335 papers that will be presented in 36 oral sessions and five interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as flip chip packaging, 3D/TSV technologies, wafer level packaging, design for RF performance and signal/power integrity, thermal and mechanical modeling, optoelectronics packaging, and materials and reliability. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from 22 countries are expected to present their work at the 67th ECTC, covering ongoing technological challenges with established disciplines or emerging topics of interest for our industry, such as additive manufacturing, heterogeneous integration, and flexible and wearable electronics.

ECTC will also feature panel and special sessions with industry experts covering a number of important and emerging topic areas. On Tuesday, May 30 at 10 a.m., Vikas Gupta and Pradeep Lall will chair a session on "Material and Package Reliability Needs/Challenges for Harsh Environments." That same day at 2 p.m., Bing Dang will chair a panel session on "Flexible Hybrid Electronics – Electronics Outside the Box," where a panel of experts will discuss how innovation in device integration and packaging will bring together thinned silicon die with printed components to deliver electronics that conform to the shape of the human body and vehicles. Tuesday evening will also include the ECTC Panel Session at 7:30 p.m. on "Panel Fan-Out Manufacturing: Why, When, and How?" chaired by CPMT President Jean Trewhella and Young Gon Kim.

Babak Sabi, Corporate Vice President and Director of Assembly and Test Technology Development, Intel Corporation, will be giving the invited keynote talk on "Advanced Packaging Opportunities and Challenges" at the ECTC Luncheon on Wednesday, May 31. Later that day and continuing to build on the success of the first-ever CPMT Women's Panel and Reception held at the 65th ECTC two years ago, this year's conference will also feature a panel discussion chaired by Kitty Pearsall on Wednesday, May 31, at 6:30 p.m. on "Emotional Intelligence (EI) – Link to Successful Leadership," with participation from distinguished women leaders and technologists in our industry. All conference attendees are invited. Also on Wednesday at 7:30 p.m., Luke England will chair the ECTC Plenary Session titled "Packaging for Autonomous Vehicle Electronics," featuring key technologists sharing their views on the evolutionary requirements for packaging and reliability challenges to support widespread implementation of self-driving vehicles on the road. On Thursday, June 1 at 8 p.m., the CPMT Seminar titled "3D Printing Tools, Technologies and Applications," will be moderated by Venkatesh Sundaram and Yasumitsu Orii from the High-Density Substrates & Boards Technical Committee of the CPMT Society.

Supplementing the technical program, ECTC also offers several Professional Development Courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE ITherm Conference this year, the 67th ECTC will offer 18 PDCs, organized by the PDC Committee chaired by Kitty Pearsall. The PDCs will take place on Tuesday, May 30, and are taught by distinguished experts in their respective fields. The Technology Corner will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than 100 Technology Corner exhibits will be open starting at 9 a.m. on Wednesday and Thursday. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a scientist, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. We would like to take this opportunity to thank all our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, program committee members, as well as all the volunteers who have helped to make the 67th ECTC another resounding success. Once again, thank you for being a part of the 67th ECTC.

Henning Braunisch
General Chair
Intel Corporation

Mark D. Poliks
Program Chair
Binghamton University

WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of CPMT, it is my great pleasure and privilege to welcome you to the 67th ECTC in Lake Buena Vista, Florida at the spectacular Walt Disney World Swan & Dolphin Resort!

The ECTC held its opening night 66 years ago and it hasn't missed a single year yet! Today, ECTC has become the premier international conference where professionals not only get a close-up look at every side of our industry, but also share research and development in technological breakthroughs across a wide range of semiconductor packaging, electronics devices, design, materials, manufacturing, and modeling.

The CPMT Society is proud to be a sponsor of ECTC and present these program highlights:

- Opening Day: Tuesday, May 30, in addition to the ever popular Professional Development Courses there will be two special sessions: "Material and Package Reliability Needs/Challenges for Harsh Environments" chaired by Vikas Gupta and Pradeep Lall and "Flexible Hybrid Electronics – Electronics Outside the Box" chaired by Bing Dang. In the evening I will co-chair the ECTC CPMT Panel Session together with Young Gon Kim at 7:30 p.m. on "Panel Fan-Out Manufacturing: Why, When, and How?" Tuesday's program highlights the breadth and depth that ECTC delivers each year.
- To encourage diversity, networking, and professional development, CPMT will host a Women's Panel and Reception Wednesday at 6:30 p.m. on "Emotional Intelligence – Link to Successful Leadership," chaired by Kitty Pearsall. All conference attendees are invited. CPMT will continue the women's networking tables during the Wednesday and Thursday luncheons.
- On Thursday, June 1, CPMT will sponsor an award luncheon session to present several prestigious IEEE and CPMT awards.
- After the traditional Gala reception on Thursday evening the CPMT High-Density Substrates & Boards technical committee will host the seminar "3D Printing Tools, Technologies and Applications," moderated by Venkatesh Sundaram and Yasumitsu Orii.

Friday will feature sessions on topics that range from the reliability of fan-out WLP, automotive electronics and power module packaging to processing for 3D integration – all showing cutting edge advances in these critical areas.

Lastly I would like to take this opportunity to thank our dedicated volunteers on the ECTC program committee for their hard work over the past year. Also, appreciation goes to the session chairs, authors, speakers, and exhibitors who are instrumental to making the 67th ECTC a great success. As always I look forward to the impact all these technical and networking events will make on the CPMT Society, our industry, and our members.

Here's to four fast paced days of in-depth analysis, peer debate, and network expansion!

Jean Trewhella, President, IEEE CPMT Society

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, meals, Technology Corner exhibits and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. Hotel "house" phones have been placed throughout the hotel and conference area for your convenience. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
Smoking is NOT permitted in the hotel. Please follow hotel policies and signs regarding this. Smoking is also NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, and / or seminars. Thank you for your consideration and cooperation.

Recording presentations via photos or video is prohibited.

ECTC Mobile App

ECTC is pleased to announce that a **free mobile app** is available again this year. The app provides information on schedules for our technical program and PDCs as well as exhibitors, sponsors, and general conference information and venue maps. The app also features tools to set your schedule so you don't miss presentations important to you, social interaction functions, and the ability to provide ratings on presentations that are used in selecting candidates for best paper awards. The app is available for iOS and Android devices from their respective app stores by searching "2017 ECTC". Look for login and password information on signage at ECTC! **All Oral Session Paper Ratings this year will be received only through this Mobile App.**

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Conference organizers reserve the right to cancel or change this program without prior notice.

ECTC Luncheon Keynote Speaker

Wednesday, May 31, 2017
12:00 Noon
Northern Hemisphere D-E

Advanced Packaging Opportunities and Challenges

Presenter: Babak Sabi, Corporate Vice President and Director of Assembly and Test Technology Development, Intel Corporation

Industry reliance on advanced packaging has been accelerating over the last few years. This trend is expected to continue in the future. Heterogeneous integration of multiple chips in a package supports Moore's Law scaling and is driving many challenges in package interconnect scaling, design environment, optical integration, electrical/thermal performance, and test. Babak Sabi, Corporate Vice President and Director of Assembly and Test Technology Development at Intel Corporation, will address future challenges and opportunities for advanced multi-chip packaging.

Since 2009, Babak has been responsible for Intel's packaging, assembly process, packaging materials, enabling technology, and test technology development. Prior to leading Assembly and Test Technology Development, Babak led the Corporate Quality Network within Intel's Technology and Manufacturing Group from 2002 to 2009. He also led a company-wide network of quality and reliability organizations responsible for product reliability, customer satisfaction, and quality business practices. Previously, Babak managed technology development quality and reliability, and was responsible for silicon technology certification, assembly, test, and board processes. Babak joined Intel in 1984, the same year he received his Ph.D. in solid state electronics from The Ohio State University.

IEEE CPMT Heterogeneous Integration Technology Roadmap Workshop

Tuesday, May 30, 2017 • 8:00 a.m. - 5:00 p.m.
Europe 4, Lobby Level

Our Industry has reinvented itself through multiple disruptive changes in technologies, products and markets. With the rapid migration of logic, memory and applications to the cloud infrastructures, the internet of things (IoT) to internet of everything (IOE), smart devices every where, and autonomous automotive, the pace of innovation is increasing to meet these challenges.

The Heterogeneous Integration Technology Roadmap (HIR), is sponsored by the IEEE CPMT Society, the Electron Devices Society (EDS), and Photonics Society together with SEMI and ASME EPPD. It will address the future directions of heterogeneous integration technologies and applications serving the future markets and applications, so very crucial to our societies' fields of interest and to our industries and academic and research communities. In addition to HIR, two other roadmaps are under development within IEEE: International Technology Roadmap for Wide Band-Gap Semiconductors (ITRW) sponsored by the IEEE Power Electronics Society (PELS), and International Technology Roadmap for Devices & Systems (IRDS), an IEEE Standards Association Industry Connection Program sponsored by the Rebooting Computing Initiative. Collaboration is underway to harmonize across the three roadmaps.

This HIR is our technology roadmap. The workshop will be held at the 2017 ECTC conference. We invite all the ECTC participants to attend this important working session for our profession and for our industry. The workshop is open to all. Registration is not necessary. There is no fee for attendance.

iNEMI Technical & Research Committee Meeting

Tuesday, May 30, 2017
9:30 a.m. - 5:30 p.m. • Oceanic 1- Lobby Level

By Invitation Only

REGISTRATION, RECEPTIONS AND GENERAL INFORMATION

Registration

ECTC registration will be open at the ECTC Registration Desk located in the Walt Disney World DOLPHIN Resort, Conference Center, Lobby Level, outside of Australia 3.

Monday, May 29, 2017 • 3:00 p.m. – 5:00 p.m.

Tuesday, May 30, 2017 • 6:45 a.m. – 8:15 a.m.*
(AM PD Courses & Special Session only)*

Tuesday, May 30, 2017 • 8:15 a.m. – 5:00 p.m.
(All conference attendees)

Wednesday, May 31, 2017 • 6:45 a.m. – 4:00 p.m.

Thursday, June 1, 2017 • 7:30 a.m. – 4:00 p.m.

Friday, June 2, 2017 • 7:30 a.m. – 12:00 Noon

The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45am start time on Tuesday, May 30 as registration becomes very congested prior to the start of morning Professional Development Courses.

Door Registration Fees

Door Registration with Proceedings on USB drive

IEEE Member JOINT Registration (full ECTC + ITHERM conference)	$1100
IEEE Member Full Registration	$835
IEEE Member Speaker / Session Chair	$730
IEEE Member One Day	$550
IEEE Member Speaker One Day	$415
Exhibit Booth Attendant	$0
Non-Member JOINT Registration (full ECTC + ITHERM conference)	$1310
Non-Member Full Registration	$1025
Non-Member Speaker / Session Chair	$730
Non-Member One Day	$550
Non-Member Speaker One Day	$415
Exhibit Booth Attendant	$0
Student	$315
Student Speaker	$315
Exhibits Only	$25

Tuesday Professional Development Courses
IEEE Members and Non-Members

Tuesday AM or PM Course with Luncheon	$500
Tuesday All-Day Courses with Luncheon	$710
Tuesday Student All-Day Courses with Luncheon	$130
Extra Luncheon Tickets for Each Day	$65
Extra Proceedings with Registration	$100

Professional Development Course Instructors Breakfast

PDC Instructors and Proctors are required to attend a briefing breakfast.

7:00 a.m. Tuesday – PDC Instructors and Proctor Briefing
(Room Location: Asia 1, Lobby Level)

Session Chairs and Speakers Breakfast

Session Chairs and speakers are required to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Microsoft Windows and Office.

7:00 a.m. Wednesday thru Friday
(Room Location: Northern Hemisphere E 3 & 4, 5th floor)

Speaker Prep Room

Speakers should prepare and review their digital presentations within the allotted times below:

7:00 a.m. – 5:00 p.m., Tuesday – Friday
(Room Location: Europe 2, lobby level)

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

MISCELLANEOUS INFORMATION

Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Message Center
Please use the hotel switchboard or the ECTC Registration Desk, located on the lobby level in the Australia 3 Foyer, to leave and pickup messages. The hotel phone number is +1 (407) 934-4000.

Press Room
Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eric.perfecto@globalfoundries.com or +1 (845) 475-1290.

LUNCHEONS

Tuesday, May 30, 2017
12:00 Noon
(Northern Hemisphere D / DE Corridor, 5th floor)
The Electronic Components and Technology Conference will sponsor a luncheon for all Professional Development Courses attendees, proctors and PDC committee members.

Wednesday, May 31, 2017
12:00 Noon
(Northern Hemisphere D & E, 5th floor)
The Electronic Components and Technology Conference will sponsor a luncheon for conference attendees. Best and Outstanding Papers will be awarded. The guest speaker will be Babak Sabi, Corporate Vice President and Director of Assembly and Test Technology Development, Intel Corporation.

Thursday, June 1, 2017
12:00 Noon
(Northern Hemisphere D & E, 5th floor)
The IEEE Components, Packaging and Manufacturing Technology Society will sponsor a luncheon for conference attendees. The CPMT awards will be presented.

Friday, June 2, 2017
12:00 Noon
(Northern Hemisphere D & E, 5th floor)
The ECTC Program Chair will sponsor a luncheon for conference attendees. You won't want to miss it!

There will be a raffle for attendees.

2017 ECTC SESSIONS & SEMINARS – Open to all conference attendees

2017 APPLIED RELIABILITY SPECIAL SESSION

Material and Package Reliability Needs/Challenges for Harsh Environments

Tuesday, May 30, 2017
10:00 a.m. – 11:30 a.m.
Southern Hemisphere I, 5th Floor

Chairs: Vikas Gupta - Texas Instruments, Inc. and Pradeep Lall - Auburn University

Speakers:
1. Robert Smith, Boeing Research & Technology
2. Przemyslaw Jakub Gromala, Bosch
3. Steve Dunford, Schlumberger
4. Anton Z. Miric, Heraeus Deutschland GmbH & Co. KG
5. Nancy Stoffel, General Electric
6. Varughese Mathew, NXP Semiconductors

2017 ECTC SPECIAL SESSION

Flexible Hybrid Electronics – Electronics Outside the Box

Tuesday, May 30, 2017
2:00 p.m. – 3:30 a.m.
Southern Hemisphere I, 5th Floor

Chair: Bing Dang - IBM Corporation

Speakers:
1. Benjamin Leever, Air Force Research Laboratory, Materials & Manufacturing Directorate
2. James L. Zunino, U.S. Army RDECOM ARDEC
3. Robert Smith, Boeing Research & Technology
4. Girish Wable, Jabil
5. John Knickerbocker, IBM Corporation

2017 ECTC PANEL SESSION

Panel Fan-Out Manufacturing: Why, When, and How?

Tuesday, May 30, 2017
7:30 p.m. – 9:00 p.m.
Southern Hemisphere II & III, 5th Floor

Chairs: Jean Trewhella, CPMT President - GLOBALFOUNDRIES and Young Gon Kim - Integrated Device Technology

Speakers:
1. Douglas Yu, TSMC
2. Tim Olson, DECA
3. Steffen Kroehnert, NANIUM
4. Rolf Aschenbrenner, IZM Fraunhofer
5. Steve Bezuk, Qualcomm Technologies, Inc.

2017 CPMT WOMEN'S PANEL AND RECEPTION

Emotional Intelligence (EI) – Link to Successful Leadership

Wednesday, May 31, 2017
6:30 p.m. – 7:30 p.m.
Southern Hemisphere IV, 5th Floor

Chair: Kitty Pearsall - Boss Precision, Inc.

Speakers:
1. Joanne Martin, JLM Consulting, LLC and former Vice President, IBM Corporation
2. Rozalia Beica, Global Director New Business Development, The Dow Chemical Company
3. Tanja Braun, Deputy Group Manager, Fraunhofer Institute for Reliability and Microintegration IZM

2017 ECTC PLENARY SESSION

Packaging for Autonomous Vehicle Electronics

Wednesday, May 31, 2017
7:30 p.m. – 9:00 p.m.
Southern Hemisphere II & III, 5th Floor

Chair: Luke England - GLOBALFOUNDRIES

Speakers:
1. Application and Market Projections – Venky Sundaram,Georgia Institute of Technology
2. Powertrain Electronics – Brent Richardson, Texas Instruments
3. Sensors – Frank Bertini, Velodyne
4. Data Processing – Dongji Xie, Nvidia
5. Wireless Communication – Raj Pendse, Qualcomm Technologies, Inc.

2017 CPMT SEMINAR

3D Printing Tools, Technologies and Applications

Thursday, June 1, 2017
8:00 p.m. – 9:30 p.m.
Southern Hemisphere II & III, 5th Floor

Chairs: Venky Sundaram - Georgia Institute of Technology and Yasumitsu Orii - Nagase, Japan

Speakers:
1. Manos Tentzeris, Georgia Institute of Technology
2. Humair Mandavia, Zuken SOZO Center
3. Simon Fried, Nano Dimension Ltd.
4. Takeshi Sato, Fuji Machine Mfg. Co., Ltd.

PROFESSIONAL DEVELOPMENT COURSES • TUESDAY, MAY 30, 2017

All courses take place on the 5th floor unless otherwise noted.

Morning Courses 8:00 a.m. – 12:00 Noon	Afternoon Courses 1:30 p.m. – 5:30 p.m.
Northern Hemisphere E1 **1. Achieving High Reliability of Lead-Free Solder Joints – Material Considerations** *Course Leader: Ning-Cheng Lee – Indium Corporation*	**Northern Hemisphere E1** **10. Flip Chip Technologies** *Course Leaders: Eric Perfecto – GLOBALFOUNDRIES; Shengmin Wen – Synaptics Inc.*
Northern Hemisphere E2 **2. Wafer Level Chip Scale Packaging** *Course Leader: Luu Nguyen – Texas Instruments, Inc.*	**Northern Hemisphere E2** **11. Package Failure Analysis – Failure Mechanisms and Analytical Tools** *Course Leaders: Rajen Dias – Amkor Technology and Deepak Goyal – Intel Corporation*
Northern Hemisphere E3 **3. LED Packaging, System, and Reliability Considerations** *Course Leader: Xuejun Fan – Lamar University*	**Northern Hemisphere E3** **12. 3D IC Integration and 3D IC Packaging** *Course Leader: John Lau – ASM Pacific Technology Ltd.*
Northern Hermisphere E4 **4. Future of Device and Systems Packaging: Strategic Technologies, Mfg. Infrastructure, and Applications** *Course Leader: Rao Tummala – Georgia Institute of Technology*	**Northern Hemisphere E4** **13. Flexible Hybrid Electronics** *Course Leader: Pradeep Lall – Auburn University*
Americas Seminar **5. Polymers and Nanocomposites for Electronic and Photonic Packaging** *Course Leaders: C. P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation*	**Americas Seminar** **14. Polymers for Electronic Packaging** *Course Leader: Jeffrey Gotro – InnoCentrix, LLC*
Southern Hemisphere III **6. Integrated Thermal Packaging and Reliability of Power Electronics** *Course Leaders: Patrick McCluskey and Avram Bar-Cohen – University of Maryland*	**Southern Hemisphere III** **15. Emerging Interconnect and System Integration Technologies** *Course Leader: Muhannad Bakir – Georgia Institute of Technology*
Southern Hemisphere IV **7. Fundamentals of Electrical Design and Fabrication Processes of Interposers, Including Their RDLs** *Course Leaders: Ivan Ndip, Markus Wöhrmann, and Michael Töpper – Fraunhofer IZM*	**Southern Hemisphere IV** **16. Package Failure Mechanisms, Reliability, and Solutions** *Course Leader: Darvin Edwards – Edwards Enterprises*
Southern Hemisphere V **8. Introduction to Mechanics Based Quality and Reliability Assessment Methodology** *Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation*	**Southern Hemisphere V** **17. Ageing of Polymers and the Influence on Microelectronic Package Reliability** *Course Leaders: Tanja Braun and Ole Hölck – Fraunhofer IZM*
Southern Hemisphere II **9. Thermo-Electric Coolers: Characterization, Reliability, and Modeling** *Course Leader: Jaime Sanchez – Intel Corporation*	**Southern Hemisphere II** **18. Thermo-Electrical Co-Design of 3D Chip Stacks** *Course Leaders: Ankur Srivastava and Avram Bar-Cohen – University of Maryland, and Jim Wilson – Raytheon*

Refreshment Breaks – 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Southern Hemisphere Foyer & Northern E Corridor

ECTC STUDENT RECEPTION

Tuesday, May 30, 2017
5:00 p.m. - 6:00 p.m.
Host: Texas Instruments, Inc.

Outside at the Cabana Deck by Dolphin Pool; (Rain Back Up – Asia 1, Lobby Level)

ECTC welcomes our student attendees and student presenters who bring their research results to our audience. The Student Reception is an event where we provide guidance to students for their job search from industry leaders. In addition to the Student Reception, in the Student Interactive Presentation Session, we provide one-on-one access to students and their research to our audience. We encourage you to attend the Student Interactive Presentation Session on Friday. This reception is sponsored by Texas Instruments.

GENERAL CHAIR'S SPEAKERS RECEPTION

Tuesday, May 30, 2017
6:00 p.m. - 7:00 p.m.

Outside at the Crescent Terrace on the Swan Hotel side; (Rain Back Up – Northern Hemisphere D / DE Corridor)

Invited session chairs and speakers are requested to attend the reception.

TECHNOLOGY CORNER RECEPTION

Wednesday, May 31, 2017
5:30 p.m. - 6:30 p.m.

Northern Hemisphere A – C, 5th Floor

An Exhibitor Sponsored Reception will be held in Northern Hemisphere A – C, 5th Floor. All attendees and guests are invited.

67th ECTC GALA RECEPTION

Thursday, June 1, 2017
6:30 p.m.

Outside at the Lake Terrace on the Swan Hotel side; (Rain Back Up – Northern Hemisphere D – E)

All badged attendees and guests are invited to attend our Gala Reception outside at the Lake Terrace.

CONTINUING EDUCATION UNITS

The IEEE Components, Packaging, and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 67th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops. Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Course CEUs will be underwritten by the conference, i.e., there are no additional costs for Professional Development Course attendees to obtain CEU credit.

2016 ECTC BEST PAPER AWARDS

BEST OF CONFERENCE PAPERS – 2016

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 66th ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500 and the authors of the Best Interactive Presentation share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

Session 2, Paper 5

High-Frequency Analysis of Embedded Microfluidic Cooling Within 3-D ICs Using a TSV Testbed

Hanju Oh, Xuchen Zhang, Gary S. May, and Muhannad S. Bakir – Georgia Institute of Technology

Best Interactive Presentation

Session 37, Paper 2

Constitutive Relations for Finite Element Modeling of SnAgCu in Thermal Cycling – How Wrong We Were!

Thaer Alghoul, Dustin Watson, Nardeeka Adams, Saif Khasawneh, Farhan Batieha, Chris Greene, and Peter Borgesen – Binghamton University

INTEL BEST STUDENT PAPER – 2016

The winning student receives a personalized plaque and a check for $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 66th ECTC:

Session 30, Paper 2

Non-Linear Finite Element Analysis on Stacked Die Package Subjected to Integrated Vapor-Hygro-Thermal-Mechanical Stress

Jing Wang and Seungbae Park, Binghamton University

OUTSTANDING PAPERS – 2016

The winning authors for Conference Outstanding Session Paper and Interactive Presentation receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

Session 13, Paper 4

Eternal Packages: Liquid Metal Flip Chip Devices

Assane Ndieguene, Pierre Albert, and Julien Sylvestre – Université de Sherbrooke; Clément Fortin and Valérie Oberson – IBM Corporation

Outstanding Interactive Presentation

Session 39, Paper 16

20" x 20" Panel Size Glass IPD Interposer Manufacturing

Yu-Hua Chen, Chun-Hsien Chien, Yu-Chung Hsieh, Wei-Ti Lin, Wen-Liang Yeh, Chien-Chou Chen, Dyi-Chung Hu, Tzyy-Jang Tseng – Unimicron Technology Corp.; Hobie Yun – Qualcomm Technologies, Inc.

TEXAS INSTRUMENTS OUTSTANDING STUDENT INTERACTIVE PRESENTATION – 2016

The winning student receives a personalized plaque and a check for US $500. The following paper was selected based on the Texas Instruments Outstanding Student Interactive Presentation competition conducted at the 66th ECTC:

Session 39, Paper 28

2D Grating Pitch Mapping of a Through Silicon Via (TSV) and Solder Ball Interconnect Region Using Laser Diffraction

Todd Houghton, Michael Saxon, Zeming Song, Hoa Nguyen, Hanqing Jiang, and Hongbin Yu - Arizona State University

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 30, 2017

9:30 a.m. – 5:30 p.m.
INEMI Meeting
Oceanic 1, Lobby Level

8:00 a.m. – 5:30 p.m.
IEEE CPMT Heterogeneous Integration Roadmap Workshop
Europe 4, Lobby Level

9:00 p.m. – 10:30 p.m.
ECTC Interconnect Committee
Europe 4, Lobby Level

Wednesday, May 31, 2017

7:00 a.m. – 8:00 a.m.
CPMT Materials & Processes TC
Europe 3, Lobby Level

7:00 a.m. – 8:00 a.m.
CPMT Energy Electronics TC
Europe 4, Lobby Level

4:30 p.m. – 5:30 p.m.
CPMT Technical Committee Chairs
Europe 1, Lobby Level

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite
(by invitation only)

9:00 p.m. – 10:30 p.m.
ECTC Opto Committee
Americas Seminar, 5th Floor

Thursday, June 1, 2017

7:00 a.m. – 8:00 a.m.
CPMT Region 8 Meeting
Europe 4, Lobby Level

7:00 a.m. – 8:00 a.m.
CPMT RF & THz Technology TC
Europe 5, Lobby Level

7:00 a.m. – 8:00 a.m.
CPMT High Density Substrates & Boards TC
Europe 1, Lobby Level

4:30 p.m. – 6:00 p.m.
CPMT Officers and Directors Meeting
Oceanic 1, Lobby Level

5:30 p.m. – 6:30 p.m.
ECTC 2017 Program Committee Meeting
Southern Hemisphere 1, 5th Floor

8:00 p.m.
67th ECTC Governing/Executive Committee Reception
General Chair's Suite

Friday, June 2, 2017

7:00 a.m. – 8:00 a.m.
CPMT Nanotechnology TC
Europe 3, Lobby Level

7:00 a.m. – 8:00 a.m.
CPMT Thermal & Mechanical TC
Asia 1, Lobby Level

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee
Europe 3, Lobby Level

4:45 p.m. – 5:45 p.m.
ECTC Steering Committee
Europe 3, Lobby Level

Program Sessions: Wednesday, May 31, 8:00 a.m. - 11:40 a.m.

Session 1: Fan-Out Packaging Process and Integration	Session 2: TSV Process, Characterization and Applications	Session 3: Flip Chip Assembly
Committee: Advanced Packaging	**Committee: Interconnections**	**Committee: Assembly & Manufacturing Technology**
Room: Southern Hemisphere I	**Room: Southern Hemisphere II**	**Room: Southern Hemisphere III**
Session Co-Chairs: Beth Keser – Intel Corporation Mike Ma – Amkor Technology Taiwan (ATT)	**Session Co-Chairs: Takafumi Fukushima – Tohoku University Tom Gregorich – SanDisk**	**Session Co-Chairs: Valerie Oberson – IBM Corporation Mark Gerber – Advanced Semiconductor Engineering Inc.**
1. 8:00 AM - Development of a Multi-Project Fan-Out Wafer Level Packaging Platform T. Braun, S. Raatz, U. Maass, M. van Dijk, H. Walter, O. Hölck, K. F. Becker, M. Töpper, R. Aschenbrenner – Fraunhofer IZM; M. Wöhrmann, S. Voges, M. Huhn, K. D. Lang – Technical University Berlin; M. Wietstruck, R.F. Scholz, A. Mai, M. Kaynak – IHP	***1. 8:00 AM - A Cost-Effective Via Last TSV Technology Using Molten Solder Filling for Automobile Application*** Yuki Ohara, Yuki Inagaki, Masaki Matsui, and Kazushi Asami – DENSO Corporation	***1. 8:00 AM - Key Properties for Successful Ultra Thin Die Pickup*** Stefan Behler – Besi Switzerland AG; Teng Wang and Arnita Podpod – IMEC
2. 8:25 AM - SLIM™, High Density Wafer Level Fan-Out Package Development with Submicron RDL Youngrae Kim, JaeHun Bae, MinHwa Chang, AhRa Jo, Ji Hyun Kim, SangEun Park, David Hiner, Mike Kelly, and WonChul Do – Amkor Technology, Inc.	***2. 8:25 AM - Accurate Depth Control of Through-Silicon Vias by Substrate Integrated Etch Stop Layers*** Matthias Wietstruck, Steffen Marschmeyer, Marco Lisker, Andreas Krueger, Dirk Wolansky, Philipp Kulse, Alexander Goeritz, Thomas Voss, Andreas Mai, and Mehmet Kaynak – IHP Microelectronics; Mesut Inac – Technical University Berlin	***2. 8:25 AM - Fine Pitch Cu Pillar with Bond on Lead (BOL) Assembly Challenges for Low Cost and High Performance Flip Chip Package*** Nokibul Islam, Vinayak Pandey, and KyungOe Kim – STATS ChipPAC, Inc.
3. 8:50 AM - Development of Novel High Density System Integration Solutions in FOWLP – Complex and Thin Wafer-Level SiP and Wafer-Level 3D Packages André Cardoso, Alberto Martins, Hugo Barros, Elisabete Fernandes, Abel Janeiro, Paulo Cardoso, and Leonor Dias – NANIUM S.A.	***3. 8:50 AM - Application of a Metallic Cap Layer to Control Cu TSV Extrusion*** Golareh Jalilvand, Omar Ahmed, Keenan Bosworth, Zhenlin Pei, Cullen Fitzgerald, and Tengfei Jiang – University of Central Florida	***3. 8:50 AM - Improvement of C2W Collective Bonding Reliability and UPH through Innovations in Machine, Materials and Methods*** Tomonori Nakamura, Farhan Shafiq, Tetsuya Otani, Osamu Watanabe, Toru Maeda, and Yoshihito Hagiwara – Shinkawa Ltd.; Keiji Honjo, Daichi Mori, Outa Egashira, Daisuke Handa, and Tamotsu Owada – Dexerials
Refreshment Break: 9:15 a.m. - 10:00 a.m. Northern Hemisphere A-C		
4. 10:00 AM - Fan-Out Chip on Substrate Device Interconnection Reliability Analysis Ian Hu, Ying-Chih Lee, Wei-Hong Lai, Meng-Kai Shih, Chin-Li Kao, David Tarng, and Ching-Pin Hung – Advanced Semiconductor Engineering, Inc.	***4. 10:00 AM - Development of TSV Electro-plating Process for Via-Last Technology*** Gilho Hwang and Kalaiselvan Ravanethran – Institute of Microelectronics, A*STAR	***4. 10:00 AM - Thermo-Compression Bonding and Mass Reflow Assembly Processes of 3D Logic Die Stacks*** Pascale Gagnon, Christian Bergeron, Richard Langlois, Stéphane Barbeau, Steve Whitehead, Katsuyuki Sakuma, Raphael Robertazzi, Christy Tyberg, Matthew Wordeman, and Michael Scheurmann – IBM Corporation
5. 10:25 AM - Embedded Si Fan-Out: A Low-Cost Wafer Level Packaging Technology Without Molding and De-Bonding Processes Daquan Yu, Zhenrui Huang, Zhiyi Xiao, Li Yang, and Min Xiang – Huatian Technology (Kunshan) Electronics Co., Ltd.	***5. 10:25 AM - Reliability Evaluation of Copper (Cu) Through-Silicon Via (TSV) Barrier and Dielectric Liner by Electrical Characterization and Physical Failure Analysis (PFA)*** Jiawei Marvin Chan and Chuan Seng Tan – Nanyang Technological University; Xu Cheng, Kheng Chooi Lee, and Werner Kanert – Infineon Technologies	***5. 10:25 AM - Chip Shooter to Enable Fine Pitch Flip Chip*** Jie Fu, Manuel Aldrete, and Milind Shah – Qualcomm Technologies, Inc.
6. 10:50 AM - Process Development and Material Characteristics of TSV-Less Interconnection Technology for FOWLP Wen-Wei Shen, Yu-Min Lin, Hsiang-Hung Chang, Tzu-Ying Kuo, Huan-Chun Fu, Yuan-Chang Lee, Shu-Man Lee, Ang-Ying Lin, Shin-Yi Huang, Tao-Chih Chang – Industrial Technology Research Institute; Alvin Lee, Jay Su, Baron Huang, Dongshun Bai and Xiao Liu – Brewer Science; Kuan-Neng Chen Chen – NCTU	***6. 10:50 AM - Vertical Delay Modeling of Copper/Carbon Nanotube Composites in a Tapered Through Silicon Via*** Madhav Rao – International Institute of Information Technology Bangalore	***6. 10:50 AM - Assembly Challenges for 75x75mm Large Body FCBGA with Emerging High Thermal Interface Material (TIM)*** Fletcher (Cheng-Piao) Tung, Max (Chin Yu) Lu, Albert (Chang Yi) Lan, and Steward (Chi An) Pan – Siliconware Precision Industries Co., Ltd.
7. 11:15 AM - First Demonstration of Panel Glass Fan-Out (GFO) Packages for High I/O Density and High Frequency Multi-Chip Integration Tailong Shi, Vanessa Smet, Venky Sundaram, Rao Tummala, and Chintan Buch – Georgia Institute of Technology; Yoichiro Sato – Asahi Glass Co., Ltd.; Lutz Parthier – Schott; Frank Wei and Cody Lee – Disco Corporation	***7. 11:15 AM - Latency, Bandwidth and Power Benefits of the SuperCHIPS Integration Scheme*** SivaChandra Jangam, Saptadeep Pal, Adeel Bajwa, Sudhakar Pamarti, Puneet Gupta, and Subramanian Iyer – University of California, Los Angeles	***7. 11:15 AM - Fine Pitch Interconnect Rework for Lead-Free Flip Chip Packages*** Malak Kanso, David Danovitch, and Elodie Nguena – Sherbrooke University; Richard Langlois and Christian Bergeron – IBM Corporation

Program Sessions: Wednesday, May 31, 8:00 a.m. - 11:40 a.m.

Session 4: Advanced Substrates and Integrated Devices	Session 5: Emerging Sensors and Microsystems Packaging	Session 6: 5G, mmWave and Beyond
Committee: **Materials & Processing**	**Committee:** **Emerging Technologies**	**Committee:** **High-Speed, Wireless & Components**
Room: Southern Hemisphere IV	**Room: Southern Hemisphere V**	**Room: Americas Seminar**
Session Co-Chairs: **Tieyu Zheng – Microsoft Corporation** **Yu-Hua Chen – Unimicron**	**Session Co-Chairs:** **Bharat Penmecha – Intel Corporation** **Ramakrishna Kotlanka – Analog Devices**	**Session Co-Chairs:** **Kemal Aygun – Intel Corporation** **Lih-Tyng Hwang – National Sun Yat-Sen University**
1. 8:00 AM - A Novel Organic Substrate with Enhanced Thermal Conductivity Xiaoliang Zeng, Yimin Yao, Yougen Hu, Kun Guo, Jiajia Sun, and Rong Sun – Shenzhen Institutes of Advanced Technology; Jianbin Xu and Ching-Ping Wong – Chinese University Hong Kong	***1. 8:00 AM - Phototriggerable, Transient Electronics: Component and Device Fabrication*** Gerald Gourdin, Oluwadamilola Phillips, Jared Schwartz, Anthony Engler, and Paul Kohl – Georgia Institute of Technology	***1. 8:00 AM - First Demonstration of 28 GHz and 39 GHz Transmission Lines and Antennas on Glass Substrates for 5G Modules*** Atom O. Watanabe, Muhammad Ali, Bijan Tehrani, Jimmy Hester, P. Markondeya Raj, Venky Sundaram, Manos M. Tentzeris, and Rao R. Tummala – Georgia Institute of Technology; Hiroyuki Matsuura – NGK Spark Plug; Tomonori Ogawa – Asahi Glass Co., Ltd.
2. 8:25 AM - Infusing Inorganics into the Subsurface of Polymer Redistribution Layer Dielectrics for Improved Adhesion to Metals Shreya Dwarakanath, Pulugurtha Markondeya Raj, Collen Z. Leng, Venky Sundaram, Mark D. Losego, Rao R Tummala, and Vanessa Smet – Georgia Institute of Technology	***2. 8:25 AM - Novel High Temperature Capacitive Pressure Sensor Utilizing SiC Integrated Circuit Twin Ring Oscillators*** Maximilian C. Scardelletti, Philip G. Neudeck, David J. Spry, Roger D. Meredith, Jennifer L. Jordan, Norman F. Prokop, Michael J. Krasowski, Glenn M. Beheim, and Gary W. Hunter – NASA Glenn Research Center	***2. 8:25 AM - Integrated Antenna-in-Package on Low-Cost Organic Substrate for Millimeter-Wave Wireless Communication Applications*** Cheng-Yu Ho, Ming-Fong Jhong, Po-Chih Pan, Chen-Chao Wang, Chun-Yen Ting, and Chih-Yi Huang – Advanced Semiconductor Engineering, Inc.
3. 8:50 AM - Development of Solder Resist with Improved Adhesion at HTSL (175 deg C for 3000 Hours) and Crack resistance at TST for Automotive IC Package Chiho Ueta, Kazuya Okada, Toko Shiina, Tadahiko Hanada, and Nobuhito Itoh – Taiyo Ink Mfg. Co., Ltd.	***3. 8:50 AM - An Experimental Magnesium Ion Battery Cell Made of Flexible Materials*** Todd Houghton, Gamal Eltohamy, and Hongbin Yu – Arizona State University	***3. 8:50 AM - Aerosol-Jet Printed Quasi-Optical Terahertz Filters*** Christopher Oakley, Amanpreet Kaur, Jennifer A. Byford, and Premjeet Chahal – Michigan State University
Refreshment Break: 9:15 a.m. - 10:00 a.m. Northern Hemisphere A-C		
4. 10:00 AM - Bondable Copper Substrates With Silver Solid Solution Coatings for High-Power Electronic Applications Yongjun Huo and Chin C. Lee – University of California, Irvine	***4. 10:00 AM - Fractal-Structured, Wearable Soft Sensors for Control of a Robotic Wheelchair via Electrooculograms*** Saswat Mishra, Yongkuk Lee, Dong Sup Lee, and Woon-Hong Yeo – Virginia Commonwealth University	***4. 10:00 AM - High Performance Chip-Partitioned Millimeter Wave Passive Devices on Smooth and Fine Pitch InFO RDL*** Che-Wei Hsu, Chung-Hao Tsai, Jeng-Shien Hsieh, Kuo-Chung Yee, Chuei-Tang Wang, and Douglas Yu – Taiwan Semiconductor Manufacturing Company, Ltd.
5. 10:25 AM - On-Chip Integrated Solid-State Micro-Supercapacitor Muhammad Amin Saleem, Rickard Andersson, and Vincent Desmaris – Smoltek AB; Bo Song and C.P Wong – Georgia Institute of Technology	***5. 10:25 AM - Micro-Hermetic Packaging Technology for Active Implantable Neural Interfaces*** Kaustubh Nagarkar, Nancy Stoffel, Eric Davis, and Jeffrey Ashe – General Electric Co.; Xiaoxiao Hou and David Borton – Brown University	***5. 10:25 AM - Directional Through Glass Via (TGV) Antennas for Wireless Point-to-Point Interconnects in 3D Integration and Packaging*** Seahee Hwangbo, Hyowon An, Sheng-Po Fang, and Yong-Kyu Yoon – University of Florida; Aric B. Shorey and Abbas M. Kazmi – Corning, Inc.
6. 10:50 AM - Development of CPU Package Embedded with Multilayer Thin Film Capacitor for Stabilization of Power Supply Tomoyuki Akahoshi, Daisuke Mizutani, Kei Fukui, Seigo Yamawaki, Hidehiko Fujisaki, Manabu Watanabe, and Masateru Koide – Fujitsu Laboratories, Ltd.	***6. 10:50 AM - Biopackaging of Minimally Invasive Ultrasound Assisted Clot Lysis Device for Stroke Treatment*** Ramona Damalerio, Ming-Yuan Cheng, Weiguo Chen, Liang Lou, and Songsong Zhang – Institute of Microelectronics, A*STAR	***6. 10:50 AM - RF Characterization and Modeling of 10 µm Fine-Pitch Cu-Pillar on a High Density Silicon Interposer*** Hélène Jacquinot, L. Arnaud, A. Garnier, F. Bana, J.C. Barbe, and S. Cheramy – CEA-Leti
7. 11:15 AM - Panel-Based Integrated Passive Device for RF Application Ming Hung Chen, Tze Hsin Chiang, Jia Hao Zhang, Hsu Chiang Shih, Sheng Chi Hsieh, Teck Chong Lee, and Chih Pin Hung – Advanced Semiconductor Engineering, Inc.	***7. 11:15 AM - A Low-Profile Flow Sensing System for Monitoring of Cerebrospinal Fluid with a New Ventriculoamniotic Shunt*** Yanfei Chen, Stephanie Greene, Puneeth Shridhar, and Youngjae Chun – University of Pittsburgh; Connor Howe and Woon-Hong Yeo – Virginia Commonwealth University; Emery Stephen – Magee-Womens Hospital of UPMC	***7. 11:15 AM - Miniature 2.4-GHz Switched Beamformer Module in IPD and its Application to Very-Low-Profile 1D and 2D Scanning Antenna Arrays*** Chia-Hao Chen, Wei-Ting Fang, and Yo-Shen Lin – National Central University

Program Sessions: Wednesday, May 31, 1:30 p.m. - 5:10 p.m.

Session 7: Fan-Out Packaging Materials and Passives	Session 8: Singulation Process Developments	Session 9: Fine Pitch Flip Chip Process Technologies
Committee: Advanced Packaging	**Committee:** Assembly & Manufacturing Technology	**Committee:** Interconnections
Room: Southern Hemisphere I	**Room: Southern Hemisphere III**	**Room: Southern Hemisphere II**
Session Co-Chairs: Luke England – GLOBALFOUNDRIES; Bora Baloglu – Amkor Technology	**Session Co-Chairs:** Garry Cunningham – NGC; Li Jiang –Texas Instruments	**Session Co-Chairs:** David Danovitch – University of Sherbrooke; Li Li – Cisco Systems, Inc.
1. 1:30 PM - Development of Liquid, Granule, and Sheet Type Epoxy Molding Compounds for Fan-Out Wafer Level Package Kenichi Ueno, Kazuhiro Dohi, Kazuyoshi Muranaka, Akira Nakao, and Yuki Ishikawa – Sanyu Rec Co., Ltd.	***1. 1:30 PM - Expanding Film and Process for High Efficiency 5 Sides Protection and FO-WLP Fabrication*** Kazutaka Honda, Naoya Suzuki, Toshihisa Nonaka, Hirokazu Noma, and Yoshinobu Ozaki – Hitachi Chemical Co., Ltd.	***1. 1:30 PM - Cu-SnAg Interconnects Evaluation for the Assembly at 10µm and 5µm Pitch*** Divya Taneja, Marion Volpert, Gilles Lasfargues, Boris Bouillard, Aurelie Vandeneynde, Tarik Chaira, Yannick Goiran, David Henry, Bertrand Chambion, and Sylvie Jarjayes – CEA-Leti; Fiqiri Hodaj – University Grenople Alps, SIMAP
2. 1:55 PM - Ultra-Low Temperature FOWLP Process for the Embedding of Low Thermal Budget Sensors and Components Using SU-8 as Dielectric Raquel Pinto, André Cardoso, Sara Ribeiro, and Carlos Brandão – NANIUM S.A.; João Gaspar, Rizwan Gill, Helder Fonseca, and Margaret Costa – INL; Filipe Cardoso and Mariana Antunes – Magnomics	***2. 1:55 PM - Laser Multi Beam Full Cut Dicing of Wafer Level Chip-Scale Packages*** Jeroen van Borkulo, Eric Tan, and Richard van der Stam – ASM Pacific Technologies	***2. 1:55 PM - Scaling Cu Pillars to 20µm Pitch and Below: Strategic Role of Surface Finish and Barrier Layers*** Ting-Chia Huang, Vanessa Smet, Pulugurtha Markondeya Raj, and Rao Tummala – Georgia Institute of Technology; Robin Taylor, Gustavo Ramos, Rick Nichols, Arnd Kilian, and Maja Tomic – Atotech
3. 2:20 PM - Integrated Copper Heat Slugs and EMI Shields in Panel Laminate (LFO) and Glass Fan-Out (GFO) Packages for High Power RF ICs Venky Sundaram, Bartlet Deprospo, Nahid Gezgin, Atomu Watanabe, P. Markondeya Raj, Fuhan Liu, Waylon Puckett, Samuel Graham, and Rao Tummala – Georgia Institute of Technology; Kyle Byers and Sean Garrison – Honeywell	***3. 2:20 PM - Plasma Dicing 300mm Framed Wafers - Analysis of Improvement in Die Strength and Cost Benefits for Thin Die Singulation*** Richard Barnett – SPTS Technologies, Ltd.	***3. 2:20 PM - Thermal Compression Bonding: Understanding Heat Transfer by in situ Measurements and Modeling*** Pieter Bex, Teng Wang, Vladimir Cherman, Melina Lofrano, Giovanni Capuz, Erik Sleeckx, and Eric Beyne – IMEC
Refreshment Break: 2:45 p.m. - 3:30 p.m. Northern Hemisphere A-C		
4. 3:30 PM - Implementation of Thick Copper Inductor Integrated into Chip Scaled Package S.B. Yang, C.C. Chen, W.L. Huang, T.L. Yang, G.C. Huang, T.Y. Chou, C.C. Hsu, C.L. Chang, H.L. Huang, C.C. Chou, C.Y. Ku, C.H. Chen, C.S. Chen, K.C. Liu, Alex Kalnitsky, Marvin Liao – Taiwan Semiconductor Manufacturing Company, Ltd.	***4. 3:30 PM - Plasma Dicing Fully Integrated Process-Flows Suitable for BEOL Advanced Packaging Fabrications*** Frank Wei and Tomotaka Tabuchi – DISCO Corporation; Thierry Lazerand, Christopher Johnston, Kenneth Mackenzie, and Marco Notarianni – Plasma-Therm, LLC	***4. 3:30 PM - A Study on Nano-Sized Silica Content and Size Effect in Non Conductive Films (NCFs) for Ultra Fine-Pitch Cu-Pillar/Sn-Ag Micro-Bump Interconnection*** HanMin Lee, SeYong Lee, SeMin Cho, YoungHyun Yu, Jong-Ho Park, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology
5. 3:55 PM - Passive Devices Fabrication on FOWLP and Characterization for RF Applications Chunmei Wang, King Jien Chui, Xiangyu Wang, Teck Guan Lim, and Mingbin Yu – Institute of Microelectronics, A*STAR; Gilbert See and Gu Yu – Applied Materials	***5. 3:55 PM - Stealth Dicing Challenges for MEMS Wafer Applications*** Daniel Ismael Cereno, and Sunil Wickramanayaka – Institute of Microelectronics, A*STAR	***5. 3:55 PM - Accelerated SLID Bonding for Fine-Pitch Interconnects with Porous Microstructure*** Jörg Meyer, Iuliana Panchenko, Steffen Bickel, and Laura Wambera – Technical University Dresden; Wieland Wahrmund and M. Jürgen Wolf – Fraunhofer IZM, ASSID
6. 4:20 PM - Compression Molding Encapsulants for Wafer-Level Embedded Active Devices: Wafer Warpage Control by Epoxy Molding Compounds Kihyeok Kwon, Yoonman Lee, Junghwa Kim, Joo Young Chung, Kyunghag Park, Yong-Yeop Kim, Donghwan Lee, and Sang Kyun Kim – Samsung SDI	***6. 4:20 PM - A Novel Pick-Up and Place Process for FO-WLP Using Tape Expansion Machine Device*** Shinya Takyu, Naoya Okamoto, Tadatomo Yamada, Toshiaki Menjo, and Masatomo Nakamura – LINTEC Corporation	***6. 4:20 PM - Low Temperature Ni/Sn/Ni Transient Liquid Phase Bonding for High Temperature Packaging Application by Imposing Temperature Gradient*** Yi Zhong, Wei Dong, Mingliang Huang, Haitao Ma, and Ning Zhao – Dalian University of Technology; C.P. Wong – Georgia Institute of Technology
7. 4:45 PM - Additive Manufacturing of Magnetic Components for Heterogenous Integration Yi Yan, Lanbing Liu, Guo-Quan Lu, and Chao Ding – Virginia Tech; Luu Nguyen and Jim Moss – Texas Instruments, Inc.; Yunhui Mei – Tianjin University	***7. 4:45 PM - Investigation of Production Quality and Reliability Risk of ELK Wafer WLCSP Package*** Pei-Haw Tsao, T.M. Chen, Y. L. Kuo, C. M. Kuo, Steven Hsu, M. J. Lii, and L. H. Chu – Taiwan Semiconductor Manufacturing Company, Ltd.	***7. 4:45 PM - Interfacial Reaction and Microstructural Evolution between Au-Ge Solder and Electroless Ni-W-P Metallisation in High Temperature Electronics Interconnects*** Li Liu – Wuhan University of Technology, Wuhan, China; Jinzi Cui – Auburn University; Jing Wang – Wolfson School of Mechanical, Electrical and Manufacturing Engineering, Loughborough University; Zhaoxia Zhou and Changqing Liu – Loughborough University

Program Sessions: Wednesday, May 31, 1:30 p.m. - 5:10 p.m.

Session 10: Harsh Environment Interconnect Reliability	Session 11: Mechanical Modeling and Characterization of Interposers and Interconnections	Session 12: Advanced Optical Components and Modules
Committee: Applied Reliability	**Committee: Thermal/Mechanical Simulation & Characterization**	**Committee: Optoelectronics**
Room: Southern Hemisphere IV	**Room: Southern Hemisphere V**	**Room: Americas Seminar**
Session Co-Chairs: Tim Chaudhry – Amkor Technology, Inc. René Rongen – NXP Semiconductors	**Session Co-Chairs: Kuo-Ning Chiang – National Tsinghua University Tony Mak – Wentworth Institute of Technology**	**Session Co-Chairs: Stephane Bernabe – CEA Leti Shogo Ura – Kyoto Institute of Technology**
1. 1:30 PM - Effect of Processing Variables on the Mechanical Reliability of Copper Pillar SnAg/Cu Solder Joints Mohammed Genanu, Babak Arfaei, and Eric Cotts – Binghamton University; Francis Mutuku and James Wilcox – Universal Instruments; Eric Perfecto – GLOBALFOUNDRIES	***1. 1:30 PM - Hybrid Approach to Conduct Failure Prognostics of Automotive Electronic Control Unit*** Bulong Wu, Dae-Suk Kim, and Bongtae Han – University of Maryland; Alicja Palczynska, Przemyslaw Jakub Gromala, and Alexandru Prisacaru – Robert Bosch GmbH	***1. 1:30 PM - Low Loss Channel-Shuffling Polymer Waveguides: Design and Fabrication*** Kohei Abe, Yutaro Oizumi, Yoichi Taira, and Takaaki Ishigure – Keio University
2. 1:55 PM - Visualization of Microstructural Evolution in Lead Free Solders During Isothermal Aging Using Time-Lapse Imagery Sudan Ahmed, Nianjun Fu, Jeffrey Suhling, and Pradeep Lall – Auburn University	***2. 1:55 PM - Semiconductor Power Package Bonding Interconnects Reliability Simulation under Transient Thermal Loads*** Qiuxiao Qian, Roger Stout, and Yong Liu – ON Semiconductor	***2. 1:55 PM - A Very High-Density On-Board Optical Module Realizing >1.3 Tb/s/inch²*** Kazuya Nagashima, Toshinori Uemura, Atsushi Izawa, Yozo Ishikawa, and Hideyuki Nasu – Furukawa Electric
3. 2:20 PM - Failure Mechanism and Kinetics Studies of Electroless Ni-P Dissolution in Pb-Free Solder Joints under Electromigration Pilin Liu, Alan Overson, Chaitra Chavali, and Deepak Goyal – Intel Corporation	***3. 2:20 PM - Correlation of Dielectric Film Flex Fatigue Resistance and Package Resin Cracking Failure*** Joseph Ross, Nicolas Pizzuti, Steven Ostrander, and Kamal Sikka – IBM Corporation	***3. 2:20 PM - Design and Demonstration of a Photonic Integrated Glass Interposer for Mid-Board Optical Engines*** Marcel Neitz and Sebastian Marx – Technical University Berlin; Markus Wöhrmann and Henning Schröder – Fraunhofer IZM; Ruiyong Zhang and Mohamed Fikry – Amphenol FCI
Refreshment Break: 2:45 p.m. - 3:30 p.m. Northern Hemisphere A-C		
4. 3:30 PM - Pad Cratering Based Failure Criterion for the Life Prediction of Board Level Cyclic Bending Test Qiming Zhang, Jeffery C. C. Lo, and Shi-Wei Ricky Lee –Hong Kong University of Science and Technology	***4. 3:30 PM - Development of FE Models and Measurement of Internal Deformations of Fuze Electronics Using X-Ray MicroCT Data with Digital Volume Correlation*** Pradeep Lall and Nakul Kothari – Auburn University; John Deep and Jason Foley – US Air Force Research Labs; Ryan Lowe – ARA Associates	***4. 3:30 PM - Optoelectronic Chip Assembly Process of Optical MCM*** Masao Tokunari, Koji Masuda, Hsiang-Han Hsu, Takashi Hisada, Shigeru Nakagawa, Richard Langlois, Patrick Jacques, and Paul Fortier – IBM Corporation
5. 3:55 PM - Road Test and Reliability Analysis of Electronic Modules Dongji Xie, Joe Hai, Jack Huang, Manthos Economou, and Zhongming Wu – Nvidia Corporation	***5. 3:55 PM - Dynamic Stress Measurements of Electronic Devices During Active Operation*** Markus Feisst, Eike Moeller, and Jürgen Wilde – University of Freiburg, IMTEK	***5. 3:55 PM - 3D Packaging of Embedded Opto-Electronic Die and CMOS IC Based on Wet Etched Silicon Interposer*** Chenhui Li, Barry Smalbrugge, Teng Li, Ripalta Stabile, and Oded Raz – Eindhoven University of Technology
6. 4:20 PM - Effects of the Inter-Metallic Compounds Microstructure on Electro-Migration of Sn-Bi Solder System Kei Murayama, Mitsuhiro Aizawa, and Takashi Kurihara – Shinko Electric Industries Company, Ltd.	***6. 4:20 PM - Smart Packaging: A Micro-Sensor Array Integrated to a Flip-Chip Package to Investigate the Effect of Humidity in Microelectronic Packages*** Aurore Quelennec, Umar Shafique, and Dominique Drouin – Université de Sherbrooke; Éric Duchesne – IBM Corporation; Hélène Frémont – Université de Bordeaux	***6. 4:20 PM - Self-Alignment with Copper Pillars Micro-Bumps for Positioning Optical Devices at Submicronic Accuracy*** Yézouma Dieudonné Zonou, Stéphane Bernabe, Daivid Fowler, Mireille Francou, and Olivier Castany – CEA-Leti; Philippe Arguel, – Laboratory for Analysis and Architecture of Systems, CNRS
7. 4:45 PM - Effect of Board and Package Type on Board Level Vibration Using Vibrational Spectrum Analysis Jeroen Jalink, Romuald Roucou, Jeroen Zaal, Joachim Lesventes, and Rene Rongen – NXP Semiconductors	***7. 4:45 PM - Nondestructive, In Situ Mapping of Die Surface Displacements in Encapsulated IC Chip Packages Using X-Ray Diffraction Imaging Techniques*** Nima E. Gorji, Rajani K. Vijayaraghavan, and Patrick J. McNally – Dublin City University; Brian K. Tanner – Durham University; Andreas N. Danilewsky – Albert Ludwigs University	***7. 4:45 PM - Thermal Management Characterization of Microassemblied High Power Distributed-Feedback Broad Area Lasers Emitting at 975nm*** Roberto Mostallino, Michel Garcia, Alexandre Larrue, Yannick Robert, Eric Vinet, Michel Lecomte, Olivier Parillaud, and Michel Krakowski – III-V Lab; Yannick Deshayes and Laurent Bechou – University of Bordeaux

Program Sessions: Thursday, June 1, 8:00 a.m. - 11:40 a.m.

Session 13: Interconnect Advances in FO & WLP	Session 14: Heterogeneous Integration	Session 15: Flip Chip and Embedding in Substrates
Committee: Interconnections	**Committee: Advanced Packaging Joint with Assembly & Manufacturing Technology**	**Committee: Advanced Packaging**
Room: Southern Hemisphere II	**Room: Southern Hemisphere III**	**Room: Southern Hemisphere I**
Session Co-Chairs: **Lei Shan – IBM Corporation** **Dingyou Zhang – Qualcomm Technologies, Inc.**	**Session Co-Chairs:** **John Knickerbocker – IBM Corporation** **Chunho Kim – Medtronic Corporation**	**Session Co-Chairs:** **Markus Leitgeb – AT&S** **Steffen Kroehnert – Nanium S.A.**
1. 8:00 AM - SLIM™ Advanced Fan-Out Packaging for High Performance Multi-Die Solutions David Hiner, Moh Kolbehdari, Michael Kelly, Young Rae Kim, Won Chul Do, JaeHun Bae, MinHwa Chang, and AhRa Jo – Amkor Technology, Inc.	***1. 8:00 AM - A Versatile Platform Towards High Reliability Compact Package for Digital Chips*** Christine Ferrandon, Laetitia Castagné, Brahim Kholti, Guillaume Waltener, Vincent Puyal, Romain Lemaire, Jean-Charles Souriau, and Gilles Simon – CEA-Leti; Lionel Toffanin – ST Microelectronics; T. Lacrevaz – IMEP-LAHC Laboratory; J. P. Peltier – e2v	***1. 8:00 AM - Solder Mobility for High-Yield Self-Aligned Flip-Chip Assembly*** Yves Martin, Swetha Kamlapurkar, Jae-Woong Nah, Nathan Marchack, and Tymon Barwicz – IBM Corporation
2. 8:25 AM - 28nm CPI (Chip/Package Interactions) in Large Size eWLB (Embedded Wafer Level BGA) Fan-Out Wafer Level Packages Kang Chen, Linda Chua, Won Kyung Choi, Seng Guan Chow, and Seung Wook Yoon – STATS ChipPAC, Inc.	***2. 8:25 AM - Glass Based 3D-IPD Integrated RF ASIC in WLCSP*** Teck Chong Lee, Yung-Shun Chang, Sheng-Chi Hsieh, Pao-Nan Lee, Yu-Chang Hsieh, and Che-Ming Hsu – Advanced Semiconductor Engineering, Inc.; Long-Ching Wang and Lijuan Zhang – Marvell Semiconductor	***2. 8:25 AM - Large Scale Cryogenic Integration Approach for Superconducting High-Performance Computing*** Rabindra Das, Vladimir Bolkhovsky, Sergey Tolpygo, Pascale Gouker, Leonard Johnson, Eric Dauler, and Mark Gouker – MIT Lincoln Laboratory
3. 8:50 AM - Multi DOE Study on 28nm (RF) WLP Package to Investigate BLR Performance of Large WLP Die with 0.35mm Ball Pitch Array Rey Alvarado, Beth Keser, Tong Cui, Ahmer Syed, Steven Xu, and Brian Roggeman – Qualcomm Technologies, Inc.	***3. 8:50 AM - Breakthrough in Cu to Cu Pillar-Concave Bonding on Silicon Substrate with Polymer Layer for Advanced Packaging, 3D, and Heterogeneous Integration*** Yu-Tao Yang, Ting-Yang Yu, Shu-Chiao Kuo, and Kuan-Neng Chen – National Chiao Tung University; Tai-Yuan Huang, Kai-Ming Yang, Cheng-Ta Ko, Yu-Hua Chen, and Tzyy-Jang Tseng – Unimicron	***3. 8:50 AM - Dense and Highly Elastic Compressible MicroInterconnects (CMIs) for Electronic Microsystems*** Paul K. Jo, Muneeb Zia, Joe L. Gonzalez, and Muhannad S. Bakir – Georgia Institute of Technology
Refreshment Break: 9:15 a.m. - 10:00 a.m. Northern Hemisphere A-C		
4. 10:00 AM - Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging John Lau, Ming Li, DeWen Tian, Nelson Fan, Eric Kuah, Wu Kai, Margie Li, JiYuen Hao, Ken Cheung – ASM Pacific Technology Ltd.; Zhang Li and Kim Hwee Tan – Jiangyin Changdian Advanced Packaging Co., Ltd.; Rozalia Beica – Dow Chemical; Yu-Hua Chen – Unimicron; Sze Pei Lim and Ning Cheng Lee – Indium Corporation, Koh Sau Wee, Jiang Ran and Cao Xi – Huawei Technologies Co. Ltd.	***4. 10:00 AM - Heterogeneous Interposer Based Integration of Chips with Copper Pillars and C4 Balls to Achieve High Speed Interfaces for ADC Application*** Andy Heinig, Michael Dittrich, Fabian Hopsch, and Robert Trieb – Fraunhofer IIS/EAS	***4. 10:00 AM - New Resin Materials for High Power Embedding*** Michael Guyenot, Christiane Mager, and Roumen Ratchev – Robert Bosch GmbH; Thomas Gottwald and A. Khoshamouz – Schweizer Electronic; Sascha Kreuer – Isola
5. 10:25 AM - A Novel 3D IC Wafer-Level Package for New Wave MEMS Che-Hau Huang, Ying-Te Ou, and Yung-Hui Wang – Advanced Semiconductor Engineering, Inc; Sebastian Schuler-Wakins, Ralf Reichenbach, David Polityko, and Uwe Hansen – Robert Bosch GmbH	***5. 10:25 AM - "FlexTrate®" - Scaled Heterogeneous Integration on Flexible Biocompatible Substrates Using FOWLP*** Tak Fukushima, Arsalan Alam, Saptadeep Pal, Zhe Wan, Siva Jangam, Goutham Ezhilarasu, Adeel Bajwa, and Subramanian Iyer – University of California, Los Angeles	***5. 10:25 AM - Advanced Embedded Packaging for Power Devices*** Naoki Hayashi, Miki Nakashima, Hiroshi Demachi, Shingo Nakamura, Tomoshige Chikai, Yukari Imaizumi, Fumihiko Taniguchi, Yoshihiko Ikemoto, Mitsuru Ooida, and Akito Yoshida – J-Devices Corporation
6. 10:50 AM - First Demonstration of Photoresist Cleaning for Fine Line RDL Yield Enhancement by an Innovative Ozone Treatment Process for Panel Fan-Out and Interposers Atul Gupta, Eric Snyder, Christiane Gottschalk, James Gunn, and Kevin Wenzel – MKS Instruments; Hao Lu, Yuya Suzuki, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology	***6. 10:50 AM - Metal Contamination Evaluation of Via-Last Cu TSV Process Using Notchless Si Etching and Wet Cleaning of the First Metal Layer*** Naoya Watanabe, Haruo Shimamoto, Katsuya Kikuchi, and Masahiro Aoyagi – Advanced Industrial Science and Technology; Hidekazu Kikuchi, Azusa Yanagisawa, and Akio Nakamura – LAPIS Semiconductor	***6. 10:50 AM - Development of Large-Size CPU Package Structure Using Embedded Thin Film Capacitor Package Substrate*** Masateru Koide, Kenji Fukuzono, and Manabu Watanabe – Fujitsu Advanced Technologies Limited; Daisuke Mizutani, Tomoyuki Akahoshi, Seigo Yamawaki, and Kei Fukui – Fujitsu Laboratories, Ltd.; Hedehiko Fujisaki – Fujitsu Interconnect Technologies Ltd.
7. 11:15 AM - Process and Reliability of Large Fan-Out Wafer Level Package Based Package-on-Package Srinivasa Rao Vempati, David Ho, Mian Zhi Ding, Ser Choong Chong, Sharon Lim PS, Tai Chong Chai, Daniel Ismael, and Ye Yong Liang – Institute of Microelectronics, A*STAR	***7. 11:15 AM - A Highly-Miniaturized System Integration Approach for an IOT Contact-Less Power Module*** Srikrishna Sitaraman, Shaoyong Wang, Tony Contreras, Jian Wang, Mingjie Fan, Yuming Song, and Terry Bowen – Tyco Electronics	***7. 11:15 AM - Laminate Chip Embedding Technology - Impact of Material Choice and Processing for Very Thin Die Packaging*** Angela Kessler, Andreas Munding, Thorsten Scharf, Boris Plikat, and Klaus Pressel – Infineon Technologies

Program Sessions: Thursday, June 1, 8:00 a.m. - 11:40 a.m.

Session 16: 3D Materials and Processing	Session 17: Materials and Processes for Flexible and Wearable Devices	Session 18: Warpage, Electromigration and Mechanical Characterization
Committee: Materials & Processing	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Room: Northern Hemisphere IV	**Room: Southern Hemisphere V**	**Room: Americas Seminar**
Session Co-Chairs: **Myung Jin Yim – Intel Corporation** **Mikel Miller – Draper Laboratory**	**Session Co-Chairs:** **C. S. Premachandran – GLOBALFOUNDRIES** **Chelakara Vaidyanathan – Ciena Corporation**	**Session Co-Chairs:** **Xuejun Fan – Lamar University** **Jiantao Zheng – Qualcomm Technologies, Inc.**
1. 8:00 AM - High Productive 3D Stacking Process Kazutaka Honda, Hirokazu Noma, Hitoshi Onozeki, Shizu Fukuzumi, and Yoshinobu Ozaki – Hitachi Chemical Co., Ltd.	***1. 8:00 AM - Nanoparticle Based Printed Sensors on Paper for Detecting Chemical Species*** Jack Lombardi, Mark Poliks, Wei Zhao, Shan Yan, Ning Kang, Jing Li, Jin Luo, Chuan-Jian Zhong, Ziang Pan, Madina L. Zabran, Sandeep S. Mittal, Kanad Ghose – State University of New York at Binghamton; Mihdhar Almihdhar and Benjamin Hsiao – Stony Brook University	***1. 8:00 AM - Model for Interaction of EMC Formulation with Operating Current and Reliability of Cu-Al Wirebonds Operating in Harsh Environments*** Pradeep Lall, Shantanu Deshpande, and Yihua Luo – Auburn University; Luu Nguyen – Texas Instruments, Inc.
2. 8:25 AM - Direct Bonding and Debonding Approach of Ultrathin Glass Substrates for High Temperature Devices Messaoud Bedjaoui and Sylvain Poulet – CEA-Leti	***2. 8:25 AM - Phototriggerable Transient Electronics: Materials and Concepts*** Oluwadamilola Phillips, Jared Schwartz, Anthony Engler, Gerald Gourdin, and Paul Kohl – Georgia Institute of Technology	***2. 8:25 AM - Interfacial Delamanination of Mold Compound in Fan-Out Packages*** V.N.N. Trilochan Rambhatla, David Samet, P Markondeya Raj, Satomi Kawamoto,, Rao R. Tummala, and Suresh K. Sitaraman – Georgia Institute of Technology
3. 8:50 AM - Wafer-Level Vacuum-Packaged Piezoelectric Energy Harvesters Utilizing Two-Step Three-Wafer Bonding Nan Wang, Chengliang Sun, Li Yan Siow, Hongmiao Ji, Darmayuda I Made, Peter Chang, Qingxin Zhang, Yuandong Gu, and Lionel You Liang Wong – Institute of Microelectronics, A*STAR	***3. 8:50 AM - Synthesis of a Soft Nanocomposite for Flexible, Wearable Bioelectronics*** Fabrice Fondjo and Jong-Hoon Kim – Washington State University; Dong Sup Lee, Connor Howe, and Woon-Hong Yeo – Virginia Commonwealth University	***3. 8:50 AM - Non-Linear Viscoelastic Modeling of Epoxy Based Molding Compound for Large Deformations Encountered in Power Modules*** Przemyslaw Gromala, Alexandru Prisacaru, and Mateus Jeronimo – Robert Bosch GmbH; Hyun-Seop Lee, Yong Sun, and Bongtae Han – University of Maryland
Refreshment Break: 9:15 a.m. - 10:00 a.m. Northern Hemisphere A-C		
4. 10:00 AM - Advances in Thin Wafer Debonding and Ultrathin 28-nm FinFET Substrate Transfer Alain Phommahaxay, Anne Jourdain, Goedele Potoms, Greet Verbinnen, Erik Sleeckx, Eric Beyne, and Gerald Beyer – IMEC; Alice Guerrero, Dongshun Bai, Kim Yess, and Kim Arnold – Brewer Science	***4. 10:00 AM - BiCMOS Integrated Microfluidic Packaging by Wafer Bonding for Lab-on-Chip Applications*** Mesut Inac – Technical University Berlin; Arnaud Pothier - Univeristy of Limoges/CNRS; Matthias Wietstruck, Alexander Göritz, Barbaros Cetindogan, Canan Baristiran-Kaynak, Steffen Marschmeyer, Mirko Fraschke, Thomas Voss, Andreas Mai, Mehmet Kaynak, and Cristiano Palego – IHP Microelectronics	***4. 10:00 AM - Warpage Modeling and Characterization of the Viscoelastic Relaxation for Cured Molding Process in Fan-Out Packages*** Shu-Shen Yeh, Po-Yao Lin, Kuang-Chun Lee, Jin-Hua Wang, Wen-Yi Lin, Ming-Chih Yew, Po-Chen Lai, Shyue-Ter Leu, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.
5. 10:25 AM - Thermally Reversible and Crosslinked Polyurethane Based on Diels-Alder Chemistry for Ultrathin Wafer Temporary Bonding at Low-Temperature Jinhui Li, Qiang Liu, Guoping Zhang, and Rong Sun – Shenzhen Institutes of Advanced Technology; Chingping Wong – Chinese University of Hong Kong; Bin Zhao – Shanghai Micro Electronics Equipment	***5. 10:25 AM - Enhanced Thermal Performance Polyimide (PI) for Improved Flexible Electronic Application*** Manuela Loeblein, Theo Levert, Emiliano Pallecchi, Siu Hon Tsang, and Edwin Hang Tong Teo – Nanyang Technological University	***5. 10:25 AM - Wafer Form Warpage Characterization Based on Composite Factors Including Passivation Films, Re-Distribution Layers, Epoxy Molding Compound Utilized in Innovative Fan-Out Package*** Cheng-Hsiang Liu, Lu-Yi Chen, Chang-Lun Lu, Hung-Chi Chen, Cheng-Yi Chen, and Shou-Chi Chang – Siliconware Precision Industries Co., Ltd.
6. 10:50 AM - Synchrotron X-Ray Microdiffraction Investigation of Scaling Effects on Plasticity and the Correlation to TSV Extrusion Laura Spinella, Jang-hi Im, and Paul Ho – University of Texas, Austin; Tengfei Jiang – University of Central Florida; Nobumichi Tamura – Lawrence Berkeley National Laboratory	***6. 10:50 AM - Nanolaminated CoNiFe Cores with Dip-Coated Fluoroacrylic Polymer Interlamination Insulation: Fabrication, Electrical Characterization, and Performance Reliability*** Minsoo Kim and Mark G. Allen – University of Pennsylvania; Jooncheol Kim – Georgia Institute of Technology	***6. 10:50 AM - Co-Design for Low Warpage and High Reliability in Advanced Package with TSV-Free Interposer (TFI)*** Faxing Che, Masaya Kawano, M.Z. Ding, Yong Han, and S. Bhattacharya – Institute of Microelectronics, A*STAR
7. 11:15 AM - Development of High Frequency Device Using Glass or Fused Silica with 3D Integration Shintarou Takahashi, Yoichiro Sato, Kohei Horiuchi, and Motoshi Ono – Asahi Glass Co., Ltd.	***7. 11:15 AM - Test-Protocol for Assessment of Flexible Power Sources in Foldable Wearable Electronics under Stresses of Daily Motion During Operation*** Pradeep Lall and Hao Zhang – Auburn University	***7. 11:15 AM - Finite Elements for Electromigration Analysis*** Elena E. Antonova and David C. Looman – ANSYS Inc.

Program Sessions: Thursday, June 1, 1:30 p.m. - 5:10 p.m.

Session 19: Recent Advances in FOWLP Technology	Session 20: MEMS and Sensor Technologies	Session 21: 3D Cu-Cu and Micro Bump Bonding Technologies
Committee: Materials & Processing	**Committee:** Advanced Packaging	**Committee:** Interconnections
Room: Southern Hemisphere IV	**Room: Southern Hemisphere I**	**Room: Southern Hemisphere II**
Session Co-Chairs: Praveen Pandojirao-S – Johnson & Johnson; Yi Li – Intel Corporation	**Session Co-Chairs:** Joseph W. Soucy – Draper; Allyson Hartzell – Veryst Engineering	**Session Co-Chairs:** Katsuyuki Sakuma – IBM Corporation; Ho-Young Son – SK Hynix
1. 1:30 PM - Innovative Excimer Laser Dual Damascene Process for Ultra-Fine Line Multi-layer Routing with 10µm Pitch Micro-Vias for Wafer-Level and Panel-Level Packaging Markus Woehrmann, Robert Gernhardt, Karin Hauck, Michael Toepper, and Tanja Braun – Fraunhofer IZM; Habib Hichri and Markus Arendt – Suss MicroTec; Klaus-Dieter Lang – Technical University Berlin	***1. 1:30 PM - Fabrication of 3D Hybrid Pixel Detector Modules Based on TSV Processing and Advanced Flip Chip Assembly of Thin Read Out Chips*** Kai Zoschke, Hermann Oppermann, Thomas Fritzsch, Mario Rothermund, and Ulf Oestermann – Fraunhofer IZM; Pawel Grybos, Krzysztof Kasinski, Piotr Maj, and Robert Szczygiel – AGH University of Science and Technology; Steve Voges and Klaus-Dieter Lang – Technical University Berlin	***1. 1:30 PM - Morphology of Low-Temperature All-Copper Interconnects Formed by Dip Transfer*** Luca Del Carro, Jonas Zuercher, Thomas Brunschwiler, and Sebastian Gerke – IBM Corporation; Tom Wildsmith – Intrinsiq Materials; Gustavo Ramos – Atotech
2. 1:55 PM - Forming a Vertical Interconnect Structure Using Dry Film Processing for Fan-Out Wafer Level Packaging Yew Wing Leong, Hsiang-Yao Hsiao, David Soon Wee Ho, Boon Long Lau, and Huamao Lin – Institute of Microelectronics, A*STAR	***2. 1:55 PM - A Novel Technology for Creating Sensors and Actuators in Processor Packages*** Feras Eid, Qing Ma, Sasha Oster, Georgios Dogiamis, Thomas Sounart, and Johanna Swan – Intel Corporation	***2. 1:55 PM - Enabling Chip-to-Substrate All-Cu Interconnections: Design of Engineered Bonding Interfaces for Improved Manufacturability and Low-Temperature Bonding*** Ninad Shahane, Kashyap Mohan, Antonia Antoniou, Pulugurtha Markondeya Raj, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Gustavo Ramos, Arnd Kilian, and Robin Taylor – Atotech; Frank Wei – Disco Corporation
3. 2:20 PM - Embedded Trench Redistribution Layers (RDL) by Excimer Laser Ablation and Surface Planer Processes Yuya Suzuki, Rao Tummala and Venky Sundaram – Georgia Institute of Technology; Habib Hichri, Markus Arendt, and Lee Seongkuk – Suss MicroTec; Frank Wei, Ye Chen, and Kwon Sang Lee – Disco Corporation; Ognian Dimov, Deepak Arora, and Sanjay Malik – Fujifilm Electronic Materials	***3. 2:20 PM - Stress-Compensating MEMS Sensor Assembly*** Harald Etschmaier, Anderson Singulani, and Coen Tak – ams AG; Kai Zoschke, Hermann Oppermann, and Danny Jaeger – Fraunhofer IZM	***3. 2:20 PM - Low-Temperature and Low-Pressure Cu-Cu Bonding by Pure Cu Nanosolder Paste for Wafer-Level Packaging*** Junjie Li, Tielin Shi, Xing Yu, Chaoliang Cheng, Jinhu Fan, Guanglan Liao, and Zirong Tang – Huazhong University of Science and Technology
Refreshment Break: 2:45 p.m. - 3:30 p.m. Northern Hemisphere A-C		
4. 3:30 PM - Temporary Bonding and Debonding Technologies for Fan-Out Wafer-Level Packaging Qi Wu, Xiao Liu, Kuo Han, Dongshun Bai, and Tony Flaim – Brewer Science	***4. 3:30 PM - 3D Monolithic Metal Orifice Plate For SERS Application: A Showcase of Low Cost MEMS Packaging*** Ning Ge, Steven Simske, Jarrid Wittkopf, Kevin Dooley, Anita Rogacs, Helen Holder, Steven Barcelo, Robert Ionescu, and Dennis Lazaroff – Hewlett Packard Inc.	***4. 3:30 PM - Dual Damascene Compatible, Copper Rich Alloy Based Surface Passivation Mechanism for Achieving Cu-Cu Bonding at 150°C for 3D IC Integration*** Asisa Kumar Panigrahi, Tamal Ghosh, Siva Rama Krishna Vanjari, and Shiv Govind Singh – Indian Institute of Technology, Hyderabad
5. 3:55 PM - Development and Evaluation of Carrier Glass Substrate for Fan-Out WLP/PLP Process Kazutaka Hayashi, Shigeki Sawamura, and Shuhei Nomura – Asahi Glass, Co., Ltd.; Naoya Suzuki and Masaaki Takekoshi – Hitachi Chemical Co., Ltd.	***5. 3:55 PM - A Phase Sensitive Measurement Technique for Boosted Response Speed of Graphene FET Gas Sensor*** Yumeng Liu, Takeshi Hayasaka, Yong Cui, Jiachen Yu, Yoshihiro Kubota, Huiliang Liu, Xiaoqian Li, Kaiming Hu, and Liwei Lin – UC Berkeley, BSAC; Vaishno Dasika and Luu Nguyen – Texas Instruments, Inc.	***5. 3:55 PM - Thermal and Electrical Performance of Direct Bond Interconnect Technology for 2.5D and 3D Integrated Circuits*** Akash Agrawal, Shaowu Huang, Guilian Gao, Liang Wang, and Laura Mirkarimi – Invensas Corporation
6. 4:20 PM - Warpage Suppression during FO-WLP Fabrication Process Masaaki Takekoshi, Keisuke Nishido, Yuhei Okada, Naoya Suzuki, and Toshihisa Nonaka – Hitachi Chemical Co., Ltd.	***6. 4:20 PM - Comparison of Packaging Concepts for High-Temperature Pressure Sensors at 500 °C*** Nilavazhagan Subbiah, Surajit Ghosh, Juergen Wilde, and Roderich Zeiser – University of Freiburg, IMTEK	***6. 4:20 PM - Electrical Performance of High Density 10 µm Diameter 20 µm Pitch Cu-Pillar with Chip to Wafer Assembly*** Lucile Arnaud, Arnaud Garnier, Rémi Franiatte, Alain Toffoli, Stéphane Moreau, Franck Bana, and Séverine Chéramy – CEA-Leti
7. 4:45 PM - Impact of Process Control on UBM/RDL Contact Resistance for Next-Generation Fan-Out Devices Patrik Carazzetti, Frantisek Balon, Mike Hoffmann, Juergen Weichart, Andreas Erhart, and Ewald Strolz – Evatec AG; Kay Viehweger – Fraunhofer IZM-ASSID	***7. 4:45 PM - High Vacuum and High Robustness Al-Ge Bonding for Wafer Level Chip Scale Packaging of MEMS Sensors*** Jinghui Xu, Zhipeng Ding, Vivek Chidambaram, Hongmiao Ji, and Yuandong Gu – Institute of Microelectronics, A*STAR	***7. 4:45 PM - Critical Factors Affecting Structural Transformations in 3D IC Micro Joints*** Hong-Wei Yang, H.Y. Yu, and C. Robert Kao – National Taiwan University

Program Sessions: Thursday, June 1, 1:30 p.m. - 5:10 p.m.

Session 22: Solder Joint & Interconnect Reliability, Characterization and Modeling	Session 23: Additive Manufacturing and Panel-Level Packaging	Session 24: Novel Methods to Assess Reliability
Committee: Thermal/Mechanical Simulation & Characterization	**Committee: Emerging Technologies**	**Committee: Applied Reliability**
Room: Americas Seminar	**Room: Southern Hemisphere V**	**Room: Southern Hemisphere III**
Session Co-Chairs: **Yong Liu – ON Semiconductor** **Erkan Oterkus – University of Strathclyde**	**Session Co-Chairs:** **Florian Herrault – HRL Laboratories, LLC** **W. Hong Yeo – Virginia Commonwealth University**	**Session Co-Chairs:** **Sridhar Canumalla – Microsoft Corporation** **Keith Newman – AMD**
1. 1:30 PM - Peridynamic Solution of Wetness Equation with Time Dependent Saturated Concentration in ANSYS Framework Cagan Diyaroglu and Erdogan Madenci – University of Arizona; Selda Oterkus and Erkan Oterkus – University of Strathclyde	***1. 1:30 PM - Will Low-Cost 3D Additive Manufactured Packaging Replace the Fan-Out Wafer Level Packages?*** Tobias Tiedje, Sebastian Lüngen, Martin Schubert, Marco Luniak, Krzysztof Nieweglowski, and Karlheinz Bock – Technical University Dresden	***1. 1:30 PM - Condition Monitoring Algorithm for Piezoresistive Silicon-Based Stress Sensor Data Obtained from Electronic Control Units*** Alexandru Prisacaru, Alicja Palczynska, and Przemyslaw Jakub Gromala – Robert Bosch GmbH; Bongtae Han – University of Maryland; G.Q. (Kouchi) Zhang – Delft University of Technology
2. 1:55 PM - A Modified Acceleration Factor Empirical Equation for BGA Type Package Min-Hsuan Hsu and Kuo-Ning Chiang – National Tsing Hua University; Chang-Chun Lee – National Chung Hsing University	***2. 1:55 PM - 3D Printing as a New Packaging Approach for MEMS and Electronic Devices*** Gabrielle Aspar, Baptiste Goubault, Olivier Lebaigue, Gilles Simon, Léa Di Cioccio, Yves Bréchet, and Jean-Charles Souriau – CEA-Leti	***2. 1:55 PM - Mechanical Characterization of SAC Solder Joints at High Temperature Using Nanoindentation*** Sudan Ahmed, Md Hasnine, Jeffrey C. Suhling, and Pradeep Lall – Auburn University
3. 2:20 PM - Effect of Mean Temperature on the Evolution of Strain-Amplitude in SAC Ball-Grid Arrays During Operation under Thermal Aging and Temperature Excursions Pradeep Lall, Kazi Mirza, and Jeff Suhling – Auburn University; David Locker – US ARMY AMRDEC	***3. 2:20 PM - 3D Printed High Frequency Coaxial Transmission Line Based Circuits*** Michael Craton, Jennifer A. Byford, Vincens Gjokaj, Premjeet Chahal, and John Papapolymerou – Michigan State University	***3. 2:20 PM - New Method to Separate Failure Modes by Transient Thermal Analysis of High Power LEDs*** Alexander Hanss, E. Liu, Gordon Elger, Maximilian Schmid, and Dominik Müller – Technische Hochschule Ingolstadt; Udo Karbowski and Robert Derix – Lumileds
Refreshment Break: 2:45 p.m. - 3:30 p.m. Northern Hemisphere A-C		
4. 3:30 PM - Characterization of Dual Side Molding SiP Module Jin-Yuan Lai, Tang-Yuan Chen, Ming-Han Wang, Meng-Kai Shih, David Tarng, and Chih-Pin Hung – Advanced Semiconductor Engineering, Inc	***4. 3:30 PM - Design and Demonstration of Highly Miniaturized, Low Cost Panel Level Glass Package for MEMS Sensors*** Chintan Buch, Daniel Struk, Klaus-Jürgen Wolter, Peter J. Hesketh, Venkatesh Sundaram, and Rao Tummala – Georgia Institute of Technology; Catherine Shearer and James Haley – EMD-Ormet Circuits; Mel Findlay – KWJ Engineering; Marc Papageorge – SPEC Sensors	***4. 3:30 PM - Improving Terahertz Signal Travel Distance for Fault Isolation*** Hemachandar Tanukonda Devarajulu, Mayue Xie, Chengqing Hu, and Deepak Goyal – Intel Corporation; Eiji Kato and Masaichi Hashimoto – Advantest Corporation
5. 3:55 PM - Flip Chip Solder Joint Pad Optimizations for Connectivity SiP Applications Quan Qi and Carlton Hanna – Intel Corporation	***5. 3:55 PM - Miniature Heterogeneous Fan-Out Packages for High-Performance, Large-Format Systems*** Carl Prevatte, Matthew A. Meitl, Erich Radauscher, David Gomez, Kanchan Ghosal, Salvatore Bonafede, Brook Raymond, Tanya Moore, António Jose Trindade, and Christopher A. Bower – X-Celeprint; Paul Hines – Micross Advanced Interconnect Technology	***5. 3:55 PM - Effective Evaluation Method: A New Delamination Test Method for MUF (Molded Underfill) Package*** Junghwa Kim, Seung Han, Woochul Na, SoYoon Kim, Ki Hyeok Kwon, Deokhoon Park, Donghwan Lee, and Sang Kyun Kim – Samsung SDI
6. 4:20 PM - Anisotropic and Multiscale Constitutive Framework for the Reliability of Microscale Interconnects Based on Damage Mechanics Zhengfang Qian – Shenzhen University; Hongtao Chen – Harbin Institute of Technology	***6. 4:20 PM - Extremely High Temperature and High Pressure (x-HTHP) Endurable SOI Device & Sensor Packaging for Harsh Environment Applications*** Keng Yuen Au and Eva Wai Leong Ching – Institute of Microelectronics, A*STAR	***6. 4:20 PM - Measuring Sodium Migration in Mold Compounds Using a Sodium Amalgam Electrode as an Infinite Source*** Stefan Schwab and Michael Nelhiebel – Kompetenzzentrum Automobil- u. Industrieelektronik; Julia Appenroth, Peter Weinberger, Herbert Hutter, Maximilian Bonta, and Andreas Limbeck – Technische Universität Wien; Sabine Holzer, Michael Bauer, and Stefan Miethaner – Infineon Technologies
7. 4:45 PM - SACQ Solder Board Level Reliability Evaluation and Life Prediction Model for Wafer Level Packages Wei Lin, Quan Pham, Bora Baloglu, and Michael Johnson – Amkor Technology, Inc.	***7. 4:45 PM - A Study on the Novel Nylon Anchoring Polymer Layer (APL) Anisotropic Conductive Films (ACFs) for Ultra Fine Pitch Chip-On-Glass (COG) Applications*** Dal-jin Yoon, Sang-Hoon Lee, and Kyung-Wook Paik – Korea Advanced Institute of Science & Technology	***7. 4:45 PM - A New Method for Prediction of Corrosion Processes in Metallization Systems for Substrates and Electrical Contacts*** Sandy Klengel, Tino Stephan, and Uwe Spohn – Fraunhofer IMWS

Program Sessions: Friday, June 2, 8:00 a.m. - 11:40 a.m.

Session 25: Characterization and Reliability of Fan-Out & WLP	Session 26: 3D Integration Processing and Reliability	Session 27: Advances in Thermal Compression and Wirebonding
Committee: Applied Reliability	**Committee:** Advanced Packaging	**Committee:** Interconnections
Room: Southern Hemisphere V	**Room: Southern Hemisphere I**	**Room: Southern Hemisphere II**
Session Co-Chairs: Lakshmi N. Ramanathan – Microsoft Corporation; Toni Mattila – Aalto University	**Session Co-Chairs:** Rozalia Beica – Dow Electronic Materials; Dean Malta – Micross Advanced Interconnect Technology	**Session Co-Chairs:** Matthew Yao – GE Energy Management; William Chen – Advanced Semiconductor Engineering, Inc.
1. 8:00 AM - The Paradoxical Role of Sulphur in Molding Compounds: Influence on High Temperature Reliability of Cu-Al Wirebond Interconnects Amar Mavinkurve, Leon Goumans, Bongkoj Bumrungkittikul, Mark-Luke Farrugia, Erik van Olst, Michiel van Soestbergen, and Rene Rongen – NXP Semiconductors	***1. 8:00 AM - Sub-Micron Electrical Interconnection Enabled Ultra-High I/O Density Wafer Level SiP Integration*** Chung Jung Wu, Tung Liang Shao, Hsiao Yun Chen, Sheng Tsung Hsiao, Yi Li Hsiao, Chih Hang Tung, Chen Hua Yu, and Wei Heng Lin – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 8:00 AM - Heterogeneous Integration at Fine Pitch (2-10 µm) Using Thermal Compression Bonding*** Adeel Ahmad Bajwa, SivaChandra Jangam, Saptadeep Pal, Niteesh Marathe, Tingyu Bai, Takafumi Fukushima, Mark Goorsky, and Subramanian Iyer – University of California, Los Angeles
2. 8:25 AM - Mechanistic Investigation and Prevention of Al Bond Pad Corrosion in Cu Wire-Bonded Device Assembly Oliver Chyan, Nick Ross, Alex Lambert, Seare Berhe, and Muthappan Asokan – University of North Texas; Mahmud Chowdhury, Shawn O'Connor, and Luu Nguyen – Texas Instruments, Inc.	***2. 8:25 AM - Temporary Bonding and De-Bonding for Multichip-to-Wafer 3D Integration Process Using Spin-On Glass and Hydrogenated Amorphous Si*** Murugesan Mariappan, Takafumi Fukushima, and Mitsumasa Koyanagi – Tohoku University	***2. 8:25 AM - Reliable Cu-Cu Thermocompression Bonding by Low Temperature Sintered Cu Nanowires*** Li Du, Tielin Shi, Zirong Tang, and Guanglan Liao – Huazhong University of Science and Technology
3. 8:50 AM - Use Condition Risk Assessment for Moisture Related Failures Min Pei, Sibasish Mukherjee, Nitin Uppal, and Milena Vujosevic – Intel Corporation	***3. 8:50 AM - Cu/Adhesive Hybrid Bonding at 180 °C in H-Containing HCOOH Vapor Ambient for 2.5D/3D Integration*** Ran He, Masahisa Fujino, Masatake Akaike, and Tadatomo Suga – University of Tokyo; Taiji Sakai and Seiki Sakuyama – Fujitsu Semiconductor	***3. 8:50 AM - Effect of Metallic Materials Films on the Properties of Copper/Tin Micro-Bump Thermo-Compression Bonding*** Yong Guan, Qinghua Zeng, Jing Chen, Yufeng Jin, and Wei Meng – Peking University; Shenglin Ma – Xiamen University
Refreshment Break: 9:15 a.m. - 10:00 a.m. Southern Hemisphere Foyer		
4. 10:00 AM - Drop Impact Reliability Test and Failure Analysis for Large Size High Density FOWLP Package on Package Zhaohui Chen, Faxing Che, Mian Zhi Ding, David Soon Wee Ho, Tai Chong Chai, and Vempati Srinivasa – Institute of Microelectronics, A*STAR	***4. 10:00 AM - 3D Packaging Challenges for High-End Applications*** Rahul Agarwal, Sukeshwar Kannan, and Luke England – GLOBALFOUNDRIES; Rick Reed, Yong Song, SangHyoun Lee, WangGu Lee, and JinKun Yoo – Amkor Technology, Inc.	***4. 10:00 AM - Thermal Bond Reliability of High Reliability New Palladium-Coated Copper Wire*** Motoki Eto, Ryo Oishi, and Takashi Yamada – Nippon Micrometal Corporation; Tomohiro Uno and Tetsuya Oyamada – Nippon Steel & Sumitomo Metal; Teruo Haibara – Nippon Micrometal Corporation
5. 10:25 AM - The Comparative Study To Enhance Board Level Reliability Performance of Wafer Level Package at 0.25 mm Pitch Using Micro-Ball Drop and Electroplated Solder Technology Kuei Hsiao Kuo, Yi Sin Ting, Chui Feng Weng, Feng Lung Chien, Katch Wan, Chun Sheng Ho, and Rick Lee – Siliconware Precision Industries Co., Ltd.	***5. 10:25 AM - A Novel Method for Air-Gap Formation around Via-Middle (VM) TSVs for Effective Reduction in Keep-Out Zones (KOZ)*** King-Jien Chui, Woon Leng Loh, Xiangyu Wang, Zhaohui Chen, and Mingbin Yu – Institute of Microelectronics, A*STAR	***5. 10:25 AM - Correlation Study of Pd Metallurgical Distributions and RF Characteristics of Pd Coated/Doped Ag-alloy Wire Bonds*** Yi-Jung Sung and Lih-Tyng Hwang – National Sun Yat-Sen University; Chang-Yi Feng – NXP Semiconductors; Eson Chuang – Precision Packaging Materials Corp.
6. 10:50 AM - Quality and Reliability Assessment of Cu Pillar Bumps for Fine Pitch Applications Othmane Jerhaoui, Stephane Moreau, David Bouchu, Gilles Romero, Denis Marseilhan, Thierry Mourier, and Arnaud Garnier – CEA-Leti	***6. 10:50 AM - Warpage Study of Large 2.5D IC Chip Module*** Chieh-Lung Lai, Hung-Yuan Li, Sam Peng, Terren Lu, and Stephen Chen – Siliconware Precision Industries Co., Ltd.	***6. 10:50 AM - Advances in Wire Bonding Technology for 3D Die Stacking and Fan-Out Wafer Level Package*** Ivy Qin, Oranna Yauw, Gary Schulze, Aashish Shah, Bob Chylak, and Nelson Wong – Kulicke and Soffa, Inc.
7. 11:15 AM - Effect of Prolonged Storage up to 1-Year on the High Strain Rate Properties of SAC Leadfree Alloys at Operating Temperatures up to 200°C Pradeep Lall, Di Zhang, Vikas Yadav, and Jeff Suhling – Auburn University; David Locker – US Army AMRDEC	***7. 11:15 AM - Board Level Reliability Optimization for 3D IC Packages with Extra Large Interposer*** Laurene Yip, Ganesh Hariharan, Raghu Chaware, Inderjit Singh, and Tom Lee – Xilinx, Inc.	***7. 11:15 AM - Development of Packaging Technology for High Temperature Resistant SiC Module of Automobile Application*** Kohei Tatsumi, Tomonori Iizuka, Kazuhito Kamei, and Masakazu Inagaki – Waseda University; Akihiro Imakire and Masayuki Hikita – Kyushu Institute of Technology; Rikiya Kamimura – FAIS; Nobuaki Sato, Hiroaki Narimatsu, Kazutoshi Ueda and Koji Shimizu – Mitsui High-tec Inc.; Kazuhiko Sugiura and Kazuhiro Tsuruta – DENSO Corporation; Keiji Toda – Toyota

Program Sessions: Friday, June 2, 8:00 a.m. - 11:40 a.m.

Session 28: Advanced Materials for Reliability Improvement	Session 29: Warpage Control and Substrates	Session 30: RF Components and Module Integration
Committee: **Materials & Processing**	**Committee:** **Assembly & Manufacturing Technology**	**Committee:** **High-Speed, Wireless & Components**
Room: Southern Hemisphere IV	**Room: Southern Hemisphere III**	**Room: Americas Seminar**
Session Co-Chairs: **Kwang-Lung Lin – National Cheng Kung University** **Bing Dang – IBM Corporation**	**Session Co-Chairs:** **Paul Tiner – Texas Instruments** **Paul Houston – Engent**	**Session Co-Chairs:** **Craig Gaw – NXP Semiconductor** **Wendem Beyene – Rambus Inc.**
1. 8:00 AM - High Performance Insulating Adhesive Film for High-Frequency Applications Junya Sato, Shin Teraki, Masaki Yoshida, and Hisao Kondo – NAMICS Corporation	***1. 8:00 AM - Innovative Advances in Copper Electroplating for IC Substrate Manufacturing*** Kousik Ganesan, Yang Sun, Chandrashekhar Pendyala, Thomas Heaton, Radek Chalupa, Marcel Wall, Suddhasattwa Nad, and Rahul Manepalli – Intel Corporation; Amaneh Tasooji – Arizona State University	***1. 8:00 AM - Next Generation High-Q Compact Size IPD Diplexer for RF Front End SiP*** Sheng-Chi Hsieh, Pao-Nan Lee, Chen-Chao Wang, Teck Chong Lee, and Hsu-Chiang Shih – Advanced Semiconductor Engineering, Inc.
2. 8:25 AM - Epoxy/Cyanate Ester Copolymer Material for Molding Compounds in High-Temperature Operations Chia-Chi Tuan, Fan Wu, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology	***2. 8:25 AM - Reflow Warpage Induced Interconnect Gaps between Package/PCB and PoP Top/Bottom Packages*** Kaiqiang Peng, Wei Xu, Zhenkai Qin, Lei Feng, Linlin Lai, and Wei Hu Koh – Huawei Technologies	***2. 8:25 AM - Self-Actuating 3D Printed Packaging for Deployable Antennas*** Ryan Bahr, Manos Tentzeris, Abdullah Nauroze, and Wenjing Su – Georgia Institute of Technology
3. 8:50 AM - High Thermal Conductivity Mold Compounds for Advanced Packaging Applications Makoto Shibuya and Luu Nguyen – Texas Instruments, Inc.	***3. 8:50 AM - Warpage Tuning Study for Multi-Chip Last Fan-Out Wafer Level Package*** Hung-Yuan Li, Allen Chen, Sam Peng, George Pan, and Stephen Chen – Siliconware Precision Industries Co., Ltd.	***3. 8:50 AM - A Simple and Efficient RF Technique for the TSV Characterization*** Xiao Sun, Stefaan Van Huylenbroeck, Geert Van der Plas, and Eric Beyne – IMEC; Cesar Roda Neve – M3 Systems
Refreshment Break: 9:15 a.m. - 10:00 a.m. Southern Hemisphere Foyer		
4. 10:00 AM - Enhanced Thermal Conductivity of the Underfill Materials using Insulated Core/Shell Filler Particles for High Performance Flip Chip Applications Tae-Ryong Kim, Kisu Joo, and Se Young Jeong – Ntrium, Inc.; Boo Taek Lim and Boung Ju Lee – National Nanofab Center; Sung-Soon Choi – Korea Electronics Technology Institute; Myung Jin Yim – Intel Corporation; Euijoon Yoon – Seoul National University	***4. 10:00 AM - Warpage Characterization of Glass Interposer Package Development*** Meng-Kai Shih, Charles Hsu, Yungshun Chang, Karenyu Chen, Ian Hu, David Tarng, CP Hung, and Teck Lee – Advanced Semiconductor Engineering, Inc.	***4. 10:00 AM - The Smallest Form Factor GPS for Mobile Devices*** Eb Andideh, Chuck Carpenter, Jason Steighner, Mike Yore, James Tung, Lynda Koerber, David Schnaufer, Jeff Moran, Suwanna Jittinorasett, Bharati Ingle, Anousa Sengsavanh, and Otto Berger – Qorvo, Inc.
5. 10:25 AM - High Thermal Performance Package with Anisotropic Thermal Conductive Material Ian Hu, Jia-Rung Ho, Jin-Feng Yang, Meng-Kai Shih,, David Tarng, and Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.	***5. 10:25 AM - The Influence of Resin Coverage on Reliability for Solder Joints Formed by One-Pass Reflow Using Resin Reinforced Low Temperature Solder Paste*** Atsushi Yamaguchi, Yasuo Fukuhara, Andy Behr, Naomichi Ohashi, Yasuhiro Suzuki, and Hirohisa Hino – Panasonic Corporation	***5. 10:25 AM - Transparent Antennas for Wireless Systems Based on Patterned Indium Tin Oxide and Thin Flexible Glass*** Mark Poliks, Yi-Lin Sung, Jack Lombardi, Robert Malay, Charles R. Westgate, and Jeremiah Dederick – Binghamton University; Ming-Huang Huang, Sean Garner, Scott Pollard, and Colin Daley – Corning, Inc.
6. 10:50 AM - The Reduction of Outgas from Pre-Applied Underfill Materials by Optimizing the Combination of Base Resin and Flux Compound Kohei Higashiguchi, Takenori Takiguchi, Masashi Okaniwa, Katsutoshi Ihara, Tsuyoshi Kida, Shu Yoshida, and Toyoji Oshima – Mitsubishi Gas Chemical	***6. 10:50 AM - Analysis of System-Level Reliability of Single-Chip Glass BGA Packages with Advanced Solders and Polymer Collars*** Vidya Jayaram, Scott McCann, Bhupender Singh, Pulugurtha Markondeya Raj, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Hiro Matsuura and Yutaka Takagi – NTK/NGK	***6. 10:50 AM - Transfer Function Reconfigurable Cavity Bandpass Filter Embedded with Metallic Grid*** Shang-Yu Hung, Guann-Pyng Li, Mark Bachman, Hsiang-Yu Chan, and Yu Guo – University of California, Irvine
7. 11:15 AM - Study of Capillary Underfill Filler Separation in Advanced Flip Chip Packages Marie-Claude Paquet – IBM Corporation; David Danovitch, Papa Souare, and Julien Sylvestre – Université de Sherbrooke	***7. 11:15 AM - A Comprehensive Study on Stress and Warpage by Design, Simulation and Fabrication of RDL-First Panel Level Fan-Out Technology for Advanced Package*** Puru Lin, Cheng-Ta Ko, Yu-Hua Chen, Wei-Tse Ho, Chi-Hai Kuo, Kuan-Wen Chen, and Tzyy-Jang Tseng – Unimicron Technology Corp.	***7. 11:15 AM - Capillary Condensation Based Wireless Volatile Molecular Sensor*** Saranraj Karuppuswami, Amanpreet Kaur, and Premjeet Chahal – Michigan State University; Nophadon Wiwatcharagoses – Mongkut's University of Technology

Program Sessions: Friday, June 2, 1:30 p.m. - 5:10 p.m.

Session 31: Auto Electronics Packaging and Power Modules	Session 32: Reliability Challenges in 2.5D/3D Interconnect	Session 33: Advanced Bonding and Soldering Technology
Committee: Advanced Packaging	**Committee: Interconnections Joint with Applied Reliability**	**Committee: Materials & Processing**
Room: Southern Hemisphere I	**Room: Southern Hemisphere II**	**Room: Southern Hemisphere IV**
Session Co-Chairs: **Jianwei Dong – Dow Electronic Materials** **Christophe Zinck – ASE**	**Session Co-Chairs:** **Nathan Lower – Rockwell Collins, Inc.** **Dongji Xie – NVIDIA Corporation**	**Session Co-Chairs:** **Kimberly Yess – Brewer Science** **Qianwen Chen – IBM Corporation**
1. 1:30 PM - Novel Polymer Substrate-Based 1.2 kV/ 40A Double-Sided Intelligent Power Module Xin Zhao, Yifan Jiang, Bo Gao, and Douglas Hopkins – North Carolina State University; Kenji Nishiguchi - Risho Kogyo Co., Ltd.; Yoshi Fukawa - TOYOTech LLC	***1. 1:30 PM - Reliability Challenges in 2.5D and 3D IC Integration*** Li Li, Paul Ton, Mohan Nagar, and Pierre Chia – Cisco Systems, Inc.	***1. 1:30 PM - Novel Large-Area Attachment for High-Temperature Power Electronics Module Application*** Chunlei Liu, Fabian Mohn, Juergen Schuderer, and Daniele Torresin – ABB Switzerland Ltd.
2. 1:55 PM - Advanced Packaging Need for Automotive In-Cabin Application Nokibul Islam, Ming-Che Hsieh, and Kang KeonTaek – STATS ChipPAC, Inc.	***2. 1:55 PM - High Frequency Electrical Performance and Thermo-Mechanical Reliability of Fine-Pitch, Copper-Metallized Through-Package-Vias (TPVs) in Ultra-Thin Glass Substrates*** Sukhadha Viswanathan, Timothy B. Huang, Kaya Demir, P. Markondeya Raj, Fuhan Liu, Venky Sundaram, and Tummala Rao – Georgia Institute of Technology; Tomonori Ogawa – Asahi Glass Co., Ltd.	***2. 1:55 PM - Bismuth-Based Transient Liquid Phase (TLP) Bonding as High-Temperature Lead-Free Solder Alternatives*** Junghyun Cho, Roozbeh Sheikhi, and Sandeep Mallampati – Binghamton University; Liang Yin and David Shaddock – General Electric Co.
3. 2:20 PM - Reliability of eWLB (embedded wafer level BGA) for Automotive Radar Applications Daniel Yap, Kim Sing Wong, and Luc Petit – STMicroelectronics; Yaojian Lin, Roberto Antonicelli, and Seung Wook Yoon – STATS ChipPAC, Inc.	***3. 2:20 PM - Reliability Evaluations on 3D ID Package Beyond JEDEC*** Raghunandan Chaware, Laurene Yip, Inderjit Singh, Kenny Ng, Michael Shen, and Antai Xu – Xilinx, Inc.	***3. 2:20 PM - Silver Sinter Paste for SiC Bonding with Improved Mechanical Properties*** Wolfgang Schmitt and Ly May Chew – Heraeus Deutschland GmbH & Co. KG
Refreshment Break: 2:45 p.m. - 3:30 p.m. Southern Hemisphere Foyer		
4. 3:30 PM - Packaging Innovations for High Voltage (HV) GaN Technology Dibyajat Mishra, Vivek Arora, Luu Nguyen, Shoichi Iriguchi, Hiroyuki Sada, Laura Clemente, Sueann Lim, Hung-Yun Lin, Siva Gurrum, Alok Lohia, J. Sauser and S. Spencer – Texas Instruments, Inc.	***4. 3:30 PM - Remarkable Suppression of Local Stress in 3D IC by Manganese Nitride-Based Filler with Large Negative CTE*** Hisashi Kino, Takafumi Fukushima, and Tetsu Tanaka – Tohoku University	***4. 3:30 PM - Diffusion Barrier Effect of Ni-W-P and Ni-Fe UBMs during High Temperature Storage*** Li-Yin Gao and Zhi-Quan Liu – Chinese Academy of Sciences; Li Liu, Jing Wang, Zhao-Xia Zhou, and Chang-Qing Liu – Loughborough University
5. 3:55 PM - Thin-Film Magnetic Inductors for Integrated Power Management Annamalai Arasu Muthukumaraswamy, King-Jien Chui, Wei Yi Lim, Serine Soh, Jun Yu, Yew Wing Leong, Huamao Lin, and Sunil Wickramanayaka – Institute of Microelectronics, A*STAR	***5. 3:55 PM - Electrical Characterization of CMP-Less Via-Last TSV under Reliability Stress Conditions*** Mingbin Yu – Institute of Microelectronics, A*STAR	***5. 3:55 PM - Study of C2W Bonding Using Cu Pillar with Side-Wall Plated Solder*** Ling Xie, Sunil Wickramanayaka, Vasarla Nagendra Sekhar, and Daniel Ismael Cereno – Institute of Microelectronics, A*STAR
6. 4:20 PM - Feasibility Investigations on Selective Laser Melting for the Development of Microchannel Cooling in Power Electronics Aarief Syed-Khaja, Antonio Perinan Freire, Christopher Kaestle, and Joerg Franke – Friedrich Alexander University	***6. 4:20 PM - A Novel Failure Analysis Technique for Semiconductor Packaging by Xenon Difluoride Gas*** Hongqing Zhang Zhang, Frank Pompeo, and Tom Wassick – IBM Corporation	***6. 4:20 PM - Fabrication and Characterization of Nanoporous Metallic Interconnects Using Electrospun Nanofiber Template and Electrochemical Deposition*** Sheng-Po Fang, Seahee Hwangbo, Hyowon An, and Yong-Kyu Yoon – University of Florida
7. 4:45 PM - POL-kw Modules for High Power Applications Liang Yin, Kaustubh Nagarkar, Arun Gowda, Christopher Kapusta, Paul Gillespie, Tammy Johnson, Risto Tuominen, and Donna Sherman – General Electric Co.; Shingo Hayashibe, Hitoshi Ito, and Tadashi Arai – Shinko Electric Industries Co., Ltd.	***7. 4:45 PM - Alternative 3D Small Form Factor Methodology of System in Package for IoT and Wearable Devices Application*** Mike Tsai, Albert Lan, Chi Liang Shih, Terence Huang, Ryan Chiu, S. L. Chung, J. Y. Chen, Frank Chu, Cheng Kai Chang, Sheng Ming Yang, Daniel Chen, and Nicholas Kao – Siliconware Precision Industries Co., Ltd.	***7. 4:45 PM - Ga Liquid Metal Embrittlement for Fine Pitch Interconnect Rework*** Elodie Nguena, David Danovitch, and Malak Kanso – University of Sherbrooke; Richard Langlois – IBM Corporation

Program Sessions: Friday, June 2, 1:30 p.m. - 5:10 p.m.

Session 34: Waveguide Devices and Chip-to-Fiber Packaging	Session 35: Thermomechanical and Thermal Characterization	Session 36: Advances in Signal and Power Integrity
Committee: Optoelectronics	**Committee: Thermal/Mechanical Simulation & Characterization**	**Committee: High-Speed, Wireless & Components**
Room: Southern Hemisphere III	**Room: Southern Hemisphere V**	**Room: Americas Seminar**
Session Co-Chairs: **Ping Zhou – LDX Optronics, Inc.** **Hiren Thacker**	**Session Co-Chairs:** **Pradeep Lall – Auburn University** **Przemyslaw Gromala – Robert Bosch GmbH**	**Session Co-Chairs:** **Zhaoqing Chen – IBM Corporation** **Amit P. Agrawal – Keyssa Inc.**
1. 1:30 PM - Design, Fabrication and Connectorization of High-Performance Multimode Glass Waveguides for Board-Level Optical Interconnects Lars Brusberg, Davide Fortusini, Wei Jiang, Aramais Zakharian, Sergey Kuchinsky, Christian Fiebig, Shenping Li, Andrey Kobyakov, and Alan Evans – Corning, Inc.; Henning Schröder – Fraunhofer IZM	***1. 1:30 PM - The Combined Effect of Mechanical Package Stress and Humidity on Chip Corrosion Probability*** Georg Lorenz and Michél Simon-Najasek – Fraunhofer IMWS; Achim Lindner – TDK-Micronas GmbH	***1. 1:30 PM - Active and Passive Techniques for Noise Sensitive Circuits in Integrated Voltage Regulator Based Microprocessor Power Delivery*** Amit Jain, Sameer Shekhar, and Yan Z. Li – Intel Corporation
2. 1:55 PM - Axially Tapered Circular Core Polymer Optical Waveguides Enabling Highly Efficient Light Coupling Takaaki Ishigure, Kenji Katori, Hoshihiko Toda, and Kazuki Yasuhara – Keio University	***2. 1:55 PM - Mechanical Characterization of Anodic Bonding Using Chevron Microchannel*** David C. Woodrum, Mohammed Nasr, Xuchen Zhang, Muhannad S. Bakir, and Suresh K. Sitaraman – Georgia Institute of Technology	***2. 1:55 PM - High Voltage Capacitors for Next-Generation Power Modules in Electric Vehicles*** Robert Spurney, Himani Sharma, P. M. Raj, and Rao Tummala – Georgia Institute of Technology; Naomi Lollis – AVX Corporation
3. 2:20 PM - First Demonstration of Single-Mode Polymer Optical Waveguides with Circular Cores for Fiber-to-Waveguide Coupling in 3D Glass Photonic Interposers Rui Zhang, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology	***3. 2:20 PM - Package-Level Si Micro-Fluid Cooler with Enhanced Jet Array for High Performance 3D Systems*** Yong Han, Boon Long Lau, and Gongyue Tang – Institute of Microelectronics, A*STAR; Seow Meng Low and Jason Goh – BeCe Pte. Ltd.	***3. 2:20 PM - Package and Printed Circuit Board Design of a 19.2 Gb/s Data Link for High-Performance Computing*** Sungjun Chun, Jose Hejase, Junyan Tang, Jean Audet, Dale Becker, Daniel Dreps, Glen Wiedemeier, Megan Nguyen, Lloyd Walls, Francesco Preda, and Daniel Douriet – IBM Corporation
Refreshment Break: 2:45 p.m. - 3:30 p.m. Southern Hemisphere Foyer		
4. 3:30 PM - 3D Optical Coupling Techniques on Polymer Waveguides for Wafer and Board Level Integration Sebastian Lüngen, Sujay Charania, Tobias Tiedje, Krzystof Nieweglowski, Sebastian Killge, Lukas Lorenz, Johann W. Bartha, and Karlheinz Bock – Technical University Dresden	***4. 3:30 PM - A Unified and Versatile Model Study for Moisture Diffusion*** Liangbiao Chen, Jenny Zhou, Hsing-wei Chu, and Xuejun Fan – Lamar University	***4. 3:30 PM - Signal and Power Integrity Analysis of High-Speed Links with Silicon Interposer*** Wendemagegnehu Beyene, Nitin Juneja, Yeon-Chang Hahm, Ravi Kollipara, and Joohee Kim – Rambus, Inc.
5. 3:55 PM - Position Dependence of Coupling Efficiency of Grating Coupler in Waveguide Cavity Shogo Ura, Kazuki Mori, Ryo Tsujimoto, and Junichi Inoue – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science & Technology	***5. 3:55 PM - Microstructure Simulation and Thermo-Mechanical Behavior Analysis of Copper Filled through Silicon Vias Using Coupled Phase Field and Finite Element Methods*** Shui-Bao Liang, Chang-Bo Ke, Han Jiang, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology	***5. 3:55 PM - Novel Parallel Resonance Peak Measurement and Lossy Transmission Line Modeling of 2-T and 3-T MLCC Capacitors for PDN Application*** Larry Smith, Javid Mohamed, Jaemin Shin, and Tim Michalka – Qualcomm Technologies, Inc.
6. 4:20 PM - Efficient, Easy-to-Use, Planar Fiber-to-Chip Coupling Process with Angle-Polished Fibers Djorn Karnick, Nils Bauditsch, Lars Eisenblätter, Thomas Kühner, Marc Schneider, and Marc Weber – Karlsruhe Institute of Technology (KIT)	***6. 4:20 PM - On the Process/History Dependence of Package Mechanical Performance*** Mingji Wang, Lou Nicholls, MiNa Mo, MinJae Lee, Quan Pham, and Yong Song – Amkor Technology, Inc.	***6. 4:20 PM - Eye-Diagram Estimation Methods for Voltage- and Probability-Dependent PAM-4 Signal on Stacked Through-Silicon Vias*** Junyong Park, Jonghoon J. Kim, Sumin Choi, Youngwoo Kim, and Joungho Kim – Korea Advanced Institute of Science & Technology; Heegon Kim – MST
7. 4:45 PM - Novel, High-Throughput, Fiber-to-Chip Assembly Employing Only Off-the-Shelf Components Nicolas Boyer, Alexander Janta-Polczynski, Stephan Martel, Swetha Kamlapurkar, Sebastian Engelmann, Paul Fortier, and Tymon Barwicz – IBM Corporation; Jean-Francois Morissette – Université de Sherbrooke; Ted Lichoulas – AFL Telecommunications	***7. 4:45 PM - Systematic Approach to Design High Power FPGA Package for Current-Carrying Capability*** Hong Shi, Siow Chek Tan, Jae-Gyung Ahn, Gamal Refai-Ahmed, and Suresh Ramalingam – Xilinx, Inc.	***7. 4:45 PM - Signal Integrity Modelling in Inhomogeneous Waveguide/PCB of Arbitrary Shape Using Broadband Green's Function*** Kung-Hau Ding – Air Force Research Laboratory; Tien-Hao Liao and Leung Tsang – University of Michigan

Wednesday, May 31, 2017
Session 37: Interactive Presentations 1
9:00 AM - 11:00 AM
Committee: Interactive Presentations
Room: Northern Hemisphere Foyer
Session Co-Chairs:
Rao Bonda – Amkor Technology
John Hunt – Advanced Semiconductor Engineering, Inc.
Deborah S. Patterson – Principal, Patterson Group
Andy Tseng – JSR Micro

1) Package-Level EMI Shielding Technology with Silver Paste for Various Applications
Kisu Joo, Tae-Ryong Kim, Jung Woo Hwang, Jin-Ho Yoon, and Se Young Jeong – Ntrium Incorporation; Myung Jin Yim – Intel Corporation

2) Effects of Current Stress for Low Temperature Cu/Sn/Cu Solid-State-Diffusion Bonding
Jian Cai, Qian Wang, and Zijian Wu – Tsinghua University; Junqiang Wang and Dejun Wang – Dalian University of Technology

3) High Throughput Low Stress Air Jetting Carrier Release for RDL First Fan-Out Wafer Level Packaging
Hao Tang, Gary Shi, and Raphael He – Micro Materials Inc.; Ming Yin, Wei Zhang, and My Nguyen – Zhejiang Microtech; Mike Chang and Sheng-Shu Yang – ITRI

4) 48×10 Gbps Cost-Effective FPC Based On-Board Optical Transmitter with PGA Connector
Teng Li, Gonzalo Guelbenzu de Villota, Chenhui Li, R. Patty Stabile, and Oded Raz – Eindhoven University of Technology; Sander Dorrestein – TE Connectivity

5) A Novel Wafer Level Integration of Liquid-Metal Injection based TSV and Integrated Passive Devices
Tao Zheng, Gaowei Xu, and Le Luo – Shanghai Institute of Microsystem and Information Technology

6) Next Generation Plating Technologies for FO-Panel Level Packaging
Ralph Zoberbier, James Welsh, Christian Ohde, and Henning Huebner – Atotech Deutschland GmbH

7) A Density Staggered Cantilever for Micron Length Gravity Probing
Qidong Wang and Liqiang Cao – Institute of Microelectronics/ Stanford University; Alexander D. Rider, David C. Moore, Charles P. Blakemore, and Giorgio Gratta – Stanford University

8) Scalability and Yield in Elastomer Stamp Micro-Transfer-Printing
David Gomez, Kanchan Ghosal, Matthew A. Meitl, Salvatore Bonafede, Carl Prevatte, Tanya Moore, Erich Radauscher, Antonio Jose Trindade, and Christopher A. Bower – X-Celeprint

9) Dynamic Strain of Ultrasonic Cu and Au Ball Bonding Measured In-situ by Using Silicon Piezoresistive Sensor
Keiichiro Iwanabe, Kenichi Nakadozono, Mamoru Sakamoto, and Tanemasa Asano – Kyushu University

10) High Transmittance Broadband THz Polarizer Using 3D-IC Technologies
Nai-Chen Chi, Ting-Yang Yu, Hsin-Cheng Tsai, Chih-Wei Luo, Kuan-Neng Chen, and Yu-Tao Yang – National Chiao Tung University; Shiang-Yu Wang – Academia Sinica

11) High Accuracy Thermal Compression Bonding Technology for Large-Sized Substrate
Noboru Asahi, Toshiyuki Jinda, Yoshihito Mizutani, Koichi Imai, Hikaru Tomita, Mikio Kawakami, Masafumi Senda, Katsumi Terada, and Yasunori Hashimoto – Toray Engineering Co., Ltd.

12) Real-Time Color-Tunable White LEDs Through Combination of Phosphor Patterns and Adaptive Liquid Lens
Huai Zheng and Sheng Liu – Wuhan University; Zefeng Zhang and Peng Yang – Huazhong University of Science & Technology

13) Yield Comparison of Die-First Face-Down and Die-Last Fan-Out Wafer Level Packaging
Amy Lujan – SavanSys Solutions LLC

14) Multi Beam Full Cut Dicing of Thin Si IC Wafers
Jeroen van Borkulo, Paul Verburg, and Richard van der Stam – ASM Pacific Technologies

15) A New Method for 3D Microstructure Fabrication via Ionic Wind
Shangru Zhou, Guoliang Li, Huai Zheng, and Sheng Liu – Wuhan University

16) A Unique Temporary Bond Solution Based on a Polymeric Material Tacky at Room Temperature and Highly Thermally Resistant Application Extension from 3D-SIC to FOWLP
Alain Phommahaxay, Goedele Potoms, Julien Bertheau, Pieter Bex, Fabrice Duval, Arnita Podpod, Teng Wang, Greet Verbinnen, Gerald Beyer, Erik Sleeckx, Eric Beyne – IMEC; Atsushi Nakamura – Fujifilm Electronic Materials Europe N.V.; Yoshitaka Kamochi – Fujifilm Corporation

17) 3D Printed Out-of-Plane Antennas for Use on High Density Boards
Mohd Ifwat Mohd Ghazali, Saranraj Karuppuswami, Amanpreet Kuar, Jennifer Byford, James Lennon, and Premjeet Chahal – Michigan State University

Wednesday, May 31, 2017
Session 38: Interactive Presentations 2
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Room: Northern Hemisphere Foyer
Session Co-Chairs:
Nam Pham – IBM Corporation
Patrick Thompson – Texas Instruments, Inc.
Eric Beyne – IMEC
Richard Rao – MicroSemi

1) Exploring DDR4 Address Bus Design for High Speed Memory Interface
Nanju Na, Juan Wang, Sean Long, Changyi Su, Thomas To, and Yong Wang – Xilinx, Inc.

2) Demonstration of High Electrical Reliability of Sub-2 Micron Cu Traces Covered with Inorganic Dielectrics for Advanced Packaging Technologies
Hiroshi Kudo, Ryohei Kasai, Jyunichi Suyama, Mitsuhiro Takeda, Yumi Okazaki, Haruo Iida, Daisuke Kitayama, Toshio Sasao, Kouji Sakamoto, Hiroaki Sato, Shouhei Yamada - Dai Nippon Printing Co., Ltd.

3) The Comparison of Package Design and Electrical Analysis in Mobile Application
Tsun-Lung Hsieh, Po-Chih Pan, Chih-Yi Huang, Ming-Fong Jhong, and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.; Yuan-Hsi Chou – University of Texas, Austin

4) Multi-band Harmonic RF Tags for Barcode Applications in a Cluttered Environment
Saranraj Karuppuswami, Mohd Ifwat Mohd Ghazali, Amanpreet Kaur, and Premjeet Chahal – Michigan State University

5) High-Band AlN Based RF-MEMS Resonator for TSV Integration
Nan Wang, Yao Zhu, Chengliang Sun, Mingbin Yu, Geng Li Chua, Srinivas Merugu, Navab Singh, and Yuandong Gu – Institute of Microelectronics, A*STAR

6) Equalization Enhancement Approaches for PAM4 Signaling for Next Generation Speeds
Jiayi He, Nana Dikhaminjia, Mikheil Tsiklauri, and James Drewniak – Missouri University of S&T; Bhyrav Mutnury and Arun Chada – Dell, Inc.

7) Data Transfer Performance Analysis and Enhancement of Critical 3D Interconnects in a 3D SIP based on Communication Channel Modeling Methodology
Min Miao, Zhensong Li, Xiaoyang Duan, and Tianfang Chen – Beijing Information Science and Technology University; Xiaole Cui, Yufeng Jin, Huan Liu, and Xin Sun – Peking University

8) A Characterization Method for Interfacial Delamination of Copper/Epoxy Mold Compound Specimens Under Mixed Mode I/III Loading
V N N Trilochan Rambhatla, David Samet, Scott R. McCann, and Suresh K. Sitaraman – Georgia Institute of Technology

9) Low Temperature Ultrasonic Bonding of Cu/Sn Microbumps with Au Layer for High Density Interconnection Applications
Qinghua Zeng, Yong Guan, Jing Chen, and Yufeng Jin – Peking University

10) Chip-Scale SERF Atomic Magnetometer without Magnetic Shield
Ling Lu, Jintang Shang, Zhihua Pan, and Yu Ji – Southeast University

11) Numerical Simulations of Joint-to-Joint Temperature Variation during Thermo-Compression Bonding
Depayne Athia and Michael Mayer – University of Waterloo; Alireza Rezvani, Horst Clauberg, and Ivy Qin – Kulicke and Soffa, Inc.

12) The Complete Packaging Reliability Studies through One Digital Image Correlation System
Yuling Niu and Jing Wang – State University of New York at Binghamton; Seungbae Park – State University of New York, Binghamton

13) Resistometric Characterization of the Interface between Au Wire Bonds to AlCuW Bond Pads
Steve Kilgore and Craig Gaw – NXP Semiconductors

14) Comparison and Consistency of On-PCB Microstrip Line Modeling by 3D Fullwave and 2D Quasi-Static Approaches for High Speed Packaging System Signal Integrity Simulations
Zhaoqing Chen – IBM Corporation

15) Real-Time Diagnosis of Wire Degradation Based on Digital Signal Analysis
Jinwoo Lee and Daeil Kwon – Ulsan National Institute of Science & Technology

Thursday, June 1, 2017
Session 39: Interactive Presentations 3
9:00 AM - 11:00 AM
Committee: Interactive Presentations
Room: Northern Hemisphere Foyer
Session Co-Chairs:
Mark Eblen – Kyocera America, Inc.
Swapan Bhattacharya – Engent Inc.
Tz-Cheng Chiu – National Cheng Kung University
Frank Wei – Disco Japan

1) Electrical Transmission Properties of HBM Interface on 2.1-D System in Package Using Organic Interposer
Yutaka Uematsu and Nobuyuki Ushifusa – Hitachi, Ltd.; Hitoshi Onozeki – Hitachi Chemical Co., Ltd.

2) The Use of Single Layer MIS in Modern Assembly
Kohan Lin, Albert Lan, Mark Liao, and Boxiang Fang – Siliconware Precision Industries Co., Ltd.

3) Physical and Electrical Characterization of 3D Embedded Capacitor: A High-Density MIM Capacitor Embedded in TSV
Ye Lin and Chuan Seng Tan – Nanyang Technological University

4) Electrical and Thermal Simulation of SWIFT™ High Density Fan-out PoP Technology
Curtis Zwenger, Bora Baloglu, George Scott, and Mike Kelly – Amkor Technology, Inc.; WonChul Do, JiHun Yi, and WonGeol Lee – Amkor Technology, Korea

5) High Reliability Challenges with Cu Wire Bonding for Automotive Devices in the AEC-Q006
JunHo Jeon, SungHo Jeon, SeokHo Na, Mina Mo, Kwangmo Lim, DaeByoung Kang, and JinYoung Kim – Amkor Technology, Inc.

6) Development of Die Attachment Technology for Power IC Module by Introducing Indium into Sintered Nano-Silver Joint
Chun An Yang and C. Robert Kao – National Taiwan University; Hiroshi Nishikawa – Osaka University

7) Effect of Nickel-Coating Modified CNTs on the Dopant Dispersion and Performance of BGA Solder Joints
Huayu Sun and Yan-Cheong Chan – City University of Hong Kong; Xiao Hu – HiSilicon Technologies; Fengshun Wu – Huazhong University of Science and Technology

8) Assessing the Reliability of High Temperature Solder Alternatives
Maan Z. Kokash, Rajesh S. Sivasubramony, Jorge L. Then Cuevas, Angelo F. Zamudio, and Peter Borgesen – Binghamton University; Alfred A. Zinn, Randall M. Stoltenberg, Jerome Chang, Y.-L. Tseng, and Dan Blass – Lockheed Martin

9) High Performance Silver Alloy Bonding Wire for Memory Devices
Tetsuya Oyamada, Tomohiro Uno, and Takashi Yamada – Nippon Steel & Sumitomo Metal Corporation; Daizo Oda – Nippon Micrometal Corporation

Wednesday & Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 10-17 for location.

10) Low Pressure Solid-State Bonding Using Silver Preforms for High Power Device Packaging
Jiaqi Wu and Chin C. Lee – University of California, Irvine

11) Fabrication, Characterization and Comparison of FR4-Compatible Composite Magnetic Materials for High Efficiency Integrated Voltage Regulators with Embedded Magnetic Core Micro-Inductors
Mohamed Bellaredj, Sebastian Mueller, Anto Davis, Paul Kohl, and Madhavan Swaminathan – Georgia Institute of Technology; Yasuhiko Mano – Ibiden

12) The Novel Failure Mechanism of the Polymer Ball Interconnected CBGA under Board Level Thermal Mechanical Stress
Jeffrey ChangBing Lee, Cheng-Chih Chen, Dem Lee, Cherie Chen, and Alice Lin – iST-Integrated Service Technology, Inc.

13) Development of Double Side Protection Process with Bump Support Film (BSF) and Backside Coating Tape for WLP
Masanori Yamagishi, Tomotaka Morishita, Motoki Nozue, Akinori Sato, Keisuke Shinomiya, and Shinya Takyu – Lintec Corporation

14) Design of Miura Folding-Based Micro-Supercapacitors as Foldable and Miniaturized Energy Storage Units
Bo Song, Yun Chen, Kyoung-sik Moon, and C. P. Wong – Georgia Institute of Technology

15) Assembly and Reliability Challenges for Next Generation High Thermal TIM Materials
Chi-An Pan, Chi-Tung Yeh, Wei-Chun Qiu, Rong-Zheng Lin, Liang-Yih Hung, Kong-Toon Ng, C. F. Lin, C. Key Chung, Don-Son Jiang, and C. S. Hsiao – Siliconware Precision Industries Co., Ltd.

16) Low Temperature Curable Polyimide Film Properties and WLP Reliability Performance with Various Curing Conditions
Yu Chuan (Steven) Chen, Katch Wan, Chen An Chang, and Rick Lee – Siliconware Precision Industries Co., Ltd.

17) The Effect of Polymer Rebound on SnBi58 Solder ACFs Joints Cracks during a Thermo-Compression Bonding
Shuye Zhang and Kyung-Wook Paik – Korea Advanced Institute of Science & Technology

Thursday, June 1, 2017
Session 40: Interactive Presentations 4
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Room: Northern Hemisphere Foyer
Session Co-Chairs:
Ibrahim Guven – Virginia Commonwealth University
Mark Poliks – Binghamton University
Nancy Iwamoto – Honeywell
Jai Agrawal – Purdue University

1) Equivalent Thermal Conductivity Model Based Full Scale Numerical Simulation for Thermal Management in Fan-Out Packages
Ningyu Wang, Yudan Pi, Wei Wang, and Yufeng Jin – Institute of Microelectronics, Peking University

2) Local Stress Analysis by XRD Single Crystal Method and Kossel Diffraction Applied to a Flip Chip Structure
Anne-Laure Lebaudy, Manuel Fendler, and Wiyao Kpobie – CEA-Leti; Raphaël Pesci – Ecole Nationale Supérieure des Arts et Métiers

3) Study of Annular Copper Filled TSVs of Sensor and Interposer Chips for 3D Integration
Cao Li and Peng Fei – Huazhong University of Science & Technology; Sheng Liu and Huai Zheng – Wuhan University

4) Investigations on the Pumping Behaviors of Copper Filler in Through-Silicon-vias (TSV)
Fei Su, Ruixia Yao, Tenghui Li, and Xiaoxu Pan – Beijing University of Aeronautics and Astronautics

5) Warpage Prediction Methodology of Extremely Thin Packages
Zhongli Ji, Yangming Liu, Anna Wu, Ning Ye, Hem Takiar, and Peng Chen – SanDisk

6) A Design Study of 5G Antennas Optimized Using Genetic Algorithms
VIncens Gjokaj, John Doroshewitz, Jeffrey Nanzer, and Premjeet Chahal – Michigan State University

7) Cu-In-Microbumps for Low-Temperature Bonding of Fine-Pitch-Interconnects
Steffen Bickel, Iuliana Panchenko, Joerg Meyer, and Volker Neumann – Technical University Dresden; Wieland Wahrmund and M. Juergen Wolf – Fraunhofer IZM

8) Via-in-Trench: A Revolutionary Panel-Based Package RDL Configuration Capable of 200-450 IO/mm/layer, an Innovation for More-than-Moore System Integration
Fuhan Liu, Chandrasekharan Nair, Hao Lu, Rui Zhang, Hang Chen, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Atsushi Kubo and Tomoyuki Ando – Tokyo Ohka Kogyo; Kwon Sang Lee – Disco Corporation

9) Simulation Analysis of a Conformal Patch Sensor for Skin Tension and Swelling Detection
Ruiqi Lim, Ming-Yuan Cheng, Ramona Damalerio, and Weiguo Chen – Institute of Microelectronics, A*STAR

10) Effect of Material Properties of Double Layer Non Conductive Films (D-NCFs) on the Reflow Reliability of Ultra Fine-Pitch Cu-Pillar/Sn-Ag Micro Bump Interconnection
SeYong Lee, JiWon Shin, and Kyung-Wook Paik – Korea Advanced Institute of Science & Technology; Woojeong Kim and Taejin Choi – Doosan

11) Wafer-Level Micro Alkali Vapor Cells with Anti-Relaxation Coating Compatible with MEMS Packaging for Chip-Scale Atomic Magnetometers
Yu Ji, Jintang Shang, Qi Gan, and Lei Wu – Southeast University

12) Low-Temperature High-Throughput Assembly Technology for Transducer Array in Medical Imaging Applications
Hoang-Vu Nguyen, Nu Bich Duyen Do, and Knut Aasmundtveit – University College of Southeast Norway

13) Highly Efficient and Stable Quantum Dot Light Emitting Diodes Optimized by Micro-Packaged Luminescent Microspheres
Kai Wang and Xiaowei Sun – Southern University of Science and Technology; Xiaobing Luo – Huazhong University of Science and Technology; Sheng Liu – Wuhan University

Friday, June 2, 2017
Session 41: Student Interactive Presentations
8:30 AM - 10:30 AM
Committee: Interactive Presentations
Room: Northern Hemisphere Foyer
Session Co-Chairs:
Yang Liu – IBM Corporation
Li Ming – ASM
Vaidyanathan Chelakara – Ciena Corporation
Suresh K. Sitaraman – Georgia Institute of Technology

1) Stress Analysis of Flexible Packaging for the Integration of Electronic Components within Woven Textiles
Menglong Li, John Tudor, Russel Torah, and Steve Beeby – University of Southampton

2) Signal Integrity Analysis of Silicon/Glass/Organic Interposers for 2.5D/3D Interconnects
Sumin Choi, Joungho Kim, Junyong Park, and Daniel H. Jung – Korea Advanced Institute of Science & Technology; Heegon Kim – Missouri S&T; Kiyeong Kim – Samsung Electronics Company, Ltd.

3) A Study on the Fabrication of Electrical Circuits on Fabrics using Cu pattern Laminated B-stage adhesive Films for Electronic Textile Applications
Seung-Yoon Jung and Kyung-Wook Paik – Korea Advanced Institute of Science & Technology

4) Electrically Testing Non-Underfilled Flip Chip Assemblies- Impacts on Interconnect Integrity
Antoine Cloutier and David Danovitch – Université de Sherbrooke; Benoit Foisy – IBM Corporation

5) Effects of Anisotropic Conductive Films (ACFs) Gap Heights on the Bending Reliability of Chip-in-Flex (CIF) Packages for Wearable Electronics Applications
Ji-Hye Kim, Tae-Ik Lee, Dal-Jin Yoon, Taek-Soo Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science & Technology

6) A Study on the Fine Pitch Flex-on-Flex (FOF) Assembly Using Flux Added Nanofiber Solder Anisotropic Conductive Films (ACFs) and Thermo-Compression Bonding Method
Ji-Soo Lee, Ji-Hye Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science & Technology

7) Infrared (IR) Soldering of Metallic Nanowires
Jirui Wang, Fan Gao, and Zhiyong Gu – University of Massachusetts, Lowell

8) Stretchable and Electrically Conductive Composites Fabricated from Polyurethane and Silver Nano/Microstructures
Bo Song, Kyoung-sik Moon, and C. P. Wong – Georgia Institute of Technology

9) Numerical and Experimental Study of Fan-Out Wafer Level Package Strength
Cheng Xu and Zhaowei Zhong – Nanyang Technological University; Won Kyoung Choi – STATS ChipPAC, Inc.

10) Effects of Passivation Layer and Electroplating Parameters of Copper Film on Wafer Warpage during Thermal Process
Gong Cheng, Heng Li, Weibo Zhang, Gaowei Xu, and Le Luo – Shanghai Institute of Microsystem and Information Technology

11) Development of Mechanical Locking Micro-Anchor Structures for a QFN Package Application
Yu-Lung Huang, Wei-Chih Lin, Mano Ajayan, and Bao-Hui Chang Chien – National Sun Yat-Sen University

12) Reliability of Cu/NiFe and Cu/Ni Metaconductor Devices for RF Applications
Timothy Clingenpeel and Yong-Kyu Yoon – University of Florida

13) A New Fan-Out Package Structure Utilizing the Self-Alignment Effect of Molten Solder to Improve the Die Shift and Enhance the Thermal Properties
Hwan-Pil Park, Jae-Yong Park, Gwancheol Seo, and Young-Ho Kim – College of Engineering / Hanyang University

14) Toughening Underfills by Stress-Absorbing Core-Shell Fillers
Chia-Chi Tuan, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology

15) Thermal Characteristic of Sn-MWCNT Nanocomposite Solder in LED Package
Choong-Jae Lee, Jae-Jung Moon, Kwang-Ho Jung, and Seung-Boo Jung – Sungkyunkwan University

16) An Evaluation of Effects of Molding Compound Properties on the Reliability of Ag Wire Bonded Components
Keisuke Yazawa – Purdue University; Carol Handwerker, John Blendell, Alexander Campbell, Wenhao Chen, Azzedin Jackson, and Matthew Parsons – Purdue Univesity; Peng Su – Juniper Networks

17) A Nonlinear Transmission Line Based Harmonic RF Tag
Mohd Ifwat Mohd Ghazali, Saranraj Karuppuswami, Amanpreet Kaur, and Premjeet Chahal – Michigan State University

18) Numerical Analysis and Optimization of Thermal Performance of LED Filament Light Bulb
Jie Liu, Huai Zheng, and Sheng Liu – Wuhan University; Chunlin Xu – Huazhong University Of Science And Technology

19) Effective and Efficient Modeling of Differential Vias Using Semi-Empirical Approach
Fanghui Ren – Oregon State University; Kevin Cai, Chunchun Sui, Jayaprakash Balachandran, and Bidyut Sen – Cisco Systems, Inc.

20) Design of Low-Profile Integrated Transformer and Inductor for Substrate-Embedding in 1-5kW Isolated GaN DC-DC Converters
Haksun Lee, Vanessa Smet, Pulugurtha Markondeya Raj, and Rao Tummala – Georgia Institute of Technology

21) Stretchable Capacitive Strain Sensors Based on a Novel Polymer Composite Blend
Todd Houghton, Jignesh Vanjaria, Thomas Murphy, and Hongbin Yu – Arizona State University

22) Thermal and Mechanical Analysis of 3D Glass Packaging for Automotive Cameras
Daniel Struk, Peter Hesketh, Chintan Buch, Klaus Wolter, and Rao Tummala – Georgia Institute of Technology

23) Miniaturization of Planar Packaged Inductor Using NiZn and Low Cost Screen Printing Technique
Colin Pardue, Mohamed F. Bellaredj, Anto K. Davis, and Madhavan Swaminathan – Georgia Institute of Technology

Thursday & Friday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 14-21 for locations.

2017 TECHNOLOGY CORNER EXHIBITS AND INTERACTIVE PRESENTATIONS

Technology Corner Exhibits

Wednesday, May 31

9:00 a.m. - 12:00 Noon / 1:30 p.m. - 6:30 p.m.

Thursday, June 1

9:00 a.m. - 12:00 Noon / 1:30 p.m. - 4:00 p.m.

Northern Hemisphere A – C

Interactive Presentation Sessions

Wednesday, May 31

Session 37: 9:00 a.m. - 11:00 a.m. / Session 38: 2:00 p.m. - 4:00 p.m.

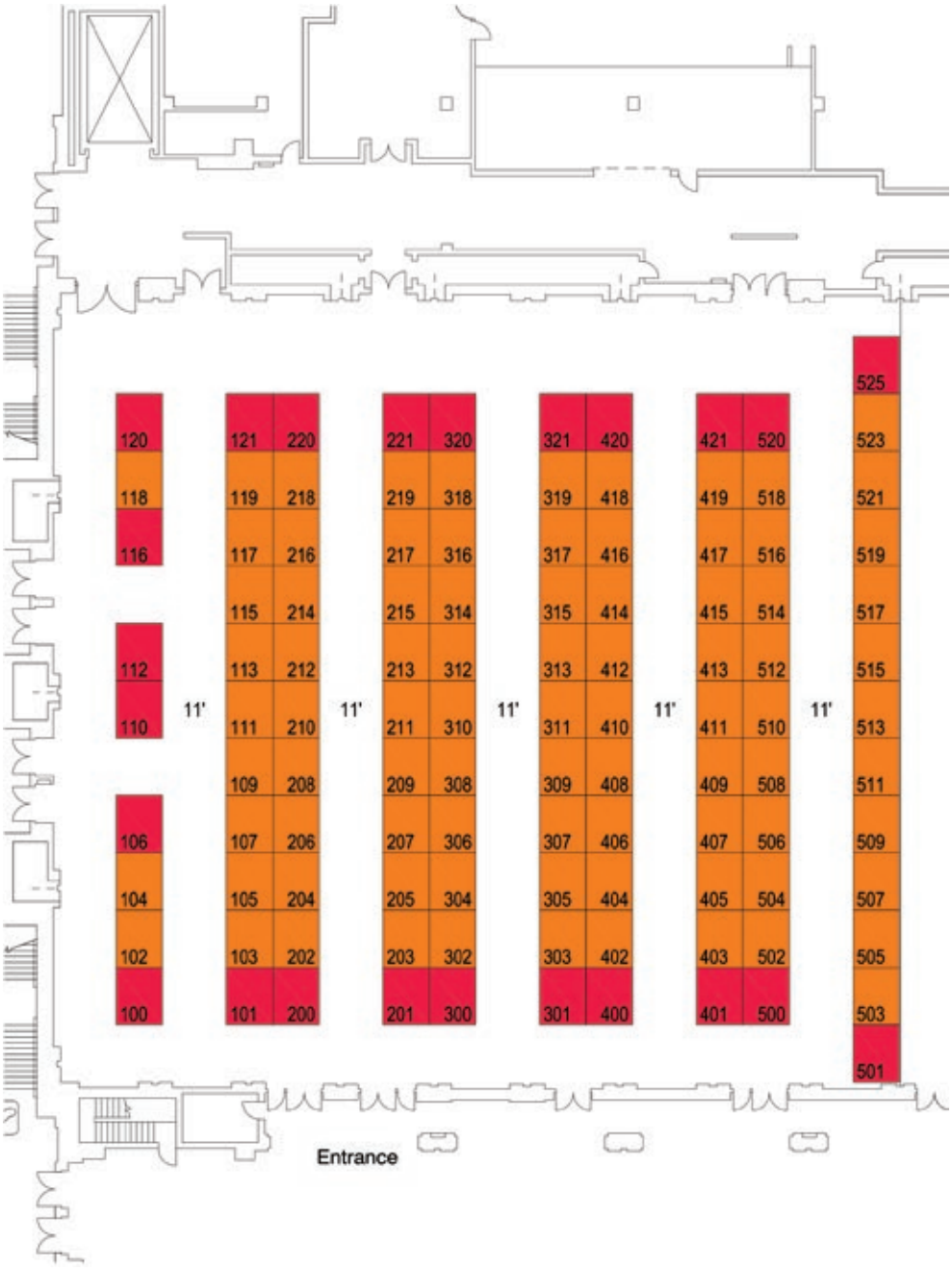
Thursday, June 1

Session 39: 9:00 a.m. - 11:00 a.m. / Session 40: 2:00 p.m. - 4:00 p.m.

Friday, June 2

Session 41: 8:30 a.m. - 10:30 a.m.

Northern Hemisphere Foyer, 5th Floor



TECHNOLOGY CORNER EXHIBITORS

3D Systems Packaging Research Center (PRC)
Georgia Institute of Technology
813 Ferst Drive, NW
Atlanta, GA 30332-0560
Phone: +1 404-894-9097
Fax: +1 404-894-3842
www.prc.gatech.edu
Contact: Dr. Venky Sundaram
Prof. Rao R. Tummala
Email: vs24@gatech.edu
rao.tummala@ece.gatech.edu
Booth 320

The 3D Systems Packaging Research Center (PRC) at the Georgia Institute of Technology is an Industry-Centric Global Academic Center dedicated to leading-edge research, education of highly-interdisciplinary students and global industry collaborations in the System-on-a-Package (SOP) vision to enable highly miniaturized, mega-functional systems in a single package. Led by Prof. Rao Tummala, the PRC's research encompasses advanced 3D systems packaging technologies including: electrical, mechanical and thermal design; ultra-thin and ultra-high density glass interposers and packages; ultrafine pitch chip-level and board-level interconnections; passive and active components and integration into power, RF, photonic and analog modules. The PRC model for industry collaboration is enabled by a world-class team of cross-disciplinary academic and research faculty, students, visiting industry engineers, and supply-chain manufacturers. The current industry consortium at PRC consists of the most comprehensive industry ecosystem of material and tool suppliers, substrate and assembly manufacturers, and end users in a wide variety of consumer and high performance applications including high performance cloud computing and networking. New applications being integrated into the consortium are new era of automotive electronics that include connectivity and infotainment, autonomous driving and all-electric cars requiring high power and high temperature electronics. Companies can join the PRC consortium for a single membership fee to access all the programs. Benefits to industry include intellectual property rights, technology transfer, access to students for recruiting, one-on-one company-to-faculty relationships, state-of-the-art R&D facilities, advanced technology prototypes, and more.

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AMICRA Microtechnologies is a worldwide leading supplier of high precision Die Attach Equipment specializing in submicron placement accuracy (±0.3µm@3s). Equipment offering supports both Die Attach and Flip Chip bonding processes including the following capability: in-situ eutectic bonding, dynamic alignment, heated tool, pulse heating, laser heating, volumetric and jet dispensing, active bond force control, high speed solutions, in-situ UV curing, 550x600mm bonding area, quantitative tilt calibration system,

etc. Market focus: Opto, Silicon Photonics, AOC, VCSEL, Laser Diode, WLP, 2.5D/3D IC, TSV, TCB, Fan-out/EWLP. Other products: High Speed Wafer Inking and inspection, Gel Fill Line and Custom Solutions.

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Amkor Technology is one of the world's largest and most accomplished providers of semiconductor packaging and test services. Founded in 1968, Amkor pioneered the outsourcing of IC assembly and test and is a strategic manufacturing partner for the world's leading semiconductor companies, foundries and electronics OEMs. Our solutions enable our customers to focus on semiconductor design and wafer fabrication while utilizing Amkor as their turnkey provider and their packaging technology innovator.Amkor's current operations include more than 10M ft^2 of floor space with production facilities, product development centers and sales & support offices located in key electronics manufacturing regions in Asia, Europe and the United States. Our broad package portfolio includes leadframe, ball grid array, chip scale and wafer level packaging. Also supported are specialty packaging with unique development and high volume production requirements (e.g., MEMS, sensors and SiP). Amkor is an industry leader in advanced packaging with development and production of large scale and complex 2.5/3D system solutions. Amkor's comprehensive manufacturing capability, scale and vision continue to strengthen our position as the "provider of choice" for semiconductor assembly and test. For more information, visitwww.amkor.com.

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Booths 523, 525

With a proven track record spanning over three decades, ASE, the OSAT market leader, continues its tradition of manufacturing expertise through orchestrated collaboration with customers, suppliers and partners, alike. Alongside a broad portfolio of established technologies, ASE is also delivering innovative advanced packaging, System-in-Package and MEMS solutions to meet growth momentum across a broad range of end markets. For more about our advances in Wire Bond, System-in-Package, Wafer Level Packaging, Fan Out, Flip Chip, MEMS & Sensors, and, 2.5D & 3D technologies, all ultimately geared towards applications to improve lifestyle and efficiency, please visit :www.aseglobal.com.

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AT&S is a leading HDI and IC substrate producer offering Embedded Component Packaging (ECP®) technology for embedding passives and bare ICs inside the laminate for IC packages and printed circuit boards. Embedding provides increased component density and smaller body size; improved signal integrity with embedded capacitors located just microns directly below the IC; thermal management with filled copper vias directly on the die backside; improved shock & drop robustness; and hidden components for security and reverse engineering resistance. Additional components can be mounted on the top and bottom surfaces and connected to the embedded components by copper-plated laser micro-vias. AT&S has six manufacturing sites in Austria (2), China (2), India, and South Korea. Embedding is available in the Leoben (Austria) factory and in 2017 will also be available in the Shanghai (China) factory. FC-BGA substrates are produced in the Chongqing (China) factory. AT&S announced participation in the Horizon 2020 EU Research and Innovation program to develop GaN-based modules targeting the production of demonstrator GaN power switches and CMOS drivers, as well as new magnetic core materials that will enable

switching frequencies up to 200 MHz. AT&S is also participating in the Panel-Level Packaging Consortium to implement fan-out panel-level packaging (FOPLP).

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The S3IP is a research and development organization that addresses research challenges in electronics packaging system design, process development, prototyping, and manufacturing for academia and the microelectronics industry. Located at Binghamton University, the Center brings together partners from government, industry and academia, providing opportunities for collaborations that will advance microelectronics research and development, with particular focus on electronics packaging design and manufacturing technology; thermal analysis and management for electronics; characterization of materials, surfaces, and physical interfaces for electronics devices and assemblies; and failure analysis and reliability improvement for electronics. Subject areas addressed include packaging of microelectronics, 2.5D/3D chip assemblies, power electronics, and integrated photonics.

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FlipChip International - Huatian (FCI-HT): FCI-HT supplies turnkey semiconductor assembly and test services to the consumer, automotive, industrial and medical industries. FCI-HT supports a wide range of customers, frequently partnering with them to engineer customized solutions including expedite bumping and backend services on Multi-Project Wafers. FCI-HT is a leader in wafer level packaging with patented technologies spanning from Cu Pillar Bumping, Spheron™ Wafer Level Chipscale Packaging, and ChipsetT™ Embedded Die Packaging. FCI-HT is a division of Huatian Technologies (HT). HT is among the top 6 OSATs in the world with over one billion dollars in annual revenue. It is listed on the Shenzhen Stock Exchange Market. Huatian has six ISO/TS16949 factories located in the US and China offering a complete range of semiconductor packaging and turnkey services.

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Interconnect Systems, Inc. (ISI), specializes in high-density module packaging and advanced system-level interconnect solutions. ISI offers design, qualification, and testing, coupled with fully integrated in-house manufacturing. Capabilities include: high-density PCB design, fine pitch SMT, flip chip, wirebond assembly, IC packaging, custom molding, over molding, and automated optical inspection.

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Invensas, a wholly owned subsidiary of Xperi Corporation (Nasdaq: XPER), is the world's leading provider of advanced semiconductor packaging and 3D interconnect technologies that enable the next generation of electronics products to be smaller, faster, lower power and contain more functionality. Invensas solutions can be found in DRAM memories, image sensors, RF devices, MEMS sensors, processors and mixed signal devices currently in high volume production at leading OEMs, ODMs, and IDMs and integrated into in billions of electronic products around the world, including smartphones, tablets, laptops, PCs and data center servers. Invensas technologies include ZiBond®, a low temperature wafer-to-wafer or die-to-wafer bonding, Direct Bond Interconnect (DBI®) wafer-to wafer or die-to-wafer bonding with electrical interconnect, Bond Via Array™ (BVA®) advanced Package-on-Package and System-in-Package solutions, and xFD® multi-die face-down packaging technology.

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Sanyu Rec Company Ltd. is a Japanese electronics material supplier to the semiconductor market place including LED market. With creative development and numerous proprietary technologies, SANYU REC contributes to these growth fields which are driven by environmental considerations and mobile applications. SANYU REC has provided a variety of products centering on encapsulation materials like liquid MUF (mold underfill) material to the market. Capillary underfill, die attach materials, and mold sheets are also in our main product lines. Not only these materials but also VPES (vacuum printing

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First Call for Papers

IEEE 68th Electronic Components and Technology Conference
www.ectc.net
To be held May 29 - June 1, 2018
at the Sheraton San Diego Hotel & Marina, San Diego, California, USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical program subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:
Fan-Out, 2.5 & 3D, TSV and Interposer, Heterogeneous Integration and SiP, Embedded and Advanced Substrates, MEMS & Sensors, Automotive, Power Module, Wearable & IoT, Bio and Medical, RF, Microwave, Millimeter-Wave & EMI, High Performance Computing and Data Center, Wafer Level & Panel Level Process, Advanced Flip-Chip, Advanced CSP and POP.

Applied Reliability:
Advanced Package Reliability (Including TSV/2.5D/3D Packaging, WCSP, Fan-Out, Embedded Technologies), Challenges in SiP Reliability, Interconnect Reliability (Including Flip-Chip, Wire-Bond), LED, RFID, High Voltage Packaging and IoT Reliability, System Level Reliability Testing/Modeling, Reliability Test Methods and Life Models, Physics of Failure, Failure Analysis Techniques and Materials Characterization, Drop and Dynamic Mechanical Reliability, Probabilistic Design for Reliability (PDfR), Automotive Reliability Requirements.

Assembly and Manufacturing Technology:
Embedded/Hybrid Package Manufacturing Process, Wearable/IoT Package Assembly, Healthcare/Fitness Component Assembly, Warpage Control/ Management in Board Level Assembly, Thin Die/Thin Mold/Thin Package Handling and Assembly, Large/Ultra Large Package (SiP, SIM, MCP) Integration and Processing, Panel Level Manufacturing for WLP, Dicing and Singulation.

Emerging Technologies:
Wearable and Medical Electronics, Flexible, Bendable, Stretchable, Disposable, or Dissolvable Packaging, Bio-Sensor Packaging, Implantable Device Packaging, New Materials and Methods for Packaging Microfluidics, MEMS and NEMS, Nano-Battery. 3D Printing, Self-Alignment and Assembly, New Additive Packaging Process Technologies and Materials. Novel Substrates, Materials and Approaches to Interconnects and Packaging, Packaging for Wireless, Photovoltaic, Redundancy, Repair, Security, Anti-Counterfeiting, Components for Internet of Things (IoT) and Smart Electronics, Heterogeneous Integration. Compact & Autonomous Sensor Packaging, Wafer Level Integrated Silicon Photonics.

High-Speed, Wireless & Components:
Modules & Sub-Systems; High-Speed, RF to THz Devices & Passive Components, Mixed-Signal; Electrical Modeling and Design; Advanced Components: Materials, Structures, Fabrication and Characterization; Power and Signal Integrity; High-Speed Data Transfer/Communications; Power Modules, Power Management; Integrated Voltage Regulators (IVR); LTE, WLAN, 5G, mm Wave and THz T/R Modules; Radars; Imagers; Wearable and Sensor Technologies for Internet of Things (IoT); Flexible Electronics; 3D Printed RF Components and Modules; Automotive Sensors; RF-MEMS, RF-Opto, RFID and Tagging; M2M Platforms; Proximity Sensors; Ambient Intelligence; Wireless Power; Wireless Sensor and Computing Nodes; Wearable and Biomedical Electronics.

Interconnections:
Interconnections: Fan-Out and Fan-In, Wafer- and Panel-Level Interconnects, 2.5D/3D, TSV Interconnect Structures for Heterogeneous Integration and SiP, Co-Designs and Process/Performance Trade-Off, Thermal/Mechanical/Electrical Tests & Reliability, Embedded Systems; Si/Glass/Organic Interposers, PoP, WLCSP, Flip-Chip, Solder Bumping and Cu Pillar, TC Bonding, IMC Interconnect, Wirebonds, RDL, Conductive Adhesives, Flexible Substrates, Power Modules, Wearables, Interconnects for Bio-Medical, Automotive, Bio-Sensor, Energy Harvesting, and Harsh Environments.

Materials & Processing:
Wafer Level Packaging, Panel Processing & Materials, Next Generation Packaging Substrates, Flexible and Wearable Electronics, Carbon Electronics, Battery Materials, 3D Materials and Processing, Emerging Electronic Materials, Novel Conductive and Non-Conductive Adhesives, Solder Alloys, Photoresist, Dielectrics and Under-Fill, Molding Compounds, Thermal Interface Materials, Optoelectronic Materials.

Thermal/Mechanical Simulation & Characterization:
Thermal, Mechanical Simulation and Characterization Including: Component, Board and System Level Modeling for Microelectronics, e.g., 3D Interconnects (TSV, Stacked Die, etc.), 2.5D Packaging (Si, Glass, Flexible Interposer, etc.), Wafer-Level-Package (WLP), Ball-Grid-Array (BGA), Embedded Packages with Active and Passive Components, System-in-Package (SiP), Power Electronic Modules, LED Packaging, and MEMS; Fab/Thin Wafer Handling, Wire Bonding and Assembly Manufacture Process; Reliability Modeling Related Fracture Mechanics, Fatigue, Electromigration, Warpage, Delamination/ Moisture, Drop Test, Material Constitutive Relations and Characterization; Novel Modeling Including Multi-Scale and Multi-Physics Techniques and Solutions; Measurement Methodologies, Characterization and Correlations.

Optoelectronics:
Integrated Photonics Modules, Fiber Optical Interconnects, Advanced Optical Connectors, Optical Waveguide Circuits, Optical Printed Circuit Board, Mid-Board/ On-Board Optical Modules, Silicon and III-V Photonics Packaging, Optical Chip-Scale and Heterogeneous Integration, Micro-Optical System Integration and Photonic System-in-Package, 3D Photonics Integration, Optoelectronic Assembly and Reliability, Materials and Manufacturing Technology, High-Efficiency LEDs and High Power Lasers, Integrated Optical Sensors.

Interactive Presentations:
Abstracts may be submitted related to any of the nine major program committee topics listed above. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to submit an abstract of no more than 750 words that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net.

If you have any questions, contact:
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Abstracts must be received by October 9, 2017. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number, and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses
In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 9, 2017.

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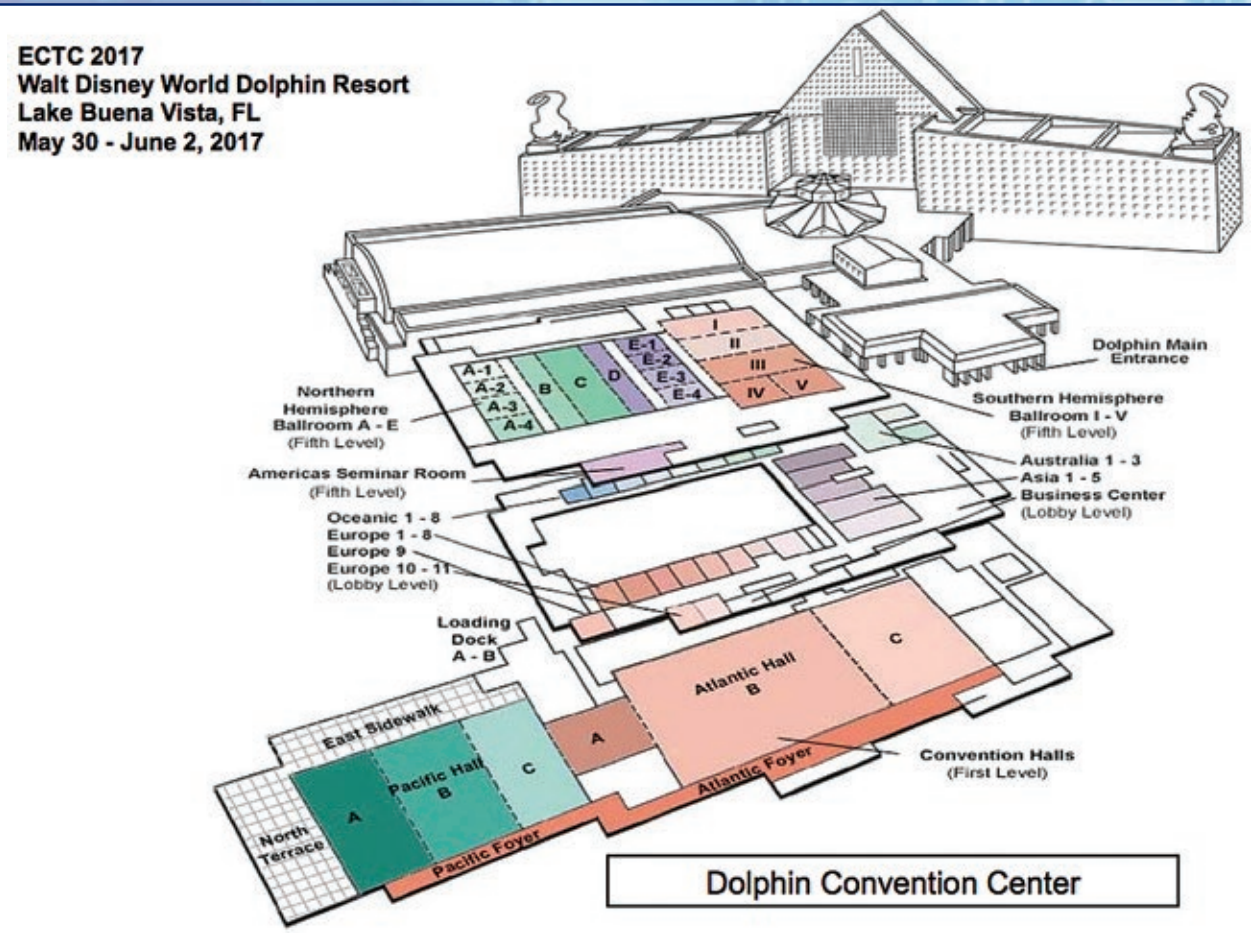

68TH ELECTRONIC COMPONENTS & TECHNOLOGY CONFERENCE

Sheraton San Diego Hotel & Marina
San Diego, California, USA
May 29 - June 1, 2018

ECTC will be 68 years old next year and we will be celebrating in San Diego, CA! The Sheraton San Diego Hotel & Marina is a tried and true venue for ECTC as ECTC has been using this property for quite some time! It touts panoramic views of the bay and the city skyline, yet is just 10 minutes from renowned attractions including the Gaslamp Quarter, Old Town, and Balboa Park.

Dubbed by many as "the only area in the US with perfect weather," San Diego is the oldest port on the West Coast and the sixth-largest city in the nation. Long known as a naval base, the military, along with tourism, still dominates the economy. In addition to rolling mountains, beautiful deserts, and seventy miles of coastline featuring some of the world's best beaches, San Diego offers a wealth of attractions. Art lovers can choose from many fine museums or catch a Shakespearean play at the Old Globe Theater. With more championship golf courses, over 85, than any other US city, you won't have a problem teeing off. The city also hosts the Major League Baseball's Padres. And one last thing, don't forget to take time to visit the world-renowned San Diego Zoo!

Conference At A Glance

MONDAY
May 29, 2017

3:00 p.m. – 5:00 p.m.
Registration
Australia Foyer

TUESDAY
May 30, 2017

6:45 a.m. – 5:00 p.m.
Registration
Australia Foyer

6:45 a.m. – 8:15 a.m.
Morning PDC Registration Only

7:00 a.m. – 7:45 a.m.
PDC Instructors and Proctors Briefing & Breakfast
Asia 1

7:00 a.m. – 5:00 p.m.
Speaker Preparation
Europe 2

9:30 a.m. – 5:30 p.m.
iNEMI Meeting
Oceanic 1
By invitation only

8:00 a.m. – Noon
Morning PDCs
See page 8 for locations

8:00 a.m. – 5:00 p.m.
CPMT Heterogeneous Integration Technology Roadmap Workshop
Europe 4

10:00 a.m. – 11:30 a.m.
ECTC Special Session
Southern Hemisphere I

10:00 a.m. – 10:20 a.m.
Morning PDC Break
Southern Hemisphere Foyer and Northern Hemisphere E Foyer

Noon
PDC Luncheon
Northern Hemisphere D-E

1:00 p.m. – 5:00 p.m.
Technology Corner Setup
Northern Hemisphere A-C

1:15 p.m. – 5:15 p.m.
Afternoon PDCs
See page 8 for locations

2:00 p.m. – 3:30 p.m.
ECTC Special Session
Southern Hemisphere I

3:00 p.m. – 3:20 p.m.
Afternoon PDC Break
Southern Hemisphere Foyer and Northern Hemisphere E Foyer

5:00 p.m. – 6:00 p.m.
ECTC Student Reception
Cabana Deck
Backup: Asia 1

6:00 p.m. – 7:00 p.m.
General Chair's Speakers Reception
Crescent Terrace on Swan Property
Backup: Northern Hemisphere D-E
By invitation only

7:30 p.m. – 9:00 p.m.
ECTC Panel Session
Southern Hemisphere II & III

WEDNESDAY
May 31, 2017

6:45 a.m. – 4:00 p.m.
Conference Registration
Australia Foyer

7:00 a.m. – 7:45 a.m.
Today's Speakers Breakfast
Northern Hemisphere E 3-4

7:00 a.m. – 5:00 p.m.
Speaker Preparation
Europe 2

8:00 a.m. – 11:40 a.m.
Sessions 1, 2, 3, 4, 5, 6
See pages 10–11 for Locations

9:00 a.m. – 11:00 a.m.
Session 37: Interactive Presentations 1
Northern Hemisphere Foyer

9:00 a.m. – Noon
Technology Corner Exhibits
Northern Hemisphere A-C

9:15 a.m. – 10:00 a.m.
Refreshment Break
Northern Hemisphere A-C

Noon
ECTC Luncheon
Northern Hemisphere D-E

1:30 p.m. – 6:30 p.m.
Technology Corner Exhibits
Northern Hemisphere A-C

1:30 p.m. – 5:10 p.m.
Sessions 7, 8, 9, 10, 11, 12
See pages 12–13 for Locations

2:00 p.m. – 4:00 p.m.
Session 38: Interactive Presentations 2
Northern Hemisphere Foyer

2:45 p.m. – 3:30 p.m.
Refreshment Break
Northern Hemisphere A-C

5:30 p.m. – 6:30 p.m.
Technology Corner Reception
Northern Hemisphere A-C

6:30 p.m. – 7:30 p.m.
CPMT Women's Panel & Reception
Southern Hemisphere IV

7:30 p.m. – 9:00 p.m.
ECTC Plenary Session
Southern Hemisphere II & III

THURSDAY
June 1, 2017

7:00 a.m. – 5:00 p.m.
Speaker Preparation
Europe 2

7:00 a.m. – 7:45 a.m.
Today's Speakers Breakfast
Northern Hemisphere E 3 & 4

7:30 a.m. – 4:00 p.m.
Conference Registration
Australia Foyer

8:00 a.m. – 11:40 a.m.
Sessions 13, 14, 15, 16, 17, 18
See pages 14–15 for Locations

9:00 a.m. – 11:00 a.m.
Session 39: Interactive Presentations 3
Northern Hemisphere Foyer

9:00 a.m. – Noon
Technology Corner Exhibits
Northern Hemisphere A-C

9:15 a.m. – 10:00 a.m.
Refreshment Break
Northern Hemisphere A-C

Noon
CPMT Luncheon
Northern Hemisphere D-E

1:30 p.m. – 4:00 p.m.
Technology Corner Exhibits
Northern Hemisphere A-C

1:30 p.m. – 5:10 p.m.
Sessions 19, 20, 21, 22, 23, 24
See pages 16–17 for Locations

2:00 p.m. – 4:00 p.m.
Session 40: Interactive Presentations 4
Northern Hemisphere Foyer

2:45 p.m. – 3:30 p.m.
Refreshment Break
Northern Hemisphere A-C

6:30 p.m. – 7:30 p.m.
67th ECTC Gala Reception
Lake Terrace on Swan Property
Backup: Northern Hemisphere D-E

8:00 p.m. – 9:30 p.m.
CPMT Seminar
Southern Hemisphere II & III

FRIDAY
June 2, 2017

7:00 a.m. – 5:00 p.m.
Speaker Preparation
Europe 2

7:00 a.m. – 7:45 a.m.
Today's Speakers Breakfast
Northern Hemisphere E 3-4

7:30 a.m. – Noon
Conference Registration
Australia Foyer

8:00 a.m. – 11:40 a.m.
Sessions 25, 26, 27, 28, 29, 30
See pages 18–19 for Locations

8:30 a.m. – 10:30 a.m.
Student Interactive Presentation Session
Northern Hemisphere Foyer

9:15 a.m. – 10:00 a.m.
Refreshment Break
Southern Hemisphere Foyer

Noon
ECTC Program Chair Luncheon
Northern Hemisphere D-E

1:30 p.m. – 5:10 p.m.
Sessions 31, 32, 33, 34, 35, 36
See pages 20–21 for Locations

2:45 p.m. – 3:30 p.m.
Refreshment Break
Southern Hemisphere Foyer

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