Conference Program and Exhibitor Listings

Don't miss out on electronic packaging's premier conference!

ECTC

The 2019 IEEE 69th Electronic Components and Technology Conference

May 28 - May 31, 2019

The Cosmopolitan of Las Vegas
Las Vegas, Nevada, USA

For more information, visit: www.ectc.net

Program Supported by:

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Sponsored by:

IEEE ELECTRONICS PACKAGING SOCIETY · IEEE

WELCOME FROM THE MAYOR, CITY OF LAS VEGAS, NEVADA

CAROLYN G. GOODMAN
MAYOR

From the Office of
Mayor Carolyn G. Goodman

ECTC 2019
ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE
LAS VEGAS, NEVADA
MAY 28-31, 2019

Greetings:

As Mayor, I am very pleased to welcome you to America's most dynamic, entertaining, and intriguing city! You could not have chosen a better locale. I am convinced that once you get a taste of what the city has to offer, you will never want to leave. Las Vegas continues to capture the world's imagination as the city where anything is possible. With world-class hotels, award-winning restaurants, luxurious spas, fantastic shopping, the finest golf courses, and spectacular entertainment, Las Vegas remains one of the most electrifying destinations in the world.

At its heart Las Vegas is all about making sure residents and visitors are well taken care of, treated courteously, and shown a great time. Beyond the neon of the fabulous Strip and the Fremont Street Experience, there is another Las Vegas--one in which we are building a world-class city featuring the best in arts, culture, sporting opportunities, and quality medical care. The Smith Center for the Performing Arts has set a high standard for art and culture in our city, and I encourage everyone to take in a concert or Broadway show at this magnificent venue. Regardless of your age, a must-visit spot is the children's interactive Discover Museum adjacent to the Smith Center. Buzzing with excitement is the Fremont East Entertainment District, a place with an energy and enthusiasm through its taverns, restaurants, and music venues.

The city also offers beautiful weather and outdoor activities, from top class golfing to opportunities for world-class hiking and rock climbing at the Red Rock Canyon National Conservation Area, to skiing at Mount Charleston, and a visit to the awe-inspiring Hoover Dam at the Lake Mead National Recreation Area. If history is more your speed, you are in luck because the National Museum of Organized Crime and Law Enforcement and the Neon Museum are two of the most interesting and unique experiences in the country.

I want to thank you for choosing Las Vegas and look forward to seeing you around town. I know you will have a fabulous time enjoying our great city and everything it has to offer. Now what are you waiting for? The party has already started! Welcome.

Sincerely,

Carolyn G. Goodman
Mayor, City of Las Vegas

CITY OF LAS VEGAS
495 S. MAIN STREET
LAS VEGAS, NEVADA 89101

VOICE 702.229.6241
FAX 702.385.7960
TTY 702.386.9108

EMAIL cgoodman@lasvegasnevada.gov
WEBSITE www.lasvegasnevada.gov

WELCOME TO LAS VEGAS FROM THE 69th ECTC GENERAL CHAIR AND PROGRAM CHAIR

On behalf of the Program Committee and Executive Committee, it is our pleasure to welcome you to the 69th Electronic Components and Technology Conference (ECTC), which will be held at The Cosmopolitan of Las Vegas in Las Vegas, Nevada from May 28-31, 2019. This premier international conference brings together key stakeholders of the global microelectronics packaging industry, such as semiconductor companies, foundry and OSAT service providers, equipment manufacturers, materials suppliers, research institutions and universities all under one roof.

For the 69th ECTC, the ECTC Program Committee has selected over 350 papers which will be presented in 36 oral sessions and five interactive presentation sessions including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as fan-out packaging, wafer-level packaging, flip-chip packaging, 3D/TSV technologies, design for RF performance and signal/power integrity, thermal and mechanical modeling, optoelectronics packaging, materials and reliability. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work.

Authors from over twenty countries are expected to present their work at the 69th ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature six special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, May 28 at 9 a.m., W. Hong Yeo and Mikel Miller will chair a special session covering "Transient Electronics: A Green Revolution for Packaging." On the same day at 2 p.m., Rena Huang and Soon Jang will chair a session focused on "Photonics on the Cutting-Edge of Technology Evolution." Tuesday evening will also include the ECTC Panel Session "Future (Visions) of Electronic Packaging" at 7:45 p.m. chaired by IEEE EPS President Avi Bar-Cohen and Karlheinz Bock, where young researchers will share their visions of future packaging technologies and participate in discussions with experts in the field.

This conference will also feature a Women's Panel and Reception jointly organized by ECTC and ITherm on Wednesday, May 29 at 6:30pm. This year, panelists from around the globe will share their perspectives on efforts to enhance the participation of women in engineering, and the panel will be chaired by Kristina Young-Fisher and Cristina Amon. On the same day at 7:30 p.m., Tanja Braun will chair the ECTC Plenary Session titled "Sensors and Packaging for Autonomous Driving." In this plenary session, experts will address the challenges and demands for sensors and packages for autonomous driving along the value chain. On Thursday, May 30 at 8 p.m., the IEEE EPS Seminar titled "Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements" will be moderated by Yasumitsu Orii and Shigenori Aoki from the High-Density Substrates & Boards Technical Committee of the IEEE EPS Society.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and the Technology Corner exhibits. Co-located with the IEEE iTHERM Conference this year, the 69th ECTC will offer eighteen PDCs, organized by the PDC Committee chaired by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 28 and are taught by distinguished experts in their respective fields. The Technology Corner will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging and services fields. More than one hundred Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons and nightly receptions.

Whether you are an engineer, a manager, a student or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. We invite you to join us during the 69th ECTC to be a part of all the 69th ECTC and be a part of all the exciting technical and professional opportunities. We also take this opportunity to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 69th ECTC a success. Once again, thank you for being a part of the 69th ECTC.

Mark Poliks
69th ECTC General Chair
Binghamton University
mpoliks@binghamton.edu

Nancy Stoffel
69th ECTC Program Chair
General Electric Research Center
stoffel@ge.com

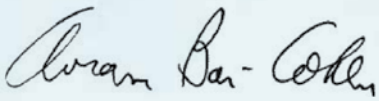
WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of the IEEE Electronics Packaging Society, it is my great pleasure and privilege to welcome you to the 69th Electronic Components and Technology Conference – the largest Packaging Conference in the world.

Building on the long history of ECTC and its predecessor Conferences, begun 69 years ago, this conference, and the electronic packaging community we serve, continue to grow in size and in impact. We expect attendance at this year's ECTC, and ITherm - the co-located EPS Thermal Phenomena Conference - to well exceed 2000 packaging professionals. Including the forthcoming EPS Asia-Pacific Flagship Conference, EPTC, in December, and the other sponsored and co-sponsored conferences and workshops, EPS is on track to serve more than 5000 Conference attendees world-wide in 2019.

I would like to take this opportunity to thank all of you for attending ECTC and our volunteers on the ECTC Executive and Program Committees, members of the Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their commitment and dedication to making the 69th ECTC and its associated activities the premier annual event of the electronic packaging community. We are fortunate to have so many of you actively engaged in this conference, and we are indebted to the large, skilled and enthusiastic team that keeps finding new ways to serve the electronic packaging community.

It is very rewarding to see the impact of these technical events and networking activities on the EPS Society, our industry, and our members. My deepest thanks and appreciation to all of you for the opportunity to work with you to develop the breakthroughs in packaging technology that will continue to drive innovation in the microelectronic industry!



Avram Bar-Cohen
EPS President 2018-2019

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Conference organizers reserve the right to cancel or change this program without prior notice.

ECTC Luncheon Keynote

Soft Electronic and Microfluidic Systems for the Skin

Wednesday, May 29, 2019 • Belmont 3, 4th Floor

John A. Rogers – Director of Center for Bio-Integrated Electronics, Northwestern University

Recent advances in materials, mechanics, and manufacturing establish the foundations for high-performance classes of electronics and other microsystems technologies that have physical properties precisely matched to the human epidermis. The resulting devices can integrate with the skin in a physically imperceptible fashion to provide continuous, clinical-quality information on physiological status. This talk will summarize the key ideas and presents specific examples in wireless monitoring for neonatal intensive care, and in capture, storage, and biomarker analysis of sweat.

ECTC Mobile App

ECTC is pleased to announce that a free mobile app is available again this year. The app provides information on schedules for our technical program and PDCs as well as exhibitors, sponsors, and general conference information and venue maps. The app also features tools to set your schedule so you don't miss presentations important to you, social interaction functions, and the ability to provide ratings on presentations that are used in selecting candidates for best paper awards.

The ECTC app is available for iOS and Android devices through the QuickMobile Events app available in the respective app stores. After downloading the app, search for "ECTC19" as the event ID, and follow the instructions to set up your account.

REGISTRATION AND GENERAL INFORMATION

Registration

ECTC registration will be open at the ECTC Registration Desk located in The Cosmopolitan Las Vegas in Las Vegas, NV, 4th floor in the Belmont Commons Foyer.

Monday, May 27, 2019 • 3:00 p.m. – 5:00 p.m.

Tuesday, May 28, 2019 • 6:45 a.m. – 8:15 a.m.*
(AM PD Courses & Special Session Only)*

Tuesday, May 28, 2019 • 8:15 a.m. – 5:00 p.m.
(All conference attendees)

Wednesday, May 29, 2019 • 6:45 a.m. – 4:00 p.m.

Thursday, May 30, 2019 • 7:30 a.m. – 4:00 p.m.

Friday, May 31, 2019 • 7:30 a.m. – 12:00 Noon

On Tuesday, May 28th light morning refreshments will be provided from 6:45 a.m. – 7:15 a.m. Come register and grab a bite to eat before the PDCs start!

The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45am start time as registration becomes very congested prior to the start of morning Professional Development Courses.

Door Registration Fees

Door Registration includes a Proceedings on USB drive

IEEE Member JOINT Registration (full ECTC + ITHERM conference)	$1160
IEEE Member Full Registration	$860
IEEE Member Speaker / Session Chair	$765
IEEE Member One Day	$565
IEEE Member Speaker One Day	$430
Exhibit Booth Attendant	$0
Non-Member JOINT Registration (full ECTC + ITHERM conference)	$1375
Non-Member Full Registration	$1055
Non-Member Speaker / Session Chair	$765
Non-Member One Day	$565
Non-Member Speaker One Day	$430
Exhibit Booth Attendant	$0
Student	$315
Student Speaker	$315
Exhibits Only	$25

Tuesday Professional Development Courses
IEEE Members and Non-Members

Tuesday AM or PM Course with luncheon	$500
Tuesday All-Day Courses with luncheon	$710
Tuesday Student All-Day Courses with luncheon	$130
Extra Luncheon Tickets for Each Day	$65
Extra Proceedings with Registration	$100

Professional Development Course Instructors Breakfast

PDC Instructors and Proctors are required to attend a briefing breakfast.

7:00 a.m. Tuesday – PDC Instructors and Proctor Briefing
(Room Location: Belmont 3, 4th floor)

Session Chairs and Speakers Breakfast

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Windows and Microsoft Office.

7:00 a.m. Wednesday thru Friday
(Room Location: Belmont 3, 4th floor, Wednesday – Thursday)
(Room Location: Belmont 5, 4th floor, Friday)

Speaker Prep Room

Speakers should prepare and review their digital presentations within the allotted times below:

7:00 a.m. – 5:00 p.m., Tuesday – Friday
(Room Location: Yaletown 2, 4th floor)

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, seminars, meals, exhibits and IP areas, and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
Please follow hotel policies and signs regarding this. Smoking is also NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, seminars, meals, exhibits and IP areas, and all conference social functions. Thank you for your consideration and cooperation.

MISCELLANEOUS INFORMATION

Hotel Concierge
The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Press Room
Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eperfecto@gmail.com or (845) 475-1290.

LUNCHEONS

Tuesday, May 28, 2019
12PM
Belmont 3, 4th floor
Our Tuesday lunch is provided for anyone attending a Professional Development Course, whether you attend just a single course or both a morning and afternoon course. PDC Proctors, session speakers, committee members or anyone else with a Tuesday lunch ticket is more than welcome to join! Possession of a lunch ticket is required for admission.

Wednesday, May 29, 2019
12PM
Belmont 3, 4th floor
This year's Wednesday luncheon will feature Dr. John A. Rogers, Director for the Center for Bio-Integrated Electronics at Northwestern University. We will also be celebrating award winners for Best and Outstanding Papers of 2018! Don't miss it! Possession of a lunch ticket is required for admission.

Thursday, May 30, 2019
12PM
Belmont 3, 4th floor
The IEEE Electronics Packaging Society will host our Thursday luncheon for conference attendees. The EPS awards will be presented. Possession of a lunch ticket is required for admission.

Friday, May 31, 2019
12PM
Belmont 3, 4th floor
Do NOT MISS Friday's luncheon! It's our annual ECTC Program Chair luncheon where lots of high dollar, valuable, and useful prizes will be raffled off! Each year the prizes seem to get better and better! Remember you must be present to win. Possession of a lunch ticket is required for admission.

Please note that due to increased attendance ECTC will have an overflow lunch room on Wednesday & Thursday located in Castellana 2, 3rd floor.
Please make sure to be in line for lunch early if your preference is the main lunch room.

Heterogeneous Integration Roadmap Workshop

Tuesday, May 28, 2019 • 8:00 a.m. - 5:00 p.m.

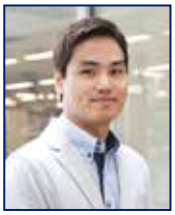
Moderators: William Chen – ASE, Bill Bottoms – 3MT Solutions and Ravi Mahajan – Intel
Condesa 3, 2nd Floor

Our industry has reinvented itself through multiple disruptive changes in technologies, products, and markets. Our industry continues to change with the rapid migration of logic, memory, and applications to the cloud, the evolution of the Internet of Things (IoT) to the Internet of Everything (IoE), the proliferation of smart devices everywhere, the rise of 5G, the increasing presence of microelectronics in wearables & health application, and in autonomous automotive, and the rapid advancement of AI . The pace of innovation is simultaneously increasing to meet these challenges. The Heterogeneous Integration Roadmap will address the future directions of heterogeneous integration technologies and applications serving the future markets and applications.

The Heterogeneous Integration Roadmap Technical Working Groups are celebrating the completion of the 1st edition of the Heterogeneous Integration Roadmap. The Technical Working Groups will be reporting out their work products and on their plan for the next edition.

We like to invite all the ECTC & ITherm participants to attend this important working session for our profession and for our industry. Registration is not required.

SPECIAL SESSIONS



2019 SPECIAL SESSION

Transient Electronics: A Green Revolution for Packaging?

Tuesday, May 28, 2019
9:00 a.m. – 11:30 a.m.
Castellana 2, 3rd Floor

Chairs: W. Hong Yeo - Georgia Institute of Technology and Mikel Miller - EMD Performance Materials

Speakers:
1. John Rogers – Northwestern University
2. Matthew MacEwan – Washington University
3. Paul Kohl – Georgia Institute of Technology
4. Mihai Irimia-Vladu – Joanneum Research Forschungsgesellschaft mbH

2019 ECTC/ITHERM WOMEN'S PANEL AND RECEPTION

Unleashing the Power of Diversity in our Workforce

Wednesday, May 29, 2019
6:30 p.m. – 7:30 p.m.
Nolita 1, 4th Floor

Chairs: Kristina Young-Fisher - GLOBALFOUNDRIES and Cristina Amon - University of Toronto

Speakers:
1. Monica Jackson – GE Aviation
2. Rolf Aschenbrenner – Fraunhofer IZM
3. Dereje Agonafer – University of Texas at Arlington
4. Jean Trewhella – GLOBALFOUNDRIES

2019 PHOTONICS SPECIAL SESSION

Photonics on the Cutting-Edge of Technology Evolution

Tuesday, May 28, 2019
2:00 p.m. – 4:30 p.m.
Castellana 2, 3rd Floor

Chairs: Rena Huang - Rensselaer Polytechnic Institute and Soon Jang - ficonTEC (USA) Corporation

Speakers:
1. Bert Offrein – IBM Research GmbH-Zurich
2. Mark Thompson – PsiQuantum
3. Roy Meade – Ayar Labs
4. Charles Kuznia – Ultra Communications, Inc.
5. Jason Eichenholz – LuminarTechnologies, Inc.

2019 PLENARY SESSION

Sensors and Packaging for Autonomous Driving

Wednesday, May 29, 2019
7:30 p.m. – 9:00 p.m.
Mont-Royal 1 & 2, 4th Floor

Chair: Tanja Braun, Fraunhofer Institute for Reliability and Microintegration (IZM)

Speakers:
1. Scott Chen – Advanced Semiconductor Engineerng, Inc.
2. Przemyslaw Jakub Gromala – Robert Bosch GmbH
3. Tu-Anh Tran – NXP Semiconductors
4. Nathan Brese – DuPont

2019 ECTC PANEL SESSION

Future (Visions) of Electronic Packaging

Tuesday, May 28, 2019
7:45 p.m. – 9:15 p.m.
Mont-Royal 1 & 2, 4th Floor

Chairs: Avi Bar-Cohen, EPS President - Raytheon and Karlheinz Bock - TU Dresden

Speakers:
1. Martin Schubert – TU Dresden
2. Shreya Dwarakanath – Georgia Institute of Technology
3. Chandrasekharan Nair – Georgia Institute of Technology
4. Siddharth Ravichandran – Georgia Institute of Technology

2019 IEEE EPS SEMINAR

Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements

Thurday, May 30, 2019
8:00 p.m. – 9:30 p.m.
Mont-Royal 1 & 2, 4th Floor

Chairs: Yasumitsu Orii - Nagase, Japan and Shigenori Aoki - Lintec

Speakers:
1. Toshihiko Nishio – SBR Technology Company
2. Eiichi Nomura – Nagase ChemteX
3. Koichi Hasegawa – JSR
4. Kenji Nishiguchi – Risho Kogyo
5. Mike Sakaguchi – Tatsuta Electric Wire & Cable
6. Yoshio Nishimura – Ajinomoto Fine Technology Co.

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 28, 2019

Morning Courses 8:00 a.m. – 12:00 Noon	Afternoon Courses 1:30 p.m. – 5:30 p.m.
Yaletown 1 **1. Achieving High Reliability of Lead-Free Solder Joints – Materials Considerations** *Course Leader: Ning-Cheng Lee – Indium Corporation*	**Yaletown 1** **10. Flip Chip Technologies** *Course Leaders: Eric Perfecto – Independent Consultant; Shengmin Wen – Synaptics Inc.*
Nolita 3 **2. Introduction to Fan-Out Wafer-Level Packaging** *Course Leader: Beth Keser – Intel Corporation.*	**Nolita 3** **11. Wafer-Level Chip-Scale Packaging (WCSP) Fundamentals** *Course Leader: Patrick Thompson - Texas Instruments, Inc.*
Nolita 2 **3. Fundamentals of Glass Technology and Applications for Advanced Semiconductor Packaging** *Course Leaders: Indrajit Dutta and Jay Zhang – Corning Inc.*	**Nolita 2** **12. Flexible Hybrid Electronics – Manufacturing and Reliability** *Course Leader: Pradeep Lall – Auburn University*
Nolita 1 **4. Moore's Law for Packaging to Replace Moore's Law for ICs** *Course Leader: Rao Tummala – Georgia Institute of Technology*	**Nolita 1** **13. Fan-Out Wafer/Panel Level Packaging and 3D IC Heterogenous Integration** *Course Leader: John Lau – ASM Pacific Technology Ltd.*
Mont-Royal 2 **5. Polymers and Nanocomposites for Electronic and Photonic Packaging** *Course Leaders: C. P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation*	**Mont-Royal 2** **14. Polymers for Wafer Level Packaging** *Course Leader: Jeffrey Gotro – InnoCentrix, LLC*
Mont-Royal 1 **6. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel Level Packages and Interposers** *Course Leaders: Ivan Ndip and Markus Wöhrmann – Fraunhofer IZM*	**Mont-Royal 1** **15. Reliability Mechanics and Modeling for IC Packaging - Theory, Implementation and Practices** *Course Leaders: Ricky Lee – HKUST and Xuejun Fan – Lamar University*
Belmont 4 **7. Solving Package Failure Mechanisms for Improved Reliability** *Course Leader: Darvin Edwards – Edwards Enterprises*	**Belmont 4** **16. Robust Electronics for Automotive Applications including Autonomous Driving** *Course Leaders: Matthias Petzold – Fraunhofer IZM, Mervi Paulasto-Kröckel – Alto University, and Klaus-Jeurgen Wolter – TU Dresden*
Belmont 8 **8. Characterization of Advanced EMCs for FO-WLP, Heterogenous Integration, and Automotive Electronics** *Course Leaders: Przemyslaw Gromala – Robert Bosch GmbH; Bongtae Han – University of Maryland*	**Belmont 8** **17. From Wafer to Panel Level Packaging** *Course Leaders: Tanja Braun and Rolf Aschenbrenner – Fraunhofer, IZM*
Castellana 1 **9. Integrated Thermal Packaging and Reliability of Power Electronics** *Course Leader: Patrick McCluskey – University of Maryland*	**Castellana 1** **18. Electronics Cooling Technologies for Handheld Devices, Computing, and High-Power Electronics** *Course Leaders: William Maltz and Guy Wagner – Electronic Cooling Solutions*

Refreshment Breaks – 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Mont-Royal Commons, Belmont Commons 4 & 8, & Castellana 1

2019 YOUNG PROFESSIONALS PANEL & RECEPTION

Tuesday, May 28, 2019
7:00 p.m. – 7:45 p.m.
Nolita 1, 4th Floor

Chair: Yan Liu, Medtronic

Panelists: EPS Board of Governors members: Avi Bar-Cohen, Chris Bailey, Karlheinz Bock, Alan Huffman, Sam Karikalan, Beth Keser, Ravi Mahajan, Toni Mattila, David McCann, Kitty Pearsall, Eric Perfecto, Jeff Suhling, Andrew Tay, and Pat Thompson

This event is designed just for you – young professionals (including current graduate students). In this active event, we will pair you with senior EPS members and professionals through a series of active and engaging activities. You will have opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

ECTC STUDENT RECEPTION

Tuesday, May 28, 2019 • 5:00 p.m. - 6:00 p.m.
Mont-Royal Commons, 4th Floor
Hosted by Texas Instruments, Inc.

Texas Instruments

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry, and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them succeed in their first job search and reach their current positions. During this reception, you can enjoy good food while networking with industry leaders and achievers. Don't miss your opportunity to interact with people who you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

GENERAL CHAIR'S SPEAKERS RECEPTION

Tuesday, May 28, 2019 • 6:00 p.m. - 7:00 p.m.
OUTSIDE at the North Blvd. Pool
(Rain Backup: Belmont 3, 4th Floor)
Invited session chairs and speakers are requested to attend the reception.

TECHNOLOGY CORNER RECEPTION

Wednesday, May 29, 2019 • 5:30 p.m. - 6:30 p.m.
Belmont 1 & 5 Ballroom, 4th Floor
All attendees and guests are invited.

69th ECTC GALA RECEPTION

Thursday, May 30, 2019 • 6:30 p.m.
Belmont 3 & 4 Ballroom, 4th Floor
All badged attendees are invited.

CONTINUING EDUCATION UNITS

The IEEE Electronics Packaging Society (EPS) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 69th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops. Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Course CEUs will be underwritten by the conference, i.e., there are no additional costs for Professional Development Course attendees to obtain CEU credit.

AWARDS FROM THE 68TH ECTC

BEST OF CONFERENCE PAPERS

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 68th ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500, and the authors of the Best Interactive Presentation share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper
Session 27, Paper 5
Material Characterization of Advanced Cement-Based Encapsulation Systems for Efficient Power Electronics with Increased Power Density
Bianca Boettge, F. Naumann, S. Klengel, M. Petzold - Fraunhofer Institute for Microstructure of Materials and Systems (IMWS); S. Behrendt, R. Eisele - FuE-Zentrum Fachhochschule Kiel GmbH; M. G. Scheibel, A.-Z. Miric - Heraeus Deutschland GmbH & Co. KG; S. Kaessner, G. Hejtmann - Robert Bosch GmbH and K. G. Nickel - University of Tuebingen

Best Interactive Presentation Paper
Session 39, Paper 6
Correlated Model For Wafer Warpage Prediction of Arbitrarily Patterned Films
Gregory T. Ostrowicki, Siva Gurrum and Amit Nangia – Texas Instruments, Inc.

INTEL BEST STUDENT PAPER

The winning student receives a personalized plaque and a check for US $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 68th ECTC:

Session 23, Paper 3
Miniaturized High-Performance Filters for 5G Small-Cell Applications
Muhammad Ali, Fuhan Liu, Atom Watanabe, P. Markondeya Raj, Venkatesh Sundaram, Manos M. Tentzeris and Rao. R. Tummala - Georgia Institute of Technology

OUTSTANDING PAPERS

The winning authors for the Conference Outstanding Session Paper and Interactive Presentation selected from the 68th ECTC proceedings receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper
Session 7, Paper 1
Laser Sintering of Dip-Based All-Copper Interconnects
Luca Del Carro, Thomas Brunschwiler – IBM Research, Zurich; Martin Kossatz, Lucas Schnackenberg, Matthias Fettke – PacTech – Packaging Technologies GmbH; and Ian Clark - Intrinsiq Materials Ltd.

Outstanding Interactive Presentation
Session 37, Paper 20
Non-destructive Assessment of the Porosity in Silver (Ag) Sinter Joints using Acoustic Waves
Sebastian Brand, Bianca Böttge, Michael Kögel, Falk Naumann, Frank Altmann - Fraunhofer Institute for Microstructure of Materials and Systems (IMWS); Jurrian Zijl, Sebastiaan Kersjes - BESI Netherlands, B.V. and Thomas Behrens - Infineon Technologies AG

TEXAS INSTRUMENTS OUTSTANDING STUDENT INTERACTIVE PRESENTATION

The winning student receives a personalized plaque and a check for US $1,000. The following paper was selected based on the Texas Instruments Outstanding Student Interactive Presentation competition conducted at the 68th ECTC:

Session 39, Paper 10
Copper Transparent Antennas on Flexible Glass by Subtractive and Semi-Additive Fabrication for Automotive Applications
Jack P. Lombardi III, Robert E. Malay, Mark D. Poliks - Binghamton University; James H. Schaffner, Hyok Jae Song - HRL Laboratories, LLC; Ming-Huang Huang, Scott C. Pollard - Corning, Inc.; and Timothy Talty – General Motors

CORNING LEADERSHIP IN GLASS AWARD

The winning authors receive an engraved Steuben crystal Euclidean award and each receive a gift card for US $100. The following paper was selected from submissions to the 68th ECTC:

Session 38, Paper 18
A Novel Inorganic Substrate by Three Dimensionally Stacked Glass Core Technology
Toshiki Iwai, Taiji Sakai, Daisuke Mizutani, Seiki Sakuyama - Fujitsu Laboratories Ltd.; Kenji Iida, Takayuki Inaba, Hidehiko Fujisaki, and Yoshinori Miyazawa - Fujitsu Interconnect Technologies Ltd.

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 28, 2019

8:00 a.m. – 5:00 p.m.
EPS Heterogeneous Integration Roadmap Workshop
Condesa 3, 2nd floor

9:00 p.m. – 10:30 p.m.
ECTC OPTO Committee
Jardins Boardroom, 2nd floor

9:00 p.m. – 10:30 p.m.
ECTC Interconnect Committee
Bellavista Boardroom, 2nd floor

Wednesday, May 29, 2019

7:00 a.m. – 8:00 a.m.
EPS Materials & Processes TC
Jardins Boardroom, 2nd floor

7:00 a.m. – 8:00 a.m.
EPS Power & Energy TC
Bellavista Boardroom, 2nd floor

4:30 p.m. – 5:30 p.m.
EPS Technical Committee Chairs
Bellavista Boardroom, 2nd floor

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite
(by invitation only)

Thursday, May 30, 2019

7:00 a.m. – 8:00 a.m.
EPS Region 8 Meeting
Condesa 5, 2nd floor

7:00 a.m. – 8:00 a.m.
EPS Nanotechnology TC
Bellavista Boardroom, 2nd floor

7:00 a.m. – 8:00 a.m.
EPS High Density Substrates & Boards TC
Jardins Boardroom, 2nd floor

7:00 a.m. – 8:00 a.m.
EPS Electrical Design, Modeling & Simulation TC
Belmont 4, 4th floor

7:00 a.m. – 8:00 a.m.
EPS Reliability TC
Condesa 6, 2nd floor

5:30 p.m. – 6:30 p.m.
ECTC 2020 Program Committee Meeting
Nolita 1, 4th floor

8:00 p.m.
69th ECTC Governing/Executive Committee Reception
General Chair's Suite

Friday, May 31, 2019

7:00 a.m. – 8:00 a.m.
EPS Emerging Technologies TC
Jardins Boardroom, 2nd floor

7:00 a.m. – 8:00 a.m.
EPS Thermal & Mechanical TC
Condesa 5, 2nd floor

7:00 a.m. – 8:30 a.m.
EPS Transaction Editors TC / AE's
Condesa 2, 2nd floor

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee
Jardins Boardroom, 2nd floor

Conference At A Glance

REGISTRATION

Monday
3:00 p.m. - 5:00 p.m.

Tuesday
6:45 a.m. - 5:00 p.m.

Wednesday
6:45 a.m. - 4:00 p.m.

Thursday
7:30 a.m. - 4:00 p.m.

Friday
7:30 a.m. - 12:00 p.m.
Belmont Commons Foyer

TECHNOLOGY CORNER EXHIBITS

Wednesday
9:00 a.m. - 12:00 p.m.
1:30 p.m. - 6:30 p.m.
Reception - 5:30 p.m. - 6:30 p.m.

Thursday
9:00 a.m. - 12:00 p.m.
1:30 p.m. - 4:00 p.m.
Belmont 1 & 5, 4th Floor

SPEAKER PREPARATION ROOM

Tuesday - Friday
7:00 a.m. – 5:00 p.m.
Yaletown 2

TUESDAY

PDC Instructors and Proctors Briefing & Breakfast
7:00 a.m. – 7:45 a.m.
Belmont 3, 4th Floor

Professional Development Courses (PDCs)
8:00 a.m. – Noon
1:30 p.m. - 5:30 p.m.
See page 9 for locations

EPS Heterogeneous Integration Roadmap Workshop
8:00 a.m. – 5:00 p.m.
Condesa 3, 2nd Floor

Special Sessions: ECTC Special Session
9:00 a.m. – 11:30 a.m.
Castellana 2, 3rd Floor

Photonics Special Session
2:00 p.m. – 4:30 p.m.
Castellana 2, 3rd Floor

Refreshment Breaks
10:00 a.m. – 10:20 a.m.
3:00 p.m. – 3:20 p.m.
Mont-Royal Commons, Belmont Commons 4 & 8, & Castellana

Lunch for PDCs
12 p.m. Noon
Belmont 3, 4th Floor

Technology Corner SetUp
1:00 p.m. – 5:00 p.m.
Belmont 1 & 5, 4th Floor

ECTC Student Reception
5:00 p.m. – 6:00 p.m.
Mont-Royal Commons, 4th Floor

General Chair's Speakers Reception
6:00 p.m. – 7:00 p.m.
OUTSIDE at the North Blvd. Pool
(Rain Backup: Belmont 3, 4th Floor)
By invitation only

Young Professionals Networking Panel
7:00 p.m. – 7:45 p.m.
Nolita 1, 4th Floor

ECTC Panel Session
7:45 p.m. – 9:15 p.m.
Mont-Royal 1 & 2, 4th Floor

WEDNESDAY

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Belmont 3, 4th Floor

Sessions 1 - 12
8:00 a.m. – 11:40 a.m.
1:30 p.m. – 5:30 p.m.
see pages 12 -15 for specifics

Interactive Presentations Sessions 37 - 38
9:00 a.m. - 11:00 a.m. or
2:00 p.m. - 4:00 p.m.
see pages 24 - 25 for specifics

Refreshment Breaks
9:15 a.m. – 10:00 a.m.
2:45 p.m. – 3:30 p.m.
Belmont 1 & 5, 4th Floor

Lunch
12 p.m. – 1:15 p.m.
Belmont 3, 4th Floor
Overflow: Castellana, 3rd Floor

ECTC/ITHERM Panel & Reception
6:30 p.m. – 7:30 p.m.
Nolita 1, 4th Floor

ECTC Plenary Session
7:30 p.m. – 9:00 p.m.
Mont-Royal 1 & 2, 4th Floor

THURSDAY

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Belmont 3, 4th Floor

Sessions 13 - 24
8:00 a.m. – 11:40 a.m.
1:30 p.m. – 5:30 p.m.
see pages 16 -19 for specifics

Interactive Presentations Sessions 39 - 40
9:00 a.m. - 11:00 a.m. or
2:00 p.m. - 4:00 p.m.
see pages 25 - 26 for specifics

Refreshment Breaks
9:15 a.m. – 10:00 a.m.
2:45 p.m. – 3:30 p.m.
Belmont 1 & 5, 4th Floor

Lunch
12 p.m. – 1:15 p.m.
Belmont 3, 4th Floor
Overflow: Castellana, 3rd Floor

69th ECTC Gala Reception
6:30 p.m. – 7:30 p.m.
Mont-Royal 1 & 2, 4th Floor

FRIDAY

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Belmont 3, 4th Floor

Sessions 25 - 36
8:00 a.m. – 11:40 a.m.
1:30 p.m. – 5:30 p.m.
see pages 20 -23 for specifics

Interactive Presentations Session 41
8:30 a.m. - 10:30 a.m.
see pages 26 - 27 for specifics

Refreshment Breaks
9:15 a.m. – 10:00 a.m.
2:45 p.m. – 3:30 p.m.
Mont-Royal Commons

Lunch
12 p.m. – 1:15 p.m.
Belmont 3, 4th Floor

Program Sessions: Wednesday, May 29, 8:00 a.m. - 11:40 a.m.

Session 1: Wafer-Level Fan-Out Process Integration	Session 2: Next-Generation Wirebonding and Die Attach	Session 3: RDL and Additive Manufacturing
Committee: Packaging Technologies	**Committee: Interconnections**	**Committee: Packaging Technologies in conjunction with Emerging Technologies**
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: **Bora Baloglu** **Amkor Technology** **Beth Keser** **Intel Corporation**	**Session Co-Chairs:** **Matthew Yao** **GE Energy Management** **Nathan Lower** **Rockwell Collins, Inc.**	**Session Co-Chairs:** **Kuldip Johal** **Atotech** **C. S. Premachandran** **GLOBALFOUNDRIES**
1. 8:00 a.m. - 3D-MiM (Must-in-Must) Technology for Advanced System Integration An-Jhih Su, Terry Ku, Chung-Hao Tsai, Kuo-Chung Yee, and Douglas Yu – Taiwan Semiconductor Manufacturing Company Ltd.	***1. 8:00 a.m. - SB²-WB a New Process Solution for Advanced Wire-Bonding*** Matthias Fettke, Andrej Kolbasow, Georg Friedrich, Anna Palys, Vinith Bejugam, and Thorsten Teutsch – Pac Tech – Packaging Technologies GmbH	***1. 8:00 a.m. - Submicron-Scale Cu RDL Patterning Based on Semi-Additive Process for Heterogeneous Integration*** Takamasa Takano, Hiroshi Kudo, Masaya Tanaka, and Miyuki Akazawa – Dai Nippon Printing Co., Ltd.
2. 8:25 a.m. - Construction on FO-MCM with C4 Bumps Built First Using Chip Last Assembly Technology Chih-Hsun Hsu, Wen-Yang Li, Chi-Jen Chen, Yih Jenn Jiang, Jui-Feng Tai, Chang-Fu Lin, and C. Key Chung – Siliconware Precision Industries Co., Ltd.	***2. 8:25 a.m. - Smart Wire Bond Solutions for SiP and Memory Packages*** Basil Milton, Aashish Shah, Hui Xu, Odal Kwon, Gary Schulze, Ivy Qin – Kulicke and Soffa, USA; Nelson Wong – Kulicke and Soffa, Singapore	***2. 8:25 a.m. - Sub-Micron RDL Patterning for Advanced Packaging*** Ken- Ichiro Mori, Yoshio Goto, Yasuo Hasegawa, Seiya Miura and Douglas Shelton – Canon Inc.
3. 8:50 a.m. - Feasibility Study of Fan-Out Panel-Level Packaging for Heterogeneous Integration Cheng-Ta Ko, Henry Yang, Curry Lin, Y.H. Chen – Unimicron Technology Corporation; John Lau, Ming Li, Penny Lo, R. So, Nelson Fan, Eric Kuah, Eric Ng, Y.M. Cheung– ASM Pacific Technology; Cao Xi - Huawei Technologies Co. Ltd.; Iris Xu, Tony Chen, Zhang Li, Kim Hwee Tan– Jiangyin Changdian Advanced Packaging Co. Ltd.; Chieh-Lin Chang, Jhih-Yuan Pan, Hsing-Hui Wu, Rozalia Beica and Marc Lin – Dow Chemical Company; Sze Pei Lim, N.C. Lee – Indium Corporation; Ming Tao, Jeffery Lo, Ricky Lee - Hong Kong University of Science and Technology	***3. 8:50 a.m. - Preparation and Application of Cu-Ag Composite Solder Preforms for Power Electronic Packaging*** Li Liu, Shengfa Liu, Hui Xiang, and Dongxiao Zhang – Wuhan University of Technology; Zhaoxia Zhou, Stuart Robertson, Canyu Liu, and Changqing Liu – Loughborough University; Zhiwen Chen – Wuhan University	***3. 8:50 a.m. - Optimization of Electrolytic Plating Processes for Challenging Fan-Out Panel-Level Package Designs*** Ralph Zoberbier, Britta Scheller, and Christian Ohde – Atotech Deutschland GmbH
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Belmont 1 & 5		
4. 10:00 a.m. - Ultra-Thin FO Package-on-Package for Mobile Application Hsiang-Yao Hsiao, Soon Wee Ho, Simon Siak Boon Lim, Leong Ching Wai, Ser Choong Chong, Pei Siang Sharon Lim, Yong Han, and Tai Chong Chai – Institute of Microelectronics A*STAR	***4. 10:00 a.m. - Au-Rich/Sn-Bi Interconnection in Chip-on-Module Package*** Jin Wang, Qian Wang, and Jian Cai – Tsinghua University; Xinnan Hou, Ke Du, and Lixin Zhao – GalaxyCore Inc.	***4. 10:00 a.m. - 3D Printed Substrates for the Design of Compact RF Systems*** Mohd Ifwat Mohd Ghazali - Universiti Sains Islam Malaysia, Michigan State University; Saikat Mondal, Saranraj Karuppuswami, and Premjeet Chahal – Michigan State University
5. 10:25 a.m. - Development of Wafer-Level Process for the Fabrication of Advanced Capacitive Fingerprint Sensor Using Embedded Silicon Fan-Out (eSiFO®) Technology Shuying Ma, Chengqian Wang, and Fengxia Zheng – Huantian Technology (Kunshan) Electronics Co., Ltd.; Daquan Yu, Xiaobing Yang, Li Ma, Ping Li, and Weidong Liu – Huantian Technology (Xi'an) Electronics Co., Ltd.; Hong Xie – Flipchip International; Jambo Yu, Jason Goodelle – Synaptics, USA	***5. 10:25 a.m. - The Properties of Cu Sinter Paste for Pressure Sintering at Low Temperature*** Jung-Lae Jo, Sinichi Yamauchi, Kei Anai, and Takahiko Sakaue – Mitsui Mining & Smelting Co., Ltd.	***5. 10:25 a.m. - Fully Additively Manufactured Tunable Active Frequency Selective Surfaces with Integrated On-Package Solar Cells for Smart Packaging Applications*** Syed Abdullah Nauroze, Xuanke He, and Manos M. Tentzeris – Georgia Institute of Technology
6. 10:50 a.m. - Three-Dimensional Integrated Circuit (3D-IC) Package Using Fan-Out Technology Jun Kyu Lee, Sang Yong Park, Young Ho Kim, Jae Cheon Lee, Sung Hyuk Lee, Chul Hyo Lee, Yong Tae Kwon, Chang Woo Lee, Jong Heon Kim, Nam Chul Kim, and Yun Hyun Sung – NEPES Corporation	***6. 10:50 a.m. - Low Temperature Sintering of Dendritic Cu Based Pastes for Power Semiconductor Device Interconnection*** Gang Li, Jilei Fan, Siyuan Liao, Pengli Zhu, Baotan Zhang, Tao Zhao, Rong Sun, and Ching-Ping Wong – Shenzhen Institutes of Advanced Technology	***6. 10:50 a.m. - First Demonstration of a Low Cost/Customizable Chip Level 3D Printed Microjet Hotspot-Targeted Cooler for High Power Applications*** Tiwei Wei – IMEC & KU Leuven; Herman Oprins and Vladimir Cherman – IMEC; Ingrid De Wolf – IMEC & KU Leuven; Eric Beyne – IMEC and Martine Baelmans – KU Leuven
7. 11:15 a.m. - Ultra High-Density I/O Fan-Out Design Optimization with Signal and Power Integrity Chih-Yi Huang, Keng Tuan Chang, Hung-Chun Kuo, Ming-Fong Jhong, Tsun-Lung Hsieh, Mi-Chun Hung, and Chen-Chao Wang – Advanced Semiconductor Engineering Inc.	***7. 11:15 a.m. - A New Development of Direct Bonding to Aluminum and Nickel Surfaces by Silver Sintering in Air Atmosphere*** Ly May Chew and Wolfgang Schmitt – Heraeus Deutschland GmbH & Co. KG; Tamira Stegmann, Erika Schwenk, and Monique Dubis – Hochschule Aschaffenburg University of Applied Sciences, Germany	***7. 11:15 a.m. - Rapid Production of Customized 3D Electronics via Hybrid Additive Manufacturing Technology*** Ji Li, Yang Wang, Peiren Wang, Jianglin He, Handa Liu, and Gengzhao Xiang – Southeast University

Program Sessions: Wednesday, May 29, 8:00 a.m. - 11:40 a.m.

Session 4: Advancements in Automotive and Power Devices	Session 5: Bonding Manufacturing Technologies	Session 6: Emerging Flexible Hybrid Electronics
Committee: Materials & Processing	**Committee: Assembly & Manufacturing Technology**	**Committee: Emerging Technologies**
Nolita 2	**Nolita 3**	**Yaletown 1**
Session Co-Chairs: **Praveen Pandojirao-S** **Johnson & Johnson** **Lewis Huang** **Senju Electronic**	**Session Co-Chairs:** **Valerie Oberson** **IBM Canada, Ltd** **Paul Houston** **Engent**	**Session Co-Chairs:** **Jong-Hoon Kim** **Washington State University Vancouver** **Hongqing Zhang** **IBM Corporation**
1. 8:00 a.m. - Solid-Liquid InterDiffusion (SLID) Bonding, for Thermally Challenging Applications Knut E Aasmundtveit, Hoang-Vu Nguyen, and Andreas Larsson – University of South-Eastern Norway; Thi-Thuy Luu – Zimmer & Peacock; Torleif A Tollefsen – TEGma	***1. 8:00 a.m. - Comprehensive Study of Copper Nano-Paste for Cu-Cu Bonding*** Ser Choong Chong and Pei Siang Lim Sharon – Institute of Microelectronics A*STAR	***1. 8:00 a.m. - Stretchable and Printable Medical Dry Electrode Arrays on Textile for Electrophysiological Monitoring*** Yougen Hu, Hui Wang, Yaoxu Xiong, Han Gu, Pengli Zhu, Guanglin Li, and Rong Sun – Shenzhen Institutes of Advanced Technology; Ommeaymen Sheikhnejad – AC2T Research GmbH; Ching-Ping Wong – Georgia Institute of Technology
2. 8:25 a.m. - Fluxless Bonding Technique of Diamond to Copper Using Silver-Indium Multilayer Structure Roozbeh Sheikhi, Yongjun Huo, and Chin C. Lee – University of California, Irvine	***2. 8:25 a.m. - Enhanced Performance of Laser-Assisted Compression Bonding (LACB) Compared with Thermal Compression Bonding (TCB) Technology*** Kwang-Seong Choi, Yong-Sung Eom, Seok Hwan Moon, Jiho Joo, and leeseul Jeong – Electronics and Telecommunications Research Institute; Kwangjoo Lee, Jung Hak Kim, and Ju hyeon Kim – LG Chem; Gil-Sang Yoon – KITECH; Kwang-Hee Lee and Chul-Hee Lee – Inha University; Geun-Sik Ahn, and Moo-Sup Shim - Protec	***2. 8:25 a.m. - Screen-Printed Flexible Coplanar Waveguide Transmission Lines: Multi-Physics Modeling and Measurement*** Nahid Aslani Amoli, Sridhar Sivapurapu, Rui Chen, Yi Zhou, Mohamed L. F. Bellaredj, Paul A. Kohl, Suresh K. Sitaraman, and Madhavan Swaminathan – Georgia Institute of Technology
3. 8:50 a.m. - Formulation and Processing of Conductive Polysulfide Sealants for Automotive and Aerospace Applications Bo Song, Fan Wu, Kyoung-Sik Moon, and C.P. Wong – Georgia Institute of Technology	***3. 8:50 a.m. - A Study of 3D Packaging Interconnection Performance Affected by Thermal Diffusivity and Pressure Transmission*** Jin-San Jung, Hyeong Gi Lee, Ji-Min Kim, Yong-Jin Park, Ji-In Yu, Yong Sung Park, Jun Su Lim, Hyun-Seok Choi, Sung-Il Cho, Dong wook Kim, and Sang-Ho An – Samsung Electronics Company, Ltd.	***3. 8:50 a.m. - Inkjet-Printed Filtering Antenna on a Textile for Wearable Applications*** Hsuan-Ling Kao and Chun-Hsiang Chuang – Chang Gung University; Cheng-Lin Cho – National Tsing Hua University
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Belmont 1 & 5		
4. 10:00 a.m. - Challenges and Approaches to Developing Automotive Grade 1/0 FCBGA Package Capability Rajen Dias, Mike Kelly, Devarajan Balaraman - Amkor Technology, Inc. USA; Hideaki Shoji and Tomio Shiraiwan - J-Devices Corporation, Japan; KwangSeok Oh and Joon Young Park - Amkor Technology, Korea	***4. 10:00 a.m. - Vertical Laser Assisted Bonding for Advanced "3.5D" Chip-Packaging*** Andrej Kolbasow, Matthias Fettke and Georg Friedrich - Pac Tech GmbH; Timo Kubsch and Thorsten Teutsch – Pac Tech USA	***4. 10:00 a.m. - Mechanical and Electrical Characterization of FOWLP-Based Flexible Hybrid Electronics (FHE) for Biomedical Sensor Application*** Yuki Susumago, Qian Zhengyang, Achille Jacquemond, Noriyuki Takahashi, Hisashi Kino, Tetsu Tanaka, and Takafumi Fukushima – Tohoku University
5. 10:25 a.m. - Advanced Substrates for GaN-Based HEMTs Devices Anthony Cibié, Julie Widiez, René Escoffier, Denis Blachier, Kremena Vladimirova, Jean-Philippe Colonna, Paul-Henri Haumesser, Stéphane Bécu, Perceval Coudrain, William Vandendaele, Jerome Biscarrat, Charlotte Gillot, Matthew Charles, Lea Di Cioccio – CEA-LETI	***5. 10:25 a.m. - Optimization of a BEOL Aluminum Deposition Process Enabling Wafer Level Al-Al Thermo-Compression Bonding*** Sebastian Schulze, Matthias Wietstruck, Mirko Fraschke, and Mehmet Kaynak – Innovations for High Performance Microelectronics; Peter Kerepesi, Helmut Kurz, and Bernhard Rebhan – EV Group, Inc.	***5. 10:25 a.m. - A Wearable Fingernail Deformation Sensing System and Three-Dimensional Finite Element Model of Fingertip*** Katsuyuki Sakuma, Bucknell Webb, Rajeev Narayanan, Avner Abrami, Jeff Rogers, John Knickerbocker, and Stephen J. Heisig – IBM Thomas J. Watson Research Center
6. 10:50 a.m. - A New Reliable, Corrosion Resistant Gold-Palladium Coated Copper Wire Material Sandy Klengel, Robert Klengel, Jan Schischka, Tino Stephan, and Matthias Petzold – Fraunhofer IMWS; Motoki Eto, Noritoshi Araki, and Takashi Yamada – Nippon Micrometal Corporation	***6. 10:50 a.m. - Self-Assembly Process for 3D Die-to-Wafer Using Direct Bonding: A Step Forward Toward Process Automatisation*** Amandine Jouve, Loïc Sanchez, Clement Castan, Maxence Laugier, Emmanuel Rolland, Brigitte Montmayeul, Rémi Franiatte, Frank Fournel, and Severine Cheramy – CEA-LETI	***6. 10:50 a.m. - Heterogeneous Integration of a Fan-Out Wafer-Level Packaging Based Foldable Display on Elastomeric Substrate*** Arsalan Alam, Amir Hanna, Randall Irwin, Goutham Ezhilarasu, Hyunpil Boo, Yuan Hu, Chee Wei Wong, Timothy Fisher, and Subramanian S. Iyer – University of California, Los Angeles
7. 11:15 a.m. - Ultrasonic-Accelerated Intermetallic Joint Formation with Composite Solder for High-Temperature Power Device Packaging Hongjun Ji, Mingyu Li, Weiwei Zhao, and Wenwu Zhang, – Harbin Institute of Technology	***7. 11:15 a.m. - A Single Bonding Process for Diverse Organic-Inorganic Integration in IoT Devices*** Tilo H. Yang, Yu-Shan Chiu, Hai-Yang Yu, and C. Robert Kao – National Taiwan University; Akitsu Shigetou – National Institute for Materials Science	***7. 11:15 a.m. - A Study on the Flexible Chip-on-Fabric (COF) Assembly Using Anisotropic Conductive Films (ACFs) Materials*** Seung-Yoon Jung and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

Program Sessions: Wednesday, May 29, 1:30 p.m. - 5:30 p.m.

Session 7: Advances in Flip Chip Packaging	Session 8: Material and Process Trends in FOWLP and PLP	Session 9: Wearables and Thin-Package Reliability and Chip Package Interaction
Committee: Packaging Technologies	**Committee: Materials & Processing**	**Committee: Thermal/Mechanical Simulation & Characterization**
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: **Mike Gallagher** **DuPont Electronics & Imaging** **Daniel Baldwin** **H.B. Fuller Company**	**Session Co-Chairs:** **Tanja Braun** **Fraunhofer IZM** **Yi Li** **Intel Corporation**	**Session Co-Chairs:** **Przemyslaw Gromala** **Robert Bosch GmbH** **Yong Liu** **ON Semiconductor**
1. 1:30 p.m. - 7nm Chip-Package Interaction Study on a Fine-Pitch Flip Chip Package with Laser Assisted Bonding and Mass Reflow Technology Ian Hsu, Chi-Yuan Chen, Stanley Lin, and Ta-Jen Yu – MediaTek, Inc.; NamJu Cho and Ming-Che Hsieh – JCET	***1. 1:30 p.m. - Laser Releasable Temporary Bonding Film with High Thermal Stability*** Yong-suk Yang, Kyo-sung Hwang, and Robin Gorrell – 3M	***1. 1:30 p.m. - Effect of Charging Cycle Elevated Temperature Storage and Thermal Cycling on Thin Flexible Batteries in Wearable Applications*** Pradeep Lall and Amrit Abrol – Auburn University; Ben Leever – US AFRL; Scott Miller – NextFlex Manufacturing Institute
2. 1:55 p.m. - Ultra Large Area SIPs and Integrated mmW Antenna Array Module for 5G mmWave Outdoor Applications Pouya Talebbeydokhti, Sidharth Dalmia, Trang Thai, Raanan Sover, Sharon Tal – Intel Corporation	***2. 1:55 p.m. - Design and Demonstration of 1µm Low Resistance RDL Using Panel Scale Processes for High-Performance Computing Applications*** Bartlet DeProspo, Chandrasekharan Nair, Varun Rajagoapal, Jenefa Kannan, Emanuel Surillo, Fuhan Liu, Mohananlingam Kathaperumal, and Rao Tummala – 3D Systems Packaging Research Center, Georgia Institute of Technology; Aya Momozawa and Atsushi Kubo – Tokyo Ohka Kogyo Co., Ltd.	***2. 1:55 p.m. - Bladder Inflation Stretch Test Method for Reliability Characterization of Wearable Electronics*** Benjamin G. Stewart and Suresh K. Sitaraman – Georgia Institute of Technology
3. 2:20 p.m. - Hybrid Approach for Large Size FC-BGA to Enhance Thermal and Electrical Performance Including Power Delivery Heeseok Lee, Yunheok Im, Junghwa Kim, Jisoo Hwang, James Jeong, Youngsang Cho, Heejung Choi, and Youngmin Shin – Samsung Electronics Company, Ltd.	***3. 2:20 p.m. - Advances in Temporary Carrier Technology for High-Density Fan-Out Device Build-Up*** Arnita Podpod, Alain Phommahaxay, Pieter Bex, John Slabbekoorn, Julien Bertheau, Adbellah Salahouelhadj, Erik Sleeckx, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC; Alice Guerrero, Kim Yess, and Kim Arnold – Brewer Science, Inc.	***3. 2:20 p.m. - Study of BEOL Failure Mode in Flip-Chip Packages at High-Temperature Conditions*** Wei Wang, Yangyang Sun, Xuefeng Zhang, Lejun Wang, Lily Zhao, Mark Schwarz, Bill Stone, and Ahmer Syed – Qualcomm Technologies, Inc.
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall - Belmont 1 & 5		
4. 3:30 p.m. - Package-on-Package Micro-BGA Microstructure Interaction with Bond and Assembly Parameter Pascale Gagnon and Clément Fortin – IBM Canada Limited; Thomas Weiss – IBM Systems	***4. 3:30 p.m. - Development of Novel Low-Temperature Curable Positive-Tone Photosensitive Dielectric Materials with High-Reliability*** Yutaro Koyama, Yu Shoji, Keika Hashimoto, Yuki Masuda, Hitoshi Araki, and Masao Tomikawa – Toray Industries, Inc.	***4. 3:30 p.m. - A Novel Metal Scheme and Bump Array Design Configuration to Enhance Advanced Si Packages CPI Reliability Performance by Using Finite Element Modeling Technique*** Kuo-Chin Chang, Mirng-Ji Lii, Steven Hsu, Hao-Chun Liu, Yen-Kun Lai, Sheng-Han Tsai, and Chieh-Hao Hsu – Taiwan Semiconductor Manufacturing Company Ltd.
5. 3:55 p.m. - Low-Cost Flip-Chip Stack for Partitioning Processing and Memory Andy Heinig and Fabian Hopsch – Fraunhofer IIS/EAS	***5. 3:55 p.m. - Highly Reliable Photosensitive Negative-Tone Polyimide with Low Cure Shrinkage*** Daisaku Matsukawa, Hiroko Yotsuyanagi, Shiori Sakakibara, Noriyuki Yamazaki, Tetsuya Enomoto, and Takeharu Motobe – Hitachi Chemical DuPont MicroSystems, Ltd., Japan	***5. 3:55 p.m. - Assessment of CMP Fill Pattern Effect on the Thermal Performance of Interconnects in Integrated Circuits BEOL*** Assaad Helou and Peter Raad – Southern Methodist University; Archana Venugopal – Texas Instruments, Inc.
6. 4:20 p.m. - High-Density Ultra-Thin Organic Substrate for Advanced Flip-Chip Package Nokibul Islam, Seung Wook Yoon, KH Tan, and Tony Chen – STATS ChipPAC Pte. Ltd.	***6. 4:20 p.m. - High Rate and Low Damage Etching Method as Pre Treatment of Seed Layer Sputtering for Fan Out Panel Level Packaging*** Tetsushi Fujinaga – ULVAC, Inc.	***6. 4:20 p.m. - Three-Dimensional Simulation of the Thermo-Mechanical Interaction Between the Micro-Bump Joints and Cu Protrusion in Cu-Filled TSVs of the High Bandwidth Memory (HBM) Structure*** Jie-Ying Zhou, Shui-Bao Liang, Cheng Wei, Wen-Kai Le, Chang-Bo Ke, Min-Bo Zhou, Xiao Ma, and Xin-Ping Zhang – South China University of Technology
7. 4:45 p.m. - Impact of Low Temperature Solder on Electronic Package Dynamic Warpage Behavior and Requirement Wei Keat Loh - Intel Corporation; Ron W. Kulterman - Flex Ltd.; Haley Fu – iNEMI; Chih Chung Hsu - CoreTech System (Moldex3D)	***7. 4:45 p.m. - Investigation and Methods Using Various Release and Thermoplastic Bonding Materials to Reduce Die Shift and Wafer Warpage for eWLB Chip-First Processes*** Michelle Fowler and John P. Massey – Brewer Science, Inc.; Tanja Braun, Steve Voges, Robert Gernhardt, and Markus Wohrmann – Fraunhofer Institute IZM	***7. 4:45 p.m. - Study of Design Optimization Method for Ultra-Low Power Micro Gas Sensor*** Eiji Nakamura, Keiji Matsumoto, Andrea Fasoli, Luisa Bozano, and Hiroyuki Mori – IBM Research

Program Sessions: Wednesday, May 29, 1:30 p.m. - 5:30 p.m.

Session 10: Dicing and Encapsulation Technologies	Session 11: Automotive and Harsh-Environment Reliability	Session 12: Advanced Photonic Devices and Packaging
Committee: **Assembly & Manufacturing Technology**	**Committee:** **Applied Reliability**	**Committee:** **Photonics**
Nolita 2	**Nolita 3**	**Yaletown 1**
Session Co-Chairs: **Garry Cunningham** **JHU/APL** **Paul Tiner** **Texas Instruments**	**Session Co-Chairs:** **Sandy Klengel** **Fraunhofer Institute for Microstructure of Materials and Systems** **Vikas Gupta** **Texas Instruments, Inc.**	**Session Co-Chairs:** **Stephane Bernabe** **CEA Leti** **Gordon Elger** **Technische Hochschule Ingolstadt**
1. 1:30 p.m. - A More Than Moore Enabling Wafer Dicing Technology Jeroen van Borkulo, Rogier Evertsen, and Richard van der Stam – ASM Pacific Technologies Inc.	***1. 1:30 p.m. - Effect of Substrate Preheating Treatment on Thermal Reliability and Micro-Structure of Ag Paste Sintering on Au Surface Finish*** Zheng Zhang, Chuantong Chen, and Katsuaki Suganuma – Osaka University; Seigo Kurosaka – C. Uyemura & Co., Ltd.	***1. 1:30 p.m. - Micro-Fabricated SERF Atomic Magnetometer for Weak Gradient Magnetic Field Detection*** Xiang Yue, Jintang Shang, and Chen Ye – Southeast University
2. 1:55 p.m. - Plasma Dicing Integration Schemes for Scribe Lane Layout and the Impact on Die Strength David Parker, Emmanuel Gourvest, and Boris Bouillard – STMicroelectronics	***2. 1:55 p.m. - Package Material Selection Criteria for High Temperature Automotive Applications*** Rene Rongen, Amar Mavinkurve, Orla O'Halloran, Norman Owens, Yann Weber, Pascal Oberndorff, Mark Luke Farrugia, Erik Van Olst, and Michiel van Soestbergen – NXP Semiconductors	***2. 1:55 p.m. - Novel Solder Pads for Self-Aligned Flip-Chip Assembly*** Yves Martin, Swetha Kamlapurkar, Nathan Marchack, Jae-Woong Nah, and Tymon Barwicz – IBM Corporation
3. 2:20 p.m. - Advanced Dicing Technologies for Combination of Wafer-to-Wafer and Collective Die to Wafer Direct Bonding Fumihiro Inoue, Alain Phommahaxay, Arnita Podpod, Samuel Suhard, Erik Sleeckx, Kenneth June Rebibis, Andy Miller, and Eric Beyne – IMEC; Hitoshi Hoshino and Berthold Moeller – Disco Hi-Tech Europe GmbH	***3. 2:20 p.m. - Solder Joint Reliability of Double-Side Mounted DDR Modules for Consumer and Automotive Applications*** Dongji Xie, Joe Hai, Zhongming Wu, and Manthos Economou – Nvidia Corp.	***3. 2:20 p.m. - Collective Curved CMOS Sensor Process: Application for High-Resolution Optical Design and Assembly Challenges*** Bertrand Chambion, Christophe Gaschet, Marc Lombard, Maïlys Fernandez, Pierre Joly, Stéphane Caplet, Fabien Zuber, Aurélie Vandeneynde, Patrick Peray, Gilles Lasfargues, Marc Zussy, Jerome Deschamps, Alexi Bedoin, and David Henry – CEA LETI
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall - Belmont 1 & 5		
4. 3:30 p.m. - Active Control of NCF Fillet Shape for 3D CoW by Multi Beam Laser Bonder Keiko Ueno, Kazutaka Honda, Tsuyoshi Ogawa, and Toshihisa Nonaka – Hitachi Chemical Company, Ltd.	***4. 3:30 p.m. - Reliability Investigation of Extremely Large Ratio Fan-Out Wafer-Level Package With Low Ball Density for Ultra-Short-Range Radar*** PuShan Huang, C.K. Yu, W.S. Chiang, M.Z. Lin, Y.H. Fang, M.J. Lin, N.W. Liu, Benson Lin, and Ian Hsu – MediaTek Inc.	***4. 3:30 p.m. - Integration and Characterization of InP Die on Silicon Interconnect Fabric*** Eric Sorensen, Boris Vaisband, SivaChandra Jangam, and Subramanian S. Iyer – University of California, Los Angeles; Tim Shirley – Keysight Technologies
5. 3:55 p.m. - Ultrafast Laser Scribe: An Improved Metal and ILD Ablation Process Julia Chiu, Aaron Gore, and Tyler Osborn – Intel Corporation; Daragh Finn, Zhibin Lin, David Lord, and Jon Mellen – Electro Scientific Industries, Inc.	***5. 3:55 p.m. - Fatigue Behavior of Lead-Free Solder Joints Under Combined Thermal and Vibration Loads*** Karsten Meier, Maria Winkler, and Karlheinz Bock – Dresden University of Technology; David Leslie and Abhijit Dasgupta – University of Maryland	***5. 3:55 p.m. - Y-Branched Multimode/Single-Mode Polymer Optical Waveguides for Low-Loss WDM MUX Device: Fabrication and Characterization*** Takaaki Ishigure, Tomoki Nakayama, Fukino Nakazaki, and Hiroki Hama – Keio University
6. 4:20 p.m. - Reliability and Benchmark of 2.5D Non-Molding and Molding Technologies Yu-Hsiang Hsiao, Che-Ming Hsu, Yi-Sheng Lin, and Chien-Lin Chang Chien – Advanced Semiconductor Engineering, Group, Inc.	***6. 4:20 p.m. - Prognostication of Accrued Damage and Impending Failure Under Temperature-Vibration in Lead Free Electronics*** Pradeep Lall, Tony Thomas, and Jeff Suhling – Auburn University; Ken Blecker – US Army ARDEC	***6. 4:20 p.m. - Vertically Stacked and Directionally Coupled Cavity-Resonator-Integrated Grating Couplers for Integrated-Optic Beam Steering*** Shogo Ura and Junishi Inoue – Kyoto Institute of Technology; Kenji Kintaka – National Institute of Advanced Industrial Science and Technology
7. 4:45 p.m. - Laser-Induced Trench Design, Optimisation and Validation for Restricting Capillary Underfill Spread in Advanced Packaging Configurations Gul Zeb and David Danovitch – Université de Sherbrooke; Eric Turcotte – IBM Canada Ltd.	***7. 4:45 p.m. - Electrochemical Impedance Spectroscopy (EIS) for Monitoring the Water Load on PCBAs under Cycling Condensing Conditions to Predict Electrochemical Migration Under DC Loads*** Simone Lauser and Theresia Richter – Robert Bosch GmbH; Verdingovas Vadimas and Rajan Ambat – Technical University of Denmark	***7. 4:45 p.m. - CiB(Chip-in-Board) Optical Engine Module Using Advanced Fan-Out Package Technology*** Sang Yong Park, Ju Hyun Nam, Ji Ni Shim, Jun Kyu Lee, Yong Tae Kwon, Chang Woo Lee, Jong Heon Kim, and Nam Chul Kim - NEPES Corporation

Program Sessions: Thursday, May 30, 8:00 a.m. - 11:40 a.m.

Session 13: Technologies Enabling 3D and Heterogeneous Integration	Session 14: Fine-Pitch Solderless Bonding	Session 15: High-Bandwidth Packaging
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **High-Speed, Wireless & Components**
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: **Peng Su** **Juniper Networks** **Subhash L. Shinde** **University of Notre Dame**	**Session Co-Chairs:** **Chuan Seng Tan** **Nanyang Technological University** **Tom Gregorich** **Zeiss Semiconductor Manufacturing Technology**	**Session Co-Chairs:** **P. Markondeya Raj** **Florida International University** **Amit P. Agrawal** **Microsemi Corporation**
1. 8:00 a.m. - Active Interposer Technology for Chiplet-Based Advanced 3D System Architectures Perceval Coudrain, Jean Charbonnier, Arnaud Garnier, Pascal Vivet, Rémi Vélard, Andrea Vinci, Fabienne Ponthenier, Roselyne Segaud, Pascal Chausse, Lucile Arnaud, Didier Lattard, Eric Guthmuller, Giovanni Romano, Alain Gueugnot, Frédéric Berger, Therry Mourier, Mathilde Gottardi, Stéphane Minoret, Céline, Ribière, Gilles Romero, Pierre-Emile Philip, Yorrick Exbrayat, Daniel Scevola, Maxime Argoud, Nacima Allouti, Raphaël Eleouet, César Fuguet Tortolero, Christophe Aumont, Denis Dutoit, Corinne Legalland, Séverine Chéramy, and Gilles Simon - CEA, LETI; Alexis Farcy, Jérôme Beltritti, Didier Campos, and Jean Michailos – STMicroelectronics	***1. 8:00 a.m. - Fine-Pitch (≤10 µm) Direct Cu-Cu Interconnects Using In-Situ Formic Acid Vapor Treatment*** SivaChandra Jangam, Umesh Mogera, Pranav Ambhore, and Subramanian Iyer – University of California, Los Angeles; Adeel Ahmed Bajwa, Tom Colosimo, and Bob Chylak – Kulicke & Soffa Industries, Inc.	***1. 8:00 a.m. - Electrical Performance Limits of Fine-Pitch Interconnects for Heterogeneous Integration*** Ahmet Durgun, Zhiguo Qian, Kemal Aygun, Ravi Mahajan, Tim Tri Hoang, and Sergey Yuryevich Shumarayev – Intel Corporation
2. 8:25 a.m. - Process Development of Power Delivery Through Wafer Vias for Silicon Interconnect Fabric Meng-Hsiang Liu, Boris Vaisband, Amir Hanna, Yandong Luo, Zhe Wan, and Subramanian Iyer – University of California, Los Angeles	***2. 8:25 a.m. - Low-Temperature Cu Interconnect With Chip-to-Wafer Hybrid Bonding*** Guilian Gao, Laura Mirkarimi, Thomas Workman, Gill Fountain, Jeremy Theil, Gabe Guevara, Ping Liu, Bongsub Lee, Pawel Mrozek, and Michael Huynh– Xperi Corporation; Catharina Rudolph, Thomas Werner, and Anke Hanisch – Fraunhofer Institute, IZM-ASSID	***2. 8:25 a.m. - A High-Bandwidth Fine-Pitch 2.57Tbps/mm In-Package Communication Link Achieving 48fJ/Bit/mm Efficiency*** Nicolas Pantano, Geert Van der Plas, Pieter Bex, Philip Nolmans, Dimitrios Velenis, and Eric Beyne – IMEC; Marian Verhelst – KU Leuven
3. 8:50 a.m. - Active Through-Silicon Interposer Based 2.5D IC Design, Fabrication, Assembly and Test Jayasanker Jayabalan, Vivek Chidambaram, Sharon Lim Pei Siang, Wang Xiangyu, Jong Ming Chinq, and Surya Bhattacharya – Institute of Microelectronics A*STAR	***3. 8:50 a.m. - Cu Microstructure of High Density Cu Hybrid Bonding Interconnection*** Seokho Kim, Pilkyu Kang, Taeyeong Kim, Kyuha Lee, Joohee Jang, Kwangjin Moon, Hoonjoo Na, Sangjin Hyun, and Kihyun Hwang – Samsung Electronics Company, Ltd.	***3. 8:50 a.m. - A New SI-PI Co-Simulation Approach for Efficient Consideration of Coupling Between PDN and SDN*** Heeseok Lee, Jisoo Hwang, Hoi-Jin Lee, and Youngmin Shin – Samsung Electronics Company, Ltd
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Belmont 1 & 5		
4. 10:00 a.m. - System on Integrated Chips (SoIC (TM)) for 3D Heterogeneous Integration Ming-Fa Chen, Fang- Cheng Chen, Wen-Chih Chiou, and Doug C.H. Yu – Taiwan Semiconductor Manufacturing Company Ltd.	***4. 10:00 a.m. - Low-Resistance and High-Strength Copper Direct Bonding in No-Vacuum Ambient Using Highly (111)-Oriented Nano-Twinned Copper*** Jing-Ye Juang, Kai-Cheng Shie, Po-Ning Hsu, Yu Jin Li, and Chih Chen – National Chiao Tung University; K. N. Tu – University of California, Los Angeles	***4. 10:00 a.m. - Signal Integrity of Submicron InFO Heterogeneous Integration for High Performance Computing Applications*** Chuei-Tang Wang, Jeng-Shien Hsieh, Victor C. Y. Chang, Shih-Ya Huang, T. Ko, Han-Ping Pu, and Douglas Yu – Taiwan Semiconductor Manufacturing Company Ltd.
5. 10:25 a.m. - Die-to-Wafer (D2W) Processing and Reliability for 3D Packaging of Advanced Node Logic Luke England, Daniel Fisher, Katie Rivera, and Bill Guthrie – GLOBALFOUNDRIES; Ping-Jui Kuo, Chang-Chi Lee, Che-Ming Hsu, Fan-Yu Min, Kuo-Chang Kang, and Chen-Yuan Weng – Advanced Semiconductor Engineering	***5. 10:25 a.m. - Sub-10µm Pitch Hybrid Direct Bond Interconnect Development for Die-to-Die Hybridization*** John P. Mudrick, Jonatan A. Sierra-Suarez, Matthew B. Jordan, T. A. Friedmann, Robert Jarecki, and M. David Henry – Sandia National Laboratories	***5. 10:25 a.m. - 28GHz Through Glass Via (TGV) Based Band Pass Filter Using Through Fused Silica Via (TFV) Technology*** Renuka Bowrothu, Seahee Hwangbo, Todd Schumann, and Yong- Kyu Yoon – University of Florida
6. 10:50 a.m. - Enabling Ultra-Thin Die to Wafer Hybrid Bonding for Future Heterogeneous Integrated Systems Alain Phommahaxay, Samuel Suhard, Pieter Bex, Serena Iacovo, John Slabbekoorn, Fumihiro Inoue, Lan Peng, Koen Kennes, Erik Sleeckx, Gerald Beyer, and Eric Beyne – IMEC	***6. 10:50 a.m. - Cu Pillar with Nanocopper Caps: The Next Interconnection Node Beyond Traditional Cu Pillar*** Ramon Sosa, Kashyap Mohan, Antonia Antoniou, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Luu Nguyen – Texas Instruments Inc.	***6. 10:50 a.m. - Innovative Packaging Solutions of 3D Double Side Molding with System in Package for IoT and 5G Application*** Mike Tsai, Ryan Chiu, Dick Huang, Feng Kao, Eric He, J. Y. Chen, Simon Chen, Jensen Tsai, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.
7. 11:15 a.m. - The Thermal Dissipation Characteristics of the Novel System-in-Package Technology (ICE-SiP) for Mobile and 3D High-End Packages Taejoo Hwang, Dan(Kyung Suk) Oh, Eunseok Song, Jaechoon Kim, Taehun Kim, Kilsoo Kim, Joungphil Lee, and Taehwan Kim – Samsung Electronics Company, Ltd.	***7. 11:15 a.m. - Cu-Cu Bonding by Low-Temperature Sintering of Self-Healable Cu Nanoparticles*** Junjie Li, Qi Liang, Chen Chen, Tielin Shi, Guanglan Liao, and Zirong Tang – Huazhong University of Science and Technology	***7. 11:15 a.m. - Enhancing Efficiency of Antenna-in-Package (AiP) by Through-Silicon-Interposer (TSI) with Embedded Air Cavity and Polyimide Dielectric Micro-Substrate*** Yunna Sun, Yunting Sun, Jiangbo Luo, Huiying Wang, Zhuoqing Yang, Yan Wang, and Guifu Ding - Shanghai Jiao Tong University; Kwangwoo Han – Samsung Electronics Company Co., Ltd.

Program Sessions: Thursday, May 30, 8:00 a.m. - 11:40 a.m.

Session 16: Advanced Materials for High-Speed Electronics	Session 17: Materials and Design for Reliability of Next-Generation Packages	Session 18: Warpage and Material Performance
Committee: Materials & Processing	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Nolita 2	**Nolita 3**	**Yaletown 1**
Session Co-Chairs: **Yoichi Taira** **Keio University** **Yu-Hua Chen** **Unimicron**	**Session Co-Chairs:** **Varughese Mathew** **NXP Semiconductors** **Lakshmi N. Ramanathan** **Microsoft Corporation**	**Session Co-Chairs:** **Pradeep Lall** **Auburn University** **Karsten Meier** **Technische Universität Dresden**
1. 8:00 a.m. - Low-Loss Glass Substrates Formulated With a Variety of Dielectric Characteristics for mm Wave Applications Kazutaka Hayashi, Nobutaka Kidera, and Yoichiro Sato – AGC Inc.	***1. 8:00 a.m. - Highly (111)-Oriented Nanotwinned Cu for High Fatigue Resistance in Fan-Out Wafer-Level Packaging*** Yu-Jin Li, Chih-Han Theng, I-Hsin Tseng, and Chih Chen – National Chiao Tung University; Benson Lin and Chia-Cheng Chang – MediaTek Inc.	***1. 8:00 a.m. - Improved Finite Element Modeling of Moisture Diffusion Considering Discontinuity at Material Interfaces in Electronic Packages*** Lulu Ma and Xuejun Fan – Lamar University; Rahul Joshi and Keith Newman – Advanced Micro Devices, Inc.
2. 8:25 a.m. - Evaluation of Fine-Pitch Routing Capabilities of Advanced Dielectric Materials for High-Speed Panel-RDL in 2.5D Interposer and Fan-Out Packages Shreya Dwarakanath, Pulugurtha Markondeya Raj, Atsushi Kubo, Fuhan Liu, Mohanalingam Kathaperumal, and Rao R. Tummala – Georgia Institute of Technology; Amit Agarwal – Microchips; Daichi Okamaoto – Taiyo Ink Mfg. Co., Ltd.	***2. 8:25 a.m. - WLCSP Package and PCB Design for Board Level Reliability*** Jason Chiu, Kuo-Chin Chang, Pei-Haw Tsao, Steve Hsu, and Mirng-Ji Lii – Taiwan Semiconductor Manufacturing Company, Ltd.	***2. 8:25 a.m. - Study of Thermal Aging Behavior of Epoxy Molding Compound for Applications in Harsh Environments*** Adwait Inamdar, Alexandru Prisacaru, Martin Fleischman, Erick Franieck, and Przemyslaw Gromala – Robert Bosch GmbH; Agnes Veres and Csaba Nemeth – Robert Bosch Kft; Yu-Hsiang Yang and Bongtae Han – University of Maryland
3. 8:50 a.m. - Attenuation of High-Frequency Signals in Structured Metallization on Glass: Comparing Different Metallization Techniques with 24 GHz, 77 GHz and 100 GHz Structures Martin Letz, Mathias Mydlak – SCHOTT AG; Matthias Jost – Technische Universität Darmstadt; Brandon T. Gore and William J. Kozlovsky – Samtec Inc.; Romeo Premerlani and Alex Bruderer – Varioprint AG; Manuel Martina and Thomas Gottwald – Schweizer Electronic AG; Tetsuya Onishi – Grand Joint Technology Ltd.; Siddharth Ravichandran – Packaging Research Center; Holger Maune – Institute for Microwave Engineering and Photonics	***3. 8:50 a.m. - Assessing the Reliability of Highly Stretchable Interconnects for Flexible Hybrid Electronics*** Rajesh Sharma Sivasubramony, Ashwin Varkey Zachariah, Mohammed Alhendi, Manu Yadav, Peter Borgesen and Mark D. Poliks – Binghamton University; Nancy C. Stoffel, David M. Shaddock, and Liang Yin – GE Global Research	***3. 8:50 a.m. - Warpage Variation Analysis and Model Prediction for Molded Packages*** Yuling Niu, Wei Wang, Zhijie Wang, Karthik Dhandapani, Mark Schwarz, and Ahmer Syed – Qualcomm Technologies, Inc.
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Belmont 1 & 5		
4. 10:00 a.m. - The Highly Effective EMI Shielding Materials for Electric and Magnetic Fields Over the Wide Range of Frequency in Near-Field Region Yoon-Hyun Kim, Kisu Joo, Kyu Jae Lee, Jung Woo Hwang, Se Young Jeong Seung Jae Lee, and Hyun Ho Park – Ntrium Inc.	***4. 10:00 a.m. - The How and Why of Biased Humidity Tests with Copper Wire*** Amar Mavinkurve, Rene Rongen, Leon Goumans, Mark Luke Farrugia, Erik van Olst, Orla O'Halloran, and Michiel van Soestbergen – NXP Semiconductors	***4. 10:00 a.m. - Peridynamics for Predicting Thermal Expansion Coefficient of Graphene*** Erdogan Madenci, Atila Barut, and Mehmet Dorduncu – The University of Arizona
5. 10:25 a.m. - Low-Loss NCF Material for High-Frequency Device Kazutaka Honda, Keiko Ueno, Tsuyoshi Ogawa, and Toshihisa Nonaka – Hitachi Chemical Company, Ltd.	***5. 10:25 a.m. - Twist Testing for Flexible Electronics*** Justin Chow and Suresh Sitaraman – Georgia Institute of Technology; Jeffrey Meth – DuPont	***5. 10:25 a.m. - Machine Learning Approach to Improve Accuracy of Warpage Simulations*** Cheryl Selvanayagam, Pham Luu Trung Duong, and Nagarajan Raghavan – Singapore University of Technology and Design; Rathin Mandal - Advanced Micro Devices Inc.
6. 10:50 a.m. - In-Situ Redox Nanowelding of Copper Nanowires with Surficial Oxide Layer as Solder for Flexible Transparent Electromagnetic Interference Shielding Xianwen Liang, Jianwen Zhou, Gang Li, Tao Zhao, Pengli Zhu, and Rong Sun – Shenzhen Institutes of Advanced Technology; Ching-Ping Wong – Georgia Institute of Technology	***6. 10:50 a.m. - Mechanical Properties and Microstructural Fatigue Damage Evolution in Cyclically Loaded Lead-Free Solder Joints*** Sinan Su, Mohd Aminul Hoque, Md Mahmudur Chowdhury, Sa'd Hamasha, Jeffrey C. Suhling, John L. Evans, and Pradeep Lall – Auburn University	***6. 10:50 a.m. - Study on Warpage of Fan-Out Panel Level Packaging (FO-PLP) Using Gen-3 Panel*** Fa Xing Che, Kazunori Yamamoto, Vempati Srinivasa Rao and Vasarla Nagendra Sekhar– Institute of Microelectronics A*STAR
7. 11:15 a.m. - Compartmental EMI Shielding Material with Jet-Dispensed Material Technology Xuan Hong, Qizhuo Zhuo Zhuo, Xinpei Cao, Dan Maslyk, Noah Ekstrom, Juliet Sanchez, Selene Hernandez, and Jinu Choi – Henkel Corporation	***7. 11:15 a.m. - Reliability Studies of Silicon Interconnect Fabric*** Niloofar Shakoorzadeh, Siva Chandra Jangam, Pranav Ambhore, Amir Hanna, and Subramanian Iyer – University of California, Los Angeles; Kaysar Rahim – Global Foundries; Han Chien – National Chiao Tung University	***7. 11:15 a.m. - Mechanical Properties of Intermetallic Compounds at Elevated Temperature by Nanoindentation*** Fan Yang, Sheng Liu, and Zhiwen Chen – Wuhan University; Zhaoxia Zhou, Canyu Liu, and Changqing Liu – Loughborough University; Li Liu – Wuhan University of Technology

Program Sessions: Thursday, May 30, 1:30 p.m. - 5:30 p.m.

Session 19: MEMS, Sensors, and IoT	Session 20: Fan-Out and Heterogeneous Integration	Session 21: 5G, mm-Wave, and Antenna-in-Package
Committee: Packaging Technologies	**Committee: Interconnections**	**Committee: High-Speed, Wireless & Components**
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: **Joseph W. Soucy** **Draper Laboratory** **Ning Ge** **Consultant**	**Session Co-Chairs:** **Jean-Charles Souriau** **CEA Leti** **Wei-Chung Lo** **ITRI**	**Session Co-Chairs:** **Maciej Wojnowski** **Infineon Technologies AG** **Xiaoxiong (Kevin) Gu** **IBM Corporation**
1. 1:30 p.m. - A MEMS Microphone in a FOWLP Horst Theuss, Christian Geissler, Franz-Xaver Muehlbauer, Claus von Waechter, Thomas Kilger, Juergen Wagner, Thomas Fischer, Ulf Bartl, Stephan Helbig, Alfred Sigl, Dominic Maier, Bernd Goller, Matthias Vobl, Matthias Herrmann, Johannes Lodermeyer and Ulrich Krumbein – Infineon Technologies; Alfons Dehe - Hahn-Schickard	***1. 1:30 p.m. - Feasibility Study of Fan-Out Wafer-Level Packaging for Heterogeneous Integrations*** John Lau, Ming Li, Nelson Fan, Eric Kuah, Raymond So, Penny Lo, Y. M. Cheung, Cao Xi – ASM Pacific Technology; Iris Xu, Tony Chen, Kim Hwee Tan, and Zhang Li – Jiangyin Changdian Advanced Packaging Co., Ltd.; Cao Xi (Huawei Technologies Co. Ltd.); Rozalia Beica – Dow Chemical Company; Sze Pei Lim, NC Lee – Indium Corporation; Cheng-Ta Ko, Henry Yang, and YH Chen – Unimicron Technology Corporation; Mian Tao, Jeffery Lo, and Ricky Lee – Hong Kong University of Science and Technology	***1. 1:30 p.m. - Vivaldi Antenna Array Fabricated Using a Hybrid Process*** Vincens Gjokaj, Cameron Crump, John Albrecht, John Papapolymerou, and Premjeet Chahal – Michigan State University
2. 1:55 p.m. - Fan-Out Wafer Level Packaging - A Platform for Advanced Sensor Packaging Tanja Braun, Karl-Friedrich Becker, Ole Hoelck, Steve Voges, Ruben Kahle, Pascal Graap, Markus Wöhrmann, and Rolf Aschenbrenner – Fraunhofer IZM; Marc Dreissigacker, Martin Schneider-Ramelow, and Klaus-Dieter Lang – Technical University Berlin	***2. 1:55 p.m. - Experiment of 22FDX® Chip Board Interaction (CBI) in Wafer Level Packaging Fan-Out (WLPFO)*** Jae Kyu Cho, Jens Paul, Simone Capecchi, Frank Kuechenmeister, and Ta-Chien Cheng – GLOBALFOUNDRIES	***2. 1:55 p.m. - Novel Multicore PCB and Substrate Solutions for Ultra Broadband Dual Polarized Antennas for 5G Millimeter Wave Covering 28GHz & 39GHz Range*** Trang Thai, Sidharth Dalmia, Josef Hagn, Pouya Talebbeydokhti, and Yossi Tsfati – Intel Corporation
3. 2:20 p.m. - 3D-MID Evaluation and Validation for Space Applications Etienne Hirt and Klaus Ruzicka – Art of Technology AG; Benedikt Wigger, Maximilian Barth, Rafat Saleh, and Florian Janek – Hahn Schickard; Ernst Müller – Universitat Stuttgart Institute of Microintegration	***3. 2:20 p.m. - FOWLP Design for Digital and RF Circuits*** Teck Guan Lim, David Soon Wee Ho, Eva Wai Leong Ching, Zihao Chen and Surya Bhattacharya – Institute of Microelectronics A*STAR	***3. 2:20 p.m. - 3D Glass Package-Integrated, High-Performance Power Dividing Networks for 5G Broadband Antennas*** Muhammad Ali, Atom Watanabe, Tong-Hong Lin, Manos Tentzeris, and Rao Tummala – Georgia Institute of Technology; Markondeya Raj Pulugurtha – Florida International University
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall - Belmont 1 & 5		
4. 3:30 p.m. - High-Temperature Pressure Sensor Package and Characterization of Thermal Stress in the Assembly up to 500 °C Nilavazhagan Subbiah, Qingming Feng, and Juergen Wilde – University of Freiburg; Gudrun Bruckner - CTR AG, Austria	***4. 3:30 p.m. - Next-Generation of 2-7 Micron Ultra-Small Microvias for 2.5D Panel Redistribution Layer by Using Laser and Photolithography Technologies*** Fuhan Liu, Chandrasekharan Nair, Gaurav Khurana, Atom Watanabe, Bartlet H. DeProspo, and Rao R. Tummala – Georgia Institute of Technology; Atsushi Kubo – Tokyo Ohka Kogyo Co., Ltd. Japan; Cheng Ping Lin, Toshiyuki Makita and Naoki Watanabe – Panasonic Corporation	***4. 3:30 p.m. - Advanced Wafer-Level PKG Solutions for 60GHz WiGig (802.11ad) Telecom Infrastructure*** Dapeng Wu, Robin Dahlbäck, Erik Öjefors, and Mats Carlsson - Sivers IMA AB; Francis Chee Peng Lim, Yew Kheng Lim, Aung Kyaw Oo, Won Kyung Choi, and Seung Wook Yoon – STATS ChipPAC Pte. Ltd.
5. 3:55 p.m. - Development of 3D WLCSP with Black Shielding for Optical Finger Print Sensor for the Application of Full Screen Smart Phone Daquan Yu, Yichao Zou, Xirui Xu, Aihua Shi, Xiaobing Yang and Zhiyi Xiao – Huantian Technology (Kunshan) Electronics Co., Ltd.	***5. 3:55 p.m. - Multilayer RDL Interposer for Heterogeneous Device and Module Integration*** Yi Hang Lin, M.C. Yew, M.S. Liu, S.M. Chen, T.M. Lai, Pravin Kavle, C.H. Lin, T.J. Fang, C.S. Chen, C.T. Yu, P.Y. Lin, Shin-Puu Jeng and K.C. Lee – Taiwan Semiconductor Manufacturing Company Ltd.	***5. 3:55 p.m. - Low-Loss Additively-Deposited Ultra-Short Copper Paste Interconnections in 3D Antenna-Integrated Packages for 5G and IoT Applications*** Atom Watanabe, Yiteng Wang, Markondeya R. Pulugurtha, Vanessa Smet, Manos Tentzeris, and Rao Tummala – Georgia Institute of Technology; Nobuo Ogura – Nagase & Co., Ltd.; P. Markondeya Raj – Florida International University
6. 4:20 p.m. - Micro Fountain-Like Resonators Jianfeng Zhang, Jintang Shang, Bin Luo, and Zhaoxi Su – Southeast University	***6. 4:20 p.m. - Effects of Dielectric Curing Conditions on the Interfacial Adhesion of Cu RDL for Fan-Out Wafer Level Packaging*** Gahui Kim and Kirak Son, and Young-Bae Park – Andong National University; Dogeun Kim - Korea Institute of Materials Science; Seok-Hyun Lee – Samsung Electronics Co., Ltd.	***6. 4:20 p.m. - Advanced Thin-Profile Fan-Out with Beamforming Verification for 5G Wideband Antenna*** Ricky Hsieh, Fu-Cheng Chu, Cheng-Yu Ho, and Chen-Chao Wang – Advanced Semiconductor Engineering Inc.
7. 4:45 p.m. - Novel Additively Manufactured Packaging Approaches for 5G/mm-Wave Wireless Modules Tong-Hong Lin, Aline Eid, Jimmy Hester, Bijan Tehrani, and Manos Tentzeris – Georgia Institute of Technology; Jo Bito – Texas Instruments, Inc.	***7. 4:45 p.m. - Al-Al Direct Bonding with Sub-µm Alignment Accuracy for Millimeter Wave SiGe BiCMOS Wafer Level Packaging and Heterogeneous Integration*** Matthias Wietstruck, Sebastian Schulze, Selin Tolunay Wipf, Christian Wipf, and Mehmet Kaynak – IHP Leibniz Institute for Innovative Microelectronics; Bernhard Rebhan, Peter Kerepesi, Helmut Kurz, Gerald Silberer, and Josef Meiler – EV Group, E. Thallner GmbH	***7. 4:45 p.m. - Integrated Compact Planar Inverted-F Antenna (PIFA) with a Shorting via Wall for Millimeter-Wave Wireless Chip-to-Chip (C2C) Communications in 3D-SiP*** Seahee Hwangbo, Renuka Bowrothu, Hae-in Kim, and Yong-Kyu Yoon – University of Florida

Program Sessions: Thursday, May 30, 1:30 p.m. - 5:30 p.m.

Session 22: Advanced Substrates and Interconnect Technology	Session 23: High-Bandwidth 3D and Photonic	Session 24: Advancements in Solder Joint Characterization and Reliability Evaluation
Committee: Materials & Processing	**Committee: Photonics in conjunction with Interconnections**	**Committee: Applied Reliability**
Nolita 2	**Nolita 3**	**Yaletown 1**
Session Co-Chairs: **Kimberly Yess** **Brewer Science** **Mikel Miller** **EMD Performance Materials**	**Session Co-Chairs:** **Takaaki Ishigure** **Keio University** **Dingyou Zhang** **Broadcom Inc.**	**Session Co-Chairs:** **Scott Savage** **Medtronic Microelectronics Center** **Pei-Haw Tsao** **Taiwan Semiconductor Manufacturing Company, Ltd.**
1. 1:30 p.m. - Temporary SiC-SiC Wafer Bonding Compatible With High Temperature Annealing Fengwen Mu and Tadatomo Suga – The University of Tokyo; Miyuki Uomoto and Takehito Shimatsu – Tohoku University	***1. 1:30 p.m. - A Highly Reliable 1.4um Pitch Via-last TSV Module for Wafer-to-Wafer Hybrid Bonded 3D-SOC Systems*** Stefaan Van Huylenbroeck, Joeri De Vos, Zaid El-Mekki, Geraldine Jamieson, Nina Tutunjyan, Karthik Muga, Michele Stucchi, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC	***1. 1:30 p.m. - Effects of In and Zn Double Addition on Eutectic Sn-58Bi Alloy*** Shiqi Zhou, Yu-An Shen, and Hiroshi Nishikawa – Osaka University; Tiffani Uresti, Vasanth Shunmugasamy, and Bilal Mansoor – Texas A&M University at Qatar
2. 1:55 p.m. - Ultrathin Glass to Ultrathin Glass Bonding Using Laser Sealing Approach Messaoud Bedjaoui, Johnny Amiran, and Jean Brun – CEA-LETI	***2. 1:55 p.m. - Nanoscale Topography Characterization for Direct Bond Interconnect*** Bongsub Lee, Pawel Mrozek, Gill Fountain, John Posthill, Jeremy Theil, Guilian Gao, Rajesh Katkar, and Laura Mirkarimi – Xperi Corporation	***2. 1:55 p.m. - Microstructural Evolution in SAC+X Solders Subjected to Aging*** Jing Wu, Jeffrey C. Suhling, and Pradeep Lall – Auburn University
3. 2:20 p.m. - Development of Resins for Bumpless Interconnects and Wafer-on-Wafer (WOW) Integration Naoko Araki and Shinji Maetani – Daicel Corporation; Kim Young Suk and Shoichi Kodama – Disco Corporation; Takayuki Ohba – Tokyo Institute of Technology	***3. 2:20 p.m. - Fully-Filled, Highly-Reliable Fine-Pitch Interposers With TSV Aspect Ratio >10 for Future 3D-LSI/IC Packaging*** Murgesan Murugesan, Takafumi Fukushima, Kiyonharu Mori, Ai Nakamura, Yisang Lee, Makoto Motoyoshi, J.C Bea, and Mitsumasa Koyanagi – Global INTegration Initiative; Shigeru Watariguchi – Meltex Inc.	***3. 2:20 p.m. - Microstructure Signature Evolution in Solder Joints, Solder Bumps, and Micro-Bumps Interconnection in a Large 2.5D FCBGA Package During Thermo-Mechanical Cycling*** Arman Ahari, Andy Hsiao, Tae-Kyu Lee, and Greg Baty – Portland State University; Peng Su – Juniper Networks
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall - Belmont 1 & 5		
4. 3:30 p.m. - Development of Novel Photosensitive Dielectric Material for Reliable 2.1D Package Yune Kumazawa, Seiji Shika, Shunsuke Katagiri, Takuya Suzuki, Tsuyoshi Kida, and Shu Yoshida – Mitsubishi Gas Chemical Company, Inc.	***4. 3:30 p.m. - 3D Silicon Photonics Interposer for Tb/s Optical Interconnects in Data Centers With Double-Side Assembled Active Components and Integrated Optical and Electrical Through Silicon Via on SOI*** Bogdan Sirbu, Yann Eichhammer, Hermann Oppermann, and Tolga Tekin – Fraunhofer IZM; Victor Sidorov and Jochen Kraft – AMS AG; Xin Yin and Johan Bauwelinck – IMEC; Christian Neumeyr – VERTILAS GmbH; Francisco Soares – Fraunhofer HHI	***4. 3:30 p.m. - Long-Term Reliability of Solder Joints in 3D ICs Under Near-Application Conditions*** Omar Ahmed, Golareh Jalilvand, Hector Fernandez, and Tengfei Jiang – University of Central Florida; Peng Su – Juniper Networks; Tae-Kyu Lee – Portland State University
5. 3:55 p.m. - High Reliability Solder Resist With Strong Adhesion and High Resolution for High Density Packaging Sawako Shimada, Kazuya Okada, Tomoya Kudo, Chiho Ueta, and Yuya Suzuki – Taiyo Ink Mfg. Co., Ltd.	***5. 3:55 p.m. - Flip-Chip III-V-to-Silicon Photonics Interfaces for Optical Sensor*** Yves Martin, Jason Orcutt, Chi Xiong, Laurent Schares, Tymon Barwicz, Martin Glodde, Swetha Kamlapurkar, Eric J. Zhang, and William M.J. Green – IBM Corporation; Victor Dolores-Calzadilla, Martin Moehrle and Ariane Sigmund – Fraunhofer HHI	***5. 3:55 p.m. - Experimental Investigation of the Correlation between a Load-Based Metric and Solder Joint Reliability of BGA Assemblies on System Level*** Fabian Schempp, Marc Dressler, Daniel Kraetschmer, and Friederike Loerke – Robert Bosch GmbH; Juergen Wilde – University of Freiburg, IMTEK
6. 4:20 p.m. - Method for Mitigating the Warpage of Ultra-thin FC-CSPs by Controlling of EMC Properties Chika Arayama, Takahiro Akashi, Yasunari Tomita, and Naoki Kanagawa – Panasonic Corporation	***6. 4:20 p.m. - Extremely Low-Profile Single Mode Fiber Array Coupler Suitable for Silicon Photonics*** Mitsuharu Hirano, Akira Furuya, Hideki Machida, Koichi Koyama, Yasunori Murakami, and Kazunori Tanaka – Sumitomo Electric Industries, Ltd.	***6. 4:20 p.m. - Fatigue Life Predictive Model Development for Decoupling Capacitors*** Krishna Tunga, Joseph Ross, Kamal Sikka, and Bakul Parikh – IBM Corporation
7. 4:45 p.m. - Innovative Socketable and Surface-Mountable BGA Interconnections Omkar Gupte, Kristie Teoh, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Gregorio Murtagian – Intel Corporation	***7. 4:45 p.m. - Micro-Lens Array Assembly for Optical Organic Substrates*** Patrick Jacques, Richard Langlois, Elaine Cyr, Alexander Janta-Polczynski, and Paul Fortier – IBM Bromont, Canada; Koji Masuda, Masao Tokunari, and Hsiang-Han Hsu – IBM Tokyo Research	***7. 4:45 p.m. - A Study of Substrate Models and Its Effect on Package Warpage Prediction*** Van Lai Pham, Jiefeng Xu, Jing Wang, Huayan Wang and Seungbae Park – Binghamton University; Charandeep Singh – Corning, Inc.

Program Sessions: Friday, May 31, 8:00 a.m. - 11:40 a.m.

Session 25: Wafer Level Packaging and Fan-In/Fan-Out Structures & Materials	Session 26: High-Speed Signaling for High-Performance Computing and Memory	Session 27: Advanced Biosensors and Bioelectronics
Committee: **Packaging Technologies**	**Committee:** **High-Speed, Wireless & Components**	**Committee:** **Emerging Technologies**
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: **Albert Lan** **Applied Materials** **Andrew Kim** **Intel Corporation**	**Session Co-Chairs:** **Rockwell Hsu** **Cisco Systems, Inc.** **Jaemin Shin** **Qualcomm Corporation**	**Session Co-Chairs:** **Zhuo Li** **Fudan University** **Jimin Yao** **Intel Corporation**
1. 8:00 a.m. - 3D Fan-Out Package Technology with Photosensitive Through Mold Interconnects Kentaro Mori, Soichi Yamashita, Takafumi Fukuda, Masahiro Sekiguchi, Hirokazu Ezawa, and Shuzo Akejima – Toshiba Corporation	***1. 8:00 a.m. - Hybrid Prepreg Conventional Build-Up Laminate for 112Gbit/s SerDes*** Kwang Won Choi, Edmund Blackshear, Eric Tremble, and David Stone – GLOBALFOUNDRIES; Jean Audet – IBM Canada Ltd.; Keiichi Hirabayashi – Shinko Electric Industries Company, Ltd.	***1. 8:00 a.m. - Flexible Probe for Electrical Neural Signal Recording*** Sajay Bhuvanendran Nair Gourikutty and Ruiqi Lim – Institute of Microelectronics A*STAR
2. 8:25 a.m. - Effects of the Materials Properties of Epoxy Molding Films (EMFs) on Fan-Out Packages (FOPs) Characteristics Sangmyung Shin, Hanmin Lee, JunMo Kim, Tae-Ik Lee, Taek-Soo Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; Youjin Kyung, Minsu Jeong, and Kwangjoo Lee – LG Chem	***2. 8:25 a.m. - PI/SI Analysis and Design Approach for HPC Platform Applications*** Sungwook Moon, Chanmin Jo, and Seungki Nam – Samsung Electronics Company, Ltd.	***2. 8:25 a.m. - Stretchable, Implantable Nanomembrane Biosensor for Wireless, Real-Time Monitoring of Hemodynamics*** Robert Herbert and Woon-Hong Yeo – Georgia Institute of Technology
3. 8:50 a.m. - Mechanism of Moldable Underfill (MUF) Process for RDL-1st Fan-Out Panel Level Packaging (FOPLP) Lin Bu, F.X. Che Vempati Srinivasa Rao, and Xiaowu Zhang – Institute of Microelectronics A*STAR	***3. 8:50 a.m. - PoP LPDDR5 (6.4 Gbps) NTODT and 1-tap DFE for Signal Integrity Enhancement*** Sunil Gupta – Qualcomm Technologies, Inc.	***3. 8:50 a.m. - A Wearable Passive pH Sensor for Health Monitoring*** Saikat Mondal, Saranraj Karuppuswami, Rachel Steinhornst, and Premjeet Chahal – Michigan State University
Refreshment Break: 9:15 a.m. - 10:00 a.m. Mont-Royal Commons		
4. 10:00 a.m. - Study of the Board Level Reliability Performance of a Large 0.3 mm Pitch Wafer-Level Package Bernd Waidhas, Jan Proschwitz, Christoph Pietryga, Thomas Wagner, and Beth Keser – Intel Deutschland GmbH	***4. 10:00 a.m. - Open CAPI Memory Interface Signal Integrity Study for High-Speed DDR5 Differential DIMM Channel With Standard Loss FR-4 Material and SNIA SFF-TA-1002 Connector*** Biao Cai, Jose Hejase, Kyle Giesen, Junyan Tang, Brian Connolly, Kyu- Hyoun Kim, and Daniel Dreps – IBM Corporation; Zhineng Fan, Rocky Huang, Luyun Yi, Qiaoli Chen, Yifan Huang, and Stephen Smith - Amphenol ICC	***4. 10:00 a.m. - Novel Packaging Structure and Processes for Micro-TFB (Thin Film Battery) to Enable Miniaturized Healthcare Internet-of-Things (IoT) Devices*** Bing Dang, Qianwen Chen, Leanna Pancoast, Yu Luo, Hongqing Zhang, Jae-woong Nah, and John Knickerbocker – IBM Corporation; Andy Shih, Po Wen Cheng, Kai Liu, Mengnian Niu, Simon Nieh – Front Edge Technologies, Inc.
5. 10:25 a.m. - Study of Board Level Reliability of eWLB (Embedded Wafer-Level BGA) for 0.35mm Ball Pitch Seung Wook Yoon, Yeow Kheng Lim, Seng Guang Chow, Kang Chen, Won Kyung Choi, and Kang Hai Lee – STATS ChipPAC Pte. Ltd.; NW Liu, Yenyao Chi, and Benson Lin – MediaTek, Inc.	***5. 10:25 a.m. - Effectiveness of Equalization and Performance Potential in DDR5 Channels With RDIMM(s)*** Nanju Na and Hing "Thomas" To – Xilinx, Inc.	***5. 10:25 a.m. - Printed Temporary Transfer Tattoos for Skin-Mounted Electronics*** Samuli Tuominen and Matti Mäntysalo – Tampere University of Technology
6. 10:50 a.m. - Board Level Reliability Study of Fan-Out Single Die Package with 350um Bump Pitch Chieh Lung Lai, Gu-Yan Lin, Tz-Yuan Chao, Yih-Sin Chen, and Feng-Lung Chien – Siliconware Precision Industries Co., Ltd.	***6. 10:50 a.m. - Inductive Links for 3D Stacked Chip-to-Chip Communication*** Xiao Sun, Nicolas Pantano, Kim Soon-Wook, Geert Van der Plas, and Eric Beyne – IMEC	***6. 10:50 a.m. - Thermoset Polymers for Bioelectronic Interfaces: Engineering of Thermomechanical Properties*** Adriana Carolina Duran-Martinez, Alexandra Joshi-Imre, Seyedmahmoud Hosseini, Daniel Del Nero, Walter E. Voit, and Melanie Ecker – The University of Texas at Dallas
7. 11:15 a.m. - The Analysis for Bump Resistance Improvement by Optimizing the Sputter Condition Ming-Sin Su, Chang-Ning Wang, Clair Tsai, T. L. Yang, Rolance Yang, W. C. Wu, C. S. Liu, J.M. Chiu, Y. F. Chen, Ponder Pang, Harry Ku, Kirin Wang, C.H. Su, Steven Hsu, Calvin Lu, K.C. Liu and Marvin Liao – Taiwan Semiconductor Manufacturing Company Ltd.	***7. 11:15 a.m. - System Co-Design of a 600V GaN FET Power Stage with Integrated Driver in a QFN System-in-Package (QFN-SiP)*** Jie Chen, Yong Xie, Django Trombley, and Rajen Murugan – Texas Instruments, Inc.	***7. 11:15 a.m. - Direct Heterogeneous Bonding of SiC to Si, SiO2, and Glass for High-Performance Power Electronics and Bio-MEMS*** Jikai Xu, Chenxi Wang, Qiushi Kang, Shicheng Zhou, and Yanhong Tian – Harbin Institute of Technology

Program Sessions: Friday, May 31, 8:00 a.m. - 11:40 a.m.

Session 28: Embedded and Integrated Technologies	Session 29: Electromigration and Innovative Reliability Test Methods	Session 30: Assembly and Process Modeling
Committee: Assembly & Manufacturing Technology in conjunction with Packaging Technology	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Nolita 2	**Nolita 3**	**Yaletown 1**
Session Co-Chairs: **Christo Bojkov** **Qorvo** **John H. Lau** **ASM Pacific Technology**	**Session Co-Chairs:** **Keith Newman** **AMD** **Pilin Liu** **Intel Corporation**	**Session Co-Chairs:** **Suresh K. Sitaraman** **Georgia Institute of Technology** **Kuo-Ning Chiang** **National Tsinghua University**
1. 8:00 a.m. - Development of Flexible Hybrid Electronics Using Reflow Assembly With Stretchable Film Weifeng Liu, William Uy, Alex Chan, and Dongkai Shangguan – Flex, Ltd.; Andy Behr, Takatoshi Abe, and Fukao Tomohiro – Panasonic Corporation	***1. 8:00 a.m. - Effect of Intermetallic Compound Growth on Electromigration Failure Mechanism in Low-Profile Solder Joints*** Hossein Madanipour, Yi-Ram Kim, and Choong-Un Kim – The University of Texas at Arlington; Ninad Shashane, Dibyajat Mishra, T. Noguchi, M. Yoshino, and Luu Nguyen – Texas Instruments, Inc.	***1. 8:00 a.m. - Explicit FE Failure Prediction of Interfaces and Interconnect in Potted Electronics Assemblies Subject to High-G Acceleration Loads*** Pradeep Lall and Kalyan Dornala – Auburn University; John Deep – US AFRL; Ryan Lowe – ARA Associates
2. 8:25 a.m. - Highly Compact RF Transceiver Module Using High Resistive Silicon Interposer with Embedded Inductors and Heterogeneous Dies Integration Gabriel Pares, Jean-Philippe Michel, Edouard Deschaseaux, Pierre Ferris, Ayssar Serhan, and Alexandre Giry – CEA-LETI	***2. 8:25 a.m. - Effect of Grain Orientation and Microstructure Evolution on Electromigration in Flip-Chip Solder Joint*** Xing Fu, Bin Zhou, Yunfei En, and Si Chen (Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, China), Ruohe Yao – South China University of Technology	***2. 8:25 a.m. - Numerical Simulation on the Formation Process of Metal Droplets by Pneumatic Diaphragm Drop-On Demand Technology*** Kun Ma, Sheng Liu, Zhiwen Chen, and Li Liu – Wuhan University of Technology; Hao Zheng and Yao Zhang – China Ship Development and Design Center
3. 8:50 a.m. - Process Induced Wafer Warpage Optimization for Multi-Chip Integration on Wafer Level Molded Wafer Chen-Yu Huang, Daniel Ng, Hung-Ho Lee, Vito Lin, Chang Fu Lin, and C. Key Chung – Siliconware Precision Industries Co., Ltd.	***3. 8:50 a.m. - High Electromigration Lifetimes of Nanotwinned Cu Redistribution Lines*** I-Hsin Tseng, Yu-Jin Li, and Chih Chen – National Chiao Tung University; Benson Lin and Chia-Cheng Chang – MediaTek, Inc.	***3. 8:50 a.m. - On Curing-Induced Residual Stresses After Molding Processes: Mold Shrinkage, Chemical Shrinkage or Both?*** Changsu Kim, Sukrut Phansalkar, Hyun-Seop Lee, and Bongtae Han – The University of Maryland
Refreshment Break: 9:15 a.m. - 10:00 a.m. Mont-Royal Commons		
4. 10:00 a.m. - Improved Structure for Package Substrates with Embedded Thin-Film Capacitor Tomoyuki Akahoshi and Daisuke Mizutani – Fujitsu Laboratories, Ltd.; Kei Fukui, Shogo Yamawaki, and Hidehiko Fujisaki – Fujitsu Interconnect Technologies, Ltd.; Manabu Watanabe and Masateru Koide – Fujitsu Advanced Technologies, Ltd.	***4. 10:00 a.m. - Non-Destructive Failure Analysis of Various Chip to Package Interaction Anomalies in FCBGA Packages Subjected to Temperature Cycle Reliability Testing*** Vishnu Vardhan Busi Reddy and I. Charles Ume – Georgia Institute of Technology; Jaimal Williamson and Luu Nguyen – Texas Instruments, Inc.	***4. 10:00 a.m. - Realistic Solder Joint Geometry Integration with Finite Element Analysis for Reliability Evaluation of Printed Circuit Board Assembly*** Chun Sean Lau, Ning Ye, and Hem Takiar – Western Digital Corporation
5. 10:25 a.m. - 3D Packaging with Embedded High-Power-Density Passives for Integrated Voltage Regulators Teng Sun, Robert Spurney, Atom Watanabe, Pulugurtha Markondeya, Himani Sharma, Rao Tummala, and – Georgia Institute of Technology; Furukawa Yoshihiro – Nitto Denko Corporation	***5. 10:25 a.m. - Assessment of Accelerometer Versus LASER for Board Level Vibration Measurements*** Varun Thukral, Maëlle Cahu, Jeroen Zaal, Jeroen Jalink, Romuald Roucou, and Rene Rongen – NXP Semiconductors	***5. 10:25 a.m. - Multi-Physics Modelling and Experimental Investigation – An Original Approach for Laser-Dicing/Grooving Process Optimization*** Jeff Moussodji Moussodji and Dominique Drouin – 3IT University de Sherbrooke; Oswaldo Chacon and Francis Santerre – IBM Canada Ltd.
6. 10:50 a.m. - A Novel Panel Level Double Side-Embedded Package for Small Size Power Devices Kunpeng Ding and Mian Huang - Shenzhen Siptory Technologies Co., Ltd.; Zhichao Wu and Jian Cai – Tsinghua University; Bowei Zhang – Wuxi Sky Chip Interconnection Technology Co., Ltd.	***6. 10:50 a.m. - Effect of Process Parameters on the Long-Run Print Consistency and Material Properties of Additively Printed Electronics*** Pradeep Lall, Amrit Abrol, Nakul Kothari, Jeff Suhling, and Sudan Ahmed – Auburn University; Ben Leever – US AFRL; Scott Miller – NextFlex Manufacturing Institute	***6. 10:50 a.m. - Thermal Characteristics of Vertically Integrated GaN/SiC-on-Si Assemblies: A Comparative Study*** Kimmo Rasilainen and Christian Fager – Chalmers University of Technology; Per Ingelhag and Peter Melin – Ericsson AB; Torbjörn M. J. Nilsson – Saab AB; Mattias Thorsell – Chalmers University of Technology & Saab AB
7. 11:15 a.m. - Chiplet Microassembly Printer Brad Rupp, Anne Plochowietz, Lara S. Crawford, Matthew Shreve, Sourobh Raychaudhuri, Sergey Butylkov, Yunda Wang, Ping Mei, Qian Wang, Jamie Kalb and Yu Wang, Eugene M. Chow and Jeng Ping Lu – Palo Alto Research Center Inc.	***7. 11:15 a.m. - A Viscoplastic-Based Fatigue Reliability Model for the Polyimide Dielectric Thin-Film*** Yu-Chen Chang and Tz-Cheng Chiu – National Cheng Kung University; Yu-Ting Yang, Yi-Hsiu Tseng, and Xi-Hong Chen – Advanced Semiconductor Engineering Group, Inc.	***7. 11:15 a.m. - Comprehensive Investigation on Warpage Management of FOPLP With Multi-Embedded Ring Designs*** Chang-Chun Lee, Yan-Yu Liou, and Pei-Chen Huang – National Tsing Hua University; Fussen Hsu, Puru Bruce Lin, Cheng-Ta Ko, and Yu-Hua Chen – Unimicron Technology Corporation

Program Sessions: Friday, May 31, 1:30 p.m. - 5:30 p.m.

Session 31: Automotive and Power Packaging	Session 32: Power and Panel Assembly	Session 33: Fan-Out, Flip Chip, and WLCSP
Committee: Packaging Technologies	**Committee: Assembly & Manufacturing Technology in conjunction with Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Mont-Royal 1	**Mont-Royal 2**	**Nolita 1**
Session Co-Chairs: **Young-Gon Kim** **Integrated Device Technology, Inc.** **Kuo-Chung Yee** **Taiwan Semiconductor Manufacturing Corporation, Inc.**	**Session Co-Chairs:** **Habib Hichri** **Suss Microtech Photonic Systems Inc.** **Shichun Qu** **Intersil, a Renesas Company**	**Session Co-Chairs:** **Ning Ye** **Western Digital** **Wei Wang** **Qualcomm Technologies, Inc.**
1. 1:30 p.m. - Development of High Power and High Junction Temperature SiC Based Power Packages Gongyue Tang, Leong Ching Wai, Teck Guan Lim, Yong Liang Ye, Ravinder Pal Singh, Lin Bu, Boon Long Lau, Tai Chong Chai, Kazunori Yamamoto, and Xiaowu Zhang – Institute of Microelectronics A*STAR	***1. 1:30 p.m. - An RDL-First Fan-out Panel-Level Package for Heterogeneous Integration Applications*** Yu-Min Lin, Sheng-Tsai Wu, Ang-Ying Lin, Shin-Yi Huang, and Tao-Chih Chang – Industrial Technology Research Institute (ITRI); Chun-Min Wang, Puru Bruce Lin, Yu-Hua Chen and Cheng-Ta Ko – Unimicron Technology Corporation; Chia-Hsin Lee and Jay Su Jay Su – Brewer Science; Kuan-Neng Chen – National Chiao Tung University	***1. 1:30 p.m. - A Sequential Finite Volume Method / Finite Element Analysis of a Power Electronic Semiconductor Chip*** Mario Gschwandl, Peter Fuchs, and Ivaylo Mitev – Polymer Competence Center Leoben GmbH; Thomas Antretter – University of Leoben; Martin Pfost – Technical University of Dortmund; Tao Qi and Thomas Krivec – AT & S Austria Technologie & Systemtechnik AG; Angelika Schingale, and Michael Decker – CPT Group, GmbH
2. 1:55 p.m. - New Developments of Copper Plating Technology for Embedded Power Chip Packages Challenges Yung-Da Chiu, Shiu-Chih Wang, David Tarng, An-Tai Wu, Allenyl Chen, Louis Chen, and Chi-Tsung Chiu – Advanced Semiconductor Engineering Inc.	***2. 1:55 p.m. - High-Density Flexible Substrate Technology with Thin Chip Embedding and Partial Carrier Release Option for IoT and Sensor Applications*** Kai Zoschke, Piotr Mackowiak, Ha-Duong Ngo, Christian Tschoban, Carola Fritsche, Kevin Kröhnert, Thorsten Fischer, and Ivan Ndip – Fraunhofer IZM; Klaus-Dieter Lang – Technical University Berlin	***2. 1:55 p.m. - Failure Life Prediction of Wafer Level Packaging Using DoS with AI Technology*** K.N Chiang, H.Y. Hsiao, and P.H Chou – National Tsing Hua University
3. 2:20 p.m. - Innovative Flip Chip Package Solutions for Automotive Applications Tom Tang, Bo-Siang Fang, David Ho, B.H. Ma, Jensen Tsai, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.	***3. 2:20 p.m. - Advances in High-Speed Plating for Vertical Glass Panel Fine-Line Plating*** Raoul Schroeder, Herbert Ötzlinger, Christian Dunkel, and Tetsuya Onishi – Semsysco GmbH	***3. 2:20 p.m. - Thermal Cycling Simulation and Sensitivity Analysis of Wafer-Level Chip-Scale Package with Integration of Metal-Insulator-Metal Capacitors*** Yong Liu and Liangbiao Chen – ON Semiconductor; Yi Zhou and Suresh K. Sitaraman – Georgia Institute of Technology
Refreshment Break: 2:45 p.m. - 3:30 p.m. Mont-Royal Commons		
4. 3:30 p.m. - Reliability of Laminated Bond Structure Using (Cu,Ni)/Sn TLP Bonding with Al Interlayer for High-Temperature Power Electronics Packaging Yanghe Liu, Shailesh Joshi, and Ercan M. Dede – Toyota Research Institute North America	***4. 3:30 p.m. - High-Yield Precision Transfer and Assembly of GaN µLEDs Using Laser Assisted Micro Transfer Printing*** Goutham Ezhilarasu, Amir Hanna, and Subramanian Iyer – University of California, Los Angeles; Ajit Paranjpe – Veeco Instruments, Inc.	***4. 3:30 p.m. - Effect of Time-Dependent Bulk Modulus on Reliability Assessment of Automotive Electronic Control Unit*** Hyun Seop Lee and Bongtae Han – University of Maryland; Przemyslaw Gromala – Robert Bosch GmbH
5. 3:55 p.m. - Silver Sintering on Organic Substrates for the Embedding of Power Semiconductor Devices Alexander Schiffmacher, Lorenz Litzenberger, and Juergen Wilde – IMTEK University of Freiburg; Till Huesgen and Vladimir Polezhaev – Kempten University of Applied Sciences	***5. 3:55 p.m. - Study of the Properties of AlN PMUT Used as a Wireless Power Receiver*** Dan Gong, Shenglin Ma, Yihsiang Chiu, and Hungping Lee – Xiamen University; Yufeng Jin – Peking University	***5. 3:55 p.m. - Thermal and Mechanical Simulations for Fan-Out Wafer-Level Packaging Technology: Introduction of a "Solder Heatsink"*** Jean Colonna, Mathilde Cartier, Gabriel Pares, Dominique Noguet, and Loic Marnat – CEA-LETI
6. 4:20 p.m. - High-Temperature Resistant Packaging Technology for SiC Power Module by Using Ni Micro-Plating Bonding Kohei Tatsumi, Isamu Morisako, Keiko Wada, Minoru Fukuomori, and Tomonori Iizuka – Waseda University; Nobuaki Sato, Koji Shimizu, and Kazutoshi Ueda – Mitsui High-tec Inc.; Masayuki Hikita – Kyushu Institute of Technology; Rikiya Kaminura – Kittakyushu Foundation for the Advancements of Industry, Science and Technology; Naoki Kawanabe – WALTS Co., Ltd. Kazuhiko Sugiura and Kazuhiro Tsuruta – DENSO Corporation; Keiji Toda – Toyota Motor Corporation	***6. 4:20 p.m. - Large Panel Size Bonder With High-Performance and High-Accuracy*** Hubert Selhofer, Hugo Pristauz, and Andreas Mayr – Besi Austria GmbH	***6. 4:20 p.m. - Wafer-Level Warpage Modeling and Validation for FOWLP Considering Effects of Viscoelastic Material Properties Under Process Loadings*** Xiaowu Zhang, Zhaohui Chen, Sharon Pei Siang Lim, Simon Siak Boon Lim, Boon Long Lau, Yong Han, Ming Chinq Jong, Songlin Liu, Xiaobai Wang, and Yosephine Andriani – Institute of Microelectronics A*STAR
7. 4:45 p.m. - Pb-Free, High Thermal and Electrical Performance Driven Die Attach Material Development for Power Packages Byong Jin Kim, DongSu Ryu, Hyeong Il Jeon, Weng Tuck Chim, Jin Young Khim, and Muhammad Hadhari Hazellah – Amkor Technology, Inc.	***7. 4:45 p.m. - Advance Embedded Packaging for Power Discrete Device*** Jing Jiang, Guanqiang Song, Jiaren Huo, Juntao Wang, and Lingwen Kong – Wuxi Sky Chip Interconnention Technology Co., Ltd.	***7. 4:45 p.m. - Ultra-Thin Package Board Level Drop Impact Modeling and Validation*** Shu-Shen Yeh, P. Y. Lin, M. C. Yew, W. Y. Lin, K. C. Lee, C. C. Yang, J. H. Wang, P. C. Lai, C. K. Hsu, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company Ltd.

Program Sessions: Friday, May 31, 1:30 p.m. - 5:30 p.m.

Session 34: Emerging Materials and Processing	Session 35: New Interconnects for Package Scaling	Session 36: RF and Power Components and Modules
Committee: Materials & Processing in conjunction with Applied Reliability	**Committee: Interconnections**	**Committee: High-Speed, Wireless & Components**
Nolita 2	**Nolita 3**	**Yaletown 1**
Session Co-Chairs: **Ziyin Lin** **Intel Corporation** **Dwayne Shirley** **Inphi**	**Session Co-Chairs:** **David Danovitch** **University of Sherbrooke** **Katsuyuki Sakuma** **IBM Corporation**	**Session Co-Chairs:** **Yong-Kyu Yoon** **University of Florida** **Craig Gaw** **NXP Semiconductor**
1. 1:30 p.m. - Flexible Graphene-Glass Fiber Composite Film With Ultrahigh Thermal Conductivity and Mechanical Strength as Highly Efficient Thermal Interface Materials Xiaoliang Zeng, Linlin Ren, and Rong Sun – Shenzhen Institutes of Advanced Technology; Jianbin Xu – The Chinese University of Hong Kong; Ching-Ping Wong – Georgia Institute of Technology	***1. 1:30 p.m. - Development of 2.3D High Density Organic Package Using Low Temperature Bonding Process With Sn-Bi Solder*** Shota Miki, Hiroshi Taneda, Naoki Kobayashi, Kiyoshi Oi, Koji Nagai, and Toshinori Koyama – Shinko Electric Industries Co. Ltd.	***1. 1:30 p.m. - Multilayer Decoupling Capacitor Using Stacked Layers of BST and LNO*** Todd Schumann, Sheng-Po Fang, and Yong-Kyu Yoon – University of Florida; Jongmin Yook and Dongsu Kim – Korea Electronics Technology Institute
2. 1:55 p.m. - Highly Thermal Conductive and Electrically Insulated Graphene Based Thermal Interface Material With Long-Term Reliability Ya Liu and Johan Liu – Chalmers University of Technology; Shujing Chen – Shanghai University; Lilei Ye and Nan Wang – SHT Smart High Tech AB	***2. 1:55 p.m. - PowerTherm Attach Process for Power Delivery and Heat Extraction in the Silicon-Interconnect Fabric Using Thermocompression Bonding*** Pranav Ambhore, Boris Vaisband, Umesha Mogera, Ujash Shah, Timothy Fisher, Mark Goorsky, and Subramaniam S. Iyer – University of California, Los Angeles	***2. 1:55 p.m. - System Co-Design of a High Current (40A) Synchronous Step-Down Converter in an Innovative Multi-chip Module (MCM) in LQFN-Type Packaging Technology*** Todd Harrison, Jie Chen, and Rajen Murugan – Texas Instruments, Inc.
3. 2:20 p.m. - Further Enhancement of Thermal Conductivity through Optimal Uses of h-BN Fillers in Polymer-Based Thermal Interface Material for Power Electronics Han Jiang, Han Zhou, Stuart Robertson, Zhaoxia Zhou, Liguo Zhao, and Changqing Liu – Loughborough University	***3. 2:20 p.m. - Interconnect Scheme for Die-to-Die and Die-to-Wafer Level Heterogeneous Integration for High-Performance Computing*** Rabindra N. Das, Vladimir Bolkhovsky, Christopher Galbraith, Daniel Oates, Jason J. Plant, Renée Lambert, Scott Zarr, Ravi Rastogi, Dmitri Shapiro, Manuel Docanto, Terence Weir, Leonard Johnson – MIT Lincoln Laboratory	***3. 2:20 p.m. - Integrating Solid State Protection with a RF-MEMS Switch for Achieving ESD Robustness*** Srivatsan Parthasarathy, Padraig Fitzgerald, Javier Salcedo, Ray Goggin, and Jean-Jacques Hajjar – Analog Devices, Inc.
Refreshment Break: 2:45 p.m. - 3:30 p.m. Mont-Royal Commons		
4. 3:30 p.m. - Wafer-Level Integration of Thin Silicon Bare Dies Within Flexible Label Jean-Charles Souriau, Ahmad Itawi, and Laëtitia Castagné – CEA-LETI	***4. 3:30 p.m. - Ultra-Wide Micro Bumps Interconnection Matrix for Particle Detection: Process and Assembly*** Jean Charbonnier, Myriam Assous, Thierry Mourier, Celine Ribière, Stéphane Minoret, Sophie Verrun, Pierre Tissier, Remi Coquand, Mehmet Bicer, Fabienne Allain, Rémi Franiatte, Gabriel Paras – CEA-LETI	***4. 3:30 p.m. - A Zero Height Small Size Low Cost RF Interconnect Substrate Technology for RF Front Ends for M.2 Modules and Sip*** Swathi Vijayakumar, Kirthika Nahalingam, Sidharth Dalmia, and Pouya Talebbeydokhti – Intel Corporation
5. 3:55 p.m. - Laser Sintering of Aerosol Jet Printed Conductive Interconnects on Paper Substrates Mohammed Alhendi, Darshana Weerawarne, Jack Lombardi, Rajesh S. Sivasubramony, Peter Borgesen, and Mark Poliks – Binghamton University; Azar Alizadeh – GE Global Research	***5. Low-Temperature Transient Liquid Phase (TLP) Bonding Using Eutectic Sn-In Solder Anisotropic Conductive Films (ACFs) for Flexible Ultrasonic Transducers*** Jae-Hyeong Park and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; Jongcheol Park – National NanoFab Center	***5. 3:55 p.m. - Open and Closed Loop Inductors for High-Efficiency System-on-Package Integrated Voltage Regulators*** Claudio Alvarez, Mohamed Bellaredj, and Madhavan Swaminathan – Georgia Institute of Technology
6. 4:20 p.m. - In-Situ Investigation of Organic Additive Interactions in Copper Electroplating Solutions With Surface Enhanced Raman Spectroscopy (SERS) Nithin Nedumthakady, Bartlet DeProspo, Himani Sharma, Nasrin Hooshmand, Sajanlal Panikkanvalappil, and Rao Tummala – Georgia Institute of Technology; Rahul Manepalli and Sashi Kandanur – Intel Corporation	***6. 4:20 p.m. - Development of a No Reflow Cu Pillar Bump to Improve Chip/Package Interactions (CPI) Process and Reliability Performance*** Kuei Hsiao (Frank) Kuo, Yen Neng Wang, Feng Lung Chien, Rick Lee, and Jiunn Jie Wang – Siliconware Precision Industries Co., Ltd.	***6. 4:20 p.m. - RF Inductors Integrated in Organic Packaging*** Denis Mercier, Jean-Philippe Michel, Christine Raynaud, and Christophe Billard – CEA-LETI
7. 4:45 p.m. - C4 Compatible Ultra-Thick Cu On-Chip Magnetic Inductor Architecture Integrated With Advanced Polymer/Cu Planarization Process S.B Yang, CC. Kuo, Y.N. Chen, K.S Yuan, G.C. Huang, C.N Ke, Grace Chang, C.C. Hsu, H.L. Huang, Kirin Wang, Harry Ku, C.S. Chen, K.C. Liu, Alex Kalnitsky and Marvin Liao - Taiwan Semiconductor Manufacturing Company Ltd.	***7. 4:45 p.m. - A Novel Interconnection Technology Using Ultra-Thin Under Barrier Metal for Multiple Chip-on-Chip Stacking Structure*** Takuya Nakamura, Kan Shimizu, Masataka Maehara, Toshihiko Hayashi, Kentaro Akiyama, and Junichiro Fujimagari – Sony Semiconductor Solutions Corporation; Tomohiro Ohkubo, Atsushi Fujiwara, and Hayato Iwamoto – Sony Semiconductor Manufacturing	***7. 4:45 p.m. - 3D Printed Interposer Layer for High-Density Packaging of IoT Devices*** Saikat Mondal, Mohd. Ifwat Mohd. Ghazali, Kanishka Wijewardena, Deepak Kumar, and Premjeet Chahal – Michigan State University

Wednesday, May 29, 2019

Session 37: Interactive Presentations 1
9:00 AM - 11:00 AM
Committee: Interactive Presentations
Room: Belmont Commons
Session Co-Chairs:
Nam Pham
IBM Corporation
Pavel Roy Paladhi
IBM Corporation

1. Comprehensive Solution for Micro Bump Coplanarity Control
Rung-De Wang, J.H. Chen, Y.N. Hsu, Chun-Chen Liu, Y.C. Wang, B.E. Ho, Y.H. Wu, Ponder Pan, Harry Ku, and Kirin Wang , Calvin Lu, K.C. Liu, and Marvin Liao– Taiwan Semiconductor Manufacturing Company Ltd.

2. Structural Enhancement for a CMOS-MEMS Microphone Under Thermal Loading by Taguchi Method
Chun-Lin Lu and Meng-Kao Yeh – National Tsing Hua University

3. A Methodology to Correct In-Fixture Measurement of Impedance by a Machine Learning Model
Bo-Siang Fang, Cha-Chu Lai, Ying-Wei Lu, Kuan-Ta Chen, Mike Tsai, and Don-Son Jiang – Siliconware Precision Industries Co., Ltd.

4. Material and Structure Design Optimization for Panel-Level Fan-Out Packaging
Ian Hu, Dao-Lang Chen, Karen Yu Chen, Meng-Kai Shih, David Tarng, Dinos Huang, and JY On – Advanced Semiconductor Engineering Inc.

5. The Microstructure and Mechanical Property of the High Entropy Alloy as a Low Temperature Solder
Yingxia Liu, Xiuchen Zhao, Zhuangzhuang Hou, and Li Pu – Beijing Institute of Technology; Quanfeng He and Yong Yang – City University of Hong Kong; King-Ning Tu – University of California, Los Angeles

6. A Versatile Fan-Out Infrastructure Based on Die-Stencil Substrate Promoted by an Advanced Multifunctional Temporary Bonding Material
Xiao Liu, Baron Huang, Hong Zhang, Lisa Kirchner, Arthur Southard, Rama Puligadda, and Tony Flaim – Brewer Science, Inc.

7. Low Temperature and Pressureless Microfluidic Electroless Bonding Process for Vertical Interconnections
Han-Tang Hung, S. Yang, I. A. Weng, and C. R. Kao – National Taiwan University; Y. H. Chen – Unimicron Technology Corporation

8. 3D Integration of CMOS-Compatible Surface Electrode Ion Trap and Silicon Photonics for Scalable Quantum Computing
Jing Tao, Yu Dian Lim, Nam Piau Chew, Peng Zhao, and Chuan Seng Tan – Nanyang Technological University; Hong Yu Li, Anak Agung Alit Apriyana, and Lin Bu – Institute of Microelectronics, Agency for Science, Technology and Research A*STAR; Luca Guidoni – Université Paris Diderot and Chuan Seng Tan-Nanyang Technological University

9. Integrated RTD Sensors for Maintaining Thermal Uniformity During TCB Process
Salwa Ben Jemaa and Julien Sylvestre – University de Sherbrooke; Pascale Gagnon – IBM Canada, Ltd.

10. Wireless Transfer of Power and Data via a Single Resonant Inductive Link
Lih-Tyng Hwang, Yi-Chen Hsieh, Chin-Wei Chan, I-Fang Lo, Heri Suryoatmojo, and Shiang-Hwua Yu – National Sun Yat-Sen University

11. Adaptive Patterning of Optical and Electrical Fan-Out for Photonic Chip Packaging
Ahmed Elmogi, Andres Desmet, Jeroen Missinne, Hannes Ramon, Joris Lambrecht, Johan Bauwelinck, and Geert Van Steenberge – Ghent University; Peter De Heyn, Marianna Pantouvaki, and Joris Van Campenhout – IMEC

12. Low Surface Reflectance at Near Infrared Wavelength Thermoplastic Optical Lens Without AR Coating
Sho Yakabe, Takuro Watanabe, and Takayuki Shimazu – Sumitomo Electric Industries, Ltd.; Ryohei Hokari and Kazuma Kurihara – National Institute of Advanced Industrial Science and Technology

13. A Novel Design of a Bandwidth Enhanced Dual-Band Impedance Matching Network with Coupled Line Wave Slowing
Deepayan Banerjee and Antra Saxena – Indraprastha Institute of Information Technology, Delhi; Mohammad Hashmi – Nazarbayev University

14. Effects of Electromigration on Microstructural Evolution and Mechanical Properties of Preferential Growth Intermetallic Compound Interconnects for 3D Packaging
Mingliang Huang and Lin Zou – Dalian University of Technology

15. Telemetry for Implantable Biosensors
Ryan Green and Erdem Topsakal – Virginia Commonwealth University

16. Ultra-Thin QFN-Like 3D Package With 3D Integrated Passive Devices
Ayad Ghannam – 3DiS Technologies; Niek van Haare and Sebastiaan Kersjes – Besi NL; Julian Bravin and Elisabeth Brandl – EV Group; Birgit Brandstätter, Hannes Kingler, and Benedikt Auer – Besi AT; Philippe Meunier – NXP Semiconductors

17. Low-Cost Non-TSV Based 3D Packaging Using Glass Panel Embedding (GPE) for Power-Efficient, High-Bandwidth Heterogeneous Integration
Siddharth Ravichandran, Fuhan Liu, Vanessa Smet, Mohanalingam Kathaperumal, and Rao Tummala – Georgia Institute of Technology; Shuhei Yamada – Murata Manufacturing Co., Ltd.

18. Polylithic Integration of 2.5D and 3D Chiplets Using Interconnect Stitching
Paul Jo, Ting Zheng, and Muhannad Bakir – Georgia Institute of Technology

19. Characterization of the Current Mechanisms and Improved Leakage Current in Silver Doped Barium Stronium Titanate
Todd Schumann, Kyoung-Tae Kim, Sheng-Po Fang, and Yong-Kyu Yoon – University of Florida

20. High-Temperature Aging Effects in SAC and SAC+X Lead-Free Solders
Mohmmad Alam, KM Rafidh Hassan, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

Wednesday, May 29, 2019

Session 38: Interactive Presentations 2
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Room: Belmont Commons
Session Co-Chairs:
Patrick Thompson
Texas Instruments, Inc.
Rao Bonda
Amkor Technology

1. Laundering Reliability of Electrically Conductive Fabrics for E-Textile Applications
Jeffrey Lee, ChangHo Lo, and Cheng-Chih Chen – Integrated Service Technology; Weifeng Liu – Flex, Ltd.

2. Preconditioning Technologies for Sputtered Seed Layers in FOPLP
Johannes Weichart, Jürgen Weichart, and Andreas Erhart – Evatec Corporation; Kay Viehweger – Fraunhofer IZM, Berlin

3. Impact of Thermal Boundary Resistance on the Thermal Design of GaN-on-Diamond HEMTs
Huaixin Guo, Yuechan Kong, and Tangsheng Chen – Nanjing Electronic Devices Institute

4. Measuring the Electric Properties of Thin Film Shape Memory Polymers in Simulated Physiological Conditions
Daniel Del Nero, Alexandra Joshi-Imre, and Walter Voit – The University of Texas at Dallas

5. Evaluation of WLP Dielectrics for High-Voltage Applications
Markus Woehrmann, Marcus Paeck, and Michael Toepper – Fraunhofer IZM; Klaus-Dieter Lang – TU Berlin

6. Mitigating the Effects of Microvortices in High-Re Deterministic Lateral Displacement by Using Symmetric Airfoil-Shaped Pillars
Jong-Hoon Kim, Kawkab Ahasan, and Brian Dincau – Washington State University

7. Plasma Dry Process Technology Development of Glass-Epoxy Film on the Silicon Substrate to Fabricate RDL for Future GPU/AI Application.
Takahide Murayama, Muneyuki Sato, Akiyoshi Suzuki, Atsuhito Ihori, Tetsushi Fujinaga, and Yasuhiro Morikawa – ULVAC, Inc.

8. Fully Solid-State Integrated Capacitors Based on Carbon Nanofibers and Dielectrics with Specific Capacitances Higher than 200 nF/mm^2
Amin Saleem, Rickard Andersson, Maria Bylund, Guilhem Pacot, Shafiq Kabir, and Vincent Desmaris – Smoltek AB; Charlotte Goemare – SmoltekAB

9. Application of Fan-Out Panel Level Packaging Techniques for Flexible Hybrid Electronics Systems
Wei-Yuan Cheng, Chen-Tsai Yang, Shau-Fei Cheng, Wei-Han Chen, Hsin-Cheng Lai, Tai-Jui Wang, and Yuh-Zheng Lee – Industrial Technology Research Institute (ITRI)

10. Structuring of Laser Activated Polymers for Sensor Applications
Kevin Cromwell, Sebastian Bengsch, Aue, and Marc Wurz – Leibniz University Hanover

Wednesday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. in Exhibit Hall - Belmont 1 & 5

11. A Deep Learning Approach for Volterra Kernel Extraction for Time Domain Simulation of Weakly Nonlinear Circuits
Thong Nguyen, Xinying Wang, Xu Chen, and Jose Schutt-Aine – University of Illinois

12. 224G Package Interconnect Study Based on Artificial Neural Network Modeling Approach
Hui Liu, Qian Ding, and Penglin Liu – Intel Corporation

13. Enhanced Reliability of a RF-SiP With Mold Encapsulation and EMI Shielding
Chan-Yuan Liu, Kuo-Hsien Liao, Yu-Chou Tseng, Dao-Long Chen, Alex Chan, Mengkai Shih, Mark Gerber, and Jason Chien – Advanced Semiconductor Engineering Inc.

14. Study of the Effect and Mechanism of a Cap Layer in Controlling the Statistical Variation of Via Extrusion
Golareh Jalilvand and Tengfei Jiang – University of Central Florida

15. Least-Squares Method Built in Processing Model of Finite Element Analysis Utilized to Obtain Accurate Prediction for Non-Axisymmetric Warpage of 2L ETS MUF FCCSP SiP
Chih-Sung Chen, Nicholas Kao, Poyu Liao, Ssu-Cheng Lai, and Don Son Jiang – Siliconware Precision Industries Co., Ltd.

16. Three-Dimensional Copper Foam-Filled Elastic Conductive Composites With Simultaneously Enhanced Mechanical, Electrical, Thermal and Electromagnetic Interference (EMI) Shielding Properties
Yougen Hu, Han Gu, Tao Zhao, Tan Lu, Pengli Zhu, and Rong Sun – Shenzhen Institutes of Advanced Technology; Ching-Ping Wong – Georgia Institute of Technology

17. Vertical Interconnect Technology for Enlarging Capacity on Micro Solid Thin Film Rechargeable Battery
Akihiro Horibe, Kuniaki Sueoka, Risa Miyazawa, Takahiro Mori, and Hiroyuki Mori – IBM Corporation

18. Characterization of Fine Pitch Hybrid Bonding Pads Using Electrical Misalignment Test Vehicles
Imed Jani, Didier Lattard, Pascal Vivet, Edith Beigné, and Lucile Arnaud – CEA-LETI; Alexis Farcy, Joris Jourdan, Yann Henrion, Emilie Deloffre, and Haim Bilgen – STMicroelectronics

19. Dynamic Characteristics Evaluation on NCF Under Challenging Conditions and Its Application
Tomonori Nakamura, Hiromi Shibahara, Osamu Watanabe, Tetsuya Utano, Daisuke Tani, Sung Chenhsiu, Toru Maeda, and Doug Day – Shinkawa Ltd.; Hidekazu Yagi, Ryoji Kojima, Daichi Mori, Tatsuo Nagamatsu, and Junichi Kaneko – Dexerials Corporation

20. Study of Electrical and Mechanical Characteristics of Inkjet-Printed Patch Antenna Under Uniaxial and Biaxial Bending
Yi Zhou, Rui Chen, Nahid Aslani Amoli, Sridhar Sivapurapu, Mohamed Bellaredj, Madhavan Swaminathan, and Suresh Sitaraman – Georgia Institute of Technology

21. Effects of Oven and Laser Sintering Parameters on the Electrical Resistance of IJP Nano-Silver Traces on Mesoporous PET Before and During Fatigue Cycling
Gurvinder Singh Khinda, Maan Z. Kokash, Mohammed Alhendi, M. Yadav, Jack P. Lombardi, Darshana L. Weerawarne, Mark D. Poliks, and Peter Borgesen – Binghamton University; Nancy C. Stoffel – GE Global Research

22. Multilayer Glass Substrate With High-Density Via Structure for All Inorganic Multi-Chip Module
Toshiki Iwai, Taiji Sakai, Daisuke Mizutani, and Seiki Sakuyama – Fujitsu Laboratories, Ltd.; Kenji Iida, Takayuki Inaba, Hidehiko Fujisaki, Akira Tamura, and Yoshinori Miyazawa – Fujitsu Interconnect Technologies Limited

23. The Poisson's Ratio of Lead-Free Solder – The Often Forgotten but Important Material Property
KM Rafidh Hassan, Mohammad Alam, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

24. Additive Laser Metal Deposition onto Silicon for Enhanced Microelectronics Cooling
Arad Azizi, Matthias Daeumer, Jacob C. Simmons, Bahgat G. Sammakia, Bruce T. Murray, and Scott Schiffres – Binghamton University

25. Moisture Barrier, Mechanical, and Thermal Properties of PDMS-PIB Blends for Solar Photovoltaic (PV) Module Encapsulant
Jinho Hah, Michael Sulkis, Chao Ren, Kyoung-Sik (Jack) Moon, Samuel Graham, and C. P. Wong – Georgia Institute of Technology

Thursday, May 30, 2019

Session 39: Interactive Presentations 3
9:00 AM - 11:00 AM
Committee: Interactive Presentations
Room: Belmont Commons
Session Co-Chairs:
Michael Mayer
University of Waterloo
Alan Huffman
Micross Advanced Interconnect Technology

1. Modeling and Design of Power Distribution Network for a Heterogeneous Integrated Active Interposer With Neuromorphic Computing Circuits
Min Miao, Tianfang Chen, Jincan Zhang, Na Li, Kunkun Li, and Liyuan Wang – Beijing Information Science and Technology University; Yang Yang, Xiaole Cui, and Yufeng Jin – Shenzhen Graduate School, Peking University; Huan Liu – Peking University

2. PCB Microstrip Line Far-End Crosstalk Mitigation by Surface Mount Capacitors
Zhaoqing Chen – IBM Corporation

3. New Cost-Effective Via-Last Approach by "One-Step TSV" After Wafer Stacking for 3D Memory Applications
Masaya Kawano, Xiang-Yu Wang, and Qin Ren – Institute of Microelectronics A*STAR

4. Microstructure and Property Changes in Cu/Sn-58Bi/Cu Solder Joints During Thermomigration
Yu-An Shen, Shiqi Zhou, and Hiroshi Nishikawa – Osaka University; Jiahui Li – City University of Hong Kong; K. N. Tu – University of California, Los Angeles

5. Simulation and Experimental Validations of EM/TM/SM Physical Reliability for Interconnects Utilized in Stretchable and Foldable Electronics
Oscar Chuang, Chang-Chun Lee, and Chia-Ping Hsieh – National Tsing University; Wei-Yuan Cheng and Steve Chiu – Industrial Technology Research Institute

6. A Complex Integrated Circuit Structure Transformation, Modeling and Simulation Method
Daixing Wang, Yufeng Jin, and Wei Wang – Peking University

7. A Study on the Oxygen Plasma Treatment on the Peel Adhesion Strength and Solder Wettability of SnBi58 Based Anisotropic Conductive Films
Shuye Zhang, Tiesong Lin, and Peng He – Harbin Institute of Technology; Mingliang Huang and Yang Wu – Dalian University of Technology; Ming Yang – Hisilicon Optoelectronics Co., Ltd.; Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

8. Numerical Analysis of the Influence of Polymeric Materials on a MEMS Package Performance Under Humidity and Temperature Loads
Mahesh Yalagach, Peter Filipp Fuchs, and Mario Gschwandl – Polymer Competence Center Leoben GmbH; Archim Wolfberger and Coen Tak Coen Tak – ams AG; Thomas Antretter and Michael Feuchter – University of Leoben; Tao Qi – AT&S

9. Electromigration-Induced β-Sn Grain Rotation in Lead-Free Flip Chip Solder Bumps
Mingliang Huang, Jiameng Kuang, and Hongyu Sun – Dalian University of Technology

10. Low-Cost MT-Ferrule-Compatible Optical Connector for Co-Packaged Optics Using Single-Mode Polymer Waveguide
Akihiro Noriki and Takeru Amano – National Institute of Advanced Industrial Science and Technology; Masatoshi Tsunoda and Toshiaki Michihiro – Kyocera Corporation

11. Characterization of Coated Silver Wire Bond Interface Using TEM
Murali Sarangapani, Eric Tan Swee Seng, and Jason Wong Chin Yeung – Heraeus Holding GmbH

12. Research on Applied Reliability of BGA Solder Balls in Extreme Marine Environment
Liyuan Liu, Tao Lu, Daojun Luo, and Hui Xiao – China Electronic Product Reliability and Environmental Testing Research Institute

13. Influence of Single/Double Sweeping Modes and Sweeping Voltage Increment/Polarity on Measurement of TSV Leakage Current
Qinghua Zeng, Jing Chen, and Yufeng Jin – Peking University

14. Improving the Solder Wettability via Atmospheric Plasma Technology
Sagung Kencana, Yee-Wen Yen, and Yu-Lin Kuo – National Taiwan University of Science and Technology; Wallace Chuang and Eckart Schellkes – Robert Bosch Taiwan Co., Ltd.

15. Orthogonal Quilt Packaging 3D Integration for High Energy Particle Detectors
Jason Kulick, Tian Lu, Carlos Ortega, Gary Bernstein, and Edit Varga – Indiana Integrated Circuits, LLC; Christopher Kenney and Julie Segal – SLAC National Accelerator Laboratory

Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. in Exhibit Hall - Belmont 1 & 5

16. Carbonized Electrodes for Electrochemical Sensing
Mohammad Aminul Haque and Nicole McFarlane – The University of Tennessee, Knoxville; Nickolay V. Lavrik and Dale Hensley – Oak Ridge National Laboratory

17. Moldability Challenges Associated With the Assembly of Thicker IC Packages for High Voltage and Power Applications
Sadia Naseem, Jack Chiang, Megan Chang, Bob Lee, and Jason Chien – Texas Instruments, Inc.

18. Highly Compact, Multiband Composite-Right/Left-Handed (CRLH) Transmission Line Based Stub for GPS Applications
Hae-In Kim, Seahee Hwangbo, Renuka Bowrothu, and Yong-Kyu Yoon – University of Florida

Thursday, May 30, 2019

Session 40: Interactive Presentations 4
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Room: Belmont Commons
Session Co-Chairs:
Mark Eblen
Kyocera International SC
Jeffrey Lee
iST-Integrated Service Technology Inc.

1. Die Thickness Optimization for Preventing Electro-Thermal Fails Induced by Solder Voids in Power Devices
Dario Vitello, Andrea Albertinetti, and Marco Rovitto – STMicroelectronics

2. 3-T (8-T) Decoupling Capacitors for Improved PDN in LPDDR4/4X/5 System
Sunil Gupta – Qualcomm Technologies, Inc.

3. Improved Correlation Between Accelerated Board Level Reliability (BLR) Testing and Customer BLR Results Using a Hybrid Closed-Form/Finite Element Methodology
Maxim Serebreni, Natalie Hernandez, Gil Sharon, Nathan Blattau, and Craig Hillman – DfR Solutions; Ken Symonds – Western Digital Corporation

4. Fabrication and Reliability Demonstration of 3 µm Diameter Photo Vias at 15 µm Pitch in Thin Photosensitive Dielectric Dry Film for 2.5 D Glass Interposer Applications
Daichi Okamoto, Yoko Shibasaki, Daisuke Shibata, and Tadahiko Hanada – Taiyo Ink Mfg. Co., Ltd.; Fuhan Liu, Mohanalingam Kathaperumal, and Rao R Tummala – Georgia Institute of Technology

5. Pre-Cure Modification of Electrically Conductive Adhesive for Low Temperature Interconnection
Jinto George and David Danovitch – University de Sherbrooke; Alexandre Leblanc and Eric Savage – IBM Corporation; Michael Ayukawa and Dexter Macaisa – Redlen Technologies

6. RDL-1st Fan-Out Panel Level Packaging (FOPLP) for Heterogeneous and Economical Packaging
Vasarla Nagendra Sekhar, Vempati Srinivasa Rao, F.X. Che, Ser Choong Chong, and Kazunori Yamamoto – Institute of Microelectronics A*STAR

7. Epoxy Composites with Surface Modified Silicon Carbide Filler for High-Temperature Molding Compounds
Fan Wu, Nicholas C Mitchell, Bo Song, Kyoung-Sik Moon, and C.P. Wong – Georgia Institute of Technology

8. Ultra Low Resistivity and High Electrical Stability Silo-Ag ECAs Produced from Curing Chemistry Optimization for Flexible Electronics
Xueqiao Wang, Kyoung-Sik Moon, Bo Song, and C.P. Wong – Georgia Institute of Technology

9. Physics of Failure Based Simulation and Experimental Testing of Quad Flat No-Lead Package
Jia-Shen Lan and Mei-Ling Wu – National Sun Yat-Sen University

10. An Assessment of Electromigration in 2.5D Packaging
Jiefeng Xu, Huayan Wang, Jing Wang, VanLai Pham, Stephen R. Cain, and S.B. Park – Binghamton University; Scott McCann and Gamal Refai-Ahmed – Xilinx, Inc.

11. Diffusion Enhanced Drive Sub 100 ˚C Wafer Level Fine-Pitch Cu-Cu Thermocompression Bonding for 3D IC Integration
Asisa Kumar Panigrahy, Satish Bonam, Tamal Ghosh, Siva Rama Krishna Vanjari, and Shiv Govind Singh – Indian Institute of Technology, Hyderabad

12. Development of Sheet Type Molding Compounds for Panel-Level Package
Kenichi Ueno, Kazuhiro Dohi, Yui Suzuki, Masakazu Hirose, and Akira Nakao – Sanyu Rec Co., Ltd.

13. Defect Detection for the TSV Transmission Channel Using Machine Learning Approach
Huan Liu, Runiu Fang, Yufeng Jin, and Yang Yang – Peking University; Min Miao – Beijing Information Science & Technology University

14. Direct Printing of Heat Sinks, Cases and Power Connectors on Insulated Substrate Using Selective Laser Melting Techniques
Rabih Khazaka, Donatien Martineau, Toni Youssef, Thanh Long Le, and Stephane Azzopardi – Safran

15. Server CPU Package Design Using PoINT Architecture
Arun Chandrasekhar, Vijaya Boddu, Erich Chuh, Krishna Bharath, Farzaneh Yahyaei-Moayyed, Srikrishnan Venkataraman, Sriram Srinivasan, Ram Viswanath, Ritesh Jain, and Huthasana Kalyanam – Intel Corporation

16. Highly Reliable Die Attach Silver Joint with Pressure-Less Sintering Process
Sihai Chen, Christine LaBarbera, and Ning-Cheng Lee – Indium Corporation; William Shambach and Jordan Palmer – Rochester Institute of Technology; Xuanyi Ding – Cornell University

17. 3D Power Packaged Device Thermo-Mechanical Modeling and Stress Analysis after Reliability Trials
Lucrezia Guarino – STMicroelectronics; Lucia Zullino, Luca Cecchetto, Fiorella Pozzobon, and Antonio Andreini

18. Direct Bonding of Low-Temperature Heterogeneous Dielectrics
Serena Iacovo, Lan Peng, Alain Phommahaxay, Fumihiro Inoue, Patrick Verdonck, Soon-Wook Kim, Erik Sleeckx, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC

19. Millimeter Wave Dual Polarization Design Using Frequency Selective Surface (FSS) for 5G Base-Station Applications
Lih-Tyng Hwang, Chung-Yi Hsu, and Chi-Hau Yang – National Sun Yat-Sen University

Friday, May 31, 2019

Session 41: Student Interactive Presentations
8:30 AM - 10:30 AM
Room: Belmont Commons
Session Co-Chairs:
Kristina Young-Fisher
GLOBALFOUNDRIES
Ibrahim Guven
Virginia Commonwealth University

1. Room-Temperature Wire Bonding with Pd Coated Cu Wire on Al Pads: Ball Bond Optimization with 2-Stage Methodology
Nicholas Kam, Michael Hook, and Michael Mayer – University of Waterloo; Celal Con and Karim Karim – KA Imaging Inc.

2. On-Chip ESD Monitor
Kannan Kalappurakal Thankappan, Boris Vaisband, and Subramanian S. Iyer – University of California, Los Angeles

3. Preparation and Characterization of Electroplated Cu/Graphene Composite
Xin Wang, Qian Wang, Jian Cai, Changming Song, and Yang Hu – Tsinghua University; Yang Zhao and Yu Pei – University of Science and Technology of China

4. Quantifying the Impact of RF Probing Variability on TRL Calibration for LTCC Substrates
Ömer Faruk Yildiz, David Dahl, and Christian Schuster – Hamburg University of Technology

5. Effects of NCF and UBM Materials on Electromigration Reliabilities of Sn-Ag Microbumps for Advanced 3D Packaging
Kirak Son, Gahui Kim, Hyodong Ryu, Young-Cheon Kim, Jeong Sam Han, and Young-Bae Park – Andong National University; Gyu-Tae Park – Amkor Technology, Inc.; Ho-Young Son and Nam-Seog Kim – SK hynix Inc.; Cheol-Woong Yang – Sungkyunkwan University

6. Ag Diffusion Control Through Sn on a Sequential Plating-Based Bumping Process
Abderrahim El Amrani, Etienne Paradis, David Danovitch, and Dominique Drouin – Université de Sherbrooke

7. Mechanical Reliability Assessment of Cu6Sn5 Intermetallic Compound and Multilayer Structures in Cu/Sn Interconnects for 3D IC Applications
Jui-Yang Wu and C. Robert Kao – National Taiwan University; Jenn-Ming Yang – University of California, Los Angeles

8. A Study on the Anchoring Polymer Layer (APL) Anisotropic Conductive Films (ACFs) with Self-Exposed Surface of Conductive Particles for Ultra-Fine Pitch Chip-on-Glass (COG) Applications
Dal-Jin Yoon and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. for Thursday in Exhibit Hall - Belmont 1 & 5 and Friday in Mont-Royal Commons

Interactive Presentations: Friday, May 31, 8:30 a.m. - 10:30 a.m.

9. Bending Properties of Fine Pitch Flexible CIF (Chip-in-Flex) Packages Using APL (Anchoring Polymer Layer) ACFs (Anisotropic Conductive Films)
Ji-Hye Kim, Dal-Jin Yoon, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

10. Effects of the Curing Properties and Viscosities of Non-Conductive Films (NCFs) on Sn-Ag Flip Chip Solder Bump Joint Morphology and Reliability
HanMin Lee, SeYong Lee, SangMyung Shin, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; TaeJin Choi and SooIn Park – Doosan Corporation Electro-Materials BG

11. Experimental Investigations on Vertical Ultrasonic Assisted Low Temperature Sintering Process
Henning Seefisch and Jens Twiefel – Leibniz University Hanover

12. Pressureless Transient Liquid Phase Sintering Bonding of Sn-58Bi with Ni Particles for High-Temperature Packaging Applications
Kyung Deuk Min, Kwang-Ho Jung, Choong-Jae Lee, and Seung-Boo Jung – Sungkyunkwan University

13. Epoxy/Triazine Copolymer Resin System for High Temperature Encapsulant Applications
Jiaxiong Li, Chao Ren, Kyoung-Sik Moon, and CP Wong – Georgia Institute of Technology

14. Low-Temperature Ag-Ag Direct Bonding Technology for Advanced Chip-Package Interconnection
Jiaqi Wu and Chin C. Lee – University of California, Irvine

15. Reliability of Micro-Alloyed SnAgCu Based Solder Interconnections for Various Harsh Applications
Sinan Su, Francy Akkara, Anto Raj, Seth Gordon, Sharath Sridhar, Sivasubramanian Thirugnanasambandam, Sa'd Hamasha, Jeffery Suhling, and John Evans – Auburn University; Cong Zhao – Apple Inc.

16. A Novel Approach of Copper-Ceramic-Joints Manufactured by Selective Laser Melting
Thomas Stoll and Matthias Kirstein – Institute for Factory Automation and Production Systems; Joerg Franke

17. Automatic Transient Thermal Impedance Tester for Quality Inspection of Soldered and Sintered Power Electronic Devices on Panel and Tile Level
Maximilian Schmid, Sri Krishna Bhogaraju, and Gordon Elger – Technical University of Applied Research

18. Time 0 Void Evolution and Effect on Electromigration
Jiefeng Xu, Van Lai Pham, Huayan Wang, Stephen R. Cain, and S.B. Park – Binghamton University; Scott McCann, Ho Hyung Lee, and Gamal Refai-Ahmed – Xilinx, Inc.

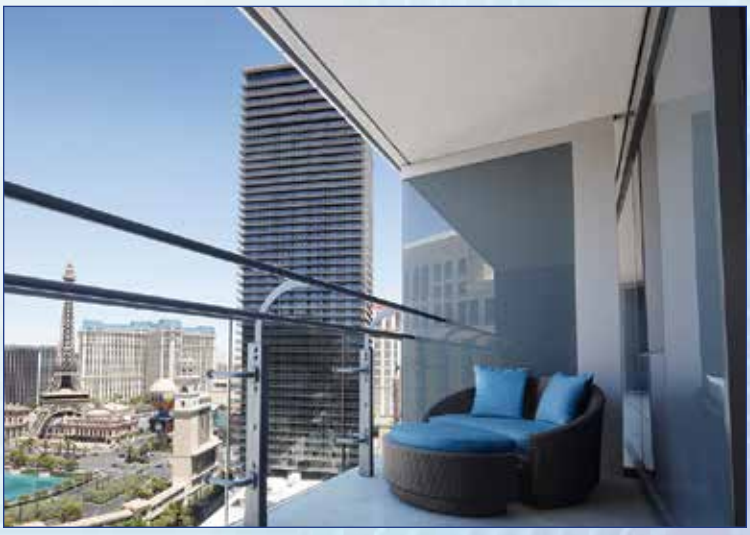
19. Quintuple Band lamda/4 Stub by Using Unbalanced Bridged CRLH Transmission Lines
Renuka Bowrothu, Seahee Hwangbo, Yong-Kyu Yoon, and Haein Kim – University of Florida

20. Product Level Design Optimization for 2.5D Package Pad Cratering Reliability during Drop Impact
Huayan Wang, Jing Wang, Jiefeng Xu, Vanlai Pham, Ke Pan, and Seungbae Park – Binghamton University; Hohyung Lee and Gamal Refai-Ahmed – Xilinx, Inc.

21. Microstructure of Pb-Free Solder Joints by Reflow and Thermo-Compression Bonding (TCB) Process
Jinho Hah, Yongja Kim, Patxi Fernandez-Zelaia, Sangil Lee, Shreyes Melkote, Kyoung-Sik Moon, and Ching-Ping Wong – Georgia Institute of Technology; Leroy Christie – ASM Pacific Assembly Products, Inc.; Paul Houston – Engent Inc.

22. Reduction of Ag Corrosion Rate During Decapsulation of Ag Wire Bond Packages
Jinho Hah, Kyoung Sik (Jack) Moon, and C. P. Wong – Georgia Institute of Technology; Yong Ja Kim – Samsung Electronics Company, Ltd.

Friday Refreshment Break: 9:15 a.m. - 10:00 a.m. in Mont-Royal Commons



Technology Corner Exhibits

Wednesday, May 29

9:00 a.m. - 12:00 Noon / 1:30 p.m. - 6:30 p.m.

Thursday, May 30

9:00 a.m. - 12:00 Noon / 1:30 p.m. - 4:00 p.m.

Belmont 1 & 5

Interactive Presentation Sessions

Wednesday, May 29

Session 37: 9:00 a.m. - 11:00 a.m. / Session 38: 2:00 p.m. - 4:00 p.m.

Thursday, May 30

Session 39: 9:00 a.m. - 11:00 a.m. / Session 40: 2:00 p.m. - 4:00 p.m.

Friday, May 31

Session 41: 8:30 a.m. - 10:30 a.m.

Belmont Commons

TECHNOLOGY CORNER EXHIBITORS

Booth 323
3D Systems Packaging Research Center (PRC)
Georgia Institute of Technology
813 Ferst Drive, NW
Atlanta, GA 30332-0560
Phone: +1-404-894-9097
Fax: +1-404-894-3842
www.prc.gatech.edu
Email: gtprc@prc.gatech.edu

The 3D Systems Packaging Research Center (PRC) at the Georgia Institute of Technology is a Center dedicated to leading-edge research, education of highly-interdisciplinary students and global industry collaborations in the System-on-a-Package (SOP) vision to enable highly miniaturized, mega-functional systems in a single package. The PRC's research encompasses advanced 3D systems packaging technologies including: electrical, mechanical and thermal design; ultra-thin and ultra-high-density glass interposers and packages; ultrafine pitch chip-level and board-level interconnections; passive and active components and integration into power, RF, photonic and analog modules. The PRC model for industry collaboration is enabled by a world-class team of cross-disciplinary academic and research faculty, students, visiting industry engineers, and supply-chain manufacturers. The current industry consortium at PRC consists of the most comprehensive industry ecosystem of material and tool suppliers, substrate and assembly manufacturers, and end users in a wide variety of consumer and high-performance applications including high performance cloud computing and networking.

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North Andover, MA 01845
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Contact: Vern Stygar
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Alpha Novatech, Inc.
473 Sapena Ct. #12
Santa Clara, CA 95054
Phone: +1-408-567-8082
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Phone: +81-3-6699-3991
www.asahi-kasei.co.jp/asahi/en/
Contact: Reiko Mishima
Email: mishima.rb@om.asahi-kasei.co.jp
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Sunnyvale, CA 94085
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ASM Pacific Technology
7850 South Hardy Drive, Suite 110
Tempe, AZ 85284
Phone: +1-602-437-4892
Cell: +1-480-560-0020
www.asmpacific.com
Contact: Terence DeCoteau
Email: Terence.decoteau@asmpt.com
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Contact: Daniel Schmidt
Email: Daniel.schmidt@atotech.com
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Binghamton, NY 13902-6000
Phone: +1-607-777-7270
Contact: Steve Czarnecki
Email: czar@binghamton.edu
The S3IP is a research and development organization that addresses research challenges in electronics packaging system design, process development, prototyping, and manufacturing for academia and the microelectronics industry. Located at Binghamton University, the Center brings together partners from government, industry and academia, providing opportunities for collaborations that will advance microelectronics research and development, with particular focus on electronics packaging design and manufacturing technology; thermal analysis and management for electronics; characterization of materials, surfaces, and physical interfaces for electronics devices and assemblies; and failure analysis and reliability improvement for electronics. Subject areas addressed include packaging of microelectronics, 2.5D/3D chip assemblies, power electronics, and integrated photonics.

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17 Rue des Martyrs
38054 Grenoble Cedex 9, France
Phone: +33633661323
www.leti.fr/en
Contact: Severine Cheramy
Email: severine.cheramy@cea.fr
CEA-LETI is an institute providing R&D and Prototyping services in the field of Micro and Nanotechnologies. Capabilities include 8" and 12" wafer process flows for advanced CMOS, 3D stacking, MEMS and Silicon Photonics. Based in Grenoble, France, CEA-LETI has offices in the US and Japan. Over the past ten years CEA-LETI has developed a wide range of expertise in the fields of silicon interposers and high density interconnects to address the needs of the semiconductor industry in market segments such as mobile telephones and low power computing. Leti is working on hybrid bonding, wafer-to-wafer or chip-to wafer integration. Pitch of few microns is envisioned, without underfill, room temperature and ambient pressure bonding. Self-alignment using capillary force is also developed for high precision, high throughput chip-to-wafer bonding. With the support of its internal IC design teams LETI provides industrial partners with a unique environment for validating new concepts through models, new design tools, test vehicles and implementing fully functional demonstrators such as wide I/O memory standard, 60 GHz RF SOCs for video data transfer or photonic interposers. Recently CEA-LETI has developed CoolCube, an original technique for stacking transistors sequentially in the same process flow for 3D-VLSI. The technology is designed to allow a connection of the stacked active layers on a nanometric scale, with a very high density, due to their alignment by a standard lithographic process. CEA-LETI is embedded in a dynamic and international ecosystem that include European and Global leaders.

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38000 Grenoble, France
Phone: +33-476-57-46-17
Fax: +33-476-47-38-14
www.mycmp.fr
Contact: Dr. Ajith-Sivadasan Moreau
Email: ajith-sivadasan.moreau@mycmp.fr
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One Riverfront Plaza
Corning, NY 14831
Phone: +1-607-974-5331
www.Corning.com
Contact: Zach Barney
Email: barneyz@corning.com
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Fax: +1-508-222-0220
www.alsic.com
Contact: Cheryl Oliveira
Email: coliveira@alsic.com
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Richardson, TX 75081
Phone: +1-972-664-1568
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7855 S. River Parkway, Suite 111
Tempe, AZ 85284
Phone: +1-480-345-9895
www.decatechnologies.com
Contact: Garry Pycroft
Email: garry.pycroft@decatechnologies.com

Deca Technologies is an electronic interconnect solutions provider that offers fan-in and fan-out wafer level chip scale packaging (WLCSP) services to the semiconductor industry. Our portfolio of proprietary, game-changing electronic interconnect solutions delivers leadership capabilities in performance, cost and technology allied to a flexible manufacturing process that enables 200mm and 300mm wafers to be managed simultaneously. Deca's process significantly reduces cycle time and permits multiple design iterations with minimal investment, thereby enabling the adoption of wafer level interconnect technologies for a wide array of semiconductor device types. Deca's FOWLP (M-Series) is rapidly gaining traction within the market courtesy of its superior reliability plus adaptive patterning capability which compensates for die shift and enables finer design rules.

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DISCO Hi-Tec America, Inc.
3270 Scott Blvd.
Santa Clara, CA 95054-3011
Phone: +1-408-987-3776
Fax: +1-408-987-3785
www.discousa.com
Contact: Aris Bernales
Email: aris_b@discousa.com

For 50 years, DISCO Hi-Tec America, Inc. has been a leader in the semiconductor industry in cutting (Kiru), grinding (Kezuru), and polishing (Migaku) technologies. DISCO's focus has expanded beyond mechanical dicing to include laser and plasma singulation. DISCO continues to be the leader in wafer thinning and polishing/stress relief with technologies such as SDBG enabling thinning of die to 20um or less. To support the increasing complexity in today's packages, DISCO has also released equipment capable of laser via drilling in non-silicon transparent materials, silicon carbide ingot slicing (KABRA), and laser lift off. In order to support research and development efforts, joint development initiatives, and next generation product prototyping, DISCO Hi-Tec America's KKM Services lab in Santa Clara offers capability to process materials with our latest advanced cutting, grinding, and polishing technologies.

Booth 422
DuPont Electronics & Imaging
455 Forest Street
Marlborough, MA 01752
Phone: +1-508-481-5970
www.dupont.com/electronic-materials
Contact: Mark Markowski
Phone: +1-774-641-4969
Email: markowski@dow.com

With the 2017 merger of Dow and DuPont, Dow Electronic Materials and DuPont Electronics & Communications have combined their portfolios and expertise to create the new DuPont Electronics & Imaging business, which is part of the new Specialty Products Division of DowDuPont (future DuPont). DuPont Electronics & Imaging is a global supplier of materials and technologies serving the semiconductor, advanced chip packaging, circuit board, electronic and industrial finishing, photovoltaic, display, and digital and flexographic printing industries. DuPont E&I's portfolio includes metallization, dielectric, lithography and assembly materials designed to meet the most demanding needs for advanced semiconductor packaging applications, such as bumping, copper pillars and redistribution layer (RDL), passivation, underbump metallization (UBM), thermal interface and lid seal adhesion used for the latest fan-out wafer level packaging (FOWLP), flip chip, system in package (SiP), and 2.5D/3D chip packages.

Booth 123
EMD Performance Materials
A business of Merck, KGaA
Darmstadt, Germany
70 Meister Avenue
Somerville, NJ 08876
Phone: +1-908-429-3578
Fax: +1-908-429-3637
www.emdgroup.com
Contact: Shaun Bennett
Email: Shaun.Bennett@emdgroup.com

EMD Performance Materials is a business of Merck KGaA, Darmstadt, Germany. Our Semiconductor Solutions business unit accelerates the semiconductor industry to develop electronic devices that are smarter, faster, more powerful & energy efficient for a more connected world. We provide highly innovative material-based solutions for the semiconductor manufacturing supply chain. From wafer fabrication towards the final stage, packaging – we are a single channel partner for the production of integrated circuits. Focusing on packaging only, we e.g. offer a variety of Thick Film Resists (TFR) from conventional DNQ & chemically amplified (CA) positive tone to photo polymerizing negative tone which are used to make patterned conductive circuitry in semiconductor packages. In addition we deliver high reliability and environmentally friendly interconnect materials to enable powerful semiconductors that are fully lead-free and ROHS compliant. When great minds get together, they inspire each other. We are proud to partner with ECTC again in 2019 to further accelerate innovation in Semiconductors.

Booth 321
Evatec NA inc.
780 Carillon Parkway, Suite 150
St Petersburg, Florida, 33716
Phone: +1-727-201-4313
Fax: +1-727-201-4605
www.evatecnet.com
Contact: Allan Jaunzens
Email: allan.jaunzens@evatecnet.com

From 5G networks and the new micro LED display technology to EMI shielding for our smart phones, our thin film deposition systems enable manufacture of the worlds highest performance semiconductor, optoelectronic and optical devices. Evatec Advanced Process Control technologies enables new levels of production yields for the most challenging thin film performance specifications in Advanced Packaging, Power Devices, MEMS, Wireless Communication , Optoelectronics and Photonics. Within Advanced Packaging our solutions on HEXAGON and CLUSTERLINE deliver high yield UBM / RDL production with stable low Rc values at up to 56 wafers per hour in FOWLP. Combining our latest batch degas, etch and deposition technologies achieves the even lower Rc values of <1mOhm needed for contacts and interconnects for next generation power management in IOT applications. For FOPLP applications our PNL cluster tools offer high throughput production up to 25 panels per hour on panel sizes of 500mm for low CoO.

Booth 409
EV Group, Inc.
7700 South River Parkway
Tempe, AZ 85284
Phone: +1-480-305-2400
Fax: +1-480-305-2401
www.evgroup.com
Email: SalesNorthAmerica@EVGroup.com

EV Group (EVG) is a leading supplier of equipment and process solutions for the manufacture of semiconductors, microelectromechanical systems (MEMS), compound semiconductors, power devices, and nanotechnology devices. Key products include wafer bonding, thin-wafer processing, lithography/nanoimprint lithography (NIL) and metrology equipment, as well as photoresist coaters, cleaners and inspection systems. Founded in 1980, EV Group services and supports an elaborate network of global customers and partners all over the world.

Booth 315
ficonTEC
25 Calle Canela
San Clemente, CA 92673
Phone: +1-949-388-5800,
+1-949-300-7715
Fax: +1-949-388-1489
www.ficontec.com
Contact: Soon Jang
Email: soon.jang@ficontec.com
ficonTEC provides a wide range of micron- and submicron-precision T&M, vision inspection, and assembly automation systems for opto-electronic, fiber-optic/array and micro-optics components, among others. Such automation systems for applications include submicron-precision LDB/die bonding, LDB stacking-unstacking, micro-lens assembly (e.g., FAC, SAC, mirror, etc.), OE component attachment, and integrated photonic device assembly. ficonTEC is also the recognized industry leader in SiPh device test, inspection, and assembly automation systems for various product development and production requirements. Our systems are designed for high-yield and -throughput, -precision semi- and full-automation production environment. ficonTEC's system platforms are pre-engineered for specific applications, where each platform for given application can be optimized for the unique needs of each customer, resulting in a competitive technical advantage. ficonTEC assists its customers with their 'lab-to-fab' activities through collaborative product/process development activities, leveraging our extensive experiences for customers' rapid time-to-market needs. Please discuss ficonTEC's capabilities for your application(s) at our booth.

Booth 213
Finetech
560 E. Germann Rd., Suite 103
Gilbert, AZ 85297
Phone: +1-480-893-1630
www.finetechusa.com
Contact: Robert Avila
Email: sales@finetechusa.com
Finetech supplies sub-micron accuracy die bonders for die attach, advanced packaging and micro assembly applications. Manual, motorized and automated models provide a prototype to production pathway. High process flexibility within one platform allows a wide range of bonding technologies: thermo-compression, ultrasonic, eutectic, epoxy, sintering, ACF/ACP, Indium and precision vacuum die bonding. Applications areas cover optical packages, sensors, Si photonics, microLEDs, Cu pillar, flip chip, chip-on-glass, chip-on-flex, MCM, MEMs and more. Finetech also provides precision dispensers and advanced rework systems for today's challenging applications. Our deep process knowledge adds value to our equipment – our engineering team works with customers to create effective solutions for specific applications. We understand that "one size" does not necessarily fit all.

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FlipChip International
Division of Huatian Tech. Group
3701 E. University Dr.
Phoenix, AZ 85034
Phone: +1-602-431-6020
www.flipchip.com
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Booth 416
Fraunhofer Center for Applied Microstructure Diagnostics CAM
Heideallee 19
06120 Halle (Saale), Germany
Phone: +49-345-55-89-130
Fax: +49-345-55-89-101
www.cam.fraunhofer.de
Contact: Prof. Dr. Matthias Petzold
Email: matthias.petzold@imws.fraunhofer.de
Fraunhofer IMWS-CAM is a leading service provider of failure diagnostics and material assessment for industry including semiconductor technologies, microelectronic components, microsystems and nanostructured materials. We consider the entire work flow from non-destructive defect localization over high precision target preparation to cutting edge nanoanalytics supplemented by micro-mechanical testing, finite element modeling and numerical simulation. Our goal is to support cooperation partners in introducing innovative materials and technologies, improving manufacturing process steps, securing reliable field use of components, analyzing field returns, and consequently optimizing manufacturing yield, product quality, reliability, and cost efficiency. In addition, we are collaborating with suppliers of microstructure diagnostics and material testing equipment in developing innovative failure analysis methods and instrumentation, problem-adapted work flows for quality and reliability control, and new industry-compatible applications for future markets.

Booth 418
Fraunhofer Institute for Reliability and Microintegration IZM
Gustav-Meyer-Allee 25
13355 Berlin, Germany
Phone: +49-30-46403-100
Fax: +49-30-46403-111
www.izm.fraunhofer.de
Contact: Georg Weigelt
Email: georg.weigelt@izm.fraunhofer.de
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FUJIFILM Electronic Materials
80 Circuit Dr.
North Kingstown, RI 02852
Phone: 800-553-6546
www.fujifilmusa.com
Contact: Sanjay Malik
Email: sanjay_malik@fujifilm.com
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250 Cheesequake Road
Parlin, NJ 08859
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www.hdmicrosystems.com
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14000 Jamboree Rd.
Irvine, CA 91626
Phone: +1-949-344-6688
Fax: +1-714-368-2265
www.henkel-adhesives.com/us/en/
Contact: Eva Laus
Email: electronics@henkel.com
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24 Union Hill Rd
Conshohocken, PA 19428
Phone: +1-610-825-6050
www.heraeus-electronics.com
Contact: James Wertin
Email: james.wertin@heraeus.com
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Hitachi Chemical Co., Ltd.
1-9-2, Marunouchi, Chiyoda-ku,
Tokyo 100-6606 Japan
Phone: +81-3-5533-7000
Fax: +81-3-5533-7077
www.hitachi-chem.co.jp
Contact: Tsuyoshi Ogawa
Email: ts-ogawa@hitachi-chem.co.jp
Hitachi Chemical is a leading company in providing various materials used in advanced semiconductor assembly packages, such as FO-WLP/PLP, 2.5 & 3D packages, SiP etc. In addition to those materials, Hitachi Chemical provides "Open Laboratory" located in Japan where any customers can utilize advanced fabrication and analytical equipment to achieve an accelerated development for complex and advanced structures. The Open Laboratory will relocate to more convenient location, closer to Tokyo, in Q4 2018. Our sales offices are located around the world, with technical engineers stationed to support customers in case of need. Please contact us if you are interested in "Open Laboratory" and materials such as die bonding films, molding related materials (EMC of solid, fine granular, liquid and film, and release film), underfill (CUF and NCF), temporary adhesives, photo-sensitive dielectric, dry film resist, solder resist, organic laminates (including low Dk/Df dielectric) and much more.

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i3 Electronics
100 Eldredge St.
Binghamton, NY 13901
Phone: +1-607-238-7077
www.i3electronics.com
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IBM Canada Ltd.
23 Airport Blvd
Bromont, Quebec, Canada J2L 1A3
Phone: +1-450-534-6496
Cell: +1-450-531-2474
www.ibm.com/assembly
Contact: Luc Comtois
Email: assembly@ca.ibm.com
At IBM Assembly and Test facility in Bromont, we have asserted our proposition in several key areas providing solutions for high current and high thermal dissipation applications in computing electronics market and developing specialized areas with attractive know- how in RF, Antennas, SiP and advanced opto electronic packaging for communication and wireless markets. Beyond our technical orientation, our experienced engineering team takes pride in using its design, assembly and test expertise to provide tailor-made solutions for our client's needs and bring forth designs, prototypes and fast manufacturing ramp ups that are key to our client's success. Several fruitful collaborations have been enacted in the past months and we already have received feedback that it provides high value to the customers that have chosen us as their development and manufacturing OSAT solution. Clients also see value in our supply chain management proposition. Clearly beyond the customer-supplier relationship, we value true partnerships for mutual growth. We have an exciting 2019 roadmap, some of the highlights include deploying high density interconnect laminates, pursuing integration and optimization of SiP packages and also deploying technical milestones to prepare for dense optical integration which is highly anticipated by several key players of the communications market in the years ahead.

Booth 527
Integrated Service Technology (iST)
2381 Zanker Road Suite 120
San Jose, CA 95131
Phone: +1-408-627-5749
www.istgroup.com
Contact: Edward Lee
Email: USSales@istgroup.com
Founded in 1994 in Taiwan, iST began its business from IC circuit debugging and modification and gradually expanded its scope of operations, including Failure Analysis, Reliability Verification, Material Analysis, Automotive Electronic Verification Platforms and Signal Integrity Testing Services. iST has offered full-scope verification and analysis services to the IC engineering industry, its customers cover the whole spectrum of the electronics industry from IC design to end products. In response to iST's mission of providing integrated solutions to customers, iST not only focuses on its core laboratory services but also enters the mass production services

Booth 511
Interconnect Systems, Inc.
741 Flynn Rd.
Camarillo, CA 93012
Phone: +1-805-482-2870
Fax: +1-805-482-8470
www.isipkg.com
Contact: Tom Casey
Email: info@isipkg.com
Interconnect Systems International, LLC ("ISI"), specializes in high-density module packaging, advanced interconnect and real time signal processing hardware. ISI offers design, qualification, and testing, coupled with fully integrated in-house manufacturing. ISI's system design capabilities include hardware, firmware and software and high-density PCB design. ISI's additional capabilities include custom manufacturing process development, fine pitch SMT, flip chip, wire bond assembly, IC packaging, custom molding, over molding, and automated optical inspection.

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JCET
46429 Landing Parkway
Fremont, CA 94538
Phone: +1-510-979-8000
Fax: +1-510-979-8001
www.statschippac.com
Contact: Chris Stai
Email: Christopher.Stai@statschippac.com
STATS ChipPAC is a leading outsourcing provider of semiconductor design, wafer bump, packaging and test solutions for well-established market such as communications, consumer and computing as well as emerging markets in automotive electronics, Internet of Things (IoT) and wearable devices. STATS ChipPAC is a member of the JCET group of companies. JCET is one of the top semiconductor packaging and test providers in the world and the largest OSAT provider in China. Headquartered in Jiangyin, China, JCET has an extensive global manufacturing base with operations in China, Singapore and South Korea. The comprehensive packaging portfolio of JCET and its subsidiaries include discrete, leaded, laminate, flip chip, Molded Interconnect System, wafer level packaging and System-in-Package technologies. For more information, visit www.statschippac.com or www.jcetglobal.com.

Booth 519
JFE Shoji
JFE Shoji Bldg., Oremachi 2-Chome
Chiyoda-ku, Tokyo
Japan 100-0004
Contact: Sosuke Kobayashi
Email: sosuke-kobayshi@jfe-shoji-ele.co.jp

Booth 208
JSR Micro, Inc.
1280 N. Mathilda Ave.
Sunnyvale, CA 94089
Phone: +1-408-543-8800
Fax: +1-408-543-8964
www.jsrmicro.com
Email: atseng@jsrmicro.com
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Booth 310
Kyocera America
1401 Route 52, Suite 203
Fishkill, NY 12524
Phone: +1-845-896-0480
Contact: Tony Soldano
Email: tony.soldano@kyocera.com
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15930 S. 48th Street Suite 110
Phoenix, AZ 85048
Phone: +1-480-966-0784
www.lintec-usa.com
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Malico Inc
5, MingLung Road
Yang-Mei Taiwan 32663
Phone: 886-3-4728155
Fax: 886-3-4725979
www.malico.com
Email: inquiry@malico.com
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Mentor, A Siemens Business
8005 SW Boeckman Rd.
Wilsonville, OR 97070
Phone: +1-503-547-3000
www.mentor.com/pcb
Contact: Jennifer Chausse
Email: sales_info@mentor.com
Mentor, A Siemens Business is the worldwide market leader in PCB systems design, advanced IC packaging solutions, and analysis technologies. Recently awarded the 3DInCites "EDA Supplier of the Year" award, Mentor will showcase its Xpedition(R) High Density Advanced Packaging (HDAP) solutions for prototyping, design, and verification of heterogeneous multi-substrate designs such as FO-WLP, 2.5D, and system-in-package. Visit booth #419 to learn more about Mentor's technologies and best practices for IC/Package/Board co-design.

Booth 223
Micross Advanced Interconnect Tech.
3021 E. Cornwallis Rd.
P.O. Box 110283
Research Triangle Park, NC 27709
Phone: +1-919-248-9216
Fax: +1-919-541-1142
www.micross.com
Contact: Alan Huffman
Email: Alan.Huffman@micross.com
Micross is the leading one-source provider of bare die & wafers, advanced interconnect technologies, custom packaging (complete hermetic packaging) and assembly, component modification services (BGA Reballing, Lead Attach, Robotic Solder Dip & Exchange), electrical & environmental testing and hi-rel products. In business for more than 40 years, our comprehensive array of hi-reliability capabilities serve the global aerospace & defense, space, medical and industrial markets. Micross Advanced Interconnect Technology (AIT), one of the premier wafer bumping & wafer level packaging facilities in the U.S., develops and provides leading edge interconnect and 3D integration technologies to customers worldwide. Our ITAR-registered facility supports wafer sizes up to 200mm and the flexibility to tailor unique solutions for your most demanding requirements. Micross possesses the sourcing, packaging, assembly, test, and logistics expertise needed to support an application throughout its entire program cycle. For more information, please visit www.micross.com.

Booth 211
Mini-Systems, Inc. (MSI)
20 David Rd.
North Attleboro, MA 02760
Phone: +1-508-695-0203
Fax: +1-508-695-6076
www.mini-systemsinc.com
Contact: Craig Tourgee
Email: ctourgee@minisystemsinc.com
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Mitsui Chemicals America
61 Metro Drive
San Jose, CA 95110
Phone: +1-408-487-2888
www.mc-tohcello.co.jp/english/
Contact: Jeff Wishes
Email: j.wishes@mitsuichem.com

ICROS™ Tape" is a brand of tape designed for the semiconductor and electronic components manufacturing process flow, such as backgrinding (BG), dicing, molding, debonding, sawing, reflow, metal lift off, protection for etching, CMOS image sensor handling, protection for back-metalizing, and etc. ICROS™ Tape has been the world's top protective tape used in semiconductor wafer BG for decades. Today, we now offer tapes used for many other processes in the semiconductor and electronic components manufacturing flow. ICROS™ Tape is continuously evolving to keep up with the latest and future technologies in the semiconductor process, such as TSV wafer BG and dicing, fan-out WLP, PLP and many other processes. We optimize the entire production processes of our protective tapes from concept to raw material design to tape design to final inspection to meet the strict requirements of semiconductor market. Everything takes place within state-of-the-art clean room production facility with strict quality controls in place every step of the way. The result is ICROS™ Tape, for many applications, ultraclean tape with superior TTV (total thickness variation).

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Nagase America Corporation
2880 Lakeside Drive, Suite 320
Santa Clara, CA 95054
Phone: +1-408-567-9728
Fax: +1-408-567-9729
www.nagasechemtex.co.jp/en/
Contact: Ippei Yamai
Email: ippei.yamai@nagase-nam.com

Nagase ChemteX is a leading company for semiconductor encapsulant of epoxy resin, especially Liquid Molding Compound (LMC) for FOWLP, 2.5D, 3D, SiP, Non-Conductive Paste (NCP) for Fine pitch FC-PKG, Underfill for Pb-free. Engineered Materials Systems, Inc. technology focus on electronic materials and negative photoresist for semiconductor, circuit assembly, photovoltaic, printer head, camera module, disk drive, printed electronics and photonics assembly product lines. These Nagase Group companies create continual improvements guiding its customers into the future.

Booth 205
NAMICS Technologies, Inc.
2055 Gateway Place, Suite 480
San Jose, CA 95110
Phone: +1-408-516-4611
Fax: +1-408-516-4617
www.namics.co.jp/e
Contact: Tony Ruscigno
Email: sales@namics-usa.com

NAMICS is a global technology leader for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components and solar cells with over 70 years of experience and expertise. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea, Hong Kong, and China, NAMICS serves its worldwide customers with enabling products for leading edge applications. We build more than products; we build relationships setting the gold standard for customer service by offering customizing products, world class customer support to provide a solution for your personal application. NAMICS CORPORATION is a leading source for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components and solar cells. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea and China, NAMICS serves its worldwide customers with enabling products for leading edge applications.

Booth: 111
nepes Corporation
9605 Scranton Road, Suite 402
San Diego, CA 92121
Phone: +1-858-429-6703
Cell: +1-669-264-6385
www.nepes.us
Contact: Masayuki Oe
Email: sales@nepes.us

nepes is a leading-edge provider of Wafer Level Packaging, Panel Level Packaging and turnkey assembly solutions including testing and DPS services. Since 2001, nepes has been providing OSAT services in partnership with Fabless and IDM customers worldwide. With ISO/TS 16949, ISO 14001, OHSAS 18001 and AEO certified facilities located in South Korea and China, nepes provides an extensive range of packages: bump, wafer level package (WLP), fan-out wafer level package (FO-WLP), fan-out wafer level System in Package (FOWL-SiP) as well as 2 and 3D modules. Its PLP (Panel Level Package) has revolutionized the mass production of advanced semiconductor packages while providing price competitiveness by utilizing an innovative process and structure based on extensive touch screen panel (TSP) and LCD production experience. nepes is well positioned to support leading semiconductor companies, foundries and electronics IDMs with their advanced packaging requirements.

Booth 218
Neu Dynamics Corp.
110 Steamwhistle Dr.
Ivyland, PA 18974
Phone: +1-215-355-2460
Fax: +1-215-355-7365
www.neudynamics.com
Contact: Don Johnson
Email: sales@neudynamics.com

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Nikon Metrology, Inc.
12701 Grand River Ave.
Brighton, MI 48116
Phone: +1-810-220-4360
Fax: +1-810-220-4300
www.nikonmetrology.com
Email: sales.nm.us@nikon.com

Nikon Metrology, Inc. offers the most complete and innovative metrology product portfolio, with state-of -the-art vision measuring instruments x-ray machines with CT options, and a complete line of 3D metrology options. These reliable and innovative solutions respond to the advanced inspection requirements of manufacturers active in aerospace, electronics, automotive and other industries. To learn more about our innovative products and to view all our product lines please visit our website.

Booth 414
Nitto Inc.
Bayside Business Park
48500 Fremont Blvd.
Fremont, CA 94538
Phone: +1-510-445-5400
Fax: +1-510-445-5480
www.nitto.com
Contact: Yasuko Ferris
Email: yasuko.ferris@nitto.com

Nitto is a global supplier of materials and equipment for semiconductor manufacturing, represented by the following products: ELEP holder tapes for back-grinding and dicing; high temperature resistant masking tape; NEL machines (Taper/Detaper/ Wafer Mounter with or without peeling function/ UV machine) for thin wafer application; ELEPMOUNT (2-in-1:

DAF+Dicing Tape conductive/non-conductive) for thin stacked chip package; REVALPHA thermal-release tape for various applications, such as dicing, grinding and MLCC production process; clear molding compound and sheet encapsulating resin.

Booth 507
Nordson DAGE
2747 Loker Avenue
West Carlsbad, CA 92010
Phone: +1-925-246-1662
www.nordsondage.com
Contact: Aram Kardjian
Email: aram.kardjian@nordsondage.com
Nordson DAGE manufacturers wire pull, ball and die shear test systems along with X-Ray inspection systems that are recognized as the industry standard. The 4800 bondtester brings the latest developments in automated wafer testing technology to users testing wafers from 200mm upwards. When combined with an integrated wafer handling device the 4800-INTEGRA™ can test multiple wafers consecutively. Automation on non-wafer samples can also be conducted on the 4000Plus which performs shear tests up to 200kg, pull tests up to 100kg and push tests up to 50kg. The 4000HS high speed bond tester is used for pull and shear testing of solder spheres to identify brittle fractures at speeds up to 4m/sec in shear and 1.3m/sec pull. Technologies such as TSV, PoP, 2.5D and 3D integration demand a new level of metrology. The XM8000 intelligent X-ray metrology system delivers fully automated, non-destructive, radiation safe defect detection of all complex devices.

Booth 509
Nordson SONOSCAN
2149 East Pratt Blvd.
Elk Grove Village, IL 60007
Phone: +1-847-437-6400
Fax: +1-847-437-1550
www.nordsonsonoscan.com
Contact: Jim Ries
Email: james.ries@nordsonsonoscan.com
Nordson SONSOCAN is a worldwide leader and innovator in Acoustic Micro Imaging (AMI) technology. We manufacture acoustic microscope instruments and automated inspection equipment to nondestructively inspect and analyze products. Our C-SAM® scanning acoustic microscope provides unmatched accuracy and robustness setting the standard in AMI for the inspection of products for hidden internal defects such as poor bonding, delaminations between layers, cracks and voids. In addition, we offer analytical services through regional testing laboratories in Asia, Europe and the U.S. and educational workshops for beginners to advance users on AMI technology.

Booth 417
NTK Technologies, Inc
3979 Freedom Circle Drive, Suite 320
Santa Clara, CA 95054
Phone: +1-408-727-5180
www.ntktech.com
Contact: Mariel Stoops
Email: mstoops@ntktech.com
NTK Technologies is a leader in IC Ceramic Packaging. For nearly half a century, NTK has developed specialized technologies to provide advanced ceramic IC packaging solutions for large and start-up semiconductor companies. NTK's technical centers support design optimization and simulation services through all development and production stages -- prototype, small volume, and volume manufacturing. With global service centers, NTK offers a wide range of packaging materials and design services for MEMS Sensors, CMOS/CCD Image Sensors, Opto, FPGA, CPU, MPU, MCM, RF, LED Substrates, Hi-Rel, Satellite, Automotive and Medical applications. Wafer Probe Substrates utilizing multilayer co-fired ceramic and multilayer thin film available. Optimum package designs for 10G to 400G. As one of the industries' largest packaging manufacturers, NTK's products and services have evolved to match the roadmaps of mainstream and advanced IC packaging applications.

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Lvl 2, 54-42 Dongtanhan
1-gil, Hwaseong-si, Gyeonggi-do, 18423
Republic of Korea
Phone: +82-31-6131147
Fax: +82-31-6131449
www.ntrium.com
Contact: Paul Kang
Email: paul.kang@ntrium.com
We are Nano Alchemists! and EMI/EMC total solution provider. Ntrium is presented with the opportunity to converge Nano-material technology and the Microelectronics packaging technology of Automotive/Semiconductor/Mobile/IT products, to ignite bright minds that solve technical problems customers face, to provide collaborate and innovative solutions. Our product list is as follows.
EMI shielding paste for spraying method / EMI shielding Film / EMI absorber / Conductive Bonding Film for camera module / Thermal Interface Material(TIM) / Conductive Particles for Elastomer Test Socket / Conductive Beads for Anisotropic Conductive Film(ACF) .Do you have the interested with our products or technology? Please visit our booth or contact us.

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PAC TECH USA
328 Martin Ave.
Santa Clara, CA 95050
Phone: +1-408-588-1925 x246
Fax: +1-408-588-1927
www.pactech.com
Contact: Berndt Otto
Email: bernd.otto@pactech.com
Pac Tech - Packaging Technologies GmbH (group member of NAGASE & CO. Ltd.) is headquartered in Germany with wholly owned subsidiaries: PacTech USA Inc. in Silicon Valley, USA, and PacTech ASIA Sdn. Bhd. in Penang, Malaysia. PacTech is comprised of three business units: EQUIPMENT MANUFACTURING: Manual & Automatic ENIG & ENEPIG plating tools, Laser solder jetting equipment, Wafer-level solder ball transfer systems, Laser assisted flip-chip bonders. SUBCONTRACT SERVICES: Flip Chip and Wafer Level Package Bumping Services including ENIG or ENEPIG for UBM (solder bumping) or OPM (wirebond). Other services include Electroplating, Laser Solder Jetting, Wafer Level Solder Balling, Re-passivation, RDL, Backmetal, Wafer Thinning, Wafer Dicing, Tape & Reel, AOI, X-Ray, SEM, FIB. CHEMISTRY: Pre-Treatment and process chemistry for electroless plating.

Booth 408
Palomar Technologies Inc.
2728 Loker Avenue West
Carlsbad, CA 92010
Phone: +1-760-931-3600
Fax: +1-760-931-5191
www.palomartechnologies.com
Email: sales@bonders.com
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Panasonic
1701 Golf Road, Ste 3-1200
Rolling Meadows, IL 60008
Phone: +1-847-637-9600
Fax: +1-847-637-9601
www.panasonicfa.com
Contact: Tae Yi
Email: mikewohlner@us.panasonic.com
Panasonic System Solutions Company of North America – Process Automation (PSSNA-PA) develops and supports innovative manufacturing processes around the core of circuit manufacturing technologies and computer-integrated manufacturing software—thereby, contributing to the growth and prosperity of our customers' businesses regardless of their mix or volume.

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Since the founding of our company in 1918, we at Panasonic have been providing better living for our customers, always making 'people' central to our activities, and thus focusing on 'people's lives'. Going forward from this, and based on our innovative electronics technology, we will continue to provide a wide variety of products, systems and services.

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10050 16th St. N.
St. Petersburg, FL 33716
Phone: +1-727-577-4999
Fax: +1-727-577-7035
www.plasmatherm.com
Email: sales@plasmatherm.com
Plasma-Therm is a U.S. manufacturer of advanced plasma-processing equipment, providing etch, deposition, and plasma dicing technologies used in semiconductor packaging, solid-state lighting, power, data storage, renewable energy, MEMS, nanotechnology, photonics, and wireless communication markets. Plasma-Therm's VERSALINE® platform is the workhorse for a variety of applications in specialty semiconductor markets. The platform's modular design allows flexible configuration of substrate handling and technologies that address the wide range of customer requirements. Plasma-Therm's Singulator® systems bring the precision and speed of plasma dicing to chip-packaging applications. Manufacturers, academic and governmental institutions depend on Plasma-Therm equipment, designed with "lab-to-fab" flexibility to meet the requirements of both R&D and volume production. Plasma-Therm's products have been adopted globally and have earned their reputation for value, reliability, and world-class support.

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Promex Industries Inc.
3075 Oakmead Village Drive
Santa Clara, CA 95051
Phone: +1-408-496-0222
www.promex-ind.com
Contact: Rosie Medina
Email: rmedina@promex-ind.com
Promex delivers innovative IC packaging and heterogeneous assembly solutions for medical, biotech and sensor-based microelectronic devices from its 30,000-sq.ft. Santa Clara, CA facility which includes Class 100/1000 cleanrooms. It features a highly skilled engineering team, broad technical capabilities, advanced packaging, microelectronics assembly expertise, scalable manufacturing capacity and is CA-FDB licensed to manufacture Class 1 & Class 2 medical devices. Onsite services include RoHS-optimized SMT, wafer thinning, dicing, wirebond, flip chip and overmolding. Its Quik-Pak Division (San Diego, CA) offers prototype and preproduction assembly services in as fast as one day; standard cycle times 3-5 days after design validation. 35 QFN design options, 2x2mm to 12x12mm body sizes. Packages include OmPP (Air Cavity/Open-molded Plastic Packages) QFN/SOIC, OcPP (Open Cavity Plastic Packages), custom air cavity and plastic overmolded. Services include wafer processing, wire bonding and flip chip for IC packaging/COB applications. Promex/Quik-Pak facilities are ISO 13485:2016, ISO 9001:2015 and ITAR registered.

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Pure Technologies
177 US Hwy # 1, No. 306
Tequesta, FL 33469 USA
Phone: +1-404-964-3791
Fax: +1-877-738-8263
Int'l Fax: +1-973-273-2132
www.puretechnologies.com
Contact: Jerry Cohn
Email: jerry@puretechnologies.com
Pure Technologies manufactures low (0.02, 0.01 cph/cm2), ultra-low (0.005, 0.002 cph/2) and super ultra-low (<0.001 cph/cm2) alpha emitting Tin (Sn), Lead-Free (including all SAC) alloys, Pb, Pb/Sn , Bi and virtually all alloys for over 23 years. These ALPHALO® products are available in various shapes and sizes – ingots, anodes, slugs, pellets, foil, rods, bricks, PbO and SnO powder, etc. for wafer-level packaging, interconnects, electroplating and sphere and powder/paste manufacturing. ALPHA-LO® reduces/eliminates soft errors from alpha particle emissions from solders, enhances performance reliability and reduces corporate liability. All materials are guaranteed and certified to be at secular equilibrium and are tested and retested over time before shipping insuring that the alpha emission rate is stable and will not increase over time.

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QualiTau
830 Maude Ave.
Mountain View CA, 94043
Phone: +1-650-282-6226
Fax: +1-650-230-9192
www.qualitau.com
Email: sales@qualitau.com
QualiTau offers a variety of reliability test equipment for characterization and development of new materials used in the manufacturing of Integrated Circuits, as well as process monitoring and process qualification. The MIRA, Infinity, ACE, and Multi-Probe reliability test systems perform tests for Hot Carrier Injection (HC), Dielectric Breakdown (TDDB), and electromigration(EM) of interconnects, TSV, Solder Bump (8 amperes max) at test temperatures of up to 450°C. QualiTau's Test Lab service is ideal for both fabless companies and foundries seeking: Reliable, independent evaluation and analysis. "Virtual" capacity during times of under-capacity. Cost-effective means of performing tests on an irregular or infrequent basis. A productive and beneficial way to "test drive" the equipment before committing to a purchase.

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Royce Instruments
480 Technology Way
Napa, CA 94558
Phone: +1-707-255-9078
Fax: +1-707-255-9079
www.royceinstruments.com
Contact: Bill Coney
Email: bconey©royceinstruments.com
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Rudolph Technologies
16 Jonspin Road
Wilmington, MA 01887
Phone: +1-978-253-6200
Fax: +1-978-658-6349
www.rudolphtech.com
Email: info@rudolphtech.com
Rudolph Technologies is a leader in the design, development, manufacture and support of defect inspection, advanced packaging lithography, process control metrology, and data analysis systems and software used by semiconductor device manufacturers worldwide. Rudolph's product suite offers hardware and software solutions for the demanding requirements of the advanced packaging market, including 2D/3D bump inspection, RDL and overlay metrology, and a lithography stepper specifically designed for the back-end. Turn data into useful information with Rudolph's proprietary software solutions including run-to-run control, fault detection and classification and yield management systems.

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Samtec, Inc.
520 Park East Blvd.
New Albany, IN 47150
Phone: +1-812-944-6733
Fax: +1-812-948-5047
www.samtec.com
Contact: Glenn Dixon
Email: glenn.dixon@samtec.com
Known as the worldwide service leader for electronic connectors and cables, Samtec has focused on leading edge high speed products and services for the last two decades. The tremendous success in these areas has driven Samtec to further move into faster and smaller arenas. We now provide full turnkey solutions for your entire signal chain from chips, through substrates, packages, connectors and cables. Samtec can help you design, model, layout, and assemble your products. Samtec continues to focus on our industry-leading FireFly™ mid-board optical/photonic engine design and manufacturing. In addition, Samtec has new capabilities in glass interposers and substrates with low loss electrical characteristics for biomedical, military/aerospace, sensors, connectivity, and industrial applications

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Sanyu Rec Company Ltd.
3-5-1 Doucho, Takatsuki
Osaka 569-8558, Japan
Phone: +81-8-0618-73654
www.sanyu-rec.jp
Contact: Yuki Ishikawa
Email: ishikawa@sanyu-rec.jp
Sanyu Rec Company Ltd. is a Japanese electronics material supplier to the semiconductor market place including LED market. With creative development and numerous proprietary technologies, SANYU REC contributes to these growth fields which are driven by environmental considerations and mobile applications. SANYU REC has provided a variety of products centering on encapsulation materials like liquid MUF materials to the market. CUF materials, die attach materials, and mold sheets are also in our main product lines. Not only these materials but also VPES (vacuum printing equipment) and pressure oven are in our product lines to offer comprehensive solutions to the customers, which distinguishes us from our competitors. SANYU REC is continuing our effort in development of unique and new technologies.

Booth 413
SavansSys
10409 Peonia Court
Austin, TX 78733
Phone: +1-512-402-9943
www.savansys.com
Contact: Amy Palesko
Email: amyl@savansys.com
SavanSys is the industry standard choice for electronics manufacturing cost modeling. The company began in the mid-nineties with a focus on multi-chip module and PCB fabrication and assembly before expanding into electronics packaging. SavanSys provides both cost modeling services and software products and maintains an extensive library of manufacturing activity costs. Projects range from multi-year ventures focused on detailed supply chain modeling to one-time projects comparing a new technology to the current industry standard. All SavanSys projects and products use activity based cost modeling, a bottom-up approach to cost that aggregates individual cost contributors (labor, material, throughput, equipment cost, etc.) for every step in a process flow.

Booth 510
SCHOTT North America, Inc.
400 York Avenue
Duryea, PA 18642, USA
Contact: Dave Vanderpool
Phone: +1-407-288-7695
Fax: +1-407-321-8847
www.us.schott.com
Email: dave.vanderpool@us.schott.com
SCHOTT Advanced Optics is a valuable partner for its customers in developing products and customized solutions for applications in optics, lithography, astronomy, opto-electronics, life sciences, and research. With a product portfolio of more than 120 optical glasses, special materials and components, we master the value chain: from customized glass development to high-precision optical product finishing and metrology. SCHOTT is one of the world's leading suppliers of thin and ultra-thin glass wafers and substrates made of different materials in sizes of between 4" and 12", with various surface qualities and customized features. The use of proprietary production processes, a wide selection of different materials, and continuous expansion of state-of-the-art processing capabilities make SCHOTT's wafer offerings unique in the industry. Process Capabilities include polishing, structuring, edge treatment, ultrasonic washing, and clean room packaging. SCHOTT's portfolio of Thin and Ultra-Thin glasses includes: AF 32® eco, an alkali-free flat glass with a CTE matched to silicon; D 263® eco, a high CTE and high transmission glass; SCHOTT AS 87 eco, a ultra-thin and toughenable glass; B 270®, a crown glass with extremely high CTE; and MEMpax®, an anodic bondable glass with a CTE corresponding to silicon. The portfolio is supplemented by FLEXINITYTM, SCHOTT's glass structuring revolution.

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Senju Comtek
2989 San Ysidro Way
Santa Clara, CA 95051
Phone: +1-408-234-4792
www.senju-m.co.jp/en
Contact: Ayano Kawa
Email: akawa@senju.com
Senju Comtek Corp. is an American Subsidiary of Senju Metal Industry Co. (SMIC) of Tokyo, Japan. Senju is a global leader in solder materials and related processing equipment with over two dozen manufacturing, technical, and sales support facilities located around the world. Our wide array of solder products includes Cu-core balls/columns, micro-spheres, flux for ball-attach and chip-attach, preforms for power electronics, low-temp solders, and high reliability alloys. Senju offers customized solutions for IC technology challenges.

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SET North America
343 Meadow Fox Ln.
Chester, NH 03036
Phone: +1-603-548-7870
Fax: +1-603-887-2000
www.set-na.com
Contact: Matt Phillips
Email: mphillips@set-na.com
SETNA is a Manufacturing and Marketing, Sales and Service Organization centered on our experience and know-how in high-accuracy bonding and the equipment, materials, competencies surrounding it including Surface Preparation with Atmospheric Plasma.
SET Bonders have been the world-standard for applications in which micron precision post bond accuracy is required. For more than twenty years the FC150 Series has been the tool of choice. The FC300 series bonders provide the highest force and bonding accuracy available in the industry, as well as handling substrates up to 300 mm. The Accμra series provide accurate and versatile die bonders for education and R&D. The Ontos7 is the atmospheric plasma system, designed by our sister company OES (Ontos Equipment systems), for and dedicated exclusively to the semiconductor manufacturing and packaging industry. Our patented (and patent pending) equipment and processes provide a unique advantage to our customers to enable low-cost, high yield, high-speed, chip-to-chip interconnect bonds at room temperature with minimal force. Ontos Atmospheric Plasma also improves surface activation for direct bonding, aqueous wetting, contamination removal, adhesive bonding, and more.

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SHENMAO AMERICA, Inc.
2156 Ringwood Ave.
San Jose, CA 95131
Phone: +1-408-943-1755
Cell: +1-408-529-6626
www.shenmao.com
Contact: Hans Schiesser
Email: hschiesser@shenmao.us
SHENMAO America, Inc. is the American Subsidiary of SHENMAO Technology, Inc. of Tao Yuan City 328, Taiwan. Shenmao is a global leader in manufacturing solder materials for over 46 years with ten manufacturing, technical, and sales support facilities located around the world. SHENMAO America, Inc. blends solder paste in San Jose, CA, USA, also supporting a wide range of products for the Semiconductor Packaging and PCB Assembly industries. SHENMAO produces SMT Solder Paste, Laser Soldering Paste, Wave Solder Bar, Solder Wire with/without Flux, Liquid and Paste Flux, Solder Preforms, Semiconductor Packaging Solder Spheres, Wafer Bumping Solder Paste, Dipping Flux, LED Die-Bonding Solder Paste, Plating Anode, and Solar PV Ribbon. 90 % of the largest EMS Companies are valued customers that are continuously using SHENMAO Technology, Inc. Solder Materials with great success. OSAT's, EMS and OEM's qualify/re-qualify our products for many years.

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Shin-Etsu MicroSi, Inc.
10028 S. 51st St.
Phoenix, AZ 85044
Phone: +1-480-893-8898
Fax: +1-480-893-8637
www.microsi.com
Email: info@microsi.com
Shin-Etsu MicroSi, Inc. is a wholly owned subsidiary of Shin-Etsu Chemical Ltd. Shin-Etsu MicroSi is a world class supplier of packaging materials for the semiconductor industry. With a global support network- Sales Engineers, R&D, Manufacturing, Quality Assurance, and Logistics- we are able to quickly develop and provide new technologies to benefit our customers. This allows our clients to meet their ever changing technical, commercial and environmental needs by implementing Shin-Etsu MicroSi's technology. Shin-Etsu MicroSi is known for supplying high performance Thermal Interface Materials, Underfills, Molding Compounds, High Purity Silicone Encapsulants, and Die Attach Materials.

Booth 420
Shinkawa USA, Inc.
1177 S. Porter Court
Gilbert, AZ 85296
Phone: +1-480-831-7988
www.shinkawa.com/en/
Contact: Doug Day
Email: d_day@shinkawausa.com
Shinkawa is a leading supplier of flip chip, die, and wire bonding equipment. The wide range of equipment supports various applications including automotive, server, mobile, and communication devices for the IoT society. For leading edge packaging technology, Shinkawa provides innovative solutions with high-accuracy and ultra-high throughput flip chip bonders for TCB and C2/C4 processes. For die and wire bonding, Shinkawa provides technologies for ultra-thin die pick up for the latest power and memory devices, and unique wire shapes for RF, memory, and many other devices. Our ultimate bonding solutions can automate process selection plus inspection by our 3D technology. Founded in 1959 in Tokyo and with a strong presence today in the semiconductor market, Shinkawa supports a diverse network of global customers.

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Shinko Electric America
1280 East Arques Avenue MS 275
Sunnyvale, CA 94085
Phone: +1-408-838-3336
Fax: +1-408-955-0368
www.shinko.com
Contact: Lorne Johnson
Email: Lorne.johnso@shinko.com
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SPTS Technologies Ltd
Ringland Way, Newport, NP18 2TA
Phone: +0044-1633-414-000
www.orbotech.com/spts
Contact: Wendy Davis
Email: enquiries@spts.com
SPTS Technologies, an Orbotech company, designs, manufactures, sells, and supports advanced etch, PVD, CVD, and MVD® wafer processing equipment and solutions for the global semiconductor and micro-device industries, with focus on the Advanced Packaging, MEMS, high speed RF device, power management and LED markets. SPTS also offers Additive Printing solutions for 3D structural printing of dams and isolating layers for IC packaging and package marking. SPTS has manufacturing facilities in Newport, Wales and Allentown, Pennsylvania, and operates across 19 countries in Europe, North America and Asia-Pacific.

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SUSS MicroTec Inc.
A SÜSS MicroTec AG Company
220 Klug Circle
Corona, CA 92880-5409
Phone: +1-951-817-3700
Fax: +1-951-817-0640
www.suss.com
Contact: info@suss.com
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2675 Antler Drive
Carson City, NV 89701
Phone: +1-619-208-0748
www.taiyo-hd.co.jp/en/
Contact: Yuya Suzuki
Email: YuyaS@taiyo-america.com
TAIYO INK MFG. CO., LTD has more than 90% market share of solder resist products on IC-Packaging industry. TAIYO introduced two new solder resist products to the market: AUS AZ3 and AUS SR3. AZ3 provides highly robust TST crack resistance with high Tg, best for large body FCBGA and high temperature automotive BGA products. SR3 offers quite low CTE (15-20ppm) with high modulus (>10GPa), being ideal for coreless/thin core applications. TAIYO additionally offer a photo-imageable dry film material with high resolution, PVI-3 HR100S. PVI-3 HR100S can be applied as a high-density build-up material for BGA substrates/ interposers, as an insulation material for embedded applications, and as an RDL dielectric for WLP / PLP products. TAIYO also develops magnetic ink materials for next generation packaging. For more details, please visit our booth.

Booth 517
TATSUTA USA Inc.
101 Metro Drive, Suite 355
San Jose, CA 95110
Phone: +1-408-642-1938
Fax: +1-408-982-3391
www.tatsuta.com
Contact: Mike Sakaguchi
Email: m-sakaguchi@tatsuta.com
TATSUTA is leading provider of EMI shielding conductive material for semiconductor industry. TATSUTA provides innovative solutions for conformal and compartment shielding. TATSUTA also provides AIP bonding & printed antenna

paste, wafer backside metallization paste, high reliability metallizing paste for FMV & TGV filling, low temperature curable & solderable paste for circuitry printing, low temperature curable 3D SMT paste, For more details, please visit our booth 517. We will provide solutions for your applications.

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TechSearch International Inc.
4801 Spicewood Springs Rd., Ste 150
Austin, TX 78759
Phone: +1-512-372-8887
Fax: +1-512-372-8889
www.techsearchinc.com
Contact: Jan Vardaman, Andrea Myers
Email: tsi@techsearchinc.com
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Teikoku Taping Systems
5090 N 40th St. Ste. 140
Phoenix, AZ 85018
Phone: +1-602-367-9916
www.teikoku-taping.com
Contact: Robert Garrett
Email: robert.garrett@teikoku-taping.com
Teikoku Taping System specializes in the design, development and manufacture of semiconductor equipment used for taping ("Haru"), de-taping ("Hagasu") and handling ("Hakobu") of wafers and panels. TTS is the leader in Dry Film Resist lamination, as well as the handling of thin wafers for back grind tape lamination, UV irradiation, removal and mounting to dicing tape on film frame. Customer support for demos, process development, field service are all based in our offices in Phoenix, AZ.

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ThreeBond International, Inc.
6184 Schumacher Park Dr.
West Chester, OH 45069
Phone: +1-408-638-7091
Fax: +1-513-779-7375
www.threebond.com
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Email: kkitamura@threebond.com
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Integrated photonic circuits, chips, wafer & panel level; Semiconductor lasers & Novel LEDs; Silicon & III-V photonics; Optical sensors and quantum sensing; Photonic SiP; Optical interconnects, interposers, waveguide and circuit boards technologies; Micro-optical systems; 3D photonics; Free space optical communications; Automotive photonics, LiDAR, 3D-Sensing; Optoelectronic assembly, materials and reliability.

Thermal/Mechanical Simulation & Characterization
Component, board & system level modeling for microelectronics; 3D/2.5D; TSV; Interposer; SiP; WLP; BGA; Embedded actives/passives; Power modules; LEDs; MEMS; Thin wafer/die handling; Wire bonding & assembly processes; Modeling of fracture mechanics, fatigue, electro-migration, warpage, delamination, drop test & material attributes; Novel modeling including multi-scale and multi-physics; Novel characterization methodologies.

Interactive Presentations
Highly encouraged at ECTC, presenter and attendee often communicate more efficiently here than in oral presentations. Abstracts can relate to any electronics packaging topic. Interactive presentation session papers are published and archived in equal merit with the other ECTC papers.

You are invited to submit an abstract of no more than 750 words that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net.

If you have any questions, contact:
Rozalia Beica, 70th ECTC Program Chair
DuPont Corporation
rozalia.beica@dupont.com

Abstracts must be received by October 6, 2019. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number, and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses
In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 16, 2019.

If you have any questions, contact:
Kitty Pearsall
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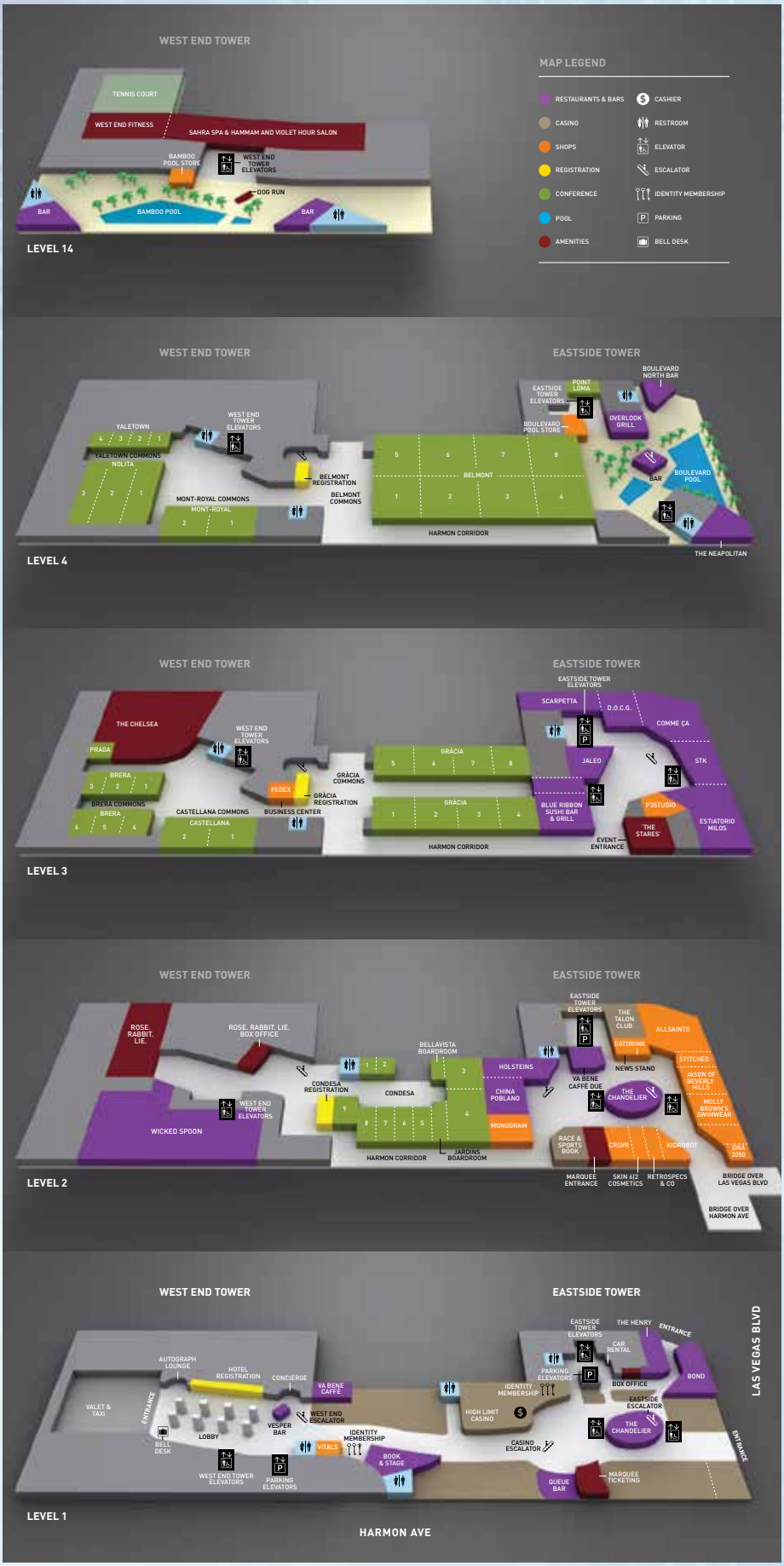

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