Advance Program & Registration

Don't miss out on electronic packaging's premier conference!

ECTC

The 2022 IEEE 72nd Electronic Components and Technology Conference

May 31 - June 3, 2022

Sheraton San Diego Hotel & Marina
San Diego, California, USA

For more information, visit: www.ectc.net

Sponsored by:

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

INTRODUCTION FROM THE IEEE 72ND ECTC PROGRAM CHAIR KARLHEINZ BOCK

The 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC) at The Sheraton San Diego Hotel and Marina, San Diego, California • May 31- June 3, 2022

On behalf of the Program and Executive Committee, it is my pleasure to invite you to IEEE's 72nd Electronic Components and Technology Conference (ECTC), which will be held at The Sheraton San Diego Hotel and Marina, San Diego, California from May 31– June 3, 2022. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses, foundry and OSAT service providers, substrate makers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1700 people have attended ECTC in the previous in-person editions and over 7500 in the virtual events in the last 2 years.

At the 72nd ECTC, around 350+ technical papers are scheduled to be presented in 36 oral sessions and 5 interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as wafer-level and fan-out packaging, 2.5D, 3D and heterogeneous integration, interposers, advanced substrates, assembly, materials modeling, reliability, packaging for harsh conditions, power packaging, interconnections, packaging for high speed and high bandwidth, photonics, flexible and printed electronics. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over twenty countries are expected to present their work at the 72nd ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature 7 special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday 5 special sessions, 90 minutes each, are scheduled.

On Tuesday morning May 31st at 8:30 a.m. Chukwudi Okoro and Benson Chan will chair the session on MicroLED Display Technology: High Volume Manufacturing (HVM) Progress and Challenges, followed by Amr Helmy chairing a special session at 10:30 a.m. with Selected Topics of IEEE EPS Heterointegration Roadmap. On Tuesday afternoon at 1:30 p.m. Jan Vardaman will present a special session on the topic Chiplets to Co-Packaged Optics followed by Kuldip Johal and Bora Baloglu presenting a special session at 3:30 p.m. titled: How will IC Substrate Technology Evolve to Enable Next-Generation Heterogeneous Integration Schemes for High-Performance Applications? As every year on Tuesday afternoon the Young Professionals reception will be organized by Yan Liu and Adeel Bajwa. On Tuesday evening Kitty Pearsall and Chris Rizzo will co-chair the EPS President's ECTC panel session on the topic: State-of-the-Art Heterogeneous Integrated Packaging Program at 7:45 p.m.

This conference will also feature a Diversity and Career focused Panel and Reception jointly organized by ECTC and ITherm on Wednesday, June 1st at 6:30 p.m. This year, panelists will share their perspectives of career opportunities while focusing on some of the specifics of the diverse workforce and inclusion. The panel will be chaired by Kim Yess, Christina Amon and Francoise von Trapp. On the same day at 7:45 p.m., Rozalia Beica and Ed Sperling will present the ECTC General Chair's Plenary Session entitled, Digital Transformation - The Cornerstone of Future Semiconductor and Advanced Packaging Growth. For Thursday, June 2nd at 8:00 p.m. Yasumitsu Orii and Shigenori Aoki will organize the IEEE EPS Seminar which will focus on Interconnect Technologies for Chiplets.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE ITherm Conference, the 72nd ECTC will offer 16 CEU-approved PDCs, organized by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 31st and are taught by distinguished experts in their respective fields. The Technology Corner exhibits will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 72nd ECTC and to be a part of all the exciting technical and professional opportunities. I also want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 72nd ECTC a success. I look forward to meeting you at The Sheraton San Diego Hotel and Marina, San Diego, California, May 31– June 3, 2022.

Karlheinz Bock
72nd ECTC Program Chair
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72nd ECTC ADVANCE REGISTRATION

Advance Registration

Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions see page 32.

Register early … save US$100 or more! All registrations received after May 4, 2022 will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk in the Seascape Foyer.

On-Site Registration Schedule

Registration will be held in the Seascape Foyer on the Lobby Level.

Monday, May 30, 2022	3:00 p.m. – 5:00 p.m.
Tuesday, May 31, 2022	6:45 a.m. – 5:00 p.m.*
**6:45 a.m. – 8:00 a.m.: Morning PDCs & morning ECTC Special Session only*	
Wednesday, June 1, 2022	6:45 a.m. – 4:00 p.m.
Thursday, June 2, 2022	7:30 a.m. – 4:00 p.m.
Friday, June 3, 2022	7:30 a.m. – 12:00 Noon

The above schedule for Tuesday will be rigorously enforced to prevent students from being late for their courses.

General Information

Conference organizers reserve the right to cancel or change the program without prior notice. The Sheraton San Diego Hotel and Marina, as well as the ECTC, are both smoke free environments.

ITherm 2022

This year ITherm is co-located with ECTC! All ITherm sessions and exhibits will take place in the Bay Tower building of the Sheraton San Diego Hotel & Marina. ALL ECTC sessions and exhibits will take place in the Marina Tower building!

Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual's belongings is the individual's responsibility.

ECTC Sponsors

With more than 70 years of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 1,500 individuals and organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Program, and several other sponsorship options that can be customized to your company's interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under "Sponsors."

To sign-up for sponsorship or to get more details, please contact Wolfgang Sauter at wsauter2@gmail.com or +1-802-922-3083.

Hotel Accommodations

Rooms for ECTC attendees have been reserved at the Sheraton San Diego Hotel and Marina. The special conference rate for a single/double occupancy room is:

US $225.00 per night

This price includes single or double occupancy in one room.

Please note these rooms are on a first come, first serve basis. If the conference rate is no longer available, attendees will be offered the next best price available.

Room reservations must be made directly with the hotel by May 4, 2022 to ensure our preferred conference rate. All reservations made after the cutoff date of May 4, 2022 at 5 p.m. Pacific Time will be accepted on a space and rate availability basis. **If you need to cancel a reservation, please do so AT LEAST 5 days before arrival for a full refund.** In the event that you check into the Sheraton San Diego Hotel and Marina and check out prior to your scheduled check out date, you will be charged a US$100 early departure fee. To avoid this fee, you must advise the hotel at or before check-in. Check-in time: 4 p.m. & check-out time: 11 a.m..

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2022 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2022 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. **ECTC's only authorized site** for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that **you personally have used** in the past to book travel. Please be advised, there are scam artists out there and if it's too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: lrenzi@renziandco.com

Transportation Services

Enjoy the free shuttle transportation, which runs every 15 minutes, between the Bay and Marina Towers as well as the San Diego International Airport. Look for the gray, white, and blue vans!

72nd ECTC CONFERENCE OVERVIEW

2022 ECTC Special Session

MicroLED Display Technology: High Volume Manufacturing (HVM) Progress and Challenges

Tuesday, May 31, 2022, 8:30 a.m. – 10:00 a.m.

Chairs: Chukwudi Okoro - Corning Inc., USA and Benson Chan - Binghamton University, USA

Liquid crystal display (LCD) and organic light-emitting diode (OLED) displays are the leading technologies in today's display industry. With continuous interest in performance improvements in areas including higher dynamic range, wider color gamut, lower power consumption, and borderless designs, however, emerging microLED display technology offers several potential advantages. Combinations of these potential advantages apply to applications such as AR/VR, tiled displays, smartwatches, and automotive displays. While progress in these technology areas has been demonstrated at the R&D level, technical challenges exist to transition the emerging microLED technology into industry pilot or manufacturing scales. Some of these challenges include, microLED fabrication, transfer assembly, light management, backplane architecture, device design and integration, and much more.

This panel session aims at addressing the progress and the remaining challenges associated with the commercialization of cost-effective microLED enabled display technology. This will be tackled with the help of a panel of microLED technology experts having diverse areas of expertise.

John Kymissis – Principal Engineer, Lumiode
Eugene Chow – Principal Scientist, Palo Alto Research Center (PARC)
Falcon Liu – Marketing Director, Playnitride
Chris Bower – CTO, XDisplay
Sean Garner – Principal Scientist, Corning Inc
Eric Virey – Senior Market and Technology Analyst, Yole Development

2022 ECTC Special IEEE EPS HIR Session

Selected Topics of IEEE EPS Heterointegration Roadmap

Tuesday, May 31, 2022, 10:30 a.m. – 12:00 p.m.

Chair: Amr Helmy, Professor of U of Toronto

This panel session will focus on the hardware design and packaging approaches that can enable scaling Machine Learning and AI systems in SiP by utilizing heterogeneous integration as a tool to expand the capabilities of SiP. Aspects including system design and architecture, CMOS chip design, hybrid integration methodologies, interconnect approaches will all be discussed in this panel

Seoung Wook Yoon – VP Corporate R&D, Samsung

More speakers to be confirmed soon.

2022 ECTC Special Session

Meeting Next Generation Packaging Challenges: Chiplets to Co-Packaged Optics

Tuesday, May 31, 2022, 1:30 p.m. – 3:00 p.m.

Chair: E. Jan Vardaman, TechSearch International, Inc.

The next generation of advanced packaging will see greater adoption of heterogeneous integration in the form of chiplets as we move into the 3nm semiconductor node. The design, assembly, and test of packages will become more complex, new substrates may be required, and with 3D formats, the move to hybrid bonding is anticipated. Energy requirements in datacenters and performance needs are driving the adoption of co-packaged optics. This panel will discuss changes in the infrastructure required to meet these needs, including the role that the foundry and the OSAT will play. New material requirements will be addressed, the importance of co-design will be highlighted, the need for new thermal solutions will be discussed, and changes in the test approach will be investigated.

Ravi Mahajan – Intel Corporation
Sandeep Razdan – Cisco
Kevin O'Buckley – Marvell Technology
Raja Swaminathan – AMD

More speakers to be confirmed soon.

2022 ECTC Special Session

How Will IC Substrate Technology Evolve to Enable Next Generation Heterogeneous Integration Schemes for High Performance Application?

Tuesday, May 31, 2022, 3:30 p.m. – 5:00 p.m.

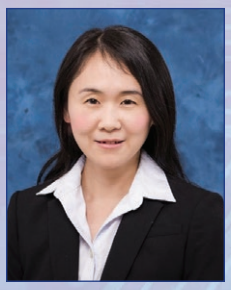
Chairs: Kuldip Johal, Atotech Group and Bora Baloglu, Amkor

The Electronics industry continues to push the limits of silicon and advanced packaging especially for applications in AI and MI that use high performance computing with HBW memory. These types of applications are the key drivers for higher I/O counts and decreasing bump pitch. This increase in I/O density continues to accelerate as silicon process note geometry continues the shrink, enabling more use of silicon interposers, to prevent this gap increasing the IC substrate manufactures also need to follow suit in terms of enabling higher I/O density while maintaining the cost advantage. The objective of this special panels session, is to have range of industry experts from OEM, OSAT, IC substrate manufacturing and material process/ equipment, to discuss how IC substrate technology can evolve to enable shrinkage of features (Line/ space, via/Pad) enabling increase I/O density for next generation high performance applications.

Panelists
OEM: Intel Rahul Manepalli Intel Fellow & Director of Substrate TD Module Engineering.
OSAT: Amkor JinYoung Khim, (Sr. VP Head of R&D)
IC Substrate: Markus Leitgeb R&D Manager AT&S
Materials: Habib Hichri Senior Fellow, Global Applications and Business Development at Ajinomoto Fine-Techno USA Corporation.
Process + Tools: Frank Bruening Global Product Director Mentalization. Atotech

2022 Young Professionals Networking Panel

Tuesday, May 31, 2022, 7:00 p.m. – 7:45 p.m.
Chairs: Yan Liu, Medtronic
and Adeel Bajwa, Kulicke and Soffa



This event is designed just for you – young professionals (including current graduate students). In this active event, we will pair you with senior EPS members and professionals through a series of active and engaging activities. You will have opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

2022 EPS President's Panel

State-of-the-Art Heterogeneous Integrated Packaging Program

Tuesday, May 31, 2022, 7:45 p.m. – 9:15 p.m.

Chairs: Kitty Pearsall, EPS President & Boss Precision, Inc. and Christopher Riso, Booz Allen Hamilton

The EPS President's Panel at this year's ECTC explores the Department of Defense (DoD) State of The Art (SOTA) Heterogeneous Integrated Packaging (SHIP) program. The primary goal of the SHIP program is the development of a sustainable business and operational model for addressing government needs in the Microelectronics (ME) packaging industry. SHIP will leverage the expertise of commercial industry to develop and demonstrate a novel model to ensure sustained DoD access to secure heterogeneous integration, advanced packaging, and test of SOTA advanced packaging and create a catalog of solution components which consist of both die and package components, IP, protocols, tool sets, and design/manufacturability and test methodologies. The session will describe present and future technology implementations for both SHIP Digital and SHIP RF.

Darren Crum, Technical Lead, State-of-the-Art Heterogeneous Integrated Packaging (SHIP) Program – Office of the Undersecretary of Defense for Research and Engineering
John Sotir, SHIP Program Director – Intel Corporation
Ted Jones, Sr. Product Line Director High Performance Solutions Services – Qorvo Inc.

2022 Plenary Session

Digital Transformation – The Cornerstone of Future Semiconductor and Advanced Packaging Growth

Wednesday, June 1, 2022, 7:45 p.m. – 9:15 p.m.

Chair: Rozalia Beica, AT&S

Panel discussions with industry experts and executives across the supply chain, with global participation, to address the impact of digital transformation on our industry, industry dynamics and future trends. Main topics that will be addressed:

- Digital transformation impact on economies and industries
- How are companies preparing for digital transformation in the semiconductor and packaging industry
- Industry trends & applications driving semiconductor adoption and growth of advanced packaging
- The economics of packaging vs. SoCs
- Industry dynamics: business model evolution, investments, supply challenges and disruption

Carolyn Evans – Chief Economist, Intel (US)
Doug Yu – VP Pathfinding and System Integration – TSMC (TW)
Jean Christophe Eloy – CEO Yole Developpement (FR)
Mike Rosa – CMO, SVP Strategy, Onto Innovation (US)
Seoung Wook Yoon – VP Corporate R&D, Samsung (KR)

2022 ECTC/ITherm Diversity and Career Growth Panel and Reception

Solving Diversification Challenges and Workforce Retention Issues

Wednesday, June 1, 2022, 6:30 p.m. – 7:30 p.m.

Chairs: Kim Yess, Brewer Science/ECTC and Christina Amon, University of Toronto/ITherm

Moderator: Francoise von Trapp, 3D InCites

The microelectronics industry is in the midst of a workforce crisis that began long before we heard the word: COVID 19. Companies are desperately seeking new young talent while simultaneously trying to retain the workforce they've worked so hard to build. By 2022, it's well understood that a diverse and inclusive workforce improves innovation, productivity, and the bottom line, yet companies in the microelectronics industry struggle to recruit both women and under-represented minorities to fill thousands of open positions.

In this discussion, we will address these challenges head on with some practical advice from the trenches. Each of our panelists bring real-life experience associated with attracting and retaining a diverse and inclusive workforce, and they are ready to share tips. So come prepared with your questions and leave with actionable items.

Bina Hallman – VP IBM System Client Advocacy and Head of D&I System Business
Antoinette Hamilton – Head of DEI at Lam Research
Najwa Khazal – General Manager, Service Technology Centres Americas, Edwards
KT Moore – VP Corporate Marketing at Cadence

These sessions are open to all conference attendees.

2022 ECTC Luncheon Keynote

Accelerating the Power of Data Infrastructure with Cloud-Optimized Silicon

Wednesday, June 1, 2022

Chris Koopmans
Chief Operations Officer, Marvell Technology

Over the past five years, Marvell Technology has transformed from being a broad, consumer-oriented company to an industry-leading data infrastructure semiconductor solutions provider. Data infrastructure is a large, fast-growing market that powers our global economy and is crucial in advancing our society. This keynote session will discuss why and how Marvell transformed itself to data infrastructure. The presentation will share insights into how data infrastructure is converging into the cloud, the emerging cloud-optimized silicon era and the technology areas the industry must tackle to accelerate the power of data infrastructure with cloud-optimized silicon.

2022 IEEE EPS Seminar

Interconnect Technologies for Chiplets

Thursday, June 2, 2022, 8:00 p.m. – 9:30 p.m.

Chairs: Yasumitzu Orii, Nagase, Japan and Shigenori Aoki, Fujitsu

For 50 years, the number of transistors that could be squeezed onto a piece of silicon had increased on a predictable schedule known as Moore's law. However, the Moore's law is reaching to the end. The new approach comes with "chiplets" which is something like high-tech Lego blocks. Instead of carving new processors from silicon as single chips, semiconductor companies assemble them from multiple smaller pieces of silicon—known as chiplets. We will discuss the several interconnect technologies for Chiplets such as Silicon Bridge, Advanced Interposer, Fan-out wafer-level packaging, and optical interconnection. We will have 6 panelists and each panelist will prepare a short set of slides to present within 10-15 minutes, followed by panel discussion.

Ravi Mahajan – Intel: ***HI Interconnects for today and tomorrow***

Akihiro Horibe – IBM Research Tokyo: ***Direct Bonded Heterogeneous Integration DBHi Si Bridge***

Yu-Hua Chen – Unimicron: ***The Challenges of Advanced Substrate for Heterogeneous Integration***

Shin-Puu Jeng – TSMC: ***Heterogeneous Integration Approaches in Foundry***

Yu-Po Wang – SPIL: ***Trend and Solution for Memory Integrated Advanced Packages***

Hideyuki Nasu – Furukawa Electric: ***High-Density Optical Transceivers and Pluggable Electrical Interfaces for Co-Packaged Optics***

Luncheons

Tuesday PDC Luncheon

All individuals attending a PDC are invited to join us for lunch. Proctors and instructors are welcome, too!

Wednesday Conference Luncheon

Please be sure to attend our Wednesday luncheon with guest speaker Chris Koopmans, Chief Operations Officer from Marvell. All conference attendees are welcome!

Thursday EPS Luncheon

Our sponsor, the IEEE Electronics Packaging Society, will be sponsoring lunch on Thursday for all conference attendees!

Friday Program Chair Luncheon

Please attend Friday's lunch hosted by the 72nd ECTC Program Chair. We will honor conference paper award recipients and raffle off a vast array of prizes including a hotel stay, free conference registrations, and many other attractive items!

General Chair's Speakers Reception

Tuesday, May 31, 2022 • 6:00 p.m. – 7:00 p.m.

(by invitation only)

ECTC Student Reception

Tuesday, May 31, 2022 • 5:00 p.m. – 6:00 p.m.

TEXAS INSTRUMENTS

Hosted by Texas Instruments, Inc.

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them to be successful in their first job search and reach their current positions. You will have the chance to enjoy good food and network with industry leaders and achievers. Don't miss the opportunity to interact with people that you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

Exhibitor Reception

Wednesday, June 1, 2022 • 5:30 p.m. – 6:30 p.m.

72nd ECTC Gala Reception

Thursday, June 2, 2022 • 6:30 p.m.

All badged attendees and their guests are invited to attend a reception hosted by Gala Reception sponsors.

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PROFESSIONAL DEVELOPMENT COURSES

Tuesday, May 31, 2022

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MORNING COURSES
8:00 a.m. – 12:00 Noon

1. ACHIEVING HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIALS CONSIDERATIONS

Course Leader: Ning-Cheng Lee – Independent Consultant

Course Objective:
This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions, and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail. The selection of novel alloys with reduced fragility will be presented. Crucial parameters for high reliability solder alloy for automotive industry will be presented. Electromigration, and tin whisker growth will also be discussed. The emphasis of this course is placed on the understanding of how the numerous factors contribute to the failure modes, and how the selection of proper solder alloys and surface finishes for achieving high reliability are key.

Course Outline:
1. Mainstream Lead-free Soldering Practice
2. Surface Finishes Issues - ENIG, ImAg, ImSn, OSP
3. Mechanical Properties - Shear, Pull, and Creep
4. Intermetallic Compounds - Interaction of Cu and Ni, Cu Content and Additive Effect
5. Failure Modes - Grain Boundary Sliding & Cavitation, Grain Coarsening, Orientation
6. Reliability - Thermal Cycle Effect of Test Condition, Surface Finish & Solder Composition Orientation
7. Reliability - Fragility: Effect of Additive on IMC Growth, Grain Size, IMC Type
8. Reliability - Rigidity & Ductility
9. Reliability - Composite Solder Enable Hierarchy Assembly & Shock Resistance
10. Reliability - Tin Whisker

Who Should Attend:
Directors, managers, design engineers, process engineers, and reliability engineers who want to achieve high reliability lead-free solder joints and would like to know how to achieve it, should take this course.

2. WAFER-LEVEL CHIP-SCALE PACKAGING (WLCSP) FUNDAMENTALS

Course Leader: Patrick Thompson – Texas Instruments, Inc.

Course Objective:
This course will provide an overview of the Wafer Level-Chip Scale Packaging (WLCSP) technology. The market drivers, end applications, benefits, and challenges facing industry-wide adoption will be discussed. Typical WLCSP configurations (bump-on-pad, bump-on-polymer, fan-in, and fan-out) will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other arenas such as RF sensors and MEMS will be reviewed. Future trends covered will include enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra-thin WLCSP, RDL (redistribution layer), stacked WLCSP, MCM in "reconstituted wafers," embedded components, and applications to large format (panel) processing. Since the technology marks the convergence of fabrication, assembly, and test, discussion will address questions on the industrial supply chain such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, outline, reliability, and equipment applicable? What are the challenges for memory? And what about other complex devices such as ASICs and microprocessors?

Course Outline:
1. WLCSP Definition
2. Trends, Categories, Examples, Challenges, Supply Chain
3. Historical Overview, Package Highlights, Assembly Flow
4. Processing and Reliability: Flex, Temperature Cycling, Drop, Electromigration
5. Fan-Out Technologies
6. Embedded Technologies
7. Conclusions

Who Should Attend:
The course will be useful to the following groups of engineers: newcomers to the field who would like to obtain a general overview of WLCSP; R&D practitioners who would like to learn new methods for solving CSP problems; and those considering WLCSP as a potential alternative for their packaging solutions.

3. FUNDAMENTALS OF RF DESIGN AND FABRICATION PROCESSES OF FAN-OUT WAFER/PANEL LEVEL PACKAGES AND INTERPOSERS

Course Leaders: Ivan Ndip and Markus Wöhrmann – Fraunhofer IZM

Course Objective:
Due to the myriad of advantages in system-integration, fan-out wafer/panel level packages (FO WLPs/PLPs) and interposers will play a key role in the development of emerging miniaturized electronic systems. The fabrication processes and RF performance of these advanced packages, especially their multi-layered redistribution layers (RDLs), required for the interconnection of the chips and other system components, will contribute significantly to the cost and performance of the entire system. The objective of this course is to provide and illustrate the fundamentals of the fabrication processes and RF design of FO WLPs/PLPs and interposers, including their multi-layered RDLs.

An overview of distinct types of wafer-level packages, fan-out technologies and interposers as well as the advantages of FO WLPs/PLPs and glass/silicon interposers will first be given. This will be followed by a thorough discussion of the materials and fundamentals of the fabrication processes of FO WLPs/PLPs, multilayered RDLs and glass/silicon interposers. The basics of efficient RF design and measurement of the fundamental building blocks of FO WLPs/PLPs and glass/silicon interposers, considering their multi-layered RDLs, will be given for frequencies right up in the millimeter-wave range. Finally, examples of these advanced packages designed and fabricated at Fraunhofer IZM will be discussed.

Course Outline:
1. Overview of Different Types of Wafer-Level Packages, Fan-Out Technologies, and Interposers
2. Advantages: FO WLPs/PLPs and Silicon/Glass Interposers
3. Materials and Fabrication Processes: FO WLPs/PLPs, Multi-layered RDLs, and Silicon/Glass Interposers
4. Fundamentals of RF Design and Measurement: FO WLPs/PLPs, RDLs, and Silicon/Glass Interposers
5. Comparison of RF Performance of Interconnects in FO WLPs/PLPs and Silicon/Glass Interposers
6. Examples of Advanced Packages Designed and Fabricated at Fraunhofer IZM

Who Should Attend:
Engineers, scientists, researchers, designers, managers, and graduate students interested in the fundamentals of electronic packaging as well as those involved in the process of electrical design, layout, processing, fabrication and/or system-integration of electronic packages should attend.

IMPORTANT NOTICE
It is extremely important to register in advance to prevent delays at door registration. Course sizes are limited.

4. ELIMINATING FAILURE MECHANISMS IN ADVANCED PACKAGES

Course Leader: Darvin Edwards – Edwards Enterprises

Course Objective:

Past and present reliability failure mechanisms that plague semiconductor packages will be explored. Major reliability challenges and failure mechanisms are detailed in critical emerging and high-volume package technologies such as TSVs, FO WLP/FOPLPs, WLCSPs, FC-BGAs, and no lead packages. Topics studied include reliability of TSV-chip interactions, micro bump mechanical reliability, electromigration performance, stress induced ILD damage under bumps and Cu pillars, saw induced ILD damage, solder joint reliability, system level drop reliability, and the impact of aging on reliability performance. For each failure mode, the resultant failure mechanisms and failure analysis techniques required to verify the mechanisms will be summarized. This solutions-focused course concentrates on key process parameters, design techniques and material selections that can eliminate failures and improve reliability, ensuring participants can design-in reliability and design-out failures for quicker time to market. Characterization and implementation of test structures and design guidelines that enable reliable first pass products will be described. A methodology for early detection of chip/package interaction (CPI) reliability risks will be described and encouraged. A methodology for early detection of chip/package interaction (CPI) reliability risks will be described.

Course Outline:

1. Introduction to Package Reliability
2. Failure Modes vs. Failure Mechanisms
3. FC-BGA Package Failure Mechanisms
4. WLCSPs Package Failure Mechanisms
5. Embedded Die & Fan-Out WLP/PLP Failure Mechanisms
6. TSV Failure Mechanisms
7. Materials, Modeling, Design Rules and Reliability
8. Summary

Who Should Attend:

This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms are beneficial. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions.

5. PACKAGING AND HETEROGENEOUS INTEGRATION FOR AUTOMOTIVE ELECTRONICS AND ADVANCED CHARACTERIZATIONS OF EMCS

Course Leader: Przemyslaw Gromala – Robert Bosch GmbH

Course Objective:

Epoxy-based molding compounds (EMCs) are widely used in the semiconductor industry as one of the most important encapsulating materials. For the advanced packaging technologies and heterogeneous integrations, EMCs play a more significant role than for the conventional plastically encapsulated packages because of thin profiles and complex process conditions required for the advanced packaging technologies. In the automotive industry where demand for more advanced packaging technologies increases rapidly for autonomous and connected cars, EMCs are often used to protect not only individual IC components but also entire electronic control units (ECUs), or power modules.

The stress caused by the mismatch of the coefficient of thermal expansion (CTE) between EMCs and adjacent materials is one of the major causes of reliability problems (e.g., excessive warpage, delamination, BRL, etc.). During assembly or even operating conditions, EMCs are subjected to temperatures beyond the glass transition temperature. Around the glass transition temperature, EMCs exhibit significant volumetric and isochoric viscosity, which leads to nonlinear viscoelastic behavior. In contrast, at low temperatures, EMCs show linear viscoelastic behavior. This complex material characteristic in the full temperature range of interest renders the design of electronic devices a nontrivial task. The mechanical behavior of EMCs must be understood clearly to offer predictive simulation strategies, which has become an integral part of the product development process.

This training will address details of such strategies, summarizes the required material characterization procedure, and closes with some representative examples

Course Outline:

1. Introduction
2. Selection of the Material (Preliminary Qualitative Analysis)
3. Material Characterization
   - Curing Shrinkage
   - Coefficient of Thermal Expansion
   - Linear Viscoelastic Properties
   - Viscoelastic Behavior
4. Thermal Aging
5. Summary

Who Should Attend:

Engineers and technical managers who are already involved in the material characterization and modeling, numerical modeling, process engineers and PhD students who need fundamental understanding or broad overview.

6. AVOIDING INELASTIC STRAINS IN SOLDER JOINT INTERCONNECTIONS OF IC PACKAGES

Course Leader: Ephraim Suhir – Portland State University

Course Objective:

This course will address the following three important questions associated with predicting and improving the reliability of solder joint interconnections (SJI) of IC packages:

1. Could inelastic strains in the solder material be avoided by a rational physical design, and if not, could the sizes of the inelastic strain areas be predicted and, if possible, minimized?
2. Considering that the difference between a highly reliable and an insufficiently reliable product is "merely" in the level of their never-zero probability of failure, and that SJIs are usually the most vulnerable structural elements in an IC package design, could this probability be assessed at the design stage?
3. Should temperature cycling accelerated testing for SJIs be replaced with a more physically meaningful, less costly, less time-and-labor-consuming and most importantly, less misleading accelerated test vehicle?

Course Outline:

1. Avoiding Inelastic Strains in Solder Material
   - Physics of Thermal Stress
     a. Stress Strain Diagram
     b. Application of Hooke's Law
     c. Interfacial Stresses
     d. Longitudinal Displacements
     e. Stresses in Bonded Joints
     f. Interfacial Shearing Strain
     g. Interfacial Peeling Stress
     h. Warpage
     i. Size of Peripheral Zones
   - Avoiding Inelastic Strain in Solder Thermal Stresses in Actual BGA/CGA System, Predictable?
   - Expected Stress Relief Due to CGA Design, and/or Inhomogeneous Bond
2. Accelerated Test Types in Electronic Packaging PD*f*R Ten Commandments
3. Low-Temperature/Random Vibration Bias as an Alternative Substitute for Temperature Cycling Accelerated Testing
4. Summary

Who Should Attend:

The course will be useful to package design and reliability engineers that need to understand the distinct types of stresses put on said package, and the impact of each, to the package.

7. FLIP CHIP TECHNOLOGIES

Course Leaders: Shengmin Wen – HaiSemi Inc. and Eric Perfecto – IBM Corporation

Course Objective:

This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various types of wafer bumping technologies, solder joint formation, substrate selection, underfill type and selection, and reliability evaluation. The course is divided into two sections. The first section focuses on the key steps of flip chip assembly technologies and their associated equipment and materials. Plenty of examples are presented to show the versatile flip chip integrations, including single die, monolithic multi-die, multi-level multi-die, as well as multi-form interconnection such as wire bond / flip chip mixed integration. Major flip chip assembly packages are discussed, such as the BGA packages, CSP packages, wafer-level fan-in and fan-out packages, chip-on-chip packages, chip-on-wafer packages, and 2.5D/3D flip chip packages that uses Si or organic

interposers, together with actual industrial leading application cases. In-depth discussions include chip package interaction (CPI), package warpage control, yield detractors for flip-chip assembly, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, and Si die floor plan optimization and its consequence on packaging, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their project's success. The second section dives into the depth of the fundamental aspect of flip chip technology. It will detail the various interconnect technologies used in today's flip chip assembly, i.e., lead-free solder bumping, highly customized Cu-Pillar bumping, intermetallic and Cu-to-Cu joining. It will discuss the various under-bump metallurgy (UBM) fabrication methods (electroplating, electroless plating and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc.

Course Outline:

1. Introduction to Flip Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Substrate Technologies, Underfill, Package Warpage Control, and Yield
5. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
6. Flip Chip Si Package Co-Design and Chip-Package Interaction
7. Flip Chip New Trends: Wafer Level CSP; Wafer Level Fan-Out; and Panel-Level Packaging
8. Bumping Ground Rules
9. Flip Chip Under-Bump Metal and Intermetallic
10. Flip Chip Solder Deposition Processes
11. Cu Pillar Technology
12. Flip Chip Solder Selection and Characterization
13. Flip Chip Electromigration
14. Non-Solder Interconnects
15. Review and Package Selection Exercise

Who Should Attend:

The goal of this course is to provide the students with a list of options to apply to their flip chip assembly applications so that a reliable, innovative, better time to market, and more cost-effective solution can be achieved. Students are encouraged to bring topics and technical issues from their past, present, and future job function for group discussions. A group exercise at the end of the class is planned to serve as a capstone project, making sure that the students can walk away with an in-depth understanding of the technology, and are ready to apply and meet their real-world packaging needs.

8. RELIABLE INTEGRATED THERMAL PACKAGING FOR POWER ELECTRONICS

Course Leader: Patrick McCluskey – University of Maryland

Course Objective:

Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation has resulted in significant improvements in efficiency over previous technologies, but it also has made it essential that the reliability of power electronics be characterized and enhanced. Recently, increased power levels, made possible by new compound semiconductor materials, combined with increased packaging density have led to higher heat densities in power electronic systems, especially inside the switching module, making thermal management more critical to performance and reliability of power electronics. This course will emphasize approaches to integrated thermal packaging that address performance limits and reliability concerns associated with increased power levels and power density. Following a quick review of active heat transfer techniques, along with prognostic health management, this short course will present the latest developments in the materials (e.g., organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS, and systems and the techniques used for their reliability assessment.

Course Outline:

1. Motivation for Integrated Thermal Packaging for Reliable Power Electronic Systems
2. Simulation and Assessment of Active Thermal Management Techniques: Air; Single Phase Liquid, Two Phase, Heat Pipes, and Thermoelectric
3. Application of Thermal Management Techniques to Commercial Power Systems
4. Durability Assessment: Failure Modeling, Simulation, Testing, and Health Monitoring
5. Reliability and Thermal Packaging of Active Devices: Si, SiC, GaN, and Interconnects
6. Reliability and Thermal Packaging of Switching Modules, Including Organic Encapsulants
7. Reliability in Rigid Assembly Packaging: PCBs; Solders; and Glass Interposers
8. Flexible Materials, Packaging, and Thermal Management: Flex Circuit and OLED, Wearables
9. Reliability of Additive Manufactured and Embedded Power Electronics

Who Should Attend:

This course is intended for practicing engineers, designers, and technical managers who work with high heat flux electronics or power electronics and want to learn more about the design, manufacturing, thermal management, and reliability of these power electronic systems.

AFTERNOON COURSES
1:15 p.m. – 5:15 p.m.

9. ADDITIVE FLEXIBLE HYBRID ELECTRONICS – MANUFACTURING AND RELIABILITY

Course Leader: Pradeep Lall – Auburn University

Course Description:

In this course, manufacture, design, assembly, and accelerated testing of additively printed flexible hybrid electronics for applications in some of the emerging areas will be covered. Manufacturing processes for additive-fabrication of flexible hybrid electronics will be discussed. Flexible hybrid electronics opens the possibilities for the development of stretchable, bendable, foldable form-factors in electronics applications, which have not been possible with the use of rigid electronics technologies. Flexible electronics may be subjected to strain magnitudes about 50-150 percent during normal operation. The integration processes and semiconductor packaging architectures for flexible hybrid electronics may differ immensely in comparison with those used for rigid electronics. The manufacture of thin electronic architectures requires the integration of thin-chips, flexible encapsulation, compliant interconnects, and stretchable inks for metallization traces. Several additive manufacturing processes for the fabrication and assembly flexible hybrid electronics have become tractable. Processes for handling, pick-and-place operations of thin silicon and compliant interposers through interconnection processes such as reflow requires an understanding of the deformation and warpage processes for development of robust process parameters which will allow for acceptable levels of yields in high-volume manufacture. Modeling of operational stresses in flexible electronics requires the material behavior under loads including constant exposure to human body temperature, saliva, sweat, ambient temperature, humidity, dust, wear, and abrasion. The strains imposed on flexible stretchable electronics may far exceed those experienced in rigid electronics requiring the consideration of finite-strain formulation in development of predictive models. The failure mechanisms, failure modes, acceleration factors in flexible electronics under operational loads of stretch, bend, fold, and loads resulting from human body proximity are significantly different than rigid electronics. The testing, qualification, and quality assurance protocols to meaningfully inform manufacturing processes and ensure reliability and survivability under exposure to sustained harsh environmental operating conditions, may differ in flexible electronics as well. Several product areas for the application of flexible electronics are tractable in the near-term including Internet-of-Things (IoT), medical wearable electronics, textile woven electronics, robotics, communications, asset monitoring and automotive electronics.

Course Outline:

1. Additive Technologies in Flexible Electronics
2. Aerosol-Jet Printing
3. Ink-Jet Printing
4. Screen-Printing and Gravure Printing

5. Laser-Direct Sintering
6. In-Mold Labeling
7. Ultra-Thin Chips
8. Die-Attach Materials for Flexible Semiconductor Packaging
9. Flexible Encapsulation Materials
10. Compliant Interconnects
11. Dielectric Materials for Large-Area Flexible Electronics
12. Stretchable Inks for Printed Traces
13. Flexible Power Sources
14. Accelerated Testing Protocols

Who Should Attend:
The targeted audience includes scientists, engineers and managers considering the use of additively printed flexible electronics or considering moving from rigid electronics to flexible electronics, as well as reliability, product or applications engineers who need a deeper understanding of additively printed flexible electronics: the advantages; limitations; and failure mechanisms.

10. FROM WAFER TO PANEL LEVEL PACKAGING

Course Leaders: Tanja Braun and Markus Wöhrmann – Fraunhofer IZM

Course Objective:
Panel Level Packaging (PLP) is one of the latest trends in microelectronics packaging. Technology developments towards heterogeneous integration including multiple die packaging, passive component integration in package and redistribution layer or package-on-package also approach larger substrate formats. These are targeted in this course. Manufacturing is currently done on wafer levels up to 12"/300 mm and 330 mm, respectively. For higher productivity and therewith lower costs, larger form factors are introduced. Instead of following the wafer level roadmaps to 450 mm, PLP might be the next big step. PLP could adapt processes, materials, and equipment from other technology areas. Printed Circuit Board (PCB), Liquid Crystal Display (LCD) or solar equipment is manufactured on panel sizes and offer new approaches also for PLP. However, an easy upscaling of technology when moving from wafer to panel level is not possible. Materials, equipment, and processes must be further developed or at least adapted. This course will give a status of the current Fan-in and Fan-out Wafer Level Packaging as well as Panel Level Packaging including Fan-out Panel Level Packaging substrate embedding approaches. This will include materials discussion, technologies, applications, and market trends as well as cost modeling

Course Outline:
1. Introduction to Advanced Packaging
2. Trends in Wafer Level Packaging
3. Fan-In and Fan-Out Wafer Level: Material; Processes; and Applications
4. Introduction and Definition of Panel Level Packaging.
5. Fan-out Panel Level Packaging: Technologies, Challenges and Opportunities
6. Substrate Embedding Technologies

Who Should Attend:
Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer Level Packaging and the transition to Panel Level Packaging should attend. Engineers and managers are welcome as detailed technology descriptions, market trends, applications, and cost modeling are presented.

11. FAN-OUT WAFER/PANEL-LEVEL PACKAGING AND CHIPLET DESIGN AND HETEROGENEOUS INTEGRATION PACKAGING

Course Leader: John Lau – Unimicron

Course Objective:
Fan-out wafer/panel-level packaging has been getting lots of traction since TSMC used their integrated fan-out to package the application processor chipset for the iPhone 7. In this lecture, the following topics will be presented and discussed. Emphasis is placed on the fundamentals and latest developments of these areas in the past few years. Their future trends will also be explored. Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with different sizes and functions, and from different fabless design houses, foundries, wafer sizes, and feature sizes into a system or subsystem on a common package substrate. These chips can be any kind of device and do not have to be chiplets. On the other hand, for chiplets, they must use heterogeneous integration to package them. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented.

Course Outline:
1. Formation of FOWLP: (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First)
2. Fabrication of Redistribution Layers (RDLs): (a) Polymer and ECD Cu + Etching, (b) PECVD and Cu Damascene + CMP, (c) Hybrid RDLs, and (d) Laser drill + LDI + PCB Cu-plating + Etching
3. Formation of FOPLP: (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First)
4. InFO: (a) InFO-PoP, and (b) InFO AiP Driven by 5G mm Wave
5. Samsung PLP: (a) PoP for Smart Watches and (b) SiP SbS for Smartphones
6. Warpages: (a) Warpage Types and (b) Allowable of Warpages
7. Reliability of FOWLP and FOPLP: (a) Thermal-Cycling Test, (b) Thermal-Cycling Simulations, (c) Drop Test, and (d) Drop Simulations
8. Examples: (a) Chip-First Panel-Level Fan-Out Packaging of Mini-LED for RGB-Display, (b) Chip-Last Panel-Level Fan-Out Packaging of Application Processor Chipset, (c) 2.3D IC Integration with Chip-First Fan-Out RDL-Interposers, and (d) 2.3D IC
9. Chiplet Design and HI Packaging vs. System-on-Chip (SoC)
10. Advantages and Disadvantages of Chiplet Design and HI Packaging
11. Examples: (a) AMD Chiplet Design and HI Packaging (EPYZ and RYZEN), (b) Intel Chiplet Design and HI Packaging (FOVEROS, FOVEROS Direct, and Ponte Vecchio), (c) TSMC Chiplet Design and HI Packaging (SoIC + CoWoS and SoIC + InFO PoP)
12. Chiplets Lateral Interconnects (Bridges): (a) Intel's EMIB, (b) IBM's DBHi, (c) Applied Materials' Bridge Embedded in Fan-Out EMC, (d) SPIL's FO EB, (e) TSMC's LSI, (f) ASE's sFOCoS, (g) IME's EFI, and (h) Amkor's S-Connect Fan-Out Interposer
13. Chiplet Design and HI Packaging on Organic Substrates: many examples: (a) Leti, (b) IME, (c) HKUST, (d) ITRI, (e) Xilinx/TSMC, (f) Altera/TSMC, (g) NVidia/TSMC, (h) AMD/UMC, (i) AMD's Active Interposer, (j) Intel's FOVEROS, (k) TSMC's SoIC, and (l) Samsung's X-Cube
14. Assembly Technologies for Chiplet Design and HI Packaging: (a) SMT, (b) Solder Bump Flip Chip, (c) CoW, (d) WoW, (e) TCB, and (f) Bumpless Cu-Cu Hybrid Bonding
15. Integration with Chip-Last Fan-Out RDL-Interposers
16. Chiplet Design and HI Packaging vs. System-on-Chip (SoC)
17. Advantages and Disadvantages of Chiplet Design and HI Packaging examples: (a) Leti, (b) IME, (c) HKUST, (d) ITRI, (e) Xilinx/TSMC, (f) Altera/TSMC, (g) NVidia/TSMC, (h) AMD/UMC, (i) AMD's Active Interposer, (j) Intel's FOVEROS, (k) TSMC's SoIC, and (l) Samsung's X-Cube
18. Chiplet Design and HI Packaging on Fan-Out RDL Substrate for High Performance Applications: many examples: (a) STATSChipPac's FOFC-eWLB, (b) ASE's FOCoS (Chip-First), (c) MediaTek's FO RDLs, (d) TSMC's InFO_oS and InFO_MS, (e) Samsung's Si-Less RDL Interposer, (f) TSMC's RDL-Interposer, (g) ASE's FOCoS (Chip-Last), (h) Shinko's Organic RDL-Interposer, and (i) Unimicron Hybrid Substrate

Who Should Attend:
If you (students, engineers, and managers) are involved with any aspect of the electronics, LED, MEMS, and optoelectronic industry, you should attend this course. It is equally suited for R&D professionals and scientists. Every attendee will receive more than 250 pages of handouts.

12. RELIABILITY ENGINEERING TESTING METHODOLOGY AND STATISTICAL KNOWLEDGE FOR QUALIFICATIONS OF CONSUMER AND AUTOMOTIVE ELECTRONIC COMPONENTS

Course Leader: Fen Chen – GM Cruise

Course Objective:
Consumer electronics industry and today's fast-growing automotive industry continue to demand ever-higher product hardware reliability. This tutorial will provide an overview of reliability

testing methodology and statistical knowledge for qualifications of consumer and automotive electronic components. The reliability testing management including various Rel testing methods and its application to product development at different phases will be first introduced. Some important statistic/probabilistic concepts including uncertainty, confidence level, and how to minimize/deal with them will be discussed. An effective approach to mitigate a low sample size and short test duration will be introduced. Then the tutorial will focus on physics of failure-based acceleration life models for some common reliability testing failures. A deep dive discussion on the temperature cycling model considering dT acceleration, dwell time acceleration, ramp rate acceleration, and Tmax acceleration will be explored. Next, a typical methodology to develop a PoF based Rel validation testing plan reference to product field mission profile will be introduced. The mission profiles of conventional vehicles and consumer smartphones will be compared. How to develop a customized mission profile for AV specifically per its deployment location will be described. Finally, some examples of hardware failure modes with their risk assessments and lifetime modeling will be presented.

Course Outline:

1. Reliability Engineering Product Qualification Methodology (Strategic Planning)
2. Reliability Engineering General Introduction
3. Knowledge-Based and Standard-Based Rel Qualification Approach
4. DfR, Rel R&R, Various Rel Testing Methods and Their Applications During Product Development
5. Reliability Engineering Basic Knowledge of Probabilities and Statistics
6. Rel Testing Uncertainty and How to Minimize & Deal with It
7. Common Rel Engineering Statistical Concepts, Methods, and Usages
8. Reliability Engineering Acceleration Lifetime Modeling Overview (Physics of Failure)
9. Various Life Acceleration Models for Consumer Products and Automotive Components Rel Failures
10. Reliability Test Plan Development Based on Mission Profile Overview (Standards, Knowledge and Experience)
11. Customized Mission Profile Development
12. GMW3172 Based Rel Validation Plan for Automotive Electronic Components
13. A Company Specific Rel Validation Plan for Smartphone
14. Failure Modes and Lifetime Prediction Case Studies
15. Time-Dependent Parametric Shift Modeling of LEDs
16. LCD Display Dark Spot Failure Mode Deep Dive
17. AV Liquid Cooling Compute System Cold Plate Buckling Failure During High Temperature Degradation
18. Automotive Roof Module Component 2D Stress-Strength Failure Rate Determination for Vastly Distributed

Who Should Attend:

Engineers and tech managers already involved in the consumer product and automotive product fields, and those who need fundamental understanding or broad overview of product reliability qualification.

13. INTRODUCTION OF TWO-PHASE COOLING OF HIGH-POWER ELECTRONICS

Course Leader: John R. Thome – JJ Cooling Innovation

Course Description:

Flow boiling heat transfer in microchannels can reliably cool heat fluxes more than 500 W/cm2 with heat transfer coefficients nearing 100'000 W/m2K with respect to the cold plate's base area. As an example, an air-cooled thermosyphon for a 2U server can cool CPU's up to 750W, presented at **ITherm 2021**. Presently, an introduction to two-phase cooling of electronics covering pumped-driven, gravity-driven (loop thermosyphons) and self-driven (pulsating heat pipes) will be presented. Whilst industry is now accepting flow boiling technology as an option for cooling in data centers, telecommunications, and power electronics in automotive, aerospace, etc., many thermal specialists are not yet familiar with flow boiling and condensation. Compared to an air-cooled heat sink, air-cooled passive two-phase cooling units reduce energy consumption and noise by the fans. Furthermore, in a thermosyphon or a pulsating heat pipe, the working fluid needs no electrical driver or flow controller, and thus provides high reliability with no moving parts or wiring. This lecture will present an introduction into microchannel flow boiling, condensation and the "workings" of two-phase cooling together with several case studies for illustrative purposes. At the end of this course, you will better understand the ins-and-outs of a two-phase cooled system, which improves the reliability, reduces first cost and operating cost, and increases longevity of cooling devices compared to air-cooling.

Course Outline:

1. Two-Phase Thermodynamics (Vapor Pressure Curve and P-v Diagram)
2. Two-Phase Flow Patterns in Microchannels (Describe Flow Patterns and Show Photos)
3. Flow Boiling in Microchannels (Depict some flow boiling test results)
4. Condensation in Microchannels (Depict Some Test Results)
5. Multi-Microchannel Evaporator Cold Plates (Describe Cold Plates and Some Test Results)
6. Introduction to Pumped-Loop Cooling Systems (Describe Some Systems)
7. Introduction to Loop Thermosyphons (Working Principles and Example System)
8. Introduction to Pulsation Heat Pipes (Working Principles and Example System)
9. Selection of Working Fluid (Discuss Pros/Cons of Selection of Fluids)

Who Should Attend:

This class is intended for senior undergraduates, graduate students and engineers working in the field of thermal management.

IMPORTANT NOTICE

It is extremely important to register in advance to prevent delays at door registration. Course sizes are limited.

14. MULTI-PHYSICS MODELING AND SIMULATION IN ELECTRONIC PACKAGING THEORY, IMPLEMENTATION AND BEST PRACTICES

Course Leader: Xuejun Fan – Lamar University

Course Objective:

This course aims to present a comprehensive coverage of multi-physics modeling and simulation for mechanics related reliability issues under various loading conditions. In addition to the introduction of fundamentals, the course contents are arranged in four modules. Module 1 covers modeling under thermal loading, such as first level failure (TSV/bump/dielectric), warpage, and temperature cycling. Module 2 deals with the modeling under mechanical loading, such as drop impact. Module 3 will cover modeling under humidity/moisture loading for moisture related problems, such as failures in soldering reflow as well as under HAST. Module 4 will focus on electromigration modeling that involves with electrical, thermal, mechanical and diffusion modeling. Theoretical foundation, modeling implementation, and the best practices for simulation will be covered. Emerging trend and future perspective in reliability mechanics and modeling will be discussed.

Course Outline:

1. Introduction to Mechanics Related Failures in Electronic Packaging
2. Reliability Issues and Modeling Under Thermal Loading
3. Reliability Issues and Modeling Under Mechanical Loading
4. Reliability Issues and Modeling Under Moisture/Humidity Loading
5. Reliability Issues and Electromigration Modeling

Who Should Attend:

This course is intended for technical managers and staff members, reliability engineers, scientific researchers, and graduate students who participate in thermal/mechanical modeling, package design, material selection, qualification and reliability assessment of chip-package interaction, package, and package/board interaction.

15. POLYMERS IN WAFER LEVEL PACKAGING

Course Leader: Jeffrey Gotro – InnoCentrix, LLC

Course Objective:

The course will provide an overview of polymers and the important structure-property-process-performance relationships for polymers used in wafer level packaging. The main learning objectives will be: 1) understand the types of polymers used in wafer level packages, including underfills (pre-applied and wafer applied), mold compounds, and substrate materials, 2) gain insights on how polymers are used in Fan-Out Wafer Level Packaging, specifically mold

compounds and polymer redistribution layers (RDL), 3) learn the key polymer and processes challenges in Fan-Out Wafer Level and Fan-Out Panel Level Packaging.

Course Outline:

1. Overview of Polymers Used in Wafer Level Packaging
2. Wafer Level Process Flows (Chip First Versus Chip Last (RDL First))
3. Epoxy Mold Compounds for eWLP, Chemistry, Formulation, Processing
4. Photosensitive Polyimides and Polybenzoxazoles for RDL, Chemistry and Processingg
5. Polymer Challenges in Fan-Out Wafer Level Packaging
6. Wafer Versus Panel Processing; Polymer Challenges and Solutions
7. Reliability Testing for Fan-Out Wafer Level Packaging
8. Pre-Applied Underfills and Wafer Level Underfills, Chemistry and Process
9. High Density Substrate Materials Including Coreless Substrates

Who Should Attend:

Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used in electronic packaging will also find this course valuable.

16. THERMAL MANAGEMENT OF ELECTRONICS

Course Leader: Jaime Sanchez – Intel Corporation

Course Objective:

This course provides the fundamentals of heat transfer applied to the design of thermal systems used to cool electronic components with an emphasis in semiconductor packages. We start with the basic theory of heat transfer and demonstrate simple concepts used today to calculate the cooling requirements for an electronic package and the impact of various parameters on the electronic package. This course covers in-depth heat transfer theory and analysis to give the student a comprehensive understanding of the key modes of heat transfer and their applications. Practical topics such as thermal interface materials, heat sink design and advanced cooling techniques are reviewed.

Course Outline:

1. Fundamentals of Heat Transfer and Its Application to Electronics Cooling
2. Techniques to Determine Cooling Requirements for a Package and Impact of Boundary Conditions
3. Simplification of Heat Transfer Equations to Analyze Cooling Solutions
4. Governing Principles of Cooling Solutions
5. Application of Numerical Methods to Calculate the Performance of Cooling Solutions
6. Introduction to Thermal Interface Materials and Their Applications
7. Techniques to Size Cooling Requirements and Trade-Offs
8. Parameters that Impact the Performance of Cooling Solutions
9. Introduction to Experimental Characterization of Cooling Solutions and Instrumentation
10. Fan Selection

Who Should Attend:

This class is intended for senior undergraduate and graduate students, as well as engineers working in the field of thermal management.

IMPORTANT NOTICE

Morning PD Courses 1 through 8 or afternoon PD Courses 9 through 16 run concurrently. Make sure you indicate which course you plan to attend in the morning and/or in the afternoon. As sessions run concurrently, attendance is only allowed at one session in the morning and one session in the afternoon.

See page 32 for registration information

AREA ATTRACTIONS

Nestled at the edge of spectacular San Diego Bay, the Sheraton San Diego Hotel & Marina enjoys panoramic views of the bay and the city skyline, yet it is just 10 minutes from renowned attractions including the Gaslamp Quarter, Old Town, and Balboa Park.

Boasting over 1,000 guest rooms and suites, located in two towers, the Sheraton offers Sweet Sleeper Beds, Shine by Sheraton bath products, and balconies with bay or city views. Enjoy the five minute scenic walk around the marina that connects both hotel towers.

In addition to all that the hotel boasts and offers, other local San Diego area attractions include its longstanding naval base on Coronado Island as well as Old Globe Theater, La Jolla, Mission Bay, and Point Loma. San Diego also boasts more championship golf courses, over 85, than any other US city. And one last thing, don't forget to take time out to visit the world renowned San Diego Zoo!

Program Sessions: Wednesday, June 1, 8:00-11:40 a.m.

Session 1: Advanced Packaging for Heterogeneous Integration and High Performance Computing	Session 2: High Performance Dielectric Materials for Advanced Packaging	Session 3: Antenna-in-Package for Communication, Radar and Energy Transfer
Committee: Packaging Technologies	**Committee: Materials & Processing**	**Committee: RF, High-Speed Components & Systems**
Session Co-Chairs: **Andrew Kim** **Advanced Micro Devices** **Email: andrew.kim@amd.com** **Mike Gallagher** **DuPont Electronic and Imaging** **Email: michael.gallagher@dupont.com**	**Session Co-Chairs:** **Lingyun (Lucy) Wei** **Dupont** **Email: lingyun.wei@dupont.com** **Yi Li** **Intel Corporation** **Email: yi.li@intel.com**	**Session Co-Chairs:** **Rajen M Murugan** **Texas Instruments** **Email: r-murugan@ti.com** **Maciej Wojnowski** **Infineon Technologies AG** **Email: maciej.wojnowski@infineon.com**
1. 8:00 AM - Organic Interposer CoWoS-R+ (plus) Technology M. L. Lin, M. S. Liu, H. W. Chen, S. M. Chen, M. C. Yew, C. S. Chen, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 8:00 AM - Ultra-Thin Mold Cap for Advanced Packaging Technology*** Nabankur Deb and Xavier Brun – Intel Corporation; Chris Masuyama, N. Hamada, Y. Hirano, K. Wada, H. Oshida, K. Ganbayashi, L. L. Zhou, and T. Y. Lyu – TOWA Corporation	***1. 8:00 AM - 77GHz Cavity Backed AiP Array in FOWLP Technology*** Mei Sun, Lim Teck Guan, and Chai Tai Chong – Institute of Microelectronics (IME), A*STAR
2. 8:25 AM - Cost-Effective RF Interposer Platform on Low-Resistivity Si Enabling Heterogeneous Integration Opportunities for Beyond 5G Xiao Sun, John Slabbekoorn, Siddhartha Sinha, Pieter Bex, Nelson Pinho, Tomas Webers, Dimitrios velenis, Andy Miller, Nadine Collaert, Geert Van der Plas, and Eric Beyne – Imec	***2. 8:25 AM - Evaluation of the Transmission Loss of Soluble Polyphenylene Ether Composite Material in a Millimeter-Wave Region*** Shoya Sekiguchi, Kota Oki, Shoko Mishima, Yuya Fukata, Kaho Shibasaki, Nobuhiro Ishikawa, and Toshiyuki Ogata – TAIYO HOLDINGS Co., Ltd.	***2. 8:25 AM - "Smart" Packaging of Self-Identifying and Localizable mmID for Digital Twinning and Metaverse Temperature Sensing Applications*** Charles Lynch, Ajibayo Adeyeye, and Manos Tentzeris – Georgia Institute of Technology
3. 8:50 AM - Chiplet-Based System PSI Optimization for 2.5D/3D Advanced Packaging Implementation Yoonjae Hwang, Sungwook Moon, Seungki Nam, and Jeong Hoon Ahn – Samsung Electronics Co., Ltd.	***3. 8:50 AM - Low-Dielectric, Low-Profile IC Substrate Material Development for 5G Applications*** Tomo Muguruma, Andy Behr, Hirosuke Saito, Koji Kishino, Fumito Suzuki, Tom Shin, and Hiroaki Umehara – Panasonic Corporation	***3. 8:50 AM - Performance Analysis and Impact of Manufacturing Tolerances for 5G mmWave Antenna in Package/Module (AiP/AiM)*** Sheng-Chi Hsieh, Cheng-Yu Ho, Hong-Sheng Huang, Chia-Ching Chu, and Chen-Chao Wang – ASE Group
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Double Side SiP of Structure Strength Analysis for 5G and Wearable Application Mike Tsai, Kevin Chang, Rios Hsieh, Wynn Li, Karina Chang, Ryan Chiu, Ethan Ding, Eric He, Tim Chang, and J. Y. Chen – Siliconware Precision Industries, Co. Ltd.	***4. 10:00 AM - Reliability Assessment of Ultra-Low-K Dielectric Material and Demonstration in Advanced Interposers*** Pragna Bhaskar, Christopher Blancher, Mohan Kathaperumal, Madhavan Swaminathan, and Mark Losego – Georgia Institute of Technology	***4. 10:00 AM - Compact Frequency Reconfigurable Array Antenna Based on Diagonally Placed Meander-Line Decouplers and PIN Diodes for Multi-Range Wireless Communications*** Suk-il Choi, Woosol Lee, and Yong-Kyu Yoon – University of Florida
5. 10:25 AM - A Laser Dicing Method for Plus-Shaped Dies for Heterogeneous Integration Applications Aakrati Jain, Kamal Sikka, Shidong Li, Juan-Manuel Gomez, Marc Bergendahl, and Spyridon Skordas – IBM Corporation; Roman Doll, Jeroen van Borkulo, Kees Biesheuvel, and Mark Mueller – ASM Laser Separation International B.V.	***5. 10:25 AM - Low Dielectric New Resin Cross-Linkers*** Takeshi Kumano, Yosuke Kurita, Kazunori Aoki, and Takashi Kashiwabara – Shikoku Chemicals Corporation	***5. 10:25 AM - High Gain and Low Back Radiation and Thin Antenna Designs Using Electromagnetic Bandgap Surface for Radar and Wearable Applications*** Lih-Tyng Hwang, Chun-Cheng Wang, Hung-Chih Lin, Ming-Yuan Huang, and Chih-Wen Kuo – National Sun Yat-sen University
6. 10:50 AM - 2.3D Hybrid Substrate with Ajinomoto Build-Up Film for Heterogeneous Integration Gary Chen, John Lau, Channing Cheng-Lin Yang, Jones Yu-Cheng Huang, Andy Yan-Jia Peng, Ning Liu, and T. J. Tseng – Unimicron Technology Corporation	***6. 10:50 AM - Solid-Diffusion Synthesis of Robust Hollow Silica Filler with Low Dk and Low Df*** Sicheng Luo, Ning Wang, Pengli Zhu, Tao Zhao, and Rong Sun – Shenzhen Institute of Advanced Electronic Materials	***6. 10:50 AM - Reconfigurable Antennas and FSS with Magnetically-Tunable Multiferroic Components*** Pawan Gaire, Veeru Jaiswal, John L. Volakis, Markondeya Raj Pulugurtha, and Shubhendu Bhardwaj – Florida International University
7. 11:15 AM - Advanced Packaging Technologies for Co-Packaged Optics Mei-Ju Lu, SinYuan Mu, ChiaSheng Cheng, and Jihan Chen – ASE Group	***7. 11:15 AM - Epoxy Wetting Flow and Adhesion Mechanism Within a Small Gap and Small Pitch Copper Pillar Structure*** Mary-Ann Gasser, Abdenacer Ait Mani, Alain Gueugnot, Thierry Mourier, and Patrick Peray – CEA-LETI; Loïc Vanel and Catherine Barentin – Institut Lumière Matière, Université Claude Bernard Lyon 1	***7. 11:15 AM - Electrically Small Folded Spherical Helix Antennas Utilizing Thick Solution Cast Nanomagnetic Films*** Nicholas Sturim and John Papapolymerou – Michigan State University; Edgar Aldama, Eric Drew, and John Zhang – Georgia Institute of Technology

Program Sessions: Wednesday, June 1, 8:00-11:40 a.m.

Session 4: Hybrid Bonding and Innovations for 3D Integration	Session 5: Bonding Technology: Novel Assembly Methods and Processes	Session 6: Emerging Modeling Including AI and Machine Learning
Committee: Interconnections	**Committee: Assembly & Manufacturing Technology**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Katsuyuki Sakuma** **IBM Corporation** **Email: ksakuma@us.ibm.com** **Seung Yeop Kook** **GlobalFoundries** **Email: seung-yeop.kook@globalfoundries.com**	**Session Co-Chairs:** **Valerie Oberson** **IBM Corporation** **Email: voberson@ca.ibm.com** **Jan Vardaman** **Techsearch International** **Email: jan@techsearchinc.com**	**Session Co-Chairs:** **Przemyslaw Gromala** **Robert Bosch GmbH** **Email: Przemyslawjakub.gromala@de.bosch.com** **Nancy Iwamoto** **Email: niwamoto@prodigy.net**
1. 8:00 AM - 3-Layer Stacking Technology with Pixel-Wise Interconnections for Image Sensors Using Hybrid Bonding of Silicon-on-Insulator Wafers Mediated by Thin Si Layers Masahide Goto, Yuki Honda, Masakazu Nanba, Yoshinori Iguchi, Takuya Saraya, Masaharu Kobayashi, Eiji Higurashi, Hiroshi Toshiyoshi, and Toshiro Hiramoto – NHK Science & Technology Research Laboratories	***1. 8:00 AM - The Influence of Copper Microstructure on Thermal Budget in Hybrid Bonding*** Laura Mirkarimi, Cyprian Uzoh, Dominik Suwito, Gill Fountain, Thomas Workman, Bongsub Lee, Jeremy Theil, and Guilian Gao – Xperi Corporation; Bryan Buckalew, Justin Oberst, and Thomas Ponnuswamy – Lam Research, Inc.	***1. 8:00 AM - Applied Modeling Framework in Integrated Circuit Design and Reliability*** Papa Momar Souare, Cedrick Bouchard, Eric Duchesne, and Francois Vachon – IBM Corporation; James Zaccardi and David Pettit – Viasat, Inc
2. 8:25 AM - Wafer to Wafer Hybrid Bonding for DRAM Applications Jinwon Park, Byungho Lee, Heesun Lee, Dail Lim, Jiho Kang, Changhyun Cho, and Myunghee Na – SK Hynix	***2. 8:25 AM - Collective Die-to-Wafer Self-Assembly for High Alignment Accuracy and High Throughput 3D Integration*** Alice Bond, Emilie Bourjot, Stéphan Borel, Thierry Enot, Pierre Montméat, Loïc Sanchez, and Frank Fournel – CEA-LETI; Johanna Swan – Intel Corporation	***2. 8:25 AM - Co-Design of Thermal Management with System Architecture and Power Management for 3D ICs*** Rishav Roy – Purdue University; Shidhartha Das, Benoit Labbe, Rahul Mathur, and Supreet Jeloka – Arm, Inc.
3. 8:50 AM - Analysis of Die Edge Bond Pads in Hybrid Bonded Multi-Die Stacks Jeremy Theil, Thomas Workman, Dominik Suwito, Laura Mirkarimi, Gill Fountain, KM Bang, Guilian Gao, Bongsub Lee, Pawel Mrozek, Cyprian Uzoh, and Michael Huynh – Xperi Corporation	***3. 8:50 AM - Fine-Pitch 30 µm Cu-Cu Bonding by Using Low Temperature Microfluidic Electroless Interconnection*** Yung-Sheng Lin, Yun-Ching Hung, Chin-Li Kao, Chung-Hung Lai, and David Tarng – ASE Group; Po-Shao Shih, Jeng-Hau Huang, and Robert C. Kao – National Taiwan University	***3. 8:50 AM - On-Chip Transient Hot Spot Detection with a Multiscale ROM in 3DIC Designs*** David Geb, Saeed Asgari, Akhilesh Kumar, Jimin Wen, Norman Chang, Stephen Pan, Mehdi Abarham, Haiyang He, and Viral Gandhi – Ansys
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - The Integration of Grounding Plane into TSV Integrated Ion Trap for Efficient Thermal Management in Large Scale Quantum Computing Device Peng Zhao, Yu Dian Lim, and Chuan Seng Tan – Nanyang Technological University; Hong Yu Li and Wen Wei Seit – Institute of Microelectronics (IME), A*STAR; Luca Guidoni – Universitée de Paris	***4. 10:00 AM - Die Bonding Solution for Flip Chip-Chip Scale Package-DIC (Digital Image Correlation) and Shadow Moiré Application*** Po Yu Liao, Ian Ho, David Lai, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.; Karen Chen, Hsin-Chih Shih, Dao-Long Chen, and David Tarng – ASE Group	***4. 10:00 AM - Implementation of Fully Coupled Electromigration Theory in COMSOL*** Zhen Cui and Guoqi Zhang – Delft University of Technology; Xuejun Fan – Lamar University
5. 10:25 AM - Wafer Stacked Wide I/O DRAM with One-Step TSV Technology Masaya Kawano, Xiang-Yu Wang, Qin Ren, Woon-Leng Loh, B.S.S. Chandra Rao, and King-Jien Chui – Institute of Microelectronics (IME), A*STAR; Tsuyoshi Kawagoe and Ichiro Homma – UltraMemory, Inc.	***5. 10:25 AM - Investigation of Low Temperature Co-Co Direct Bonding and Co-Passivated Cu-Cu Direct Bonding*** Demin Liu, Kuan-Chun Mei, Han-Wen Hu, Yi-Chieh Tsai, Huang-Chung Cheng, and Kuan-Neng Chen – National Yang Ming Chiao Tung University	***5. 10:25 AM - Peridynamic Modeling of Non-Fourier and Non-Fickian Diffusion in a Finite Element Framework*** Sundaram Vinod Anicode and Erdogan Madenci – University of Arizona
6. 10:50 AM - Recess Effect Study and Process Optimization of Sub-10 µm Pitch Die-to-wafer Hybrid Bonding Haoxiang Ren, Yu-Tao Yang, and Subramanian S. Iyer – University of California, Los Angeles	***6. 10:50 AM - Process and Design Optimization for Hybrid Cu Bonding Void*** Hyoeun Kim, Juhyeon Kim, Yeongseon Kim, Sun-Kyoung Seo, Chajea Jo, and Dae-Woo Kim – Samsung Electronics Co., Ltd.	***6. 10:50 AM - Feature Vector Based Remaining Useful-Life Assessment in Mechanical Shock and Vibration for Lead Free Electronics*** Pradeep Lall and Tony Thomas – Auburn University; Ken Blecker – US Army CCDC-AC
7. 11:15 AM - A Performance Testing Method of Bernoulli Picker for Ultra-Thin Die Handling Application Juno Kim, Dae Ho Min, Kangsan Lee, Kyeongbin Lim, and Minwoo Daniel Rhee – Samsung Electronics Co., Ltd.	***7. 11:15 AM - Laser-Assisted Bonding (LAB) Process and Its Bonding Materials as Technologies Enabling the Low-Carbon Era*** Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Ho-Gyeong Yun, Seok Hwan Moon, Ki-Seok Jang, Chanmi Lee, In-Seok Kye, Yoon-Hwan Moon, and Yong-Sung Eom – Electronics and Telecommunications Research Institute	***7. 11:15 AM - Genetic Algorithm Assisted Design of RDL Vias for a Fan-Out Panel Level SiC MOSFET Power Module Packaging*** Jiajie Fan, Jing Jiang, and Zhuorui Tang – Fudan University; Yichen Qian – Hohai University; Xuejun Fan – Lamar University; Guoqi Zhang – Delft University of Technology

Program Sessions: Wednesday, June 1, 1:30-5:10 p.m.

Session 7: Advanced Flip Chip and Embedded Substrate Technologies	Session 8: Hybrid and Direct Bonding Development and Characterization	Session 9: Millimeter-Wave Antenna-in-Package: Design, Manufacturing and Test
Committee: Packaging Technologies	**Committee: Interconnections**	**Committee: RF, High-Speed Components & Systems**
Session Co-Chairs: **Markus Leitgeb** **AT&S** **Email: m.leitgeb@ats.net** **Luu Nguyen** **Psi Quantum** **Email: lnguyen@psiquantum.com**	**Session Co-Chairs:** **Wei-Chung Lo** **Industrial Technology Research Institute** **Email: lo@itri.org.tw** **C. Key Chung** **TongFu Microelectronics Co., Ltd.** **Email: chungckey@hotmail.com**	**Session Co-Chairs:** **Xiaoxiong (Kevin) Gu** **Email: xgu@ieee.org** **P. Markondeya Raj** **Florida International University** **Email: mpulugur@fiu.edu**
1. 1:30 PM - Flip-Chip Chip Scale Package (FCCSP) Process Characterization and Reliability of Coreless Thin Package with 7 nm Si Technology Eduardo De Mesa, Thomas Wagner, Beth Keser, Jan Proschwitz, and Bernd Waidhas – Intel Corporation	***1. 1:30 PM - Development of Face-to-Face and Face-to-Back Ultra-Fine Pitch Cu-Cu Hybrid Bonding*** Yoshihisa Kagawa, Takumi Kamibayashi, Kenya Nishio, Taichi Yamada, Yuriko Yamano, Akihisa Sakamoto, Kan Shimizu, Tomoyuki Hirano, and Hayato Iwamoto – Sony Semiconductor Solutions Corporation	***1. 1:30 PM - A 16 Element Antenna Integrated Package for 37-40GHz Operation*** Selaka Bulumulla – GlobalFoundries; Syed Rahman, Arun Natarajan, and Harish Krishnaswamy – MixComm
2. 1:55 PM - In-Package Ring Hybrid Coupler with On-Chip Termination Robert Trieb and Andy Heinig – Fraunhofer Institute for Integrated Circuits IIS	***2. 1:55 PM - Surface Energy Characterization for Die-Level Cu Hybrid Bonding*** Katsuyuki Sakuma, Roy Yu, Michael Belyansky, Marc Bergendahl, and Dale McHerron – IBM Corporation; Ming Li, Yiu Ming Cheung, Siu Cheung So, So Ying Kwok, and Siu WIng Lau – ASM Pacific Technologies, Ltd.	***2. 1:55 PM - FOWLP AiP for SOTM Applications*** Mei Sun, Teck Guan Lim, and Yong Han – Institute of Microelectronics (IME), A*STAR
3. 2:20 PM - Superconducting Molybdenum Multi-Chip Module Approach for Cryogenic and Quantum Applications Archit Shah, Sherman Peek, Vaibhav Gupta, Bhargav Yelamanchili, David Tuckerman, Chris Cantaloube, John Sellers, and Michael Hamilton – Auburn University	***3. 2:20 PM - Comprehensive Study on Advanced Chip on Wafer Hybrid Bonding with Copper/Polyimide Systems*** Toshiaki Shirasaka, Tadashi Okuda, and Tomoaki Shibata – Showa Denko Materials Co., Ltd.; Satoshi Yoneda and Daisaku Matsukawa – HD MicroSystems, Ltd.; M. Mariappan, Mitsumasa Koyanagi, and Takafumi Fukushima – Tohoku University	***3. 2:20 PM - Characteristics of Glass-Embedded FOAiP with Antenna Arrays for 60GHz mmWave Applications*** I-Hung Lin, Ying-Chieh Pan, and Tom Ni – Hon Hai Precision Industry Co., Ltd; Cheng-Chen Lin and Ben-Je Lwo – National Defense University
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - Functional Interposer Embedded with Multi-Terminal Si Capacitor for 2.5D/3D Applications Using Planarization and Bumpless Chip-on-Wafer (COW) Yoshiaki Satake, Tatsuya Funaki, Kyosuke Kobinata, Youngsuk Kim, and Takayuki Ohba – Tokyo Institute of Technology; Seiji Hidaka, Hitoshi Matsuno, and Shunsuke Abe – Murata Manufacturing Co., Ltd.; Chih-Cheng Hsiao and Sheng-Yi Li – Industrial Technolo	***4. 3:30 PM - Two-Step Ar/N2 Plasma-Activated Al Surface for Al-Al Direct Bonding*** Liangxing Hu, Yu Dian Lim, Peng Zhao, Michael Joo Zhong Lim, and Chuan Seng Tan – Nanyang Technological University	***4. 3:30 PM - Implementation of a Sub-THz FCCSP Organic Package for Millimeter Wave Applications*** Neelam Prabhu Gaunkar, Georgios Dogiamis, Telesphor Kamgaing, and Adel Elsherbini – Intel Corporation
5. 3:55 PM - 3D Embedded Power Package Module to Integrate Various Power Systems Byong Jin Kim, Hyeong Il Jeon, Dae Young Park, Gi Jeong Kim, Nam-Hee Cho, and Jin Young Khim – Amkor Technology	***5. 3:55 PM - Novel Ga Assisted Low Temperature Bonding for Fine Pitch Interconnects*** Shan-Bo Wang, An-Hsuan Hsu, Chin-Li Kao, and David Tarng – ASE Group; Chien-Lung Liang and Kwang-Lung Lin – National Cheng Kung University	***5. 3:55 PM - Slot Bow-Tie Antenna Integration in Flip-Chip and Embedded Die Enhanced QFN Package for WR8 and WR5 Frequency Band*** Aditya Jogalekar, Oscar Medina, Andrew Blanchard, Rashaunda Henderson, and Mahadevan Iyer – The University of Texas at Dallas; Tony Tang, Rajen Murugan, and Hassan Ali – Texas Instruments
6. 4:20 PM - Demonstration of Substrate Embedded Ni-Zn Ferrite Core Solenoid Inductors Using a Photosensitive Glass Substrate Jein Yu, Dongsu Kim, Insub Han, and Jongmin Yook – Korea Electronics Technology Institute	***6. 4:20 PM - Characterization of Die-to-Wafer Hybrid Bonding Using Heterogeneous Dielectrics*** Minki Kim, Soojeoung Park, Aeni Jang, Hyuekjae Lee, Seungduk Baek, ChungSun Lee, Ilhwan Kim, Jumyong Park, Youngkun Jee, Dae-Woo Kim, and Un-Byoung Kang – Samsung Electronics Co., Ltd.	***6. 4:20 PM - Antenna-Integrated, Die-Embedded Glass Package for 6G Wireless Applications*** Xiaofan Jia, Xingchen Li, Kyoung-sik Moon, Joon Woo Kim, Kai-Qi Huang, Matthew B. Jordan, and Madhavan Swaminathan – Georgia Institute of Technology
7. 4:45 PM - Fabrication and Characterization of Package Embedded Inductors for Integrated Voltage Regulators Prahalad Murali, Venkatesh Avula, Marisa Ahmed, Mark Losego, and Madhavan Swaminathan – Georgia Institute of Technology; Claudio Alvarez – Intel Corporation; Yusuke Oishi, Tomohito Uemura, Ryo Nagatsuka, and Naoki Watanabe – Panasonic Corporation	***7. 4:45 PM - Solder and Organic Adhesive Hybrid Bonding Technology with Non-Strip Type Photosensitive Resin and Injection Molded Solder (IMS)*** Keiji Matsumoto, Takahito Watanabe, Risa Miyazawa, Toyohiro Aoki, and Takashi Hisada – IBM Corporation; Yuzo Nakamura, Yasuhisa Kayaba, Jun Kamada, and Kazuo Kohmura – Mitsui Chemicals, Inc.	***7. 4:45 PM - Design and Testing of a WR28 Waveguide Blind Mating Interconnect for mmWave ATE OTA Applications*** Shiota Natsuki, Kikuchi Aritomo, Yuchang Liu, Daniel Lam, Takasu Hiromitsu, Mineo Hiroyuki, Kato Yasuyuki, and Jose Moreira – Advantest

Program Sessions: Wednesday, June 1, 1:30-5:10 p.m.

Session 10: Novel Photonics Packaging Technology	Session 11: Automotive and Harsh Environment	Session 12: Manufacturing and Assembly Process Modeling
Committee: Photonics	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Ajey Jacob** **University of Southern California** **Email: ajey@isi.edu** **Vivek Raghuraman** **Broadcom Corporation** **Email: vivek.raghuraman@gmail.com**	**Session Co-Chairs:** **Pilin Liu** **Intel Corporation** **Email: pilin.liu@intel.com** **Lakshmi N. Ramanathan** **Meta, Inc.** **Email: laksh_r@hotmail.com**	**Session Co-Chairs:** **Pradeep Lall** **Auburn University** **Email: lall@auburn.edu** **Yong Liu** **ON Semiconductor** **yong.liu@onsemi.com**
1. 1:30 PM - Demonstration of Fan-Out Silicon Photonics Module for Next Generation Co-Packaged Optics (CPO) Application Bruce Chou, Aaron Zilkie, and David McCann – Rockley Photonics	***1. 1:30 PM - Cu-Al IMC Degradation Under High Electric Fields During HTOL Test*** Amar Mavinkurve, Rene Rongen, and Michiel van Soestbergen – NXP Semiconductors	***1. 1:30 PM - Multi-Physics Simulation of Wafer-to-Wafer Bonding Dynamics*** Nathan Ip, Nima Nejadsadeghi, and Carlos Fonseca – Tokyo Electron America, Inc.; Norifumi Kohama and Kimio Motoda – Tokyo Electron Kyushu, Ltd.
2. 1:55 PM - Optical Performance and Reliability Assessment from Self-Aligned Single Mode Fiber Attach for O-Band Silicon Photonics Platform Jae Kyu Cho, Benjamin Fasano, Vaishnavi Karra, Alberto Cestero, Norman Robson, George Wu, Thomas Houghton, Takako Hirokawa, Yusheng Bian, and Koushik Ramachandran – GlobalFoundries	***2. 1:55 PM - Effect of Underfill Property Evolution on Solder Joint Reliability in Automotive Applications*** Pradeep Lall, Madhu Kasturi, Yunli Zhang, Haotian Wu, Jeff Suhling, and Ed Davis – Auburn University	***2. 1:55 PM - Simulation and Verification of Ag-Cu Core-Shell Sintered Paste for Power Semiconductor Die-Attach Applications*** Xinyue Wang, Zejun Zeng, and Pan Liu – Fudan University; Jing Zhang – Heraeus Materials Technology, Ltd.; Guoqi Zhang – Delft University of Technology
3. 2:20 PM - Optical Fiber Pigtail Integration for Co-Package Alexander Janta-Polczynski – IBM Corporation; Martin Robitaille – LXsim	***3. 2:20 PM - Impact of the Final Finish on the Solder Joint Reliability and IMC Formation After Thermal Storage*** Britta Schafsteller, Sven Lamprecht, and Gustavo Ramos – Atotech Deutschland GmbH	***3. 2:20 PM - Transient Thermal Modeling of Die Bond Process in Multiple Die Stacked Flash Memory Package*** Yangming Liu, Ning Ye, Bo Yang, Xu Wang, Jacky Liu, Shenghua Huang, and Chin-Tien Chiu – Western Digital
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - A Novel Packaging Platform for High-Performance Optical Engines in Hyperscale Data Center Applications Sajay Bhuvanendran Nair Gourikutty, Ming Chinq Jong, Chockanathan Vinoth Kanna, David Soon Wee Ho, Seit Wen Wei, Sharon Lim Pei Siang, Jiaqi Wu, Teck Guan Lim, Rathin Mandal, and Surya Bhattacharya – Institute of Microelectronics (IME), A*STAR; Jason Tsung-Liow – Rain Tree Photonics Pte. Ltd.	***4. 3:30 PM - New Lifetime Model for Advanced Power Semiconductor Interconnects*** Alexander Schiffmacher, Ahmad Bashiti, David Strahringer, and Juergen Wilde – University of Freiburg; Carsten Kempiak and Andreas Lindemann – Otto-von-Guericke University; Jacek Rudzki – Danfoss Silicon Power GmbH	***4. 3:30 PM - Novel Method for NCF Flow Simulation in HBM Thermal Compression Bonding Process to Optimize the NCF Shape*** Jong Pa Hong, Su Chang Lee, Sun Woo Han, Sang Kun Oh, Sang Sik Park, Hyeong Mun Kang, Won Keun Kim, Kil Soo Kim, and Dan Oh – Samsung Electronics Co., Ltd.
5. 3:55 PM - Advanced 2.5D and 3D Packaging Technologies for Next Generation Silicon Photonics in High Performance Networking Applications Sandeep Razdan, Jie Xue, Peter De Dobbelaere, Aparna Prasad, and Vipul Patel – Cisco Systems, Inc.	***5. 3:55 PM - Thermal and Mechanical Optimization to Enable Reliable High Performance Liquid-Cooled Compute System for Level 4 Autonomous Driving*** Fen Chen, Gilberto Madrid, Brian Schlotterbeck, Jagdeep Singh, Adli Nureddin, Tyler Sawyer, Zoran Stefanoski, Spencer Klimpke, Hector Guajardo, Arul Ramalingam, and Maik Duwensee – Cruise Automation	***5. 3:55 PM - Numerical Evaluation on SiO2 Based Chip to Wafer Hybrid Bonding Performance by Finite Element Analysis*** Lin Ji and Sasi Kumar Tippabhotla – Institute of Microelectronics (IME), A*STAR
6. 4:20 PM - 90-Degree Bent Core Polymer Optical Waveguide Coupler for Low Loss Lens-Less Light Coupling Between Laser/Photodetector and Fiber Daiki Suemori, Maho Ishii, Naohiro Kohmu, and Takaaki Ishigure – Keio University	***6. 4:20 PM - Comprehensive Study of Long-Term Reliability of Copper Bonding Wires at Harsh Automotive Conditions*** Robert Klengel, Sandy Klengel, Sebastian Tismer, and Thomas Ackermann – Fraunhofer Institute for Microstructure of Materials and Systems (IMWS); Noritoshi Araki, Motoki Eto, Teruo Haibara, and Takashi Yamada – Nippon Micrometal Corporation; Jochen Feldmann, Ralph Binner, and Henk Peters – Elmos Semiconductor SE	***6. 4:20 PM - A Novel Equivalent Model for Underfill Molding Process on 2.2D Structure for High Performance Applications*** Yu-En Liang, Chia-Peng Sun, and Chih Chung Hsu – CoreTech System (Moldex3D); Dyi-Chung Hu and EH Chen – SiPlus Co., Ltd.; Jeffrey (Chang-Bing) Lee – iST-Integrated Service Technology, Inc.
7. 4:45 PM - Lossless High-Speed Silicon Photonic MZI Switch with a Micro-Transfer-Printed III-V Amplifier Jing Zhang, Clemens J. Kruckel, and Laurens Bogaert – Ghent University; Bahawal Haq; Johanna Rimböck, Bozena Matuskova, and Stefan Ertl – EV Group; Agnieszka Gocalinska, Emanuele Pelucchi, and Brian Corbett – Tyndall National Institute	***7. 4:45 PM – Post Wire Bonding Coating for Prevention of Corrosion of Wire Bonded Packages by Chlorine Containing Foreign Particles*** Varughese Mathew, Sheila Chopin, Guangming Li, and Sean Xu – NXP Semiconductors	***7. 4:45 PM - Key Steps from Laboratory Towards Mass Production: Optimization of Electroless Plating Process Through Numerical Simulation*** Simon Johannes Gräfner, Jeng-Hau Huang, Yu-An Chen, Po-Shao Shih, Ching-Han Huang, and C. Robert Kao – National Taiwan University

Program Sessions: Thursday, June 2, 8:00-11:40 a.m.

Session 13: Technologies for Heterogeneous Integration, Automotive and Power Electronics	Session 14: Novel Bonding and and Stacking Technologies	Session 15: Enhanced Methods & Processes for Heterogeneous Integration Assembly
Committee: Packaging Technologies	**Committee: Materials & Processing joint with Assembly & Manufacturing Technology**	**Committee: Assembly & Manufacturing Technology**
Session Co-Chairs: **Dean Malta** **Micross Advanced Interconnect Technology** **Email: Dean.Malta@micross.com** **Peng Su** **Juniper Networks** **Email: pensu@juniper.net**	**Session Co-Chairs:** **Bing Dang** **IBM Corporation** **Email: dangbing@us.ibm.com** **Hongbin Yu** **Arizona State University** **Email: yuhb@asu.edu**	**Session Co-Chairs:** **Christo Bojkov** **Qorvo** **Email: cbojkov.ectc@gmail.com** **Jason Rouse** **Corning Incorporated** **Email: rousejh@corning.com**
1. 8:00 AM - A Novel 3D Driver-Integrated Silicon Carbide Half-Bridge Power Module with Low Stray Inductance Chun-Kit Cheung and Ziyang Gao – Hong Kong Applied Science & Technology Research Institute	***1. 8:00 AM - Behavior of Bonding Strength on Wafer-to-Wafer Cu-Cu Hybrid Bonding*** Shunsuke Furuse, Nobutoshi Fujii, Kengo Kotoo, Naoki Ogawa, Taichi Yamada, Takaaki Hirano, Suguru Saito, Yoshiya Hagimoto, and Hayato Iwamoto – Sony Semiconductor Solutions Corporation	***1. 8:00 AM - Super Fine Jet Underfill Dispense Technique for Robust Micro Joint in Direct Bonded Heterogeneous Integration (DBHi) Silicon Bridge Packages*** Akihiro Horibe, Chinami Marushima, Takahito Watanabe, Aakrati Jain, Eric Turcotte, Isabel de Sousa, Takashi Hisada, and Kamal Sikka – IBM Corporation
2. 8:25 AM - Static/Transient Thermal Analysis and Design Optimization of a Lead Frame Based Dual Side Cooling SiC Power Module Gongyue Tang and Kazunori Yamamoto – Institute of Microelectronics (IME), A*STAR	***2. 8:25 AM - Development of Polyimide Base Photosensitive Permanent Bonding Adhesive for Middle to Low Temperature Hybrid Bonding Process*** Satoshi Yoneda, Kenya Adachi, Daisaku Matsukawa, and Takahiro Tanabe – HD Microsystems, Ltd.; Kaori Kobayashi, Toshiaki Shirasaka, Shizu Fukuzumi, and Tadashi Okuda – Showa Denko Materials Co., Ltd.	***2. 8:25 AM - Assembly Challenges and Demonstrations of Ultra-Large Antenna in Package for Automotive Radar Applications*** Sharon Pei Siang Lim, Ser Choong Chong, David Ho Soon Wee, and Tai Chong Chai – Institute of Microelectronics (IME), A*STAR
3. 8:50 AM - Impact of Reliability Tests on the Adhesion of the Epoxy Mold Compound David Guillon, Andris Avots, Katrin Schlegel, Milad Maleki, and Isabell Ehrler – Hitachi Energy	***3. 8:50 AM - Direct Bonding Using Low Temperature SiCN Dielectrics*** Serena Lacovo, Fuya Nagano, Venkat Sunil Kumar Channam, Anne Jourdain, Kris Vanstreels, Alain Phommahaxay, and Eric Beyne – Imec; Edward Walsby, Kath Crook, and Keith Buchanan – SPTS Technologies	***3. 8:50 AM - Investigation on Package Warpage and Reliability of the Large Size 2.5D Molded Interposer on Substrate (MIoS) Package*** Soohyun Nam, Jinhyun Kang, Ilbok Lee, Hae Jung Yu, Chajea Jo, and Dae-Woo Kim – Samsung Electronics Co., Ltd.
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Advanced Thermal Integration for HPC Packages with Two-Phase Immersion Cooling Po-Yao Lin, Sheng-Liang Kuo, Kathy Yan, Wen-Ming Chen, and Marvin De-Dui Liao – Taiwan Semiconductor Manufacturing Company, Ltd.	***4. 10:00 AM - Heterogeneous Integration by the 3D Stacking of Thin Silicon Die*** Pavani Vamsi Krishna Nittala, Karthika Haridas, and Prosenjit Sen – Indian Institute of Science	***4. 10:00 AM - Characterizations and Challenges of Adhesion Promotion Solutions for HSIO Package Development*** Yi Yang, Marcel Wall, Rengarajan Shanmugam, Sarah Wozny, Xin Yan, Mohit Khurana, Rajeev Ranjan, Dilan Seneviratne, Kassandra Nikkhah, and Suddhasattwa Nad – Intel Corporation
5. 10:25 AM - Hybrid Stacked-Die Package Solution for Extremely Small-Form-Factor Package Heeseok Lee, Kyoung Min Lee, Daehan Youn, Kyojin Hwang, and Junghwa Kim – Samsung Electronics Co., Ltd.	***5. 10:25 AM - Prolongation of Surface Activation Effect Using Self-Assembled Monolayer for Low Temperature Bonding of Au*** Kai Takeuchi and Tadatomo Suga – Meisei University; Beomjoon Kim – University of Tokyo	***5. 10:25 AM - Heterogeneous Integration for Chiplets on FOWLP Development Line*** Chai Tai Chong, David Ho, Chong Ser Chong, Sharon Lim PS, and Surya Bhattacharya – Institute of Microelectronics (IME), A*STAR
6. 10:50 AM - Thermo-Mechanical Analysis of Thermal Compression Bonding Chip-Join Process Prabudhya Roy Chowdhury, Katsuyuki Sakuma, Sathya Raghavan, Marc Bergendahl, Kamal Sikka, Sayuri Kohara, Takashi Hisada, Hiroyuki Mori, Divya Taneja, and Isabel De Sousa – IBM Corporation	***6. 10:50 AM - Mini LED Array Transferred onto a Flexible Substrate Using Simultaneous Transfer and Bonding (SITRAB) Process and Anisotropic SITRAB Film (ASF)*** Jiho Joo, Gwang-Mun Choi, Chanmi Lee, In-Seok Kye, Ki-seok Jang, Yong-Sung Eom, and Kwang-Seong Choi – Electronics and Telecommunications Research Institute; Jeong Duck Kim and Seok Tae Hwang – Nexstar Technology Co., Ltd.	***6. 10:50 AM - Split-Fabric: A Novel Wafer-Scale Hardware Obfuscation Methodology Using Silicon Interconnect Fabric*** Yousef Safari and Boris Vaisband – McGill University; Yu-Tao Yang and Subramanian S. Iyer – University of California, Los Angeles; Toshifumi Nakatani – Maxentric Technologies LLC; Neal Levine – Defense Microelectronics Activity (DMEA)
7. 11:15 AM - Dimensional Parameters Controlling Capillary Underfill Flow for Void-Free Encapsulation of a Direct Bonded Heterogeneous Integration (DBHi) Si-Bridge Package Chinami Marushima, Toyohiro Aoki, Koki Nakamura, Risa Miyazawa, Akihiro Horibe, Isabel De Sousa, Takashi Hisada, and Kamal Sikka – IBM Corporation	***7. 11:15 AM - Characterization of Non-Conductive Paste Materials (NCP) for Thermocompression Bonding in a Direct Bonded Heterogeneously Integrated (DBHi) Si-Bridge Package*** Akihiro Horibe, Takahito Watanabe, Chinami Marushima, Hiroyuki Mori, Sayuri Kohara, Roy Yu, Marc Bergendahl, Teddie Magbitang, Rudy Wojtecki, Divya Taneja, and Maxime Godard – IBM Corporation	***7. 11:15 AM - A Self-Aligned Structure Based on V-Groove for Accurate Silicon Bridge Placement*** Yang Qiu, Yann Beilliard, and Isabel De Sousa – University of Sherbrooke; Dominique Drouin – IBM Corporation

Program Sessions: Thursday, June 2, 8:00-11:40 a.m.

Session 16: Hybrid & Direct Bonding Innovation, Optimization & Yield Improvement	Session 17: Novel Characterization Techniques and Test Methods	Session 18: Flexible, Wearable Sensors and Electronics
Committee: Interconnections	**Committee: Applied Reliability**	**Committee: Emerging Technologies**
Session Co-Chairs: **Xin Yan** **Intel Corporation** **Email: xin.yan@intel.com** **Kangwook Lee** **SK Hynix** **Email: steward.lee@sk.com**	**Session Co-Chairs:** **Sandy Klengel** **Fraunhofer IZM** **Email: sandy.klengel@imws.fraunhofer.de** **Pei-Haw Tsao** **Taiwan Semiconductor Manufacturing Company, Ltd.** **Email: phtsao@tsmc.com**	**Session Co-Chairs:** **Chukwudi Okoro** **Corning Incorporated** **Email: okoroc@corning.com** **Isaac Robin Abothu** **Siemens Healthineers** **Email: Isaac.abothu@siemens-healthineers.com**
1. 8:00 AM - The Wafer Bonding Yield Improvement Through Control of SiCN Film Composition and Cu Pad Shape Dail Rim, Byungho Lee, Jinwon Park, Changhyun Cho, Jiho Kang, and Ilseop Jin – SK Hynix	***1. 8:00 AM - Sn Whisker Growth from SnAgCu-(TiO2/ZnO) Nano-Composite Solder Alloys*** Balázs Illés, Halim Chio, Oliver Krammer, Attila Geczy, and Tamás Hurtony – Budapest University of Technology and Economics; Agata Skwarek and Jacek Ratajczak – Łukasiewicz Research Network - Institute of Microelectronics (IME), A*STAR	***1. 8:00 AM - Robustness and Reliability of Novel Anisotropic Conductive Epoxy for Stretchable Wearable Electronics*** Andrew Stemmermann, Daniel Balder, and Madhu Stemmermann – SunRay Scientific, Inc.; Nancy Stoffel – General Electric; Riadh Al-Haidari, Behnam Garakani, Udara Somarathna, El Medhi Abbara, Mohammed Alhendi, and Mark Poliks – Binghamton University; Christopher Tabor – Air Force Research Laboratory
2. 8:25 AM - Low Temperature Wafer-to-Wafer Hybrid Bonding by Nanocrystalline Copper Wei-Lan Chiu, Ou-Hsiang Lee, Chia-Wen Chiang, and Hsiang-Hung Chang – Industrial Technology Research Institute	***2. 8:25 AM - QFN (Quad Flat No–Lead) Solder Joint Under Thermal Cycling: Identification of Two Failure Mechanisms*** Emna Ben Romdhane, Pierre Romanille, and Samuel Pin – IRT Saint-Exupéry; Alexandrine Guédon-Garcia and Hélène Frémont – IMS Laboratory; Patrick Nugyen – Elemca	***2. 8:25 AM - Wireless Nanomembrane Electronics and Soft Packaging Technologies for Noninvasive, Real-Time Monitoring of Muscle Activities*** Hojoong Kim and Woon-Hong Yeo – Georgia Institute of Technology; Hyojung J. Choo – Emory University
3. 8:50 AM - Cu-SiO2 Hybrid Bonding Yield Enhancement Through Cu Grain Enlargement M. Mariappan and T. Fukushima – Global INTegration Initiative; K. Mori and M. Koyanagi – T-Micro; M. Sawa and E. Sone – JCU Corporation	***3. 8:50 AM - Tracking In-Die Mechanical Stress Through Silicon Embedded Sensors for Advanced Packaging Applications*** Sharad Saxena, Christopher Hess, Michele Quarantelli, Alberto Piadena, Larg Weiland, Rakesh Vallishayee, Yuan Yu, Dennis Ciplickas, Tomasz Brozek, and Andrzej Strojwas – PDF Solutions	***3. 8:50 AM - Modeling of Spreading Behavior of UV-Curable Dielectric Ink from its Rheological Characteristics*** Sujie Kang, Jung Shin Lee, Jung Woo Cho, Sun Woo Park, Seungdon Lee, Hyunjin Lee, and Daniel Min Woo Rhee – Samsung Electronics Co., Ltd.
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - A Holistic Development Platform for Hybrid Bonding Liu Jiang, Srikrishna Sitaraman, Sefa Dag, Mohammad Masoomi, Kwangwon Choi, Ying Wang, Prayudi Linato, Gilbert See, El Mehdi Bazizi, and Blessy Alexander – Applied Materials, Inc.	***4. 10:00 AM - Damage Evolution of Double-Sided Copper Conductor on Multi-Layer Flexible Substrate Under Bending*** Rui Chen, Justin Chow, and Suresh Sitaraman – Georgia Institute of Technology	***4. 10:00 AM - Fabrication of Flexible Li-ion Battery Electrodes Using "Battlets" Approach with Ionic Liquid Electrolyte for Powering Wearable Devices*** Guangqi Ouyang, Grace Whang, Emily MacInnis, Haoxiang Ren, Henry Sun, Randall Irwin, and Subramanian S. Iyer – University of California, Los Angeles
5. 10:25 AM - Low Temperature Fine-Pitch Cu-Cu Bonding Using Au Nanoparticles as Intermediate Jun-Peng Fang, Jian Cai, Qian Wang, and Xiu-Yu Shi – Tsinghua University; Kai Zheng and Yi-Kang Zhou – Semiconductor Technology Innovation Center (Beijing) Corporation	***5. 10:25 AM - Investigation of Stress Generated by Interconnection Processes with Micro-Raman Spectroscopy (mRS)*** E Liu, Sri Krishna Bhogaraju, Kerstin Lux, and Gordon Elger – Technische Hochschule Ingolstadt; Rokeya Mumtahana Mou – Fraunhofer IVI	***5. 10:25 AM - Smart Biofeedback Earbud Achieved by SIP with 3D Composite Polymer Package*** Kuei-Hao Tseng, Chih-Lung Lin, Kai-Hung Wang, and Harrison Chang – ASE Group
6. 10:50 AM - Wet Atomic Layer Etching of Copper Structures for Highly Scaled Copper Hybrid Bonding and Fully Aligned Vias Christopher Netzband and Sitaram Arkalgud – TEL Technology Center, America, LLC; Paul Abel and Jacques Faguet – Tokyo Electron America, Inc.	***6. 10:50 AM - Development and Application of the Moisture-Dependent Viscoelastic Model of Polyimide in Hygro-Thermo-Mechanical Analysis of Fan-Out Interconnect*** Chia-Ming Yang and Tz-Cheng Chiu – National Cheng Kung University; Wei-Jie Yin, Dao-Long Chen, Chin-Li Kao, and David Tarng – ASE Group	***6. 10:50 AM - Current Carrying Capacity of Inkjet Printed Nano-Silver Interconnects on Mesoporous PET Substrate*** El Mehdi Abbara, Gurvinder Singh Khinda, Mohammed Alhendi, Riadh Alhaidari, Behnam Garakani, Udara Somarathna, and Mark Poliks – Binghamton University
7. 11:15 AM - A Study on Bonding Pad Structure and Layout for Fine Pitch Hybrid Bonding SeonKyeong Seo, HyoEun Kim, YeongSeon Kim, Chaje Cho, and DaeWoo Kim – Samsung Electronics Co., Ltd.	***7. 11:15 AM - A Novel Quantitative Adhesion Measurement Method for Thin Polymer and Metal Layers for Microelectronic Applications*** Markus Woehrmann, Michael Schiffer, Piotr Mackowiak and Klaus-Dieter Lang – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University of Berlin	***7. 11:15 AM - Fabrication of Wearable Strain Sensor by Using a Novel Hybrid Cu Ink Composed of Bimodal Cu Particle Ink and Cu-Based Metal-Organic Decomposition Ink*** Cong Gan, Hai-Jun Huang, Bin Hou, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

Program Sessions: Thursday, June 2, 1:30–5:10 p.m.

Session 19: Advances in Fan-Out Panel Level Packaging	Session 20: Enhancements in Fine-Pitch Interconnects, Redistribution Layers and Through-Vias	Session 21: Millimeter-Wave RF Components and Modules for 5G
Committee: Packaging Technologies	**Committee: Materials & Processing**	**Committee: RF, High-Speed Components & Systems**
Session Co-Chairs: **Albert Lan** **Applied Materials, Inc.** **Email: Albert_Lan@amat.com** **Jie Fu** **Apple, Inc.** **Email: fujie6@gmail.com**	**Session Co-Chairs:** **Ivan Shubin** **RAM Photonics LLS** **Email: ishubin@gmail.com** **Jayaram Vidya** **Intel Corporation** **Email: vidya.jayaram@intel.com**	**Session Co-Chairs:** **Craig Gaw** **NXP Semiconductor** **Email: c.a.gaw@ieee.org** **Jaemin Shin** **Apple, Inc.** **Email: sjm1218@gmail.com**
1. 1:30 PM - Panel Level Packaging – Where are the Technology Limits? Tanja Braun, Ole Hölck, Mattis Obst, Steve Voges, Ruben Kahle, Lars Böttcher, Mathilde Billaud, Lutz Stobbe, Karl-Friedrich Becker, and Rolf Aschenbrenner – Fraunhofer IZM; Marcus Voitel – Technical University Berlin	***1. 1:30 PM - A Study of Failure Mechanism in the Formation of Fine RDL Patterns and Vias for Heterogeneous Packages in Chip Last Fan-Out Panel Level Packaging*** Yoon Young Jeon, Youngmin, Minju Kim, Sangyun Lee, Hyun-Dong Lee, Changbo Lee, and Joon Seok Oh – Samsung Electronics Co., Ltd.	***1. 1:30 PM - Metaconductor Based Highly Energy Efficient Differential Striplines for 112 Gbps Data Bus with Sub 0.1 dB/mm Package Insertion Loss*** Hae-In Kim, Saeyeong Jeon, and Yong-Kyu Yoon – University of Florida; Rockwell Hsu and Brice Achkir – Cisco Systems, Inc.
2. 1:55 PM - Study of Reliable Via Structure for Fan-Out Panel Level Package (FOPLP) Da-Hee Kim, Jae-Ean Lee, Gyujin Choi, Sunguk Lee, Giho Jeong, Hongwon Kim, Seokwon Lee, and Dong wook Kim – Samsung Electronics Co., Ltd.	***2. 1:55 PM - Novel Plasma Process for Build-Up Film in the Fine Wiring Fabrication*** Daisuke Hironiwa, Yasuhiro Morikawa, Atsuhito Ihori, and Ryuichiro Kamimura – ULVAC, Inc.	***2. 1:55 PM - Multi-Terminal Ultra-Thin 3D Nanoporous Silicon Capacitor Technology for High-Speed Circuits Decoupling*** Mohamed Mehdi Jatlaoui, Seiji Hidaka, and Ryo Kasai – Murata Integrated Passive Solutions, SAS; Sho Kubota, Masato Takesawa, Charles Muller, Florent Lallemand, Shunsuke Abe, Takashi Takeuchi, and Hitoshi Matsuno – Murata Manufacturing Co., Ltd.
3. 2:20 PM - A Hybrid Panel Level Package (Hybrid PLP) Technology Based on a 650-mm x 650-mm Platform Eoin O´Toole, Luís Silva, Filipe Cardoso, José Silva, Aníbal Coelho, Márcio Souto, Nuno Delduque, José Silva, WonChul Do, and JinYoung Khim – Amkor Technology	***3. 2:20 PM - Fine Copper Lines with High Adhesion on High Rigidity Dielectrics*** Masataka Nishida, Hirokazu Noma, Masaki Yamaguchi, and Kazuyuki Mitsukura – Showa Denko Materials Co., Ltd.	***3. 2:20 PM - Mechanical and Ka-Band Electrical Reliability Testing of Interconnects in 5G Wearable System-on-Package Designs Under Bending*** Yi Zhou, Kexin Hu, Manos M. Tentzeris, and Suresh K. Sitaraman – Georgia Institute of Technology
Refreshment Break: 2:45–3:30 p.m.		
4. 3:30 PM - Package Reliability Evaluation of 600mm FOPLP with 6-Sided Die Protection with 0.35mm Ball Pitch Jacinta Aman Lim, Brett Dunlap, Sungeun Hong, Hyung-Jin Shin, and Byung Cheol Kim – nepes Corporation	***4. 3:30 PM - Fabrication and Characterization of Nanoporous Gold (NPG) Interconnects for Wafer Level Packaging*** Lothar Dietrich, Hermann Oppermann, Christina Lopper, and Piotr Mackowiak – Fraunhofer IZM	***4. 3:30 PM - X-band Passive Circuits Using 3-D Printed Hollow Substrate Integrated Waveguides*** Yihang Chu, Yamini Kotriwar, Ethan Kepros, Brian Wright, and Premjeet Chahal – Michigan State University
5. 3:55 PM - Panel-Based Large-Scale RDL Interposer Fabricated Using 2-Micron Pitch Semi-Additive Process for Chiplet-Based Integration Hiroshi Kudo, Takamasa Takano, Hiroshi Mawatari, Daisuke Kitayama, Takahiro Tai, Tsuyoshi Tsunoda, and Satoru Kuramochi – Dai Nippon Printing (DNP) Co., Ltd.	***5. 3:55 PM - Role of (111) Nanotwinned Cu on Dissolution Behavior and Interfacial Reaction in Micro-Scale Nanotwinned Cu/Sn/Ni Interconnects*** Mingliang Huang, Shengbo Wang, and Jing Ren – Dalian University of Technology	***5. 3:55 PM - A Novel Simulation Methodology Reflecting System Power Scenario Using a Markov-Chain-based Stochastic Random Power Model*** Woo-Jin Na, Kun Joo, Rakjoo Sung, Kyudong Lee, Ji-Hye Yang, Kyungsun Kim, Young-Ho Lee, Seung-Hee Mun, SungJoo Park, and Jeong-Hyeon Cho – Samsung Electronics Co., Ltd.
6. 4:20 PM - Harnessing the Power of 4nm Silicon with Gen 2 M-Series™ Fan-Out and Adaptive Patterning® Providing Ultra-High-Density 20µm Device Bond Pad Pitch Robin Davis and Benedict San Jose – Deca Technologies	***6. 4:20 PM - Approaches for a Solely Electroless Metallization of Through-Glass Vias*** Aleksandra M. Zawacka, Maren S. Prediger, Alexander Kassner, and Folke Dencker – Leibniz University Hannover; Marc C. Wurz – Ulm University	***6. 4:20 PM - Towards Mass Production of Air Filled Substrate Integrated Waveguides (AFSIW) for Ultra-Low Loss, Broadband Radar Applications*** Heinrich Trischler and Erich Schlaffer – AT&S; Siddhartha Sinha and Ilja Ocket – Imec
7. 4:45 PM - All Copper Is Not Created Equal – Examples of Grain Engineering In Plating Yun Zhang, Jing Wang, Peipei Dong, Xingxing Zhang, Wei Zhao, and Josh Liang – Shinhao Materials LLC; Michael Herkommer, Klaus Leyendecker, and Volker Wohlfarth – Umicore Galvanotechnik GmbH	***7. 4:45 PM - Atmospheric HF Vapor Based Silicon Etching with Pt Catalyst for High Fidelity Through Silicon Via (TSV) Fabrication*** Sunghyun Hwang and Yong-Kyu Yoon – University of Florida; William N. Carr – Phononic MEMS, Inc.	***7. 4:45 PM - Characterisation of RF Components and Connectors for Advanced 5G Applications*** Kimmo Rasilainen, Marko E. Leinonen, Olli Kursu, Klaus Nevala, Shayan Hasan Naushahi, Juha-Matti Ojakoski, Markus Berg, and Aarno Pärssinen – University of Oulu

Program Sessions: Thursday, June 2, 1:30–5:10 p.m.

Session 22: AI, Quantum Computing and Novel 3D Packaging Solutions	Session 23: Advanced Processes for Manufacturing and Yield Enhancement	Session 24: Thermal Management and Warpage Analysis of Highly Integrated Packages
Committee: Emerging Technologies	**Committee: Assembly & Manufacturing Technology**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Yang Liu** **Nokia Bell Labs** **Email: yang3d@gmail.com** **Vaidyanathan Chelakara** **Acacia Communications** **Email: cvaidyanathan@acacia-inc.com**	**Session Co-Chairs:** **Shichun Qu** **Email: shichun.qu@gmail.com** **Mark Gerber** **ASE Group** **Email: mark.gerber@aseus.com**	**Session Co-Chairs:** **Karsten Meier** **Technische Universität Dresden** **Email: karsten.meier@tu-dresden.de** **Suresh K. Sitaraman** **Georgia Institute of Technology** **Email: suresh.sitaraman@me.gatech.edu**
1. 1:30 PM - RF Characterization on Nb-Based Superconducting Silicon Interconnect Fabric for Future Large-Scale Quantum Applications Yu-Tao Yang, Haoxiang Ren, Su Kong Chong, Gang Qiu, Shu-Yun Ku, Yang Cheng, Chaowei Hu, Tiema Qian, Kuan-Neng Chen, Ni Ni, and Kang L. Wang – University of California, Los Angeles	***1. 1:30 PM - Demonstration of Flexible Encapsulation in Assembly Industry*** Chao-Wei Liu, Ming-Hung Chen, Tun-Ching Pi, Jen-Chieh Kao, and Yung-I Yeh – ASE Group	***1. 1:30 PM - Thermal Challenges and Design Considerations in Heterogeneous Integrated Through-Silicon-Interposer Platform with Flipped III-V HEMT Chiplets*** Haoran Chen, Teck Guan Lim, and Gongyue Tang – Institute of Microelectronics (IME), A*STAR
2. 1:55 PM - Development of Cu-Cu Side-by-Side Interconnection Using Controlled Electroless Cu Plating Yu-An Chen, Po-Shao Shih, Fu-Ling Chang, Simon Johannes Gräfner, Jeng-Hau Huang, Ching-Han Huang, and C. Robert Kao – National Taiwan University; Yung-Sheng Lin, Yun-Ching Hung, Chin-Li Kao, and David Tarng – ASE Group	***2. 1:55 PM - Stress Mitigation in Large Area Organic-Inorganic Assemblies*** Randall Irwin, Emily MacInnis, Dharani Yakkaluru, and Subramanian S. Iyer – University of California, Los Angeles	***2. 1:55 PM - Assessment of Thermal-Aware Floorplans in a 3D IC for Server Applications*** Ki Wook Jung, Sungeun Jo, Minwoo Cho, Seunggeol Ryu, Sunggu Kang, Jaechoon Kim, and Dan (Kyung Suk) Oh – Samsung Electronics Co., Ltd.
3. 2:20 PM - Design of Compact Microwave Multiplexer for RF Reflectometry Characterization of Silicon-Based Spin Qubits Vignesh Shanmugam Bhaskar and Mihai Dragos Rotaru – Institute of Microelectronics (IME), A*STAR	***3. 2:20 PM - 10µm Pitch Bumping of Singulated Die Using a Temporary Metal-Embedded Chip Assembly Process*** Souheil Nadri, B.-A. Clayton Tu, Florian Herrault, Courtney Wilt, Partia Naghibi, Marko Pavlov, Joel Wong, and Vu Phan – HRL Laboratories, LLC	***3. 2:20 PM - Effect of Storage on Reliability of Thin-Flexible Laminated and Unlaminated Batteries in Wearable Applications*** Pradeep Lall and Ved Soni – Auburn University
Refreshment Break: 2:45–3:30 p.m.		
4. 3:30 PM - Small Package Size Low Power CMOS Image Sensor Using Two Different Type Small Through Silicon Vias Technology for 3D Packaging Hoi-Jin Lee, Heeseok Lee, and Kyunghwan Lee – Samsung Electronics Co., Ltd.	***4. 3:30 PM - Realization of High A/R and Fine Pitch Cu Pillars Incorporating High Speed Electroplating with Novel Strip Process*** Se-Chul Park, Jong-Ho Park, Seonghoon Bae, Jun-young Park, Taehwa Jeong, Hyojin Yun, Kwangok Jeong, Seokbong Park, Ju-il Choi, Un-Byoung Kang, and Dongwoo Kang – Samsung Electronics Co., Ltd.	***4. 3:30 PM - Modeling and Design for System-Level Reliability and Warpage Mitigation of Large 2.5D Glass BGA Packages*** Vidya Jayaram, Omkar Gupte, and Vanessa Smet – Georgia Institute of Technology
5. 3:55 PM - Stability Analysis of Nanoscale Copper-Carbon Hybrid Interconnects Bhawana Kumari and Manodipan Sahoo – Indian Institute of Technology Dhanbad; Rohit Sharma – Indian Institute of Technology Ropar	***5. 3:55 PM - High Density Thin Film Flex Technology for Advanced Packaging Applications*** Kai Zoschke, Hermann Oppermann, Markus Wöhrmann, Christine Kallmayer, Christian Tschoban, Kevin Kröhnert, Christina Lopper, Danny Jaeger, Mario Lutz, and Olaf Wünsch – Fraunhofer IZM	***5. 3:55 PM - Effective Computational Models for Addressing Asymmetric Warping of Fan-Out Reconstituted Wafer Packaging*** Yu-Chin Lee, Chia-Yu Chen, and Kuo-Shen Chen – National Cheng-Kung University; Jen-Hsien Wong, Wei-Hong Lai, Tang-Yuan Chen, Dao-Long Chen, and David Tarng – ASE Group
6. 4:20 PM - Functional Testing of AI Cores Through Thinned 3D I/O Buffer Dies in 3D Die-Stacked Modules Mukta Farooq, Arvind Kumar, Saekyu Lee, Ravi Bonam, Juan Gomez, James Kelly, Kohji Hosokawa, Akiyo Nomura, Yasuteru Kohda, Timothy Dickson, and Katsuyuki Sakuma – IBM Corporation	***6. 4:20 PM - 300mm Full Thickness Si Based IC Singulation Using Plasma Dicing for Advanced Packaging Technologies*** Rajesh Surapaneni, Julia Chiu, Brad Hamlin, and Xavier Brun – Intel Corporation; Richard Barnett, Matthew Muggeridge, Hannah Bhaskar and N. Richards – KLA Corporation	***6. 4:20 PM - Warpage and RDL Stress Analysis in Large Fan-Out Package with Multi-chiplet Integration*** Jen-Hsien Wong, NanYi Wu, Wei-Hong Lai, Chung-Hao Chen, Yi-Hsien Wu, Tang-Yuan Chen, Teck Chong Lee, Chin-Li Kao, and C.P. Hung – ASE Group
7. 4:45 PM - Exploring the Impact of Parametric Variability on Eye Diagram of On-Chip Multi-Walled Carbon Nanotube Interconnects Using Fast Machine Learning Techniques Km Dimple, Surila Guglani, Rahul Kumar, Sourajeet Roy, and Brajesh Kumar Kaushik – Indian Institute of Technology Roorkee; Suyash Kushwaha and Rohit Sharma – Indian Institute of Technology Ropar	***7. 4:45 PM - Investigation of Low-k WLCSP Die Strength Impact Induced by Singulation Process*** C. C. Chen, Y. S. Wu, K. H. Chen, W. S. Tseng, P. H. Tsao, and S. T. Leu – Taiwan Semiconductor Manufacturing Company, Ltd.	***7. 4:45 PM - The Optimal Solution of Fan-Out Embedded Bridge (FO-EB) Package Evaluation during the Process and Reliability Test*** David Lai and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.

Program Sessions: Friday, June 3, 8:00-11:40 a.m.

Session 25: Advancements in 2.5D and 3D Packaging Technology

Committee: Packaging Technologies

Session Co-Chairs:
John Knickerbocker
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1. 8:00 AM - A Study on Memory Stack Process by Hybrid Copper Bonding (HCB) Technology
Sanghoon Lee, Youngkun Jee, SangCheon Park, Soohwan Lee, Bohee Hwang, Gyeongjae Jo, Chungsun Lee, Jeomyoung Park, Unbyoung Kang, and Jongho Lee – Samsung Electronics Co., Ltd

2. 8:25 AM - High Performance and Energy Efficient Computing with Advanced SoICTM Scaling
S. W. Liang, Gene C. Y. Wu, K. C. Yee, C. T. Wang, Ji James Cui, and Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

3. 8:50 AM - Investigation of Moisture-Induced Warpage of Chip-on-Wafer in 2.5D IC Package
Shuai Shao, Yi-Ting Chen, Shih-Yen Chen, Ken Lee, Shin Low, and Inderjit Singh – Xilinx, Inc.

4. 10:00 AM - 3D Packaging for Heterogeneous Integration
Rahul Agarwal, Patrick Cheng, Priyal Shah, Brett Wilkerson, Raja Swaminathan, and John Wuu – Advanced Micro Devices, Inc.

5. 10:25 AM - Low Temperature Backside Damascene Processing on Temporary Carrier Wafer Targeting 7µm and 5µm Pitch Microbumps for N Equal and Greater Than 2 Die to Wafer TCB Stacking
Jaber Derakhshandeh, Eric Beyne, Gerald Beyer, Giovanni Capuz, Vladimir Cherman, Inge De Preter, Carine Gerets, Ehsan Shafahian, Koen Kennes, Geraldine Jamieson, and Tom Cochet – Imec

6. 10:50 AM - Demonstration of a Glass-Based 3D Package Architecture with Embedded Dies for High-Performance Computing
Siddharth Ravichandran, Vanessa Smet, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology

7. 11:15 AM - 3DIC Stacking Process Investigation by Soldering Bonding Technology
Jay Li, Wei Jhen Chen, Joe Lin, Mu Hsuan Chan, Tank Lo, Bruce Xu, Liang Yih Hung, Nicholas Kao, Don Son Jiang, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.

Session 26: Soldered and Sintered Interconnections

Committee: Interconnections

Session Co-Chairs:
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Infineon Technologies
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Changqing Liu
Loughborough University
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1. 8:00 AM - Novel Ag Salt Paste for Large Area Cu-Cu Bonding in Low Temperature Low Pressure and Air Condition
Chuantong Chen, Bowen Zhang, and Katsuaki Suganuma – Osaka University; Takuya Sekiguchi – Toppan Forms Co., Ltd.

2. 8:25 AM - Bonding Properties of Cu Paste in Low Temperature Pressureless Processes
Satoshi Konno, Takashi Hattori, Shinichi Yamauchi, and Kei Anai – Mitsui Mining & Smelting Co., Ltd.

3. 8:50 AM - Tight-Pitched 10 µm-Width Solder Joints for c-2-c and c-2-w 3D-Integration in NCF Environment
M. Mariappan, H. Hashimoto, J. Bea, and T. Fukushima – Global INTegration Initiative; S. Fukuzumi and T. Shibata – Showa Denko Materials; M. Koyanagi – T-Micro

4. 10:00 AM - Influence of Micro-Voids in Flip Chip Bump on Electromigration Reliability
Kei Murayama and Kiyoshi Oi – Shinko Electric Industries Co., Ltd.; Kor Lee – Intel Corporation; Toshiaki Ono – Nordson ES; Sze Lim – Indium Corporation; Yvonne Yeo – IBM Corporation; Keith Sweatman Martell – Nippon Superior Co., Ltd.; Haruo Shimamo – National Institute of Advanced Industrial Science and Technology; Masahiro Tsuriya – iNEMI

5. 10:25 AM - Study of Failure and Microstructural Evolution in SAC Solder Interconnects Induced by AC Electromigration Condition
Yi Ram Kim, Allison Osmanson, and Choong-Un Kim – University of Texas at Arlington; Patrick Thompson and Qiao Chen – Texas Instruments

6. 10:50 AM - A Study on Warpage and Reflow Profile for Extreme Extension of Mass Reflow Bonding
Ji-won Shin, Dong-uk Kwon, Young Ja Kim, Young Min Lee, and Dong Woo Kang – Samsung Electronics Co., Ltd.; Haoxiang Ren, Krutikesh Sahoo, Yu-Pei Huang, Yutao Yang, Ankit Kuchhangi, and Subramanian S. Iyer – University of California, Los Angeles

7. 11:15 AM - Low Temperature Formation of SAC-SnBi BGA Interconnections Using Solid Liquid Inter-Diffusion (SLID)
Divya Taneja, Richard Langlois, Nicolas Boyer, and Eric Dalpe – IBM Corporation; David Danovitch and Malak Kanso – University of Sherbrooke

Session 27: Interconnection Reliability

Committee: Applied Reliability

Session Co-Chairs:
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Seung-Hyun Chae
SK Hynix
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1. 8:00 AM - Process-Reliability Relationships of SnBiAg and SnIn Solders for Component Attachment on Flexible Direct-Write Additive Circuits in Wearable Applications
Pradeep Lall and Jinesh Narangaparambil – Auburn University; Scott Miller – NextFlex National Manufacturing Institute

2. 8:25 AM - Interconnection Reliability of Mini LEDs for Display Applications
In-Seok Kye, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ki-Seok Jang, Yong-Sung Eom, and Kwang-Seong Choi – Electronics and Telecommunications Research Institute; Yong-Jun Oh – Hanbat National University

3. 8:50 AM - Study of Long-Term Solder Joint and Board-Level Reliability Performance of Thin Nickel Plating ENEPIG Laminate LGA Package
Seok Phyo Tchun, Joo Yeop Kim, and Arun Raj – Analog Devices

4. 10:00 AM - Thermal Cycling Induced Interconnect Stability Degradation Mechanism in Low Melting Temperature Solder Joints
Kendra Young – Portland State University; Raiyo Aspandiar and Satyajit Walwadkar – Intel Corporation; Nilesh Badwe – Indian Institute of Technology Kanpur; Young-Woo Lee – MK Electron; Tae-Kyu Lee – Cisco Systems, Inc.

5. 10:25 AM - Fabrication and Reliability Analysis of Quasi-Single Crystalline Cu Joints by Using Highly <111>-Oriented Nanotwinned Cu
Jia-Juen Ong, Dinh-Phuc Tran, You-Yi Lin, Po-Ning Hsu, and Chih Chen – National Yang Ming Chiao Tung University

6. 10:50 AM - A Comparative Study of the Thermomechanical Reliability of Fully Filled and Conformal Through Glass Via (TGV)
Ke Pan, Yangyang Lai, and Seungbae Park – Binghamton University; Chukwudi Okoro, Dhananjay Joshi, and Scott Pollard – Corning Corporation

7. 11:15 AM - Broadband Characterization of Polymers Under Reliability Stresses and Impact of Capping Layer
Nicolas Pantano, Emmanuel Chery, Maaike Op de Beeck, John Slabbekoorn, and Eric Beyne – Imec

Refreshment Break: 9:15-10:00 a.m.

Program Sessions: Friday, June 3, 8:00-11:40 a.m.

Session 28: Packaging Assembly: Solder, Sintering, and Thermal Interface Materials	Session 29: Materials and Processes for Fan-Out and Advanced Packaging	Session 30: High-Speed Challenges in Power and Signal Integrity
Committee: Materials & Processing joint with High-Speed, Wireless & Components	**Committee: Materials & Processing**	**Committee: RF, High-Speed Components & Systems**
Session Co-Chairs: **Zia Karim** **Yield Engineering Systems** **Email: zkarim@yieldengineering.com** **Mark Poliks** **Binghamton University** **Email: mpoliks@binghamton.edu**	**Session Co-Chairs:** **Tanja Braun** **Fraunhofer IZM** **Email: tanja.braun@izm.fraunhofer.de** **Praveen Pandojirao-S** **Johnson & Johnson** **Email: praveen@its.jnj.com**	**Session Co-Chairs:** **Amit Agrawal** **Microchip Technologies** **Email: amit.agrawal@microchip.com** **Chuei-Tang Wang** **Taiwan Semiconductor Manufacturing Company, Ltd.** **Email: ctwangm@tsmc.com**
1. 8:00 AM - High Thermal Graphite Thermal Interface Material (TIM) Solution Applied to Fan-Out Platform Pin-Jing Su, Dan Lin, Shane Lin, Xi-Zhang Xu, Rung Jeng Lin, Liang-Yih Hung, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.	***1. 8:00 AM - High Fluorescence Photosensitive Materials for AOI Inspection of Fan-Out Panel Level Package*** Kiseok Kim, Jinyoung Kim, Okseon Yoon, Seunghun Chae, Jihye Shim, and Sooryeon Kim – Samsung Electronics Co., Ltd.	***1. 8:00 AM - Novel Power Delivery Network Design and Pre-Silicon Validation Supporting Heterogeneous Dies on a Single Package*** Judy Amanor-Boadu, Rishik Bazaz and Priyanka Bakliw – Intel Corporation
2. 8:25 AM - Optimizing Reflowed Solder Thermal Interface Material (sTIMs) Processes for Emerging Heterogeneous Integrated Packages DaeWoon Lee, Bret Hable, David Heller, Robert Jarrett, Xike Zhao, and Thomas Nash – Heller Industries, Inc.; Ryan Mayberry and Andy Mackie – Indium Corporation	***2. 8:25 AM - Selective Epoxy Mold Compound Slurry for Advanced Packaging Technology*** Tri Widodo, Xavier Brun, and C. Noda – Intel Corporation; N. Tsunoda, Y. Ichige, S. Arata, S. Nomura, and S. Kondo – Showa Denko Materials Co., Ltd.	***2. 8:25 AM - Integration of Foundry MIM Capacitor and OSAT Fan-Out RDL for High Performance RF Filters*** Pao-Nan Lee, Yu-Chang Hsieh, Wei-Chu Hsu, and Chen-Chao Wang – ASE Group; Hung-Lun Lo, Chang Ho Li, Fan-Hsiu Huang, and James Lin – WIN Semiconductors Corp.
3. 8:50 AM - Large, High Conductivity Direct-Fill Copper Thermal Vias for High Power Devices Alfred Zinn, Nhi Ngo, Alex Capanzana, Hannah Zinn, and Randall Stoltenberg – Kuprion, Inc.	***3. 8:50 AM - Low Warpage Printable Liquid Mold Compound for Laser Direct Structuring*** Charlie (Chunlin) He, Ruud deWit, Jie Cao, Tim Champagne, Rose Guino, Tony Winster, Ramachandran Trichur, Mario Saliba, and Frank Song – Henkel Corporation; Florian Roick and Simon Heitmann – LPKF Laser & Electronics AG	***3. 8:50 AM - Optimization of 2.5D Organic Interposer Channel for Die and Chiplets*** Srikrishna Sitaraman, Steven Verhaverbeke, Samer Banna, Mukhles Sowwan, Liu Jiang, El Mehdi Bazizi, Blessy Alexander, and Buvna Ayyagari-Sangamalli – Applied Materials, Inc.
Refreshment Break: 9:15-10:00 a.m.		
4. 10:00 AM - Vacuum Fluxless Reflow Technology for Fine Pitch First Level Interconnect (FLI) Bumping Applications Yue Deng, Liang He, Hossein Madanipour, Jung Kyu Han, Gang Duan, and Rahul Manepalli – Intel Corporation; Xike Zhao, David Wright, Bret Halbe, Fred Tarazi, and Dror Trifon – Heller Industries, Inc.	***4. 10:00 AM - Large-Scale Production of Boron Nitride Nanosheets-Based Epoxy Nanocomposites with Ultrahigh Through-Plane Thermal Conductivity for Electronic Encapsulation*** Zhijian Sun, Michael Yu, Jiaxiong Li, Macleary Moran, Mohanalingam Kathaperumal, Kyoung-Sik Moon, Madhavan Swaminathan, and Chi-Ping Wong – Georgia Institute of Technology	***4. 10:00 AM - Reference Clock Assessment Techniques for PCIe Gen5 and Beyond*** Matt Doyle, Matteo Cocchini, Layne Berge, Dale Becker, Matteo Cocchini, and Jason Bjorgaard – IBM Corporation
5. 10:25 AM - Thermal Performance of Advanced Thermal Interface Materials for High Power Flip Chip Lidded Ball Grid Array (FCLBGA) YoungJoon Koh, SangHyuk Kim, EunSook Sohn, and JinYoung Khim – Amkor Technology	***5. 10:25 AM - Photonic Debond: Scalability and Advancements*** Luke Prenger, Xavier Martinez, and Andrea Chacko – Brewer Science, Inc.; Vikram Turkani, Lauren Reimnitz, Vahid Akhavan, and Kurt Schroder – NovaCentrix	***5. 10:25 AM - Co-Design and Signal-Power Integrity/EMI Co-Analysis of a Switchable High-Speed Inter-Chiplet Serial Link on an Active Interposer*** Min Miao, Xiaolong Duan, Liang Sun, Tao Li, Shiliang Zhu, Zhuanzhuan Zhang, Jin Li, Danya Zhang, Hao Wen, Xuena Liu, and Zhensong Li – Beijing Information Science & Technology University
6. 10:50 AM - Non-Oil Bleed Thermal Gap Fillers for Long-Term Reliability of Solid State Drive Vigneshwarram Kumaresan and Mutharasu Devarajan – Western Digital	***6. 10:50 AM - A Novel Method of Low Temperature, Pressureless Interconnection for Wafer Level Scale 3D Packaging*** Po-Shao Shih, Yu-An Chen, Simon Johannes Gräfner, Jeng-Hau Huang, Ching-Han Huang, and C. Robert Kao – National Taiwan University	***6. 10:50 AM - Fast Channel Analysis and Design Approach Using Deep Learning Algorithm for 112Gbs HSI Signal Routing Optimization*** Sodam Han, Sungwook Moon, Seungki Nam, Jiyoung Park, Sangin You, and Jungil Son – Samsung Electronics Co., Ltd.
7. 11:15 AM - Printed Silver Micro-Pillars Embedded in a Phase Change Material Matrix for Thermal Management Applications Roberto Aga and Laura Davidson – KBR/AFRL; Carrie Bartsch and Emily Heckman – Air Force Research Laboratories	***7. 11:15 AM - Cracking-Less Heat-Resistant Electroless Ni-P Plating Film for Wide Bandgap Power Modules*** Ming-chun Hsieh, Chuantong Chen, Aiji Suetake, Zheng Zhang, and Katsuaki Suganuma – Osaka University; Ryuji Saito, Norihiko Hasegawa, Kei Hashizume, and Kuniaki Otsuka – Okuno Chemical Industries Co., Ltd.	***7. 11:15 AM - Package Design and Measurements for Radar Emulator Using Accelerators and Photonics*** Mercy Daniel-Aguebor, Mutee Ur Rehman, Serhat Erdogan, Kyoung-sik Moon, Nikita Ambasana, Saibal Mukhopadhya, and Madhavan Swaminathan – Georgia Institute of Technology; Liang Yuan Dai, Keren Bergman, Daniel Jang, and Mingoo Seok – Columbia University

Program Sessions: Friday, June 3, 1:30-5:10 p.m.

Session 31: Fan-Out Packaging Technologies and Applications	Session 32: Advanced Interconnect and Wire Bond Technologies for Flexible Device Applications	Session 33: Advanced Reliability Modeling and Characterization
Committee: Packaging Technologies	**Committee: Interconnections joint with Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Sam Karikalan** **Broadcom Inc.** **Email: sam.karikalan@broadcom.com** **Kuo-Chung Yee** **Taiwan Semiconductor Manufacturing Corporation, Ltd.** **Email: kcyee@tsmc.com**	**Session Co-Chairs:** **Ho-Young Son** **SK Hynix** **Email: hoyoung.son@sk.com** **Matthew Yao** **General Electric** **Email: matthew.yao@ge.com**	**Session Co-Chairs:** **Wei Wang** **Qualcomm Technologies, Inc.** **Email: wwang@g.clemson.edu** **Tz-Cheng Chiu** **National Cheng Kung University** **Email: tcchiu@mail.ncku.edu.tw**
1. 1:30 PM - Fan-Out Wafer Level Package for Memory Applications Ho-Young Son, Ki-Jun Sung, Bok-Kyu Choi, Jong-Hoon Kim, and Kangwook Lee – SK Hynix	***1. 1:30 PM - Infrared Curing of Flip Chip Electrically Conductive Adhesive (ECA) Interconnections*** Romaric Kabre and David Danovitch – University of Sherbrooke; Valerie Oberson and Magali Côté – IBM Corporation	***1. 1:30 PM - In-Situ Monitoring of Thermo-Mechanical Induced Stresses in Electronic Control Unit – from the Assembly to Use in the Field*** Przemyslaw Gromala, Daniel Riegel, Georg Konstantin, and Alexander Kabakchiev – Robert Bosch GmbH
2. 1:55 PM - Substrate Silicon Wafer Integrated Fan-Out Technology (S-SWIFT) Packaging with Fine Pitch Embedded Trace RDL SangHyun Jin, WonChul Do, JinSuk Seong, HyunGoo Cha, YunKyung Jeong, and JinYoung Khim – Amkor Technology	***2. 1:55 PM - Room-Temperature Cu Direct Bonding Technology Enabling 3D Integration with Micro-LEDs*** Yuki Susumago, Shunsuke Arayama, Tadaaki Hoshi, Hisashi Kino, Tetsu Tanaka, and Takafumi Fukushima – Tohoku University	***2. 1:55 PM - Reliability Challenges of High-Density Fan-Out Packaging for High-Performance Computing Applications*** Laurene Yip, Charles Lai, Rosa Lin, and Cooper Peng – MediaTek, Inc.
3. 2:20 PM - Advanced Fan-Out Packaging Technology for Hybrid Substrate Integration Lihong Cao, Teck Chong Lee, Rick Chen, Yung-Shun Chang, Hsingfu Lu, Nicholas Chao, Yen-Liang Huang, Chen-Chao Wang, and Chih-Yi Huang – ASE Group	***3. 2:20 PM - Ag to Ag Direct Bonding Via a Pressureless, Low-Temperature, and Atmospheric Stress Migration Bonding Method for 3D Integration Packaging*** Zheng Zhang, Aiji Suetake, Ming-Chun Hsieh, Chuantong Chen, Hiroshi Yoshida, and Katsuaki Suganuma – Osaka University	***3. 2:20 PM - A Comprehensive Study of Crack Initiation and Delamination Propagation at the Cu/Polyimide Interface in Fan-Out Wafer Level Package during Reflow Process*** Hong-Guang Wang, Guang-Chao Lyu, Yun-Kai Deng, Wei-Lin Hu, Bing-Xian Yang, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - Advanced Chip Last Process Integration for Fan-Out Wafer Level Packaging (WLP) Taewon Yoo, Seok Hyun Lee, Kyoung Lim Suk, Eung Kyu Kim, Won Kyoung Choi, Dae-Woo Kim, and Dong Wook Kim – Samsung Electronics Co., Ltd.	***4. 3:30 PM - Plating and Recrystallization of Galvanic Cu Films on Roll Annealed and Polycrystalline Cu Foils and the Effect of Intermediate Electroless Cu Layers*** Tobias Bernhard, R. Massey, Zhiou Li, Joerg-F. Schulze, Kilian Klaeden, Sebastian Zarwell, E. Steinhaeuser, and F. Bruening – Atotech Deutschland GmbH	***4. 3:30 PM - Observation of Fatigue and Creep Ratcheting Failure in Solder Joints Under Pulsed Direct Current Electromigration Testing*** Allison Osmanson, Yi Ram Kim, and Choong-Un Kim – University of Texas at Arlington; Patrick Thompson, Qiao Chen, and Sylvester Ankamah-Kusi – Texas Instruments
5. 3:55 PM - Development of Two-Tier FO-WLP AiPs for Automotive Radar Application Soon Wee Ho, Hsiang-Yao Hsiao, Boon Long Lau, Sharon Pei Siang Lim, Teck Guan Lim, and Tai Chong Chai – Institute of Microelectronics (IME), A*STAR	***5. 3:55 PM - Evaluation of an Anisotropic Conductive Epoxy for Interconnecting Highly Stretchable Conductors to Various Surfaces*** Riadh Al-Haidari, Behnam Garakani, Mohammed Alhendi, Udara Somarathna, and Mark Poliks – Binghamton University; Christopher Tabor and Michelle Yuen – Air Force Research Laboratory; Madhu Stemmermann – SunRay Scientific, Inc.; Nancy Stoffel – General Electric	***5. 3:55 PM - Evolution of SAC305 Mechanical Behavior Due to Damage Accumulation During Cycling*** Mohammad Ashraful Haq, Mohd Aminul Hoque, Golam Rakib Mazumder, Jeffrey C. Suhling, and Pradeep Lall – Auburn University
6. 4:20 PM - Chip-Last FOWLP Based Antenna-in-Package (FO-AiP) for 5G mmWave Application Klaus Ahn, Jade Park, Bruce Lee, Lewis Kang, Jay Kim, Kyeongrok Shin, Sung Hyuk Kim, Jea-Duck Lee, and Myoung Kee Kim – nepes Corporation; Ho-Seon Lee and Byeong-Gyu Park – RFcore, Ltd.	***6. 4:20 PM – Laser Soldered Wire Bonding on Liquid Printed and Sputtered Contact Structures on Thin-Flexes and Injection Molded Devices*** Matthias Fettke, Andrej Kolbasow, Timo Kubsch, and Thorsten Teutsch – PacTech Packaging Technologies GmbH; Tobias Seifert, Franz Selbmann, Frank Roscher, Kerstin Kreyssig, and Mario Baum – Fraunhofer Institute for Electronic Nano Systems ENAS; Soumya Deep Paul - Center for Microtechnologies, Technische Universität Chemnitz	***6. 4:20 PM - Board-Level Solder Joint Reliability of QFN Packages with Enclosure and Placement Effects in Various Form Factors*** Chun-Sean Lau, Ahmad Faridzul Hilmi, Ning Ye, and Yang Bo – Western Digital Corporation
7. 4:45 PM - A Heterogeneously Integrated and Flexible Inorganic Micro-Display on FlexTRATE(TM) Using Fan-Out Wafer-Level Packaging and Color Conversion Layers Henry Sun, Goutham Ezhilarasu, Guangqi Ouyang, Randall Irwin, and Subramanian S. Iyer – University of California, Los Angeles	***7. 4:45 PM - Cu/Co Metaconductor Based Highly Energy-Efficient Bonding Wires for Next Generation Millimeter Wave Electronic Interconnects*** Saeyeong Jeon, Hae-In Kim, Woosol Lee, and Yong-Kyu Yoon – University of Florida	***7. 4:45 PM - Shape Dependency of Fatigue Life in Solder Joints of Chip Resistors*** Jonghwan Ha, Chongyang Cai, Pengcheng Yin, Yangyang Lai, Ke Pan, Junbo Yang, and Seungbae Park – Binghamton University

Program Sessions: Friday, June 3, 1:30-5:10 p.m.

Session 34: Processing Enhancements in Fan-Out and Heterogeneous Integration	Session 35: Packaging with Additive Manufacturing for Harsh Conditions	Session 36: Modeling and Characterization of Interfaces and Interconnects
Committee: Materials & Processing joint with Applied Reliability	**Committee: Emerging Technologies**	**Committee: Thermal/Mechanical Simulation & Characterization**
Session Co-Chairs: **Qianwen Chen** **IBM Corporation** **Email: chenq@us.ibm.com** **Jae Kyu Cho** **GlobalFoundries** **Email: jaekyu.cho@globalfoundries.com**	**Session Co-Chairs:** **Rohit Sharma** **IIT Ropar** **Email: rohit@iitrpr.ac.in** **Benson Chan** **Binghamton University** **Email: chanb@binghamton.edu**	**Session Co-Chairs:** **Tieyu Zheng** **Microsoft Corporation** **Email: tizheng@microsoft.com** **Xuejun Fan** **Lamar University** **Email: xuejun.fan@lamar.edu**
1. 1:30 PM - Optimization of Temporary Carrier Technology for HDFO Packaging JinKun Yoo, DooWon Lee, KiYeul Yang, Ji Hyun Kim, WonChul Do, and Jin Young Khim – Amkor Technology	***1. 1:30 PM - High Temperature Die Interconnection Approaches*** Firas Alshatnawi, Mohammed Alhendi, Rajesh Sivasubramony, Riadh Al-Haidari, El Mehdi Abbara, Udara Somarathna, Mark Poliks, and Peter Borgesen – Binghamton University; David Shaddock, Nancy Stoffel, and Cathleen Hoel – General Electric	***1. 1:30 PM - Sustained High Temperature Fracture Toughness Evolution of Chip-UF and Substrate-UF Interfaces in FCBGAs for Automotive Applications*** Pradeep Lall, Padmanava Choudhury, and Aathi Pandurangan – Auburn University
2. 1:55 PM - Optimization of PI & PBO Layers Lithography Process for High Density Fan-Out Wafer Level Packaging & Next Generation Heterogeneous Integration Applications Employing Digitally Driven Maskless Lithography Thomas Uhrmann, Boris Povazay, Tobias Zenger, Bernd Thallner, Roman Holly, and Bozena Matuskova Lednicka – EV Group; Mario Reybrouck, Niels Van Herck, Bart Persijn, Dimitri Janssen, and Stefan Vanclooster – FUJIFILM Electronic Materials N.V.	***2. 1:55 PM - 3D Cryogenic Interposer for Quantum Computing Application*** Hongyu Li, Norhanani Jaafar, and King-Jien Chui – Institute of Microelectronics (IME), A*STAR; Aaron Chit Siong Lau, Rainer Cheow Siong Lee, Calvin Pei Yu Wong, and Kuan Eng Johnson Goh – Institute of Materials Research and Engineering (IMRE), A*STAR	***2. 1:55 PM - Nonlinear Finite Element Analysis of an Automotive High-Power Module Under Impact Loading*** Liangbiao Chen, Yong Liu, Alex Yao, Sam Lin, and CH Chew – ON Semiconductor
3. 2:20 PM - Analysis of Pattern Distortion by Panel Deformation and Addressing it by Using Extremely Large Exposure Field Fine-Resolution Lithography John Chang, James Webb, Corey Shay, and Timothy Chang – Onto Innovation	***3. 2:20 PM - Flexible Metamaterial Lens for Magnetic Field and Signal-to-Noise Ratio Improvements in 1.5 T and 3 T Magnetic Resonance Imaging*** Woosol Lee, Marcelo Febo, and Yong-Kyu Yoon – University of Florida; Josh Lane – Texas Instrument	***3. 2:20 PM - Magnetic-Based Interfacial Adhesion Measurement Technique with Environmental Conditions*** Rui Chen and Suresh Sitaraman – Georgia Institute of Technology; Nicholas Ginga – University of Alabama in Huntsville
Refreshment Break: 2:45-3:30 p.m.		
4. 3:30 PM - Solutions to Overcome Warpage and Voiding Challenges in Fan-Out Wafer-Level Packaging Vidya Jayaram, Vipul Mehta, Yiqun Bai, and John C. Decker – Intel Corporation	***4. 3:30 PM - Self-Healing of Interconnect Cracks for Reliable and Defect-Free Smart Manufacturing of Flexible Packages*** Akeeb Hassan, Asahi Tomitaka, Reshmi Banerjee, and P. Markondeya Raj – Florida International University	***4. 3:30 PM - Fracture Simulation of Redistribution Layer in Fan-Out Wafer-Level Package Based on Fatigue Crack Growth Characteristics of Insulating Polymer*** Koichi Nagase and Atsushi Fujii – Asahi Kasei Corporation; Kaiwen Zhong and Yoshiharu Kariya – Shibaura Institute of Technology
5. 3:55 PM - Dry Etch Processing in Fan-Out Panel-Level Packaging – An Application for High-Density Vertical Interconnects and Beyond Friedrich-Leonhard Schein, Christian Voigt, and Lutz Gerhold – Technische Universität Berlin; Ioannis Tsigaras, Mohamed Elghazzali, Hirofumi Sawamoto, Ewald Strolz, and Roland Rettenmeier – Evatec AG; Ruben Kahle and Lars Böttcher – Fraunhofer IZM	***5. 3:55 PM - Additively Manufactured RF GRIN Lenses For Highly Directive, Low Power Transmitters*** Jonathon Copley, Hatem Elbidweihy, and Connor S. Smith – United States Naval Academy; Christopher R. Milligan and Nam Nicholas Mai – Department of Defense	***5. 3:55 PM - Development on Fatigue Life Model of Lead-Free Solder for First Failure Prediction*** Faxing Che, Yeow Chon Ong, Hong Wan Ng, Ling Pan, Christopher Glancey, Koustav Sinha and Richard Fan – Micron Technology, Inc.
6. 4:20 PM - Fabrication, Characterization and Electromechanical Reliability of Stretchable Circuitry for Health Monitoring Systems Behnam Garakani, Udara Somarathna, Riadh Alheydari, Firas Alshatnawi, Detlef-M. Smilgies, and Mark D. Poliks – Binghamton University	***6. 4:20 PM - A Low Profile Two-Phase Immersion Cooling Stack-up based on Detachable Boiling Enhancement Layer on Lidded Electronic Packages*** Jimmy Chuang, Y. L. Li, Jin Yang and David Shia – Intel Corporation	***6. 4:20 PM - An Extensive Simulation Study of the Interfacial Delamination in Molded Underfill Flip-Chip Packages by Finite Element Method Based on Virtual Crack Closure Technique*** Guang-Chao Lyu, Hong-Guang Wang, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology
7. 4:45 PM - Buried Power Rails and Nano-Scale TSV: Technology Boosters for Backside Power Delivery Network and 3D Heterogeneous Integration Anne Jourdain, Michele Stucchi, Geert Van der Plas, Gerald Beyer, and Eric Beyne – Imec	***7. 4:45 PM - Ultraprecise Deposition of Micrometer-Size Conductive Features for Advanced Packaging*** Aneta Wiatrowska, Piotr Kowalczewski, Karolina Fiaczyk, Lukasz Witczak, Jolanta Gadzalinska, Mateusz Lysien, Ludovic Schneider, and Filip Granek – XTPL SA	***7. 4:45 PM - Mechanical Simulation and Modeling for Reliability of 6-in-1 Power Module*** Rathin Mandal, Kazunori Yamamoto, and Gongyue Tang – Institute of Microelectronics (IME), A*STAR

Interactive Presentations: Wednesday, June 1, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

Wednesday, June 1, 2022

Session 37: Interactive Presentations 1
Time: 9:00 AM – 11:00 AM

Committee: Interactive Presentations

Session Co-Chairs:
Mark Eblen
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Jeffrey Lee
iST-Integrated Service Technology, Inc.
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Kuo-Ning Chiang
National Tsinghua University
Email: knchiang@pme.nthu.edu.tw

1. The Effect of Thermal Stress on Reliability of Printed Vias on Flexible Substrates
Udara Somarathna, Mohammed Alhendi, and Mark Poliks – Binghamton University; Darshana Weerawarne – University of Colombo; Joseph Iannotti, Christopher J. Kapusta, and Nancy Stoffel – General Electric; Stephen G. Gonya – Lockheed Martin

2. Mechanical Property Evolution in SAC+Bi Lead Free Solders Subjected to Various Thermal Exposure Profiles
Mohammad Al Ahsan, S M Kamrul Hasan, Mohammad Ashraful Haq, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

3. Extreme Low-Temperature High Strain-Rate Constitutive Behavior Evolution of Doped and Undoped Lead Free Solders Under Sustained High Temperature Exposure
Pradeep Lall, Vishal Mehta, Vikas Yadav, Mrinmoy Saha, and Jeffrey C. Suhling – Auburn University; Dave Locker – US Army CCDC-AC

4. Effects of β-Sn Crystal Orientation on the Deformation Behavior of SAC305 Solder Joints
Debabrata Mondal, Mohammad Ashraful Haq, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

5. Reconstructing More Sinterable Surfaces for Copper Nanoparticles to Form High-Strength Cu-Cu Joints in Air Atmosphere
Yudui Zhang, Tao Zhao, Pengli Zhu, Rong Sun, and Liang Xu – Shenzhen Institute of Advanced Electronic Materials; Chuncheng Wang and Yue Yao – Osaka University

6. Two/Multi-Photon Imaging for Characterization of Fine Line Features and Microvias in Advanced Packaging
Mohanalingam Kathaperumal, Pragna Bhaskar, Christopher Blancher, Pratik Nimbalkar, Fuhan Liu, and Madhavan Swaminathan – Georgia Institute of Technology; Bai Nie – Intel Corporation

7. Development of Advanced Liquid Cooling Solution on Data Centre Cooling
Xiaowu Zhang, Yong Han, Gongyue Tang, Haoran Chen, and Boon Long Lau – Institute of Microelectronics (IME), A*STAR

8. The Effects of Bi Doping and Aging on Viscoplasticity of Sn-Ag-Cu-Bi alloys
Vishnu Shukla, Nicholas Ayers, Andrea Moreno, Natalie Crutchfield, Devin Lyons, and Tengfei Jiang – University of Central Florida; Omar Ahmed, Peng Su, and Bernard Glasauer – Juniper Networks

9. Numerical Simulation of Cu/Polymer-Dielectric Hybrid Bonding Process Using Finite Element Analysis
Sasi Kumar Tippabhotla, Lin Ji, and Yong Han – Institute of Microelectronics (IME), A*STAR

10. Investigating Moisture Diffusion in Mold Compounds (MCs) for Fan-Out-Wafer-Level-Packaging (FOWLP)
Abdellah Salahouelhadj, Mario Gonzalez, Arnita Podpod, and Eric Beyne – Imec

11. Mechanical and Thermal Characterization Analysis of Chip-Last Fan-Out Chip on Substrate
Weijie Yin, Wei-Hong Lai, Ying-Xu Lu, KarenYU Chen, Hung-Hsien Huang, Tang-Yuan Chen, Chin-Li Kao, and CP Hung – ASE Group

12. Low Cost Copper Based Sintered Interconnect Material for Optoelectronics Packaging
Sri Krishna Bhogaraju, Maximilian Schmid, E Liu, Rodolfo Saccon, Gordon Elger, Klaus Müller, and Georg Pirzer – Institute of Innovative Mobility; Holger Klassen – Osram Opto Semiconductors GmbH

13. Anisotropy of Curing Residual Stress of Underfill in the Encapsulation Under Three-Dimensionally Constrained Condition Based on In-Situ Characterization
Tao Peng, Xiaohui Peng, Wenjie Wu, Liang Peng, Gang Li, Jingbao Yang, Yuanyuan Yang, Jing Chen, CaiPing Zhu, Pengli Zhu, and Rong Sun – Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences

14. Study of Small Polyimide Open Size in Contact Resistance and Reliability for Flip Chip Cu Pillar Package
Kuei Hsiao Kuo, Shaun Xiao, Abram Hwang, Kui Chang, Jovi Chang, and Feng Lung Chien – Siliconware Precision Industries Co., Ltd.

15. Package Design Through Reliable Predictive Modeling and Its Validation
Pengcheng Yin and Seungbae Park – Binghamton University; Biju Jacob, Liang Yin, and Arun Gowda – General Electric

16. Thermo-Mechanical Reworkable Epoxy Underfill in Board-Level Package: Material Characteristics and Reliability Criteria
Lip Teng Saw and Mutharasu Devarajan – Western Digital

17. Block Thermal Model for High Power Lidded Packages
Daijiao Wang and Sam Karikalan – Broadcom, Inc.

18. A Parameter Study for the Design Optimization to Relieve Pattern Stress of PCB Under the Temperature Cycling Condition
Hyunggyun Noh, Kyungwoo Lee, Jinsu Bae, Yuchul Hwang, Hoosung Kim, and Sangwoo Pae – Samsung Electronics Co., Ltd.

19. Characterization and Reliability of a High Bandwidth, High Frequency Flexible Connector for Signal Delivery
Randall Irwin and Subramanian S. Iyer – University of California, Los Angeles

20. Investigation of Reflow Effect and Empirical Lifetime Modeling on the Board Level Solder Joint Reliability
Kwangwon Seo, Keunho Rhew, Choongpyo Jeon, Youngsung Choi, Jinsoo Bae, Hoosung Kim, and Sangwoo Pae – Samsung Electronics Co., Ltd.

21. Finite Element Influence Analysis of Power Module Design Options
Marius van Dijk and Olaf Wittler – Fraunhofer IZM; Ping-Chi Hung – Universal Scientific Industrial Co., Ltd.; Willy H. Lai, C. Y. Hsieh, and Thomas Wang – ASE Group; Martin Schneider-Ramelow – Technical University Berlin

22. Solder Joint Fatigue Studies Subjected to Board-Level Random Vibration for Automotive Applications
Valeriy Khaldarov and Alexander Shalumov – ASONIKA, LLC; Andy Zhang – Texas Instruments; Dongji Xie – Nvidia Corporation; Jeffrey Lee – iST-Integrated Service Technology; Xue Shi – Bosch Automotive Products; Romuald Roucou – NXP Semiconductors; Sushil Doranga – Lamar University

23. 2-D Fluid Simulation Approach for Miniwave Soldering
Reinhardt Seidel, Marcel Sippel, and Jörg Franke – FAPS, FAU Erlangen-Nürnberg

24. Component Level Reliability Evaluation of Low Cost 6-Sided Die Protection Versus Wafer Level Chip Scale Packaging with 350 µm Ball Pitch
Jacinta Aman Lim, Byung-Cheol Kim, Rizi Valencia-Gacho, and Brett Dunlap – nepes Corporation

25. Simulation of the Filler Stuck Mechanism in Molding Process and Verification
Tzu Chieh Chien, Shih Kun Lo, Yen Hua Kuo, Hui Chung Liu, Zong Yuan Li, Yi Nong Lin, Lu Ming Lai, and Kuang Hsiung Chen – ASE Group

26. Inlet/Outlet Induced Failures During Flip-Chip Bonding of Large Area Chip with Embedded Microchannels
Jianyu Du and Jiajie Kang – China University of Geosciences; Yuchi Yang, Han Xu, Deyin Zheng, Qi Wang, and Wei Wang – Institute of Microelectronics (IME), A*STAR; Huaiqiang Yu – Electronics Technology Group Corporation

Wednesday, June 1, 2022

Session 38: Interactive Presentations 2
Time: 2:00 PM – 4:00 PM

Committee: Interactive Presentations

Session Co-Chairs:
Pavel Roy Paladhi
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Amanpreet Kaur
Oakland University
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Saikat Mondal
Intel Corporation
Email: saikat.mondal@intel.com

1. Multi-Layers Chips on Wafer Stacking Technologies with Carbon Nano-Tubes as Through-Silicon Vias and Its Potential Applications for Power-Via technologies
Bo-Zhou Liao, Yi-Ting Tsai, Liang-Hsi Chen, Ting-Wei Chen, Kai-Cheng Chen, Yi-Cheng Chan, Hong-Yi Lin, Min-Hung Lee, and Ming-Han Liao, National Taiwan University

2. A De-Embedding and Embedding Procedure for High-Speed Channel Eye Diagram Oscilloscope Measurement
Zhaoqing Chen – IBM Corporation

3. Physics-Based Nested-ANN Approach for Fan-Out Wafer Level Package Reliability Prediction
Peilun Yao, Jun Yang, Yonglin Zhang, Xiaoshun Fan, Haibin Chen, Jinglei Yang, and Jingshen Wu – Hong Kong University of Science and Technology

4. A Fully Additive Approach for the Fabrication of Split-Ring Resonator Metasurfaces
Roghayeh Imani, Sarthak Acharya, Shailesh Chouhan, and Jerker Delsing – Luleå University of Technology

5. 60 GHz 0-360˚ Passive Analog Delay Line in Liquid Crystal Technology Based on a Novel Conductor-Backed Fully-Enclosed Coplanar Waveguide
Jinfeng Li – Imperial College London

6. Development of Smart Sensor Array Mat for Retail Inventory Management
Ruiqi Lim, Musafargani Sikkandhar, and Ming-Yuan Cheng – Institute of Microelectronics (IME), A*STAR

7. Modeling and Mitigating Fiber Weave Effect Using Layer Equivalent Model and Monte Carlo Method
Chin-Hsun Wang and Ruey-Beei Wu – National Taiwan University; Ming-Tsun Lu, Jun-Rui Huang, and Ching-Sheng Chen – Unimicron Technology Corporation

8. Die Floorplan and PKG Design Impacts on Power Integrity Performances of Multiple Blocks in a Single Power Domain
Jun So Pak, James Jeong, Taehoon Kim, Byung-Su Kim, Minkyu Kim, Jisoo Hwang, Serhoon Lee, and Heeseok Lee – Samsung Electronics Co., Ltd.

9. System Level Power Supply Induced Jitter Suppression for Multi-lane High Speed Serial Links
Goeun Kim, Doohee Lim, Tamal Das, Eunjung Lee, and Sangin You – Samsung Electronics Co., Ltd.

10. Heterogeneously Integrated Quantum Chip Interposer Packaging
Ramesh Kudalippalliyalil, Sujith Chandran, Akhilesh Jaiswal, and Ajey P. Jacob – University of Southern California; Kang L. Wang – University of California, Los Angeles

11. System-Level Verification of a Packaged Silicon Photonics-Based Transceiver
Yao Sun, Po Dong, Minhua Chen, Kejia Zheng, Changyi Li, Li Zhang, Wei Si, Shanshan Zeng - II-VI Shihuan Ran and Linjie Zhou - Shanghai Jiaotong University

12. A Novel Frequency Mixing Based Beam-Steering Phased Array for K-Band Applications
Yu Ping Liu and Amanpreet Kaur – Oakland University

13. Automated Detection and Segmentation of HBMs in 3D X-ray Images Using Semi-Supervised Deep Learning
Ramanpreet Pahwa, Richard Chang, Wang Jie, Xu Xun, Lile Cai, and Sheng Foo Chuan – I2R; David Ho Soon Wee, Chong Ser Choong, and Vempati Srinivasa Rao – Institute of Microelectronics (IME), A*STAR

14. Electrospray Printing of Polyimide Films for Electronics Packaging Applications
Bryce Kingsley, Emma Pawliczak, Thomas Hurley, and Paul Chiarot – Binghamton University

15. Addressing 5G NR Filter Challenges with Hybrid Technologies
Lijun Chen and Feng Ling – Xpeedic

16. Hybrid Lithography Approach for Single Mode Polymeric Waveguides and Out of Plane Coupling Mirror
David Weyers, Akash Mistry, Krzysztof Nieweglowski, and Karlheinz Bock – TU Dresden

17. Performance of Flexible Microwave Antenna Under Environmental Stress
Emuobosan Enakerakpo, Ashraf I. Umar, Mohammed Alhendi, Dylan Richmond, and Mark D. Poliks – Binghamton University; Tom Rovere and Stephen Gonya – Lockheed Martin

18. TSV-less Power Delivery for Wafer-Scale Interposers
Haoxiang Ren, Saptadeep Pal, Guangqi Ouyang, Randall Irwin, Yu-Tao Yang, and Subramanian S. Iyer – University of California, Los Angeles

19. Modeling the Effect of Surface Roughness for Screen-Printed Silver Ink on Flexible Substrates
Mohamed Abdelatty, Ashraf Umar, Gurvinder Khinda, Mohammed Alhendi, and Mark Poliks – Binghamton University

20. Modeling the Effect Trace Profiles on the RF Performance of Additively Manufactured Microstrip Transmission Lines on Polyimide Substrates
Ashraf Umar, Mohamed Y. Abdelatty, Gurvinder S. Khinda, Mohammed Alhendi, and Mark D. Poliks – Binghamton University

21. A Broadband High-Efficiency Charge Pump for Ambient RF Energy Harvesting - Powering Underground and Wearable RFID Based Sensors
Yihang Chu and Premjeet Chahal – Michigan State University

22. Modeling of Adaptive Receiver Performance Using Generative Adversarial Networks
Priyank Kashyap, Dror Baron, Chau-Wai Wong, Tianfu Wu, Chris Cheng, and Paul Franzon – North Carolina State University; Yongjin Choi and Sumon Dey – Hewlett Packard Enterprise

Thursday, June 2, 2022

Session 39: Interactive Presentations 3
Time: 9:00 AM – 11:00 AM

Committee: Interactive Presentations

Session Co-Chairs:
Pat Thompson
Texas Instruments, Inc.
Email: patrick.thompson@ti.com

Pradeep Lall
Auburn University
Email: lall@auburn.edu

Michael Mayer
University of Waterloo
Email: mmayer@uwaterloo.ca

1. The Investigation of Dry Plasma Technology in Each Step for the Fabrication of High Performance Redistribution Layer
Daisuke Hironiwa, Haw Wen Chen, Yasuhiro Morikawa, Takashi Kurimoto, and Ryuichiro Kamimura – ULVAC, Inc.

2. Chip Last Fan-Out Chip on Substrate (FOCoS) Solution for Chiplets Integration
Teck-Chong Lee, Shu-Han Yang, Hsin-Yi Wu, and Yun-Jun Lin – ASE Group

3. Die to Wafer Hybrid Bonding for Chiplet and Heterogeneous Integration: Die Size Effects Evaluation-Small Die Applications
Guilian Gao, Laura Mirkarimi, Gill Fountain, Dominik Suwito, Jeremy Theil, Thomas Workman, Cyprian Uzoh, Bongsub Lee, KM Bang, and Gabe Guevara – Xperi Corporation

4. Yield Improvement in Chip to Wafer Hybrid Bonding
Ser Choong Chong, Cereno Daniel Ismael, Pei Siang Lim, Cheng Yi Shim, Wai Song Lai, and Woon Leng Loh – Institute of Microelectronics (IME), A*STAR

5. Study of Parameter Tuning for the Curing Condition on ABF Type for Large FCBGA Package
Rick Ye, Eric Chen, Wen-Yu Teng, Andrew Kang, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.

6. Next Gen Laser-Assisted Bonding (LAB) Technology
SeokHo Na, MinHo Gim, ChoongHoe Kim, DongHyeon Park, DongSu Ryu, DongJoo Park, and JinYoung Khim – Amkor Technology

7. Swelling Analysis of Negative-tone Photosensitive Dielectric Materials for Fine Pitch Redistribution Layers
Daiki Yukimori, Go Inoue, Nobuhiro Ishikawa, and Toshiyuki Ogata – TAIYO HOLDINGS Co., Ltd.

8. RF Characterization in Range of 18GHz in Fan-Out Package Structure Molded by Epoxy Molding Compound with EMI Shielding Property
Eun Ha, Haksan Jeong, Kyung Deuk Min, Kyung-Yeol Kim, Dong-Gil Kang, and Seung-Boo Jung – Sungkyunkwan University

9. Plasma Chamber Environment Control to Enhance Bonding Strength for Wafer-to-Wafer Bonding Processing
Wooyoung Kim, Yongin Lee, Wonyoung Choi, Kyeongbin Lim, Bumki Moon, and Minwoo Rhee – Samsung Electronics Co., Ltd.

10. Study of Large Exposure Field Lithography for Advanced Chiplet Packaging
Hiromi Suda, Douglas Shelton, Hiroki Takada, Yoshio Goto, Kosuke Urushihara, and Ken-Ichiro Shindoa – CANON

11. Epoxy Resin with Metal Complex Additives for Improved Reliability of Epoxy-Copper Joint
Jiaxiong Li, John Wilson, Dylan Cheung, Zhijian Sun, Kyoung-sik Moon, Madhavan Swaminathan, and Ching-Ping Wong – Georgia Institute of Technology

12. Wirebonding Based 3-D SiC IC Stacks for High Temperature Applications
Feng Li and Srividya Raveendran – University of Idaho

13. Electrical Design and Modeling of Silicon Carbide Power Modules for Inverter Application
Vignesh Shanmugam Bhaskar, Jong Ming Chinq, Kazunori Yamamoto, and Gongyue Tang – Institute of Microelectronics (IME), A*STAR

14. Reliability of Component Attachment Using ECA and LTS on Flexible Additively Printed Ink-Jet Circuits for Signal-Filtering in Wearable Applications
Pradeep Lall, Kartik Goyal, and Jinesh Narangaparambil – Auburn University; Scott Miller – NextFlex National Manufacturing Institute

15. Micro-Spray with Silver Ink for Maskless Selective-Area EMI Shielding
Kisu Joo, Kyu Jae Lee, Jung Yoon Moon, Yoon-Hyun Kim, Jinhwan Chung, Se Young Jeong, and Seung Jae Lee – Ntrium, Inc.

16. Embedded-IC Package Using Si-Interposer for mmWave Applications
Hyun-Beom Lee and Jong-Min Yook – Korea Electronics Technology Institute; Young-Gon Kim and Wansik Kim – LIG Nex1 Corporation; Sosu Kim – Agency for Defense Development; Byung-Wook Min – Yonsei University

17. Carrier Systems for Collective Die-to-Wafer Bonding
Koen Kennes, Alain Phommahaxay, Samuel Suhard, Pieter Bex, Steven Brems, Xiao Liu, Sebastian Tussing, Gerald Beyer, and Eric Beyne – Imec; Alice Guerrero – Brewer Science, Inc.

18. Superb Sinterability of the Cu Paste Consisting of Bimodal Size Distribution Cu Nanoparticles for Low-Temperature and Pressureless Sintering of Large-Area Die Attachment and the Sintering Mechanism
Bin Hou, Hai-Jun Huang, Chun-Meng Wang, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

19. Reliability of Ag Bonding Wires and iCoated Variants from the Perspective of IMC Degradation and Correlation to Wire and Epoxy Molding Compound Material Properties Under Corrosive Environment
Randolph Flauta, April Joy Garete, Mark Luke Farrugia, and Sreetharan Sekaran – Nexperia; Haibin Chen – Hong Kong University of Science and Technology

20. Design and Simulation to Reduce the Crosstalk of Ultra-Fine Line Width/Space in the Redistribution Layer(RDL)
Ziyu Liu, Lin Chen, and Qingqing Sun – Fudan University; Long Bai and Ziyuan Zhu – Southwest University

21. Evolution of Interconnect EDA for Chiplets and Heterogeneous Integration
Craig Bishop – Deca Technologies

22. Evaluation of High Melting Temperature Lead-Free Solder for Clip Bonding Assembly of MOSFET Loss Free Package
Fred Fuliang Le, Joseph Daniel Perez, Wing Onn Chaw, Alex Yap, Mark Luke Farrugia, and Yoon Kheong Leong – Nexperia; Zunyu Guan and Haibin Chen – Hong Kong University of Science and Technology

23. Influence of Tribo-Mechanical Characteristics of Advanced EN Coating for Electronic Packaging Enclosures
Muralidharan Sundararajan and Mutharasu Devarajan – Western Digital

24. Analysis on Optimal Chip Floorplanning Considering Various Types of Decoupling Capacitors in Package PDN
Jisoo Hwang, James Jeong, Heejung Choi, Jun So Pak, Heeseok Lee, Minkyu Mike Kim, and Ilryong Kim – Samsung Electronics Co., Ltd.

25. Novel Polymer Design for Ultra-Low Stress Dielectrics
Matthias Koch, Jens Pradella, and Gregor Larbig – Merck KGaA

Thursday, June 2, 2022

Session 40: Interactive Presentations 4
Time: 2:00 PM – 4:00 PM

Committee: Interactive Presentations

Session Co-Chairs:
Mark Poliks
Binghamton University
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Rao Bonda
Amkor Technology, Inc.
Email: rao.bonda@amkor.com

Kristina Young
GlobalFoundries
Email: Kristina.Young@globalfoundries.com

1. Ultra-High Conductivity Interconnects for 77K CMOS Using Heterogeneous Integration
Golam Sabbir and Subramanian S. Iyer – University of California, Los Angeles

2. Functional Demonstration of < 0.4 pJ/bit, 9.8 µm Fine-Pitch Dielet-to-Dielet Links for Advanced Packaging Using Silicon Interconnect Fabric
Krutikesh Sahoo, Uneeb Rathore, SivaChandra Jangam, Tri Nguyen, Dejan Markovic, and Subramanian S. Iyer – University of California, Los Angeles

3. Integration of High Performance GaN LEDs for Communication Systems and Smart Society
Zeinab Shaban, Mehrdad Saei, Brian Corbett, and Zhi Li – Tyndall National Institute

4. Low Temperature Metal-to-Metal Direct Bonding in Atmosphere Using Highly (111) Oriented Nanotwinned Silver Interconnects
Ching-Yao Cheng, Po-Hsien Wu, Leh-Ping Chang, and Fan-Yi Ouyang – National Tsing Hua University

5. Scalable through Mold Interconnection Realization for Advanced Fan Out Wafer Level Packaging Applications
Aurélia Plihon, Edouard Déschaseaux, Rémi Franiatte, Jérome Dechamp, Simon Vaudaine, Jennifer Guillaume, Catherine Brunet-Manquat, Stéphane Moreau, and Perceval Coudrain – CEA-LETI

6. A Hybrid Bonding Interconnection with a Novel Low Temperature Bonding Polymer System
Yu-Min Lin, Po-Chih Chang, Wei-Lan Chiu, Tao-Chih Chang, and Hsiang-Hung Chang – Industrial Technology Research Institute; Baron Huang, Chia-Hsin Lee, Mei Dong, and Duo Tsai – Brewer Science, Inc.; Chang-Chun Lee – National Tsing Hua University; Kuan-Neng Chen – National Yang Ming Chiao Tung University

7. Signal Integrity Design and Analysis with Link Budget Results of HBM2E Module on Latest High Density Organic Laminate
Frank Libsch, Hiroyuki Mori, and Xiaoxiong Gu – IBM Corporation

8. Chiplets Integrated Solution with FO-EB Package in HPC and Networking Application
Po Yuan (James) Su, David Ho, Jacy Pu, and Yu Po Wang – Siliconware Precision Industries Co., Ltd.

9. Effect of Isothermal Aging on the Properties of In-48Sn and In-Sn-8Cu Alloys
Duy Le Han, Hiroaki Tatsumi, Fupeng Huo, and Hiroshi Nishikawa – Osaka University

10. Ag Die-Attach Paste Modified by WC Additive for High-Temperature Stability Enhancement
Yang Liu, Chuantong Chen, Takuya Naoe, Hiroshi Nishikawa, and Katsuaki Suganuma – Osaka University; Minoru Ueshima and Takeshi Sakamoto – Daicel Corporation

11. PSI Design Solutions for High-Speed Die-to-Die Interface in Chiplet Applications
Taeyun Kim, Sungwook Moon, Chanmin Jo, Seungki Nam, and Yongho Lee – Samsung Electronics Co., Ltd.

12. Thermal Compression Cu-Cu Bonding Using Electroless Cu and the Evolution of Voids Within Bonding Interface
Ching-Han Huang, Po-Shao Shih, Jeng-Hau Huang, S.J. Gräfner, Yu-An Chen, and C. Robert Kao – National Taiwan University

13. Novel Zero Side-Etch Process for <1µm Package Redistribution Layers
Pratik Nimbalkar, Pragna Bhaskar, Christopher Blancher, Mohanalingam Kathaperumal, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology

14. Printed Microwave Connector
Jotham Kasule, Shokat GanjeheizadehRohani, Mark Pothier, Yuri Piro, Alkim Akyurtlu, and Craig Armiento – University of Massachusetts Lowell

15. MaxQFP - A High Density QFP
Chu-Chung Stephen Lee, TuAnh Tran, Andrew Mawer, Glenn Daves, X. S. Pang, and J. Z. Yao – NXP Semiconductors

16. Creep and Microstructure Evolutions in SAC305 Lead Free Solder Subjected to Different Thermal Exposure Profiles
S. M. Kamrul Hasan, Mohammad Al Ahsan, Jeffrey C. Suhling, Pradeep Lall, Abdullah Fahim, and K. M. Rafidh Hassan – Auburn University

17. Modeling of Cu-Cu Thermal Compression Bonding
Kai-Cheng Shie, Dinh-Phuc Tran, Hung-Che Liu, and Chih Chen – National Yang Ming Chiao Tung University; A. M. Gusak – Cherkasy National University; K. N. Tu – City University of Hong Kong

18. Mechanical Properties and Microstructures of Cu/In-48Sn Alloy/Cu with Low Temperature TLP Bonding
DongGil Kang, KyungDeuk Min, Kyung-Yeol Kim, HakSan Jeong, Eun Ha, and Seung-Boo Jung – Sungkyunkwan University

19. Novel Pressure-Assist and Pressure-Less Silver Sintering Paste for SiC Power Device Attachment on Lead Frame Based Package
Leong Ching Wai, Kazunori Yamamoto, Gongyue Tang, and Jacob Jordan Soh – Institute of Microelectronics (IME), A*STAR

20. Modeling High-Frequency and DC Path of Embedded Discrete Capacitor Connected by Double-Side Terminals with Multi-Layered Organic Substrate and RDL Based Fan-Out Package
Heeseok Lee, Kyojin Hwang, Henry Kwon, Jisoo Hwang, Junso Pak, and Ju Yeon Choi – Samsung Electronics Co., Ltd.

Interactive Presentations: Thursday, June 2, 2:00 p.m. - 4:00 p.m and Friday, June 3, 8:30 a.m. - 10:30 a.m.

21. Pretreatment and Structuring of Spatial Circuit Carriers Based on Alumina for High Temperatures and High Frequencies
Philipp Braeuer, Thomas Stoll, Martin Muckelbauer, Alexander Hensel, and Joerg Franke – Institute FAPS, FAU

22. Characterization of Low Loss Dielectric Materials for High-Speed and High-Frequency Applications
ZN Lee, John Lau, CT Ko, Tim Xia, Eagle Lin, Henry Yang, Bruce Lin, Tony Peng, Leo Chang, Jia Chen, and Yi-Hsiu Fang – Unimicron Technology Corporation

23. Evaluation on Bonding Reliability of SAC305/Sn-57.5Bi-0.4Ag BGA Solder Joints with Drop Impact Test
Geunsik Oh, Kyung Deuk Min, Eun Ha, Jun Ho Jang, and Seung-Boo Jung – Sungkyunkwan University

24. High Throughput Void-Free Soldering with Pneumatic Reflow Method in Lead-Free Solder Die Attach
Huan-Ping Su and Auger Horng – Ableprint Technology Co., Ltd.; Chun-Cheng Lee – Shenmao Technology Co., Ltd.

25. Influence of Prepreg Material Properties on Printed Circuit Board (PCB) Stack-up
Tomin Liu and Mutharasu Devarajan – Western Digital

Friday, June 3, 2022

Session 41: Student Interactive Presentations
Time: 9:00 AM – 11:00 AM

Committee: Interactive Presentations

Session Co-Chairs:

Ibrahim Guven
Virginia Commonwealth University
Email: iguven@vcu.edu

Alan Huffman
SkyWater Technology
Email: alan.huffman@ieee.org

Biao Cai
IBM Corporation
Email: biaocai@us.ibm.com

1. Machine Learning Assisted Counterfeit IC Detection Through Non-Destructive Infrared (IR) Spectroscopy Material Characterization
Chengjie Xi, John True, Nathan Jessurun, Aslam Khan, Mark Tehranipoor, and Navid Asadizanjani – University of Florida

2. Pressureless and Low Temperature Sintering by Ag Paste for the High Temperature Die-Attachment in Power Device Packaging
Chuncheng Wang – Osaka University; Xu Zhang, Yudui Zhang, Tao Zhao, Pengli Zhu, Rong Sun, Hiroshi Nishikawa, and Liang Xu – Shenzhen Institute of Advanced Electronic Materials

3. Smartphone App-Enabled Flex sEMG Patch using FOWLP
Pragathi Venkatesh, Randall Irwin, Arsalan Alam, Michael Molter, Ayush Kapoor, Bilwaj Gaonkar, Luke Macyszyn, and Subramanian S. Iyer – University of California, Los Angeles; M. Selvan Joseph – California State University, Los Angeles

4. A Deep Learning Approach for Reflow Profile Prediction
Yangyang Lai, Jun Kataoka, Ke Pan, Jonghwan Ha, Junbo Yang, Karthik A. Deo, Jiefeng Xu, and Seungbae Park – Binghamton University

5. Effects of Temperature on the Adhesive Performance of High Tg Underfill in 2.5D Heterogeneous Integrated Packaging
Guolin Zhao, Haoliang Lin, Houya Wu, Bin Wang, Yuanyuan Yang, Gang Li, Pengli Zhu, and Rong Sun – Chinese Academy of Sciences; Ching-Ping Wong – Georgia Institute of Technology; Wenhui Zhu – Central South University

6. Demonstration and Comparison of Vertical Via-less Interconnects in Laminated Glass Panels from 40 -170GHz
Lakshmi Narasimha Vijay Kumar, Kyoung-Sik Moon, and Madhavan Swaminathan – Georgia Institute of Technology; Kimiyuki Kanno, Hirokazu Ito, Taku Ogawa, and Koichi Hasegawa – JSR Corporation

7. Monte Carlo Particle Simulation of Avalanche Breakdown in a Reverse Biased Diode with Full Band Structure
Ze Sun, Manish Kizhakkeveettil Mathew, and DongHyun Kim – Missouri University of S&T; Ryan From – Boeing

8. Characterization and Analysis of Moisture Absorption in Embedded System in Packaging
Rongwei Gao, Rui Ma, Jun Li, Qidong Wang, Liqiang Cao, and Meiying Su – Institute of Microelectronics of Chinese Academy of Science

9. Methods of Printing Copper for PCB Repair
Dylan Richmond, Emuobosan Enakerakpo, Mohammed Alhendi, and Mark Poliks – Binghamton University; Peter McClure and Jim Wilcox – Universal Instruments Corp.

10. Novel Sn–Cu Based Composite Solder Preforms Capable of Low Temperature Reflow for Die Attachment of High Temperature Power Electronics and the Transient Liquid Phase Bonding Process
Ru-Zeng Shi, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

11. Trust Validation of Chiplets Using a Physical Inspection Based Certificate Authority
Nidish Vashistha, Md Mahfuz Al Hasan, Fahim Rahman, Navid Asadizanjani, and Mark Tehranipoor – University of Florida

12. Security Challenges of MEMS Devices in HI Packaging
Aslam Khan, Keon Sahebkar, Chengjie Xi, Mark Tehranipoor, Ryan F. Need, and Navid Asadizanjani – University of Florida

13. Influence of Height Difference Between Chip and Substrate on RDL in Silicon-Based Fan-Out Package
Xiao Han, Wei Wang, and Yufeng Jin – Peking University

14. Symmetric-Cell EBG Theory and Its Applications to Vias Daisy Chain for Residual Stub Detection
Yu-Kuang Wang and Ruey-Beei Wu – National Taiwan University; Ming-Tsun Lu, Jun-Rui Huang, and Ching-Sheng Chen – Unimicron Technology Corporation

15. Millimeter-Wave Antenna Design and Performance Analysis for Automotive Applications
Mohammad Pervez, Amanpreet Kaur, and Md Mamun Ur Rashid – Oakland University

2022 TECHNOLOGY CORNER EXHIBITS

The ECTC 2022 Technology Corner Exhibition is happy to welcome back dozens of organizations representing the full spectrum of materials, services, equipment, and products for the electronic packaging industry. Complementing the strength of the ECTC technical program, the Exhibition provides an unparalleled opportunity for engineers and decision makers to discuss and collaborate with representatives from leading electronic packaging companies. With scheduled refreshment breaks and social events that will take place in the Exhibition space, located in the newly renovated Eventide Pavilion, exhibitors and attendees will enjoy continual interactions with conference attendees. Exhibit hours will be from 9:00 AM to Noon and 1:30 to 6:30 PM on Wednesday, June 1, 2022, and 9:00 AM to Noon and 1:30 to 4:00 PM on Thursday, June 2, 2022. Exhibit booth remaining availability is extremely limited for 2022. The 2022 Exhibit Application can be found at www.ectc.net and clicking the 'Exhibits' link. For additional information or questions, please contact Alan Huffman, ECTC Exhibits Chair at +1-336-380-5124 or email alan.huffman@ieee.org and ectc.exhibits@gmail.com.

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By Internet: Submit your registration electronically via www.ectc.net. Your registration must be received by the cutoff date, May 4, 2022, to qualify for the early registration discounts.

You may contact our registration staff at lrenzi@renziandco.com for additional information. Payment can be made by Visa, Mastercard, or American Express.

HOTEL RESERVATIONS

The Sheraton San Diego Hotel and Marina • Marina Tower • 1380 Harbor Island Drive San Diego, CA 92101, USA

Hotel reservations for ECTC 2022 can be made one of two ways:

1) Contact the Sheraton San Diego Hotel and Marina at +1-619-291-2900 and reference the ECTC Conference to receive the conference rate of US$225 per night. Also ask to be placed in the Marina Tower, if possible!

or …

2) Log onto www.ectc.net and click on the Location tab near the top of the page to find a special online hotel registration link.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2022 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2022 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. **ECTC's only authorized site** for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that **you personally have used** in the past to book travel. Please be advised, there are scam artists out there and if it's too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: lrenzi@renziandco.com

72nd Electronic Components & Technology Conference

2022 ECTC REGISTRATION INFORMATION

Conference Registration		Advance Registration	Door Registration
IEEE Member	Attendee (full ECTC conference)	US $800	US $925
	Attendee (Joint ECTC + ITHERM conferences)	$1000	$1225
	Attendee One-Day Registration	$600	$600
	Speaker or Chair (full ECTC conference)	$675	$825
	Speaker or Chair One-Day Registration	$525	$430
Non-IEEE Member	Attendee (full ECTC conference)	$1000	$1125
	Attendee (Joint ECTC + ITHERM conferences)	$1225	$1475
	Attendee One-Day Registration	$600	$600
	Speaker or Chair (full ECTC conference)	$675	$825
	Speaker or Chair One-Day Registration	$525	$525
Student	Attendee or Speaker (full conference)	$315	$315
Exhibits			
Access to Exhibits Only (not attending conference)		$50	$50
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Professional Development Courses (PDCs) Note: all PDCs include a luncheon			
IEEE Member	Full PDC (both a.m. and p.m.)	$625	$625
	Single PDC (a.m. or p.m.)	$440	$440
Non-IEEE Member	Full PDC (both a.m. and p.m.)	$675	$675
	Single PDC (a.m. or p.m.)	$490	$490
Student	Full PDC (both a.m. and p.m.) or Single PDC	$150	$150
Other Registration Options			
Extra Proceedings		$100	$100
Extra Luncheon Tickets		$65	$65
Cancellation Fee		$50	$50

Please log onto www.ectc.net/registration to register for the 2022 ECTC.

There will be no refunds or cancellations after May 4, 2022. Please note that a $50 cancellation fee will be in effect for all cancellations made on or prior to May 4, 2022. Substitutions can be made at any time.

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CONFERENCE OVERVIEW

May 31, 2022

Morning Professional Development Courses
8:00 a.m. - 12:00 p.m.

1. Achieving High Reliability of Lead-Free Solder Joints -- Materials Considerations
2. Wafer-Level Chip-Scale Packaging (WCSP) Fundamentals
3. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel Level Packages and Interposers
4. Eliminating Failure Mechanisms in Advanced Packages
5. Packaging and Heterogeneous Integration for Automotive Electronics and Advanced Characterization of EMCs
6. Avoiding inelastic strains in solder joint interconnections of IC packages
7. Flip Chip Technologies
8. Reliable Integrated Thermal Packaging for Power Electronics

Afternoon Professional Development Courses
1:15 p.m. - 5:15 p.m.

9. Additive Flexible Hybrid Electronics – Manufacturing and Reliability
10. From Wafer to Panel Level Packaging
11. Fan-out Wafer/panel-level Packaging and Chiplet Design and Heterogeneous Integration Packaging
12. Reliability Engineering Testing Methodology and Statistical Knowledge for Qualifications of Consumer and Automotive Electronic Components
13. Introduction of Two-Phase Cooling of High-Power Electronics
14. Multi-Physics Modeling and Simulation in Electronic Packaging Theory, Implementation and Best Practices
15. Polymers in Wafer Level Packaging
16. Thermal Management of Electronics

ECTC Special Session
8:30 a.m. - 10:00 a.m.
"MicroLED Display Technology: High Volume Manufacturing (HVM) Progress and Challenges"

ECTC Special Session
10:30 a.m. - 12:00 p.m.
"Selected Topics of IEEE EPS Heterointegration Roadmap"

ECTC Special Session
1:30 p.m. - 3:00 p.m.
"Meeting Next Generation Packaging Challenges: Chiplets to Co-Packaged Optics"

ECTC Special Session
3:30 p.m. - 5:00 p.m.
"How Will IC Substrate Technology Evolve to Enable Next Generation Heterogeneous Integration Schemes for High Performance Applications?"

Young Professionals Networking Panel
7:00 p.m. - 7:45 p.m.

ECTC EPS President's Panel Session
7:45 p.m. - 9:15 p.m.
"State-of-the-Art Heterogeneous Integration Packaging Program"

June 1, 2022

Technical Sessions
8:00 a.m. - 11:40 a.m.

1. Advanced Packaging for Heterogeneous Integration and High Performance Computing
2. High Performance Dielectric Materials for Advanced Packaging
3. Antenna-in-Package for Communication, Radar and Energy Transfer
4. Hybrid Bonding and Innovations for 3D Integration
5. Bonding Technology: Novel Assembly Methods and Processes
6. Emerging Modeling Including AI and Machine Learning

Interactive Presentation Sessions 37 & 38
9:00 a.m. - 11:00 a.m.
2:00 p.m. - 4:00 p.m.

ECTC Luncheon Keynote
"Accelerating the power of data infrastructure with cloud-optimized silicon"

Interactive Presentation Sessions 37 & 38
9:00 a.m. - 11:00 a.m.
2:00 p.m. - 4:00 p.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.

7. Advanced Flip Chip and Embedded Substrate Technologies
8. Hybrid and Direct Bonding Development and Characterization
9. Millimeter-Wave Antenna-In-Package: Design, Manufacturing and Test
10. Novel Photonics Packaging Technology
11. Automotive and Harsh Environment
12. Manufacturing and Assembly Process Modeling

ECTC/ITHERM Diversity and Career Growth Panel and Reception
6:30 p.m. - 7:30 p.m.
"Solving Diversification Challenges and Workforce Retention Issues"

ECTC General Chair's Plenary Session
7:45 p.m. - 9:15 p.m.
"Digital Transformation – The Cornerstone of Future Semiconductor and Advanced Packaging Growth"

June 2, 2022

Technical Sessions
8:00 a.m. - 11:40 a.m.

13. Technologies for Heterogeneous Integration, Automotive and Power Electronics
14. Novel Bonding and and Stacking Technologies
15. Enhanced Methods & Processes for Heterogeneous Integration Assembly
16. Hybrid & Direct Bonding Innovation, Optimization & Yield Improvement
17. Novel Characterization Techniques and Test Methods
18. Flexible, Wearable Sensors and Electronics

Interactive Presentation Sessions 39 & 40
9:00 a.m. - 11:00 a.m.
2:00 p.m. - 4:00 p.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.

19. Advances in Fan-Out Panel Level Packaging
20. Enhancements in Fine-Pitch Interconnects, Redistribution Layers and Through-Vias
21. Millimeter-Wave RF Components and Modules for 5G
22. AI, Quantum Computing and Novel 3D Packaging solutions
23. Advanced Processes for Manufacturing and Yield Enhancement
24. Thermal Management and Warpage Analysis of Highly Integrated Packages

IEEE Special Session
8:00 p.m. - 9:30 p.m.
"Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements"

June 3, 2022

Technical Sessions
8:00 a.m. - 11:40 a.m.

25. Advancements in 2.5D and 3D Packaging Technology
26. Soldered and Sintered Interconnections
27. Interconnection Reliability
28. Packaging Assembly: Solder, Sintering, and Thermal Interface Materials
29. Materials and Processes for Fan-Out and Advanced Packaging
30. High-Speed Challenges in Power and Signal Integrity

Student Interactive Presentations Session 41
8:30 a.m. - 10:30 a.m.

Technical Sessions
1:30 p.m. - 5:10 p.m.

31. Fan-Out Packaging Technologies and Applications
32. Advanced Interconnect and Wire Bond Technologies for Flexible Device Applications
33. Advanced Reliability Modeling and Characterization
34. Processing Enhancements in Fan-Out and Heterogeneous Integration
35. Packaging with Additive Manufacturing for Harsh Conditions
36. Modeling and Characterization of Interfaces and Interconnects

Session Summary by Interest Area

Packaging Technologies
S1, S7, S13, S19, S25, S31

Applied Reliability
S11, S17, S27, S33

Assembly & Manufacturing Technology
S5, S15, S23, S28

Emerging Technologies
S18, S22, S35

RF, High-Speed Components & Systems
S3, S9, S21, S30

Interconnections
S4, S8, S16, S26, S32

Materials & Processing
S2, S14, S20, S28, S29, S34

Thermal/Mechanical Simulation & Characterization
S6, S12, S24, S33, S36

Photonics
S10

Interactive Presentations
S37, S38, S39, S40, S41

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