Conference Program and Exhibitor Listings

Don't miss out on electronic packaging's premier conference!

ECTC

The 2022 IEEE 72nd Electronic Components and Technology Conference

May 31 - June 3, 2022

Sheraton San Diego Hotel & Marina
San Diego, California, USA

For more information, visit: www.ectc.net

Sponsored by:

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

WELCOME TO THE 72nd ECTC FROM THE GENERAL CHAIR AND PROGRAM CHAIR

On behalf of the Program Committee and Executive Committee, it is our pleasure to welcome you to the 72nd Electronic Components and Technology Conference (ECTC), held at The Sheraton San Diego Hotel and Marina, San Diego, California from May 31– June 3, 2022. This premier international conference brings together key stakeholders of the global microelectronics packaging industry, such as semiconductor companies, foundry and OSAT service providers, equipment manufacturers, materials suppliers, research institutions and universities all under one roof.

At the 72nd ECTC, around 350+ technical papers are scheduled to be presented in 36 oral sessions and 5 interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as wafer-level and fan-out packaging, 2.5D, 3D and heterogeneous integration, interposers, advanced substrates, assembly, materials modeling, reliability, packaging for harsh conditions, power packaging, interconnections, packaging for high speed and high bandwidth, photonics, flexible and printed electronics. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work.

Authors from over twenty countries are expected to present their work at the 72nd ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

Chris Koopmans, Chief Operations Officer, Marvell, will deliver the ECTC Luncheon Keynote speech entitled, "Accelerating the power of data infrastructure with cloud-optimized silicon."

Additionally, a half-day workshop on Heterogeneous Integration Roadmap, chaired by Bill Chen and Bill Bottoms, will be held on Tuesday. ECTC will also feature 7 special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday 5 special sessions, 90 minutes each, are scheduled. On Tuesday morning May 31st at 8:30 a.m. Chukwudi Okoro and Benson Chan will chair the session on "MicroLED Display Technology: High Volume Manufacturing (HVM) Progress and Challenges," followed by Amr Helmy chairing a special session at 10:30 a.m. with "Selected Topics of the IEEE EPS Heterointegration Roadmap." On Tuesday afternoon at 1:30 p.m. Jan Vardaman will present a special session on the topic "Chiplets to Co-Packaged Optics," followed by Kuldip Johal and Bora Baloglu presenting a special session at 3:30 p.m. titled: "How will IC Substrate Technology Evolve to Enable Next-Generation Heterogeneous Integration Schemes for High-Performance Applications?" On Tuesday evening Kitty Pearsall and Chris Riso will co-chair the EPS President's ECTC panel session on the topic: "State-of-the-Art Heterogeneous Integrated Packaging Program."

We are continuing our tradition and bringing back the networking events focused on young professionals and diversity. Yan Liu and Adeel Bajwa will chair the Young Professionals Meetup. This is a great networking opportunity for young engineers, researchers, and students, to meet senior EPS members and professionals, learn more about industry activities, receive career guidance, and engage through a series of activities.

This conference will also feature our Diversity and Career focused Panel and Reception jointly organized by ECTC and ITherm on Wednesday, June 1st at 6:30 p.m. This year, panelists will share their perspectives of career opportunities while focusing on some of the specifics of the diverse workforce and inclusion. The panel will be chaired by Kim Yess, Christina Amon and Francoise von Trapp. On the same day at 7:30 p.m., Rozalia Beica together with Jean-Christophe Eloy will present the ECTC General Chair's Plenary Session entitled, "Digital Transformation - The Cornerstone of Future Semiconductor and Advanced Packaging Growth". For Thursday, June 2nd at 7:30 p.m. our colleagues from Japan, Yasumitsu Orii and Shigenori Aoki, will be chairing the IEEE EPS Seminar which will focus on "Interconnect Technologies for Chiplets."

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE ITherm Conference, the 72nd ECTC will offer 16 CEU-approved PDCs, organized by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 31st and are taught by distinguished experts in their respective fields. The Technology Corner exhibits will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. We cordially invite you to make your plans now to join us for the 72nd ECTC and to be a part of all the exciting technical and professional opportunities. We also want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 72nd ECTC a success. We look forward to meeting you at The Sheraton San Diego Hotel and Marina, San Diego, California, May 31– June 3, 2022.

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WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of the IEEE Electronics Packaging Society, I am delighted to welcome you to the 72nd Electronic Components and Technology Conference – the world's premier event for electronics packaging.

Starting 72 years ago, ECTC continues to grow, innovate, and serve our community with an exciting technical program detailing the latest advances in electronics packaging. Building upon the outstanding event from last in-person years and the very positive feedback to our virtual conferences, we expect attendance at ECTC 2022 to well exceed 1400 packaging professionals. This is a fantastic achievement. Our conference portfolio continues to find innovative ways to grow and serve our community. Together with ECTC and our Asia-Pacific flagship conference EPTC, to be held in December, EPS expects to reach similar well attended in-person conferences world-wide in 2022.

These achievements would not be possible without the dedication and commitment of our conference organizers and volunteers. I would like to express my sincere thanks to the ECTC Executive and Program Committees, members of the EPS Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their outstanding efforts in bringing you this year's exciting event. We are fortunate to have such an enthusiastic team that keeps finding new ways to serve the electronic packaging community.

May I also thank our authors, presenters, and sponsors for their contributions to this year's event. It is very rewarding to see the significant benefits that events such as ECTC have on the Electronics Packaging Society, our industry, and our members.

In addition to conferences, EPS has been implementing its exciting plans for membership, chapters, publications, education, and technology to provide a unique service to our members worldwide. You can find more information about these activities at the EPS website.

Finally, may I thank you for attending this year's ECTC. Enjoy the conference, and I look forward to meeting you again at one of our future events.

Kitty Pearsall
EPS President 2021-2022

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, seminars, meals, exhibits and IP areas, and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
Please follow hotel policies and signs regarding this. Smoking is also NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, seminars, meals, exhibits and IP areas, and all conference social functions. Thank you for your consideration and cooperation.

ECTC Mobile App

ECTC is pleased to announce that a free mobile app is available this year. The app provides information on schedules for our technical program and PDCs as well as exhibitors, sponsors, and general conference information and venue maps. The app also features tools to set your schedule, so you don't miss presentations important to you, social interaction functions, and the ability to provide ratings on presentations that are used in selecting candidates for best paper awards. The app is available for iOS and Android devices from their respective app stores by searching "Whova". After downloading the Whova app please log in using the email address you used to register for ECTC, and the ECTC content will appear automatically.

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Conference organizers reserve the right to cancel or change this program without prior notice.

ECTC Luncheon Keynote

Accelerating the Power of Data Infrastructure with Cloud-Optimized Silicon

Wednesday, June 1, 2022 • 12:00 p.m.

Chris Koopmans – Chief Operations Officer, Marvell

Pacific Jewel Ballroom

Over the past five years, Marvell Technology has transformed from being a broad, consumer-oriented company to an industry-leading data infrastructure semiconductor solutions provider. Data infrastructure is a large, fast-growing market that powers our global economy and is crucial in advancing our society. This keynote session will discuss why and how Marvell transformed itself to data infrastructure. The presentation will share insights into how data infrastructure is converging into the cloud, the emerging cloud-optimized silicon era and the technology areas the industry must tackle to accelerate the power of data infrastructure with cloud-optimized silicon

2022 ECTC Heterogeneous Integration Roadmap (HIR) Workshop

Tuesday, May 31, 2022 • 8:00 a.m. - 4:30 p.m.

Chairs: William Chen – ASE, Bill Bottoms – 3MTS and Ravi Mahajan – Intel

Pacific Jewel C

Heterogeneous Integration uses packaging technology to integrate dissimilar chips, devices or components with different materials and functions, and from different fabless design houses, foundries, wafer materials, feature sizes and companies into a system or subsystem. 23 Technical working groups will present on their areas of expertise. This workshop is a full-day event with the following schedule, incorporating two ECTC 2022 special sessions.

Workshop Segments:

- 8:00 a.m. – Heterogeneous Integration Workshop • HIR Shared Vision
- 9:00 a.m. – Future Networks & Beyond • Panel Organizer: Tim Lee
- 10:30 a.m. – HIR Selected Topics • Panel Organizer: Amr Helmy
- 12:00 Noon – Lunch
- 1:00 p.m. – Packaging for HPC & Data Center • Panel Organizer: Kanad Ghose
- 2:30 p.m. – Medical Health & Wearables • Panel Organizer: Mark Poliks
- 4:00 p.m. – Wrap-Up

REGISTRATION AND GENERAL INFORMATION

REGISTRATION

ECTC registration will be open at the ECTC Registration Desk located in The Sheraton San Diego Hotel and Marina in San Diego, CA, in the Seascape Foyer.

Monday, May 30, 2022 – 3:00 p.m. - 5:00 p.m.
Tuesday, May 31, 2022 – 6:45 a.m. - 8:15 a.m.*
(AM PD Courses & Special Session Only)*
Tuesday, May 31, 2022 – 8:15 a.m. - 5:00 p.m.
(All conference attendees)
Wednesday, June 1, 2022 – 6:45 a.m. - 4:00 p.m.
Thursday, June 2, 2022 – 7:30 a.m. - 4:00 p.m.
Friday, June 3, 2022 – 7:30 a.m. - 12:00 p.m.

On Tuesday, May 31st light morning refreshments will be provided from 6:45am – 7:15am. Come pick up your registration materials EARLY and grab a bite to eat before the PDC's start!

The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45am start time as registration becomes very congested prior to the start of morning Professional Development Courses.

DOOR REGISTRATION FEES

Door Registration with Proceedings Download

IEEE Member JOINT Registration
(full ECTC + ITHERM conference) $1225
IEEE Member Full Registration $925
IEEE Member Speaker / Session Chair $825
IEEE Member One Day $600
IEEE Member Speaker One Day $525
Exhibit Booth Attendant $0

Non-Member JOINT Registration
(full ECTC + ITHERM conference) $1475
Non-Member Full Registration $1125
Non-Member Speaker / Session Chair $825
Non-Member One Day $600
Non-Member Speaker One Day $525
Exhibit Booth Attendant $0

Student $315
Student Speaker $315

Exhibits Only $50

Tuesday Professional Development Courses

IEEE Members
Tuesday AM or PM Course with Luncheon $440
Tuesday All-Day Courses with Luncheon $625

Non-Members
Tuesday AM or PM Course with Luncheon $490
Tuesday All-Day Courses with Luncheon $675

Tuesday Student All-Day Courses with Luncheon $150

Extra Luncheon Tickets for Each Day $65

PROFESSIONAL DEVELOPMENT COURSE INSTRUCTORS BREAKFAST

PDC Instructors and Proctors are required to attend a briefing breakfast.

7:00 a.m. Tuesday – PDC Instructors and Proctor Briefing

(Room Location: Pacific Jewel B)

Session Chairs and Speakers Breakfast

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC.

7:00 a.m. Wednesday thru Friday

(Room Location: Pacific Jewel A)

Speaker Prep Room

Speakers should prepare and review their digital presentations within the allotted times below:

7:00 a.m. – 5:00 p.m., Tuesday – Friday

(Room Location: Tidepool 1)

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

MISCELLANEOUS INFORMATION

Hotel Concierge

The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Press Room

Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts please contact ECTC Publicity Chair, Eric Perfecto, at eperfecto@gmail.com or (845) 475-1290.

LUNCHEONS

Tuesday, May 31, 2022
12PM (Pacific Jewel Ballroom)
Our Tuesday lunch is provided for anyone attending a Professional Development Course, whether you attend just a single course or both a morning and afternoon course. PDC Proctors, session speakers, committee members or anyone else with a Tuesday lunch ticket is more than welcome to join! Possession of a lunch ticket is required for admission.

Wednesday, June 1, 2022
12PM (Pacific Jewel Ballroom)
This year's Wednesday luncheon will feature Chris Koopmans, Chief Operations Officer, Marvell Technology. We will also be celebrating award winners for Best and Outstanding Papers of 2021! Don't miss it! Possession of a lunch ticket is required for admission.

Thursday, June 2, 2022
12PM (Pacific Jewel Ballroom)
The IEEE Electronics Packaging Society will host our Thursday luncheon for conference attendees. The EPS awards will be presented. Possession of a lunch ticket is required for admission.

Friday, June 3, 2022
12PM (Pacific Jewel Ballroom)
Do NOT MISS Friday's luncheon! It's our annual ECTC Program Chair luncheon where lots of high dollar, valuable, and useful prizes will be raffled off! Each year the prizes seem to get better and better! Remember you must be present to win. Possession of a lunch ticket is required for admission.

2022 ECTC SESSIONS & SEMINARS – Open to all conference attendees

2022 ECTC SPECIAL SESSION

MicroLED Display Technology: High Volume Manufacturing (HVM) Progress and Challenges

Tuesday, May 31, 2022
8:30 a.m. – 10:00 a.m.

Pacific Jewel A

Chairs: Chukwudi Okoro - Corning Inc., USA
and Benson Chan - Binghamton University, USA

John Kymissis – Principal Engineer, Lumiode
Eugene Chow – Principal Scientist, Palo Alto Research Center (PARC)
Falcon Liu – Marketing Director, Playnitride
Chris Bower – CTO, XDisplay
Sean Garner – Principal Scientist, Corning Inc
Eric Virey – Senior Market and Technology Analyst, Yole Development

2022 ECTC SPECIAL IEEE EPS HIR SESSION

Selected Topics of IEEE EPS Heterointegration Roadmap

Tuesday, May 31, 2022
10:30 a.m. – 12:00 p.m.

Pacific Jewel C

Chair: Amr Helmy
Professor of U of Toronto

Seoung Wook Yoon – VP Corporate R&D, Samsung

More speakers to be confirmed soon.

2022 ECTC SPECIAL SESSION

Meeting Next Generation Packaging Challenges: Chiplets to Co-Packaged Optics

Tuesday, May 31, 2022
1:30 p.m. – 3:00 p.m.

Pacific Jewel A

Chair: E. Jan Vardaman
TechSearch International, Inc.

Ravi Mahajan – Intel Corporation
Sandeep Razdan – Cisco
Kevin O'Buckley – Marvell Technology
Raja Swaminathan – AMD

2022 ECTC SPECIAL SESSION

How Will IC Substrate Technology Evolve to Enable Next Generation Heterogeneous Integration Schemes for High Performance Applications?

Tuesday, May 31, 2022
3:30 p.m. – 5:00 p.m.

Pacific Jewel A

Chairs: Kuldip Johal, Atotech Group
and Bora Baloglu, Amkor

OEM: Intel Rahul Manepalli Intel Fellow & Director of Substrate TD Module Engineering.
OSAT: Amkor JinYoung Khim, (Sr. VP Head of R&D)
IC Substrate: Markus Leitgeb R&D Manager AT&S
Materials: Habib Hichri Senior Fellow, Global Applications and Business Development at Ajinomoto Fine-Techno USA Corporation.
Process + Tools: Frank Bruening Global Product Director Mentalization. Atotech

2022 YOUNG PROFESSIONALS NETWORKING PANEL & RECEPTION

Tuesday, May 31, 2022
7:00 p.m. – 7:45 p.m.

Silver Pearl 3

Chairs: Yan Liu, Medtronic
and Adeel Bajwa, Kulicke and Soffa

This event is designed just for you – young professionals (including current graduate students). In this active event, we will pair you with senior EPS members and professionals through a series of active and engaging activities. You will have opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

2022 EPS PRESIDENT'S PANEL SESSION

State-of-the-Art Heterogeneous Integrated Packaging Program

Tuesday, May 31, 2022
7:45 p.m. – 9:15 p.m.

Silver Pearl 1 & 2

Chairs: Kitty Pearsall, EPS President & Boss Precision, Inc.
and Christopher Riso, Booz Allen Hamilton

Darren Crum, Technical Lead, State-of-the-Art Heterogeneous Integrated Packaging (SHIP) Program – Office of the Undersecretary of Defense for Research and Engineering
John Sotir, SHIP Program Director – Intel Corporation
Ted Jones, Sr. Product Line Director High Performance Solutions Services – Qorvo Inc.

2022 ECTC SESSIONS & SEMINARS – Open to all conference attendees

2022 ECTC/ITHERM DIVERSITY & CAREER GROWTH PANEL & RECEPTION

Solving Diversification Challenges and Workforce Retention Issues

Wednesday, June 1, 2022
6:30 p.m. – 7:30 p.m.

Silver Pearl 3

Chairs: Kim Yess, Brewer Science/ECTC
and Christina Amon, University of Toronto/ITherm

Moderator: Francoise von Trapp, 3D InCites

Bina Hallman – VP IBM System Client Advocacy and Head of D&I System Business
Antoinette Hamilton – Head of DEI at Lam Research
Najwa Khazal – General Manager, Service Technology Centres Americas, Edwards
KT Moore – VP Corporate Marketing at Cadence

2022 PLENARY SESSION

Digital Transformation – The Cornerstone of Future Semiconductor and Advanced Packaging Growth

Wednesday, June 1, 2022
7:45 p.m. – 9:15 p.m.

Silver Pearl 1 & 2

Chair: Rozalia Beica, AT&S

Carolyn Evans – Chief Economist, Intel (US)
Doug Yu – VP Pathfinding and System Integration – TSMC (TW)
Jean Christophe Eloy – CEO Yole Developpement (FR)
Mike Rosa – CMO, SVP Strategy, Onto Innovation (US)
Seoung Wook Yoon – VP Corporate R&D, Samsung (KR)Director Mentalization. Atotech

CONTINUING EDUCATION UNITS

The IEEE Electronics Packaging Society (EPS) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 72nd ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops. Complete details will be available at the conference. All costs associated with ECTC Professional Development Course CEUs will be underwritten by the conference, i.e., there are no additional costs for Professional Development Course attendees to obtain CEU credit.

2022 IEEE EPS SEMINAR

Interconnect Technologies for Chiplets

Thursday, June 2, 2022
8:00 p.m. – 9:30 p.m.

Silver Pearl 1 & 2

Chairs: Yasumitzu Orii, Nagase, Japan
and Shigenori Aoki, Lintec

Ravi Mahajan – Intel: ***HI Interconnects for today and tomorrow***

Akihiro Horibe – IBM Research Tokyo: ***Direct Bonded Heterogeneous Integration DBHi Si Bridge***

Yu-Hua Chen – Unimicron: ***The Challenges of Advanced Substrate for Heterogeneous Integration***

Shin-Puu Jeng – TSMC: ***Heterogeneous Integration Approaches in Foundry***

Yu-Po Wang – SPIL: ***Trend and Solution for Memory Integrated Advanced Packages***

Hideyuki Nasu – Furukawa Electric: ***High-Density Optical Transceivers and Pluggable Electrical Interfaces for Co-Packaged Optics***

ECTC STUDENT RECEPTION

Tuesday, May 31, 2022 • 5:00 p.m. - 6:00 p.m.

Pacific Jewel Foyer

Hosted by Texas Instruments, Inc.

Texas Instruments

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry, and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them succeed in their first job search and reach their current positions. During this reception, you can enjoy good food while networking with industry leaders and achievers. Don't miss your opportunity to interact with people who you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

GENERAL CHAIR'S SPEAKERS RECEPTION

Tuesday, May 31, 2022 • 6:00 p.m. - 7:00 p.m.

Pacific Jewel B

Invited session chairs and speakers
are requested to attend the reception.

EXHIBIT HALL TECHNOLOGY CORNER RECEPTION

Wednesday, June 1, 2022 • 5:30 p.m. - 6:30 p.m.

Eventide Pavilion

All attendees and guests are invited.

72nd ECTC GALA RECEPTION

Thursday, June 2, 2022 • 6:30 p.m.

OUTSIDE: Eventide Gardens
(Exit doors at Seascape Foyer)

All badged attendees are invited.

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 31, 2022

Morning Courses 8:00 a.m. – 12:00 Noon	Afternoon Courses 1:30 p.m. – 5:30 p.m.
Shorebreak **1. Achieving High Reliability of Lead-Free Solder Joints – Materials Considerations** *Course Leader: Ning-Cheng Lee – Independent Consultant*	**Shorebreak** **9. Additive Flexible Hybrid Electronics – Manufacturing and Reliability** *Course Leader: Pradeep Lall – Auburn University*
Silver Pearl 1 **2. Wafer-Level Chip-Scale Packaging (WLCSP) Fundamentals** *Course Leader: Patrick Thompson – Texas Instruments, Inc.*	**Silver Pearl 1** **10. From Wafer to Panel Level Packaging** *Course Leaders: Tanja Braun and Markus Wöhrmann – Fraunhofer IZM*
Silver Pearl 2 **3. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel Level Packages and Interposers** *Course Leaders: Ivan Ndip and Markus Wöhrmann – Fraunhofer IZM*	**Silver Pearl 2** **11. Fan-Out Wafer/Panel-Level Packaging and Chiplet Design and Heterogeneous Integration Packaging** *Course Leader: John Lau – Unimicron*
Silver Pearl 3 **4. Eliminating Failure Mechanisms in Advanced Packages** *Course Leader: Darvin Edwards – Edwards Enterprises*	**Silver Pearl 3** **12. Reliability Engineering Testing Methodology and Statistical Knowledge for Qualifications of Consumer and Automotive Electronic Components** *Course Leader: Fen Chen – GM Cruise*
Driftwood **5. Packaging and Heterogeneous Integration for Automorive Electronics and Advanced Characterizations of EMCs** *Course Leader: Przemyslaw Gromala – Robert Bosch GmbH*	**Driftwood** **13. Introduction of Two-Phase Cooling of High-Power Electronics** *Course Leader: John R. Thome – JJ Cooling Innovation*
Coral 1 & 2 **6. Avoiding Inelastic Strains in Solder Joint Interconnections of IC Packages** *Course Leader: Ephraim Suhir – Portland State University*	**Coral 1 & 2** **14. Multi-Physics Modeling and Simulation in Electronic Packaging Theory, Implementation and Best Practices** *Course Leader: Xuejun Fan – Lamar University*
Coral 3 & 4 **7. Flip Chip Technologies** *Course Leaders: Shengmin Wen – HaiSemi Inc. and Eric Perfecto – IBM Corporation*	**Coral 3 & 4** **15. Polymers in Wafer Level Packaging** *Course Leader: Jeffrey Gotro – InnoCentrix, LLC*
Coral 5 **8. Reliable Integrated Thermal Packaging for Power Electronics** *Course Leader: Patrick McCluskey – University of Maryland*	**Coral 5** **16. Thermal Management of Electronics** *Course Leader: Jaime Sanchez – Intel Corporation*

Refreshment Breaks
10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Silver Pearl Foyer & Coral Foyer

COMMITTEE MEETINGS

ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday May 31, 2022

8:00 a.m. – 5:00 p.m.
EPS HIR Workshop
Pacific Jewel C

9:00 p.m. – 10:30 p.m.
ECTC OPTO Committee
Room 518

9:00 p.m. – 10:30 p.m.
ECTC Interconnect Committee
Rooms 411/415

Wednesday June 1, 2022

7:00 a.m. – 8:00 a.m.
EPS High Density Substrates & Boards TC
Room 511

7:00 a.m. – 8:00 a.m.
EPS Power & Energy TC
Room 514

7:00 a.m. – 8:00 a.m.
EPS 3D TSV TC
Rooms 411/415

7:00 a.m. – 8:00 a.m.
EPS EDMS TC
Driftwood 1

7:00 a.m. – 8:00 a.m.
EPS Reliability TC
Driftwood 2

4:30 p.m. – 5:30 p.m.
EPS Technical Committee Chairs
Room 511

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite (by invitation only)

Thursday, June 2, 2022

7:00 a.m. – 8:00 a.m.
EPS Chapter Chairs Meeting
Shorebreak

7:00 a.m. – 8:00 a.m.
EPS Nanotechnology TC
Room 511

7:00 a.m. – 8:00 a.m.
EPS Materials & Processes TC
Room 514

7:00 a.m. – 8:00 a.m.
EPS Emerging Tech TC
Driftwood 1

7:00 a.m. – 8:00 a.m.
EPS Photonics TC
Driftwood 2

5:30 p.m. – 6:30 p.m.
ECTC 2023 Program Committee Meeting
Silver Pearl 3

8:00 p.m.
72nd ECTC Governing/ Executive Committee Reception
General Chair's Suite

Friday June 3, 2022

7:00 a.m. – 8:00 a.m.
EPS RF & Thz Tech. TC
Room 514

7:00 a.m. – 8:00 a.m.
EPS Thermal & Mechanical TC
Driftwood 1

7:00 a.m. – 8:00 a.m.
EPS Transaction Editors TC / AE's
Room 511

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee
Shorebreak

4:45p.m. – 5:45 p.m.
ECTC / EPS Steering Committee
Shorebreak

ECTC BEST PAPER AWARDS

BEST OF CONFERENCE PAPERS – 2021

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 71st ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500, and the authors of the Best Interactive Presentation share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

Session 34, Paper 6

Proof of Concept: Glass-Membrane Based Differential Pressure Sensor

Anatoly Glukhovskoy, Maren S. Prediger, Jennifer Schäfer - Leibniz University; Norbert Ambrosius, Aaron Vogt, Rafael Santos, Roman Ostholt - LPKF Laser & Electronics AG; Marc Christopher Wurz - Leibniz University

Best Interactive Presentation Paper

Session 42, Paper 6

System in Package Embedding III-V Chips by Fan-Out Wafer Level Packaging for RF Applications

Arnaud Garnier, Laetitia Castagné, Florent Gréco - CEA-Leti; Thomas Guillemet - Thales DMS; Laurent Maréchal, Mehdy Neffati - United Monolithic Semiconductors; Rémi Franiatte, Perceval Coudrain - CEA-Leti; Stéphane Piotrowicz - III-V Lab; Gilles Simon - CEA-Leti

INTEL BEST STUDENT PAPER – 2021

The winning student receives a personalized plaque and a check for US $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 71st ECTC.

Session 21, Paper 4

Mechanical Behavior and Reliability of SAC+Bi Lead Free Solders with Various Levels of Bismuth

KM Rafidh Hassan, Jing Wu, Mohammad S. Alam, Jeffrey Suhling, and Pradeep Lall - Auburn University

OUTSTANDING PAPERS – 2021

The winning authors for the Conference Outstanding Session Paper and Interactive Presentation selected from the 71st ECTC proceedings receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

Session 25, Paper 6

Ultra-Thinning of 20-nm Node DRAMs Down to 3 µm for Wafer-on-Wafer (WOW) Applications

Zhiwen Chen, Naoko Araki, Youngsuk Kim, Tadashi Fukuda, Koji Sakui, Tomoji Nakamura - Tokyo Institute of Technology; Tatsuji Kobayashi, Takashi Obara - Micron Memory Japan; Takayuki Ohba - Tokyo Institute of Technology

Outstanding Interactive Presentation

Session 40, Paper 6

Cu-Recrystallization and the Formation of Epitaxial and Non-Epitaxial Cu/Cu/Cu Interfaces in Stacked Blind Micro Via Structures

Tobias Bernhard, S. Dieter, Roger Massey, S. Kempa, E. Steinhäuser, Frank Brüning - Atotech Deutschland GmbH

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Program Sessions: Wednesday, June 1, 8:00 a.m. - 11:40 a.m.

Session 1: Advanced Packaging for Heterogeneous Integration and High Performance Computing	Session 2: High Performance Dielectric Materials for Advanced Packaging	Session 3: Antenna-in-Package for Communication, Radar and Energy Transfer
Committee: Packaging Technologies	**Committee: Materials & Processing**	**Committee: RF, High-Speed Components & Systems**
Silver Pearl 1	**Silver Pearl 2**	**Silver Pearl 3**
Session Co-Chairs: **Andrew Kim – Advanced Micro Devices** **Email: andrew.kim@amd.com** **Mike Gallagher – DuPont Electronic and Imaging** **Email: michael.gallagher@dupont.com**	**Session Co-Chairs:** **Lingyun (Lucy) Wei – Dupont** **Email: lingyun.wei@dupont.com** **Yi Li – Intel Corporation** **Email: yi.li@intel.com**	**Session Co-Chairs:** **Rajen M Murugan – Texas Instruments** **Email: r-murugan@ti.com** **Maciej Wojnowski – Infineon Technologies AG** **Email: maciej.wojnowski@infineon.com**
1. 8:00 AM - Organic Interposer CoWoS-R+ (plus) Technology M. L. Lin, M. S. Liu, H. W. Chen, S. M. Chen, M. C. Yew, C. S. Chen, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 8:00 AM - Ultra-Thin Mold Cap for Advanced Packaging Technology*** Nabankur Deb and Xavier Brun – Intel Corporation; Chris Masuyama, N. Hamada, Y. Hirano, K. Wada, H. Oshida, K. Ganbayashi, L. L. Zhou, and T. Y. Lyu – TOWA Corporation	***1. 8:00 AM - 77GHz Cavity Backed AiP Array in FOWLP Technology*** Mei Sun, Lim Teck Guan, and Chai Tai Chong – Institute of Microelectronics (IME), A*STAR
2. 8:25 AM - Cost-Effective RF Interposer Platform on Low-Resistivity Si Enabling Heterogeneous Integration Opportunities for Beyond 5G Xiao Sun, John Slabbekoorn, Siddhartha Sinha, Pieter Bex, Nelson Pinho, Tomas Webers, Dimitrios velenis, Andy Miller, Nadine Collaert, Geert Van der Plas, and Eric Beyne – Imec	***2. 8:25 AM - Evaluation of the Transmission Loss of Soluble Polyphenylene Ether Composite Material in a Millimeter-Wave Region*** Shoya Sekiguchi, Kota Oki, Shoko Mishima, Yuya Fukata, Kaho Shibasaki, Nobuhiro Ishikawa, and Toshiyuki Ogata – TAIYO HOLDINGS Co., Ltd.	***2. 8:25 AM - "Smart" Packaging of Self-Identifying and Localizable mmID for Digital Twinning and Metaverse Temperature Sensing Applications*** Charles Lynch, Ajibayo Adeyeye, and Manos Tentzeris – Georgia Institute of Technology
3. 8:50 AM - Chiplet-Based System PSI Optimization for 2.5D/3D Advanced Packaging Implementation Yoonjae Hwang, Sungwook Moon, Seungki Nam, and Jeong Hoon Ahn – Samsung Electronics Co., Ltd.	***3. 8:50 AM - Low-Dielectric, Low-Profile IC Substrate Material Development for 5G Applications*** Tomo Muguruma, Andy Behr, and Tom Shin – Panasonic Industrial Devices Sales Company of America; Hirosuke Saito, Koji Kishino, Fumito Suzuki, Hiroaki Umehara – Panasonic Industry Co., Ltd.	***3. 8:50 AM - Performance Analysis and Impact of Manufacturing Tolerances for 5G mmWave Antenna in Package/Module (AiP/AiM)*** Sheng-Chi Hsieh, Cheng-Yu Ho, Hong-Sheng Huang, Chia-Ching Chu, and Chen-Chao Wang – ASE Group
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Eventide Pavilion		
4. 10:00 AM - Double Side SiP of Structure Strength Analysis for 5G and Wearable Application Mike Tsai, Kevin Chang, Rios Hsieh, Wynn Li, Karina Chang, Ryan Chiu, Ethan Ding, Eric He, Tim Chang, and J. Y. Chen – Siliconware Precision Industries, Co. Ltd.	***4. 10:00 AM - Reliability Assessment of Ultra-Low-K Dielectric Material and Demonstration in Advanced Interposers*** Pragna Bhaskar, Christopher Blancher, Mohan Kathaperumal, Madhavan Swaminathan, and Mark Losego – Georgia Institute of Technology	***4. 10:00 AM - Compact Frequency Reconfigurable Array Antenna Based on Diagonally Placed Meander-Line Decouplers and PIN Diodes for Multi-Range Wireless Communications*** Suk-il Choi, Woosol Lee, and Yong-Kyu Yoon – University of Florida
5. 10:25 AM - A Laser Dicing Method for Plus-Shaped Dies for Heterogeneous Integration Applications Aakrati Jain, Kamal Sikka, Shidong Li, Juan-Manuel Gomez, Marc Bergendahl, and Spyridon Skordas – IBM Corporation; Roman Doll, Jeroen van Borkulo, Kees Biesheuvel, and Mark Mueller – ASM Laser Separation International B.V.	***5. 10:25 AM - Low Dielectric New Resin Cross-Linkers*** Takeshi Kumano, Yosuke Kurita, Kazunori Aoki, and Takashi Kashiwabara – Shikoku Chemicals Corporation	***5. 10:25 AM - High Gain and Low Back Radiation and Thin Antenna Designs Using Electromagnetic Bandgap Surface for Radar and Wearable Applications*** Lih-Tyng Hwang, Chun-Cheng Wang, Hung-Chih Lin, Ming-Yuan Huang, and Chih-Wen Kuo – National Sun Yat-sen University
6. 10:50 AM - 2.3D Hybrid Substrate with Ajinomoto Build-Up Film for Heterogeneous Integration Gary Chen, John Lau, Channing Cheng-Lin Yang, Jones Yu-Cheng Huang, Andy Yan-Jia Peng, Ning Liu, and T. J. Tseng – Unimicron Technology Corporation	***6. 10:50 AM - Solid-Diffusion Synthesis of Robust Hollow Silica Filler with Low Dk and Low Df*** Sicheng Luo, Ning Wang, Pengli Zhu, Tao Zhao, and Rong Sun – Shenzhen Institute of Advanced Electronic Materials	***6. 10:50 AM - Reconfigurable Antennas and FSS with Magnetically-Tunable Multiferroic Components*** Pawan Gaire, Veeru Jaiswal, John L. Volakis, Markondeya Raj Pulugurtha, and Shubhendu Bhardwaj – Florida International University
7. 11:15 AM - Advanced Packaging Technologies for Co-Packaged Optics Mei-Ju Lu, SinYuan Mu, ChiaSheng Cheng, and Jihan Chen – ASE Group	***7. 11:15 AM - Epoxy Wetting Flow and Adhesion Mechanism Within a Small Gap and Small Pitch Copper Pillar Structure*** Mary-Ann Gasser, Abdenacer Ait Mani, Alain Gueugnot, Thierry Mourier, and Patrick Peray – CEA-LETI; Loïc Vanel and Catherine Barentin – Institut Lumière Matière, Université Claude Bernard Lyon 1	***7. 11:15 AM - Electrically Small Folded Spherical Helix Antennas Utilizing Thick Solution Cast Nanomagnetic Films*** Nicholas Sturim and John Papapolymerou – Michigan State University; Edgar Aldama, Eric Drew, and John Zhang – Georgia Institute of Technology

Program Sessions: Wednesday, June 1, 8:00 a.m. - 11:40 a.m.

Session 4: Hybrid Bonding and Innovations for 3D Integration	Session 5: Bonding Technology: Novel Assembly Methods and Processes	Session 6: Emerging Modeling Including AI and Machine Learning
Committee: Interconnections	**Committee: Assembly & Manufacturing Technology**	**Committee: Thermal/Mechanical Simulation & Characterization**
Coral 1 & 2	**Coral 3 & 4**	**Coral 5**
Session Co-Chairs: **Katsuyuki Sakuma – IBM Corporation** **Email: ksakuma@us.ibm.com** **Seung Yeop Kook – GlobalFoundries** **Email: seung-yeop.kook@globalfoundries.com**	**Session Co-Chairs:** **Valerie Oberson – IBM Corporation** **Email: voberson@ca.ibm.com** **Jan Vardaman – TechSearch International** **Email: jan@techsearchinc.com**	**Session Co-Chairs:** **Przemyslaw Gromala – Robert Bosch GmbH** **Email: Przemyslawjakub.gromala@de.bosch.com** **Nancy Iwamoto** **Email: niwamoto@prodigy.net**
1. 8:00 AM - 3-Layer Stacking Technology with Pixel-Wise Interconnections for Image Sensors Using Hybrid Bonding of Silicon-on-Insulator Wafers Mediated by Thin Si Layers Masahide Goto, Yuki Honda, Masakazu Nanba, Yoshinori Iguchi, Takuya Saraya, Masaharu Kobayashi, Eiji Higurashi, Hiroshi Toshiyoshi, and Toshiro Hiramoto – NHK Science & Technology Research Laboratories	***1. 8:00 AM - The Influence of Copper Microstructure on Thermal Budget in Hybrid Bonding*** Laura Mirkarimi, Cyprian Uzoh, Dominik Suwito, Gill Fountain, Thomas Workman, Bongsub Lee, Jeremy Theil, and Guilian Gao – Xperi Corporation; Bryan Buckalew, Justin Oberst, and Thomas Ponnuswamy – Lam Research, Inc.	***1. 8:00 AM - Applied Modeling Framework in Integrated Circuit Design and Reliability*** Papa Momar Souare, Cedrick Bouchard, Eric Duchesne, and Francois Vachon – IBM Corporation; James Zaccardi and David Pettit – Viasat, Inc
2. 8:25 AM - Wafer to Wafer Hybrid Bonding for DRAM Applications Jinwon Park, Byungho Lee, Heesun Lee, Dail Lim, Jiho Kang, Changhyun Cho, and Myunghee Na – SK Hynix	***2. 8:25 AM - Collective Die-to-Wafer Self-Assembly for High Alignment Accuracy and High Throughput 3D Integration*** Alice Bond, Emilie Bourjot, Stéphan Borel, Thierry Enot, Pierre Montméat, Loïc Sanchez, and Frank Fournel – CEA-LETI; Johanna Swan – Intel Corporation	***2. 8:25 AM - Co-Design of Thermal Management with System Architecture and Power Management for 3D ICs*** Rishav Roy – Purdue University; Shidhartha Das, Benoit Labbe, Rahul Mathur, and Supreet Jeloka – Arm, Inc.
3. 8:50 AM - Analysis of Die Edge Bond Pads in Hybrid Bonded Multi-Die Stacks Jeremy Theil, Thomas Workman, Dominik Suwito, Laura Mirkarimi, Gill Fountain, KM Bang, Guilian Gao, Bongsub Lee, Pawel Mrozek, Cyprian Uzoh, and Michael Huynh – Xperi Corporation	***3. 8:50 AM - Fine-Pitch 30 µm Cu-Cu Bonding by Using Low Temperature Microfluidic Electroless Interconnection*** Yung-Sheng Lin, Yun-Ching Hung, Chin-Li Kao, Chung-Hung Lai, and David Tarng – ASE Group; Po-Shao Shih, Jeng-Hau Huang, and Robert C. Kao – National Taiwan University	***3. 8:50 AM - On-Chip Transient Hot Spot Detection with a Multiscale ROM in 3DIC Designs*** David Geb, Saeed Asgari, Akhilesh Kumar, Jimin Wen, Norman Chang, Stephen Pan, Mehdi Abarham, Haiyang He, and Viral Gandhi – Ansys
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Eventide Pavilion		
4. 10:00 AM - The Integration of Grounding Plane into TSV Integrated Ion Trap for Efficient Thermal Management in Large Scale Quantum Computing Device Peng Zhao, Yu Dian Lim, and Chuan Seng Tan – Nanyang Technological University; Hong Yu Li and Wen Wei Seit – Institute of Microelectronics (IME), A*STAR; Luca Guidoni – Universitée de Paris	***4. 10:00 AM - Die Bonding Solution for Flip Chip-Chip Scale Package-DIC (Digital Image Correlation) and Shadow Moiré Application*** Po Yu Liao, Ian Ho, David Lai, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.; Karen Chen, Hsin-Chih Shih, Dao-Long Chen, and David Tarng – ASE Group	***4. 10:00 AM - Implementation of Fully Coupled Electromigration Theory in COMSOL*** Zhen Cui and Guoqi Zhang – Delft University of Technology; Xuejun Fan – Lamar University
5. 10:25 AM - Wafer Stacked Wide I/O DRAM with One-Step TSV Technology Masaya Kawano, Xiang-Yu Wang, Qin Ren, Woon-Leng Loh, B.S.S. Chandra Rao, and King-Jien Chui – Institute of Microelectronics (IME), A*STAR; Tsuyoshi Kawagoe and Ichiro Homma – UltraMemory, Inc.	***5. 10:25 AM - Investigation of Low Temperature Co-Co Direct Bonding and Co-Passivated Cu-Cu Direct Bonding*** Demin Liu, Kuan-Chun Mei, Han-Wen Hu, Yi-Chieh Tsai, Huang-Chung Cheng, and Kuan-Neng Chen – National Yang Ming Chiao Tung University	***5. 10:25 AM - Peridynamic Modeling of Non-Fourier and Non-Fickian Diffusion in a Finite Element Framework*** Sundaram Vinod Anicode and Erdogan Madenci – University of Arizona
6. 10:50 AM - Recess Effect Study and Process Optimization of Sub-10 µm Pitch Die-to-wafer Hybrid Bonding Haoxiang Ren, Yu-Tao Yang, and Subramanian S. Iyer – University of California, Los Angeles	***6. 10:50 AM - Process and Design Optimization for Hybrid Cu Bonding Void*** Hyoeun Kim, Juhyeon Kim, Yeongseon Kim, Sun-Kyoung Seo, Chajea Jo, and Dae-Woo Kim – Samsung Electronics Co., Ltd.	***6. 10:50 AM - Feature Vector Based Remaining Useful-Life Assessment in Mechanical Shock and Vibration for Lead Free Electronics*** Pradeep Lall and Tony Thomas – Auburn University; Ken Blecker – US Army CCDC-AC
7. 11:15 AM - A Performance Testing Method of Bernoulli Picker for Ultra-Thin Die Handling Application Juno Kim, Dae Ho Min, Kangsan Lee, Kyeongbin Lim, and Minwoo Daniel Rhee – Samsung Electronics Co., Ltd.	***7. 11:15 AM - Laser-Assisted Bonding (LAB) Process and Its Bonding Materials as Technologies Enabling the Low-Carbon Era*** Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Ho-Gyeong Yun, Seok Hwan Moon, Ki-Seok Jang, Chanmi Lee, In-Seok Kye, Yoon-Hwan Moon, and Yong-Sung Eom – Electronics and Telecommunications Research Institute	***7. 11:15 AM - Genetic Algorithm Assisted Design of RDL Vias for a Fan-Out Panel Level SiC MOSFET Power Module Packaging*** Jiajie Fan, Jing Jiang, and Zhuorui Tang – Fudan University; Yichen Qian – Hohai University; Xuejun Fan – Lamar University; Guoqi Zhang – Delft University of Technology

Program Sessions: Wednesday, June 1, 1:30 p.m. - 5:30 p.m.

Session 7: Advanced Flip Chip and Embedded Substrate Technologies	Session 8: Hybrid and Direct Bonding Development and Characterization	Session 9: Millimeter-Wave Antenna-in-Package: Design, Manufacturing and Test
Committee: **Packaging Technologies**	**Committee:** **Interconnections**	**Committee:** **RF, High-Speed Components & Systems**
Silver Pearl 1	**Silver Pearl 2**	**Silver Pearl 3**
Session Co-Chairs: **Markus Leitgeb – AT&S** **Email: m.leitgeb@ats.net** **Luu Nguyen – Psi Quantum** **Email: lnguyen@psiquantum.com**	**Session Co-Chairs:** **Wei-Chung Lo – Industrial Technology Research Institute** **Email: lo@itri.org.tw** **C. Key Chung – TongFu Microelectronics Co., Ltd.** **Email: chungckey@hotmail.com**	**Session Co-Chairs:** **Xiaoxiong (Kevin) Gu** **Email: xgu@ieee.org** **P. Markondeya Raj – Florida International University** **Email: mpulugur@fiu.edu**
1. 1:30 PM - Flip-Chip Chip Scale Package (FCCSP) Process Characterization and Reliability of Coreless Thin Package with 7 nm Si Technology Eduardo De Mesa, Thomas Wagner, Beth Keser, Jan Proschwitz, and Bernd Waidhas – Intel Corporation	***1. 1:30 PM - Development of Face-to-Face and Face-to-Back Ultra-Fine Pitch Cu-Cu Hybrid Bonding*** Yoshihisa Kagawa, Takumi Kamibayashi, Kenya Nishio, Taichi Yamada, Yuriko Yamano, Akihisa Sakamoto, Kan Shimizu, Tomoyuki Hirano, and Hayato Iwamoto – Sony Semiconductor Solutions Corporation	***1. 1:30 PM - A 16 Element Antenna Integrated Package for 37-40GHz Operation*** Selaka Bulumulla – GlobalFoundries; Syed Rahman, Arun Natarajan, and Harish Krishnaswamy – MixComm
2. 1:55 PM - In-Package Ring Hybrid Coupler with On-Chip Termination Robert Trieb and Andy Heinig – Fraunhofer Institute for Integrated Circuits IIS	***2. 1:55 PM - Surface Energy Characterization for Die-Level Cu Hybrid Bonding*** Katsuyuki Sakuma, Roy Yu, Michael Belyansky, Marc Bergendahl, and Dale McHerron – IBM Corporation; Ming Li, Yiu Ming Cheung, Siu Cheung So, So Ying Kwok, and Siu WIng Lau – ASM Pacific Technologies, Ltd.	***2. 1:55 PM - FOWLP AiP for SOTM Applications*** Mei Sun, Teck Guan Lim, and Yong Han – Institute of Microelectronics (IME), A*STAR
3. 2:20 PM - Superconducting Molybdenum Multi-Chip Module Approach for Cryogenic and Quantum Applications Archit Shah, Sherman Peek, Vaibhav Gupta, Bhargav Yelamanchili, David Tuckerman, Chris Cantaloube, John Sellers, and Michael Hamilton – Auburn University	***3. 2:20 PM - Comprehensive Study on Advanced Chip on Wafer Hybrid Bonding with Copper/Polyimide Systems*** Toshiaki Shirasaka, Tadashi Okuda, and Tomoaki Shibata – Showa Denko Materials Co., Ltd.; Satoshi Yoneda and Daisaku Matsukawa – HD MicroSystems, Ltd.; M. Mariappan, Mitsumasa Koyanagi, and Takafumi Fukushima – Tohoku University	***3. 2:20 PM - Characteristics of Glass-Embedded FOAiP with Antenna Arrays for 60GHz mmWave Applications*** I-Hung Lin, Ying-Chieh Pan, and Tom Ni – Hon Hai Precision Industry Co., Ltd; Cheng-Chen Lin and Ben-Je Lwo – National Defense University
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall - Eventide Pavilion		
4. 3:30 PM - Functional Interposer Embedded with Multi-Terminal Si Capacitor for 2.5D/3D Applications Using Planarization and Bumpless Chip-on-Wafer (COW) Yoshiaki Satake, Tatsuya Funaki, Kyosuke Kobinata, Youngsuk Kim, and Takayuki Ohba – Tokyo Institute of Technology; Seiji Hidaka, Hitoshi Matsuno, and Shunsuke Abe – Murata Manufacturing Co., Ltd.; Chih-Cheng Hsiao and Sheng-Yi Li – Industrial Technolo	***4. 3:30 PM - Two-Step Ar/N2 Plasma-Activated Al Surface for Al-Al Direct Bonding*** Liangxing Hu, Yu Dian Lim, Peng Zhao, Michael Joo Zhong Lim, and Chuan Seng Tan – Nanyang Technological University	***4. 3:30 PM - Implementation of a Sub-THz FCCSP Organic Package for Millimeter Wave Applications*** Neelam Prabhu Gaunkar, Georgios Dogiamis, Telesphor Kamgaing, and Adel Elsherbini – Intel Corporation
5. 3:55 PM - 3D Embedded Power Package Module to Integrate Various Power Systems Byong Jin Kim, Hyeong Il Jeon, Dae Young Park, Gi Jeong Kim, Nam-Hee Cho, and Jin Young Khim – Amkor Technology	***5. 3:55 PM - Novel Ga Assisted Low Temperature Bonding for Fine Pitch Interconnects*** Shan-Bo Wang, An-Hsuan Hsu, Chin-Li Kao, and David Tarng – ASE Group; Chien-Lung Liang and Kwang-Lung Lin – National Cheng Kung University	***5. 3:55 PM - Slot Bow-Tie Antenna Integration in Flip-Chip and Embedded Die Enhanced QFN Package for WR8 and WR5 Frequency Band*** Aditya Jogalekar, Oscar Medina, Andrew Blanchard, Rashaunda Henderson, and Mahadevan Iyer – The University of Texas at Dallas; Tony Tang, Rajen Murugan, and Hassan Ali – Texas Instruments
6. 4:20 PM - Demonstration of Substrate Embedded Ni-Zn Ferrite Core Solenoid Inductors Using a Photosensitive Glass Substrate Jein Yu, Dongsu Kim, Insub Han, and Jongmin Yook – Korea Electronics Technology Institute	***6. 4:20 PM - Characterization of Die-to-Wafer Hybrid Bonding Using Heterogeneous Dielectrics*** Minki Kim, Soojeoung Park, Aeni Jang, Hyuekjae Lee, Seungduk Baek, ChungSun Lee, Ilhwan Kim, Jumyong Park, Youngkun Jee, Dae-Woo Kim, and Un-Byoung Kang – Samsung Electronics Co., Ltd.	***6. 4:20 PM - Antenna-Integrated, Die-Embedded Glass Package for 6G Wireless Applications*** Xiaofan Jia, Xingchen Li, Kyoung-sik Moon, Joon Woo Kim, Kai-Qi Huang, Matthew B. Jordan, and Madhavan Swaminathan – Georgia Institute of Technology
7. 4:45 PM - Fabrication and Characterization of Package Embedded Inductors for Integrated Voltage Regulators Prahalad Murali, Venkatesh Avula, Marisa Ahmed, Mark Losego, and Madhavan Swaminathan – Georgia Institute of Technology; Claudio Alvarez – Intel Corporation; Yusuke Oishi, Tomohito Uemura, Ryo Nagatsuka, and Naoki Watanabe – Panasonic Corporation	***7. 4:45 PM - Solder and Organic Adhesive Hybrid Bonding Technology with Non-Strip Type Photosensitive Resin and Injection Molded Solder (IMS)*** Keiji Matsumoto, Takahito Watanabe, Risa Miyazawa, Toyohiro Aoki, and Takashi Hisada – IBM Corporation; Yuzo Nakamura, Yasuhisa Kayaba, Jun Kamada, and Kazuo Kohmura – Mitsui Chemicals, Inc.	***7. 4:45 PM - Design and Testing of a WR28 Waveguide Blind Mating Interconnect for mmWave ATE OTA Applications*** Shiota Natsuki, Kikuchi Aritomo, Yuchang Liu, Daniel Lam, Takasu Hiromitsu, Mineo Hiroyuki, Kato Yasuyuki, and Jose Moreira – Advantest

Program Sessions: Wednesday, June 1, 1:30 p.m. - 5:30 p.m.

Session 10: Novel Photonics Packaging Technology	Session 11: Automotive and Harsh Environment	Session 12: Manufacturing and Assembly Process Modeling
Committee: Photonics	**Committee: Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Coral 1 & 2	**Coral 3 & 4**	**Coral 5**
Session Co-Chairs: **Ajey Jacob – University of Southern California** **Email: ajey@isi.edu** **Vivek Raghuraman – Broadcom Corporation** **Email: vivek.raghuraman@gmail.com**	**Session Co-Chairs:** **Pilin Liu – Intel Corporation** **Email: pilin.liu@intel.com** **Lakshmi N. Ramanathan – Meta, Inc.** **Email: laksh_r@hotmail.com**	**Session Co-Chairs:** **Pradeep Lall – Auburn University** **Email: lall@auburn.edu** **Yong Liu – ON Semiconductor** **yong.liu@onsemi.com**
1. 1:30 PM - Demonstration of Fan-Out Silicon Photonics Module for Next Generation Co-Packaged Optics (CPO) Application Bruce Chou, Aaron Zilkie, and David McCann – Rockley Photonics	***1. 1:30 PM - Cu-Al IMC Degradation Under High Electric Fields During HTOL Test*** Amar Mavinkurve, Rene Rongen, and Michiel van Soestbergen – NXP Semiconductors	***1. 1:30 PM - Multi-Physics Simulation of Wafer-to-Wafer Bonding Dynamics*** Nathan Ip, Nima Nejadsadeghi, and Carlos Fonseca – Tokyo Electron America, Inc.; Norifumi Kohama and Kimio Motoda – Tokyo Electron Kyushu, Ltd.
2. 1:55 PM - Optical Performance and Reliability Assessment from Self-Aligned Single Mode Fiber Attach for O-Band Silicon Photonics Platform Jae Kyu Cho, Benjamin Fasano, Vaishnavi Karra, Alberto Cestero, Norman Robson, George Wu, Thomas Houghton, Takako Hirokawa, Yusheng Bian, and Koushik Ramachandran – GlobalFoundries	***2. 1:55 PM - Effect of Underfill Property Evolution on Solder Joint Reliability in Automotive Applications*** Pradeep Lall, Madhu Kasturi, Yunli Zhang, Haotian Wu, Jeff Suhling, and Ed Davis – Auburn University	***2. 1:55 PM - Simulation and Verification of Ag-Cu Core-Shell Sintered Paste for Power Semiconductor Die-Attach Applications*** Xinyue Wang, Zejun Zeng, and Pan Liu – Fudan University; Jing Zhang – Heraeus Materials Technology, Ltd.; Guoqi Zhang – Delft University of Technology
3. 2:20 PM - Optical Fiber Pigtail Integration for Co-Package Alexander Janta-Polczynski – IBM Corporation; Martin Robitaille – LXsim	***3. 2:20 PM - Impact of the Final Finish on the Solder Joint Reliability and IMC Formation After Thermal Storage*** Britta Schafsteller, Sven Lamprecht, and Gustavo Ramos – Atotech Deutschland GmbH	***3. 2:20 PM - Transient Thermal Modeling of Die Bond Process in Multiple Die Stacked Flash Memory Package*** Yangming Liu, Ning Ye, Bo Yang, Xu Wang, Jacky Liu, Shenghua Huang, and Chin-Tien Chiu – Western Digital
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall - Eventide Pavilion		
4. 3:30 PM - A Novel Packaging Platform for High-Performance Optical Engines in Hyperscale Data Center Applications Sajay Bhuvanendran Nair Gourikutty, Ming Chinq Jong, Chockanathan Vinoth Kanna, David Soon Wee Ho, Seit Wen Wei, Sharon Lim Pei Siang, Jiaqi Wu, Teck Guan Lim, Rathin Mandal, and Surya Bhattacharya – Institute of Microelectronics (IME), A*STAR; Jason Tsung-Liow – Rain Tree Photonics Pte. Ltd.	***4. 3:30 PM - New Lifetime Model for Advanced Power Semiconductor Interconnects*** Alexander Schiffmacher, Ahmad Bashiti, David Strahringer, and Juergen Wilde – University of Freiburg; Carsten Kempiak and Andreas Lindemann – Otto-von-Guericke University; Jacek Rudzki – Danfoss Silicon Power GmbH	***4. 3:30 PM - Novel Method for NCF Flow Simulation in HBM Thermal Compression Bonding Process to Optimize the NCF Shape*** Jong Pa Hong, Su Chang Lee, Sun Woo Han, Sang Kun Oh, Sang Sik Park, Hyeong Mun Kang, Won Keun Kim, Kil Soo Kim, and Dan Oh – Samsung Electronics Co., Ltd.
5. 3:55 PM - Advanced 2.5D and 3D Packaging Technologies for Next Generation Silicon Photonics in High Performance Networking Applications Sandeep Razdan, Jie Xue, Peter De Dobbelaere, Aparna Prasad, and Vipul Patel – Cisco Systems, Inc.	***5. 3:55 PM - Thermal and Mechanical Optimization to Enable Reliable High Performance Liquid-Cooled Compute System for Level 4 Autonomous Driving*** Fen Chen, Gilberto Madrid, Brian Schlotterbeck, Jagdeep Singh, Adli Nureddin, Tyler Sawyer, Zoran Stefanoski, Spencer Klimpke, Hector Guajardo, Arul Ramalingam, and Maik Duwensee – Cruise Automation	***5. 3:55 PM - Numerical Evaluation on SiO2 Based Chip to Wafer Hybrid Bonding Performance by Finite Element Analysis*** Lin Ji and Sasi Kumar Tippabhotla – Institute of Microelectronics (IME), A*STAR
6. 4:20 PM - 90-Degree Bent Core Polymer Optical Waveguide Coupler for Low Loss Lens-Less Light Coupling Between Laser/Photodetector and Fiber Daiki Suemori, Maho Ishii, Naohiro Kohmu, and Takaaki Ishigure – Keio University	***6. 4:20 PM - Comprehensive Study of Long-Term Reliability of Copper Bonding Wires at Harsh Automotive Conditions*** Robert Klengel, Sandy Klengel, Sebastian Tismer, and Thomas Ackermann – Fraunhofer Institute for Microstructure of Materials and Systems (IMWS); Noritoshi Araki, Motoki Eto, Teruo Haibara, and Takashi Yamada – Nippon Micrometal Corporation; Jochen Feldmann, Ralph Binner, and Henk Peters – Elmos Semiconductor SE	***6. 4:20 PM - A Novel Equivalent Model for Underfill Molding Process on 2.2D Structure for High Performance Applications*** Yu-En Liang, Chia-Peng Sun, and Chih Chung Hsu – CoreTech System (Moldex3D); Dyi-Chung Hu and EH Chen – SiPlus Co., Ltd.; Jeffrey (Chang-Bing) Lee – iST-Integrated Service Technology, Inc.
7. 4:45 PM - Lossless High-Speed Silicon Photonic MZI Switch with a Micro-Transfer-Printed III-V Amplifier Jing Zhang, Clemens J. Kruckel, and Laurens Bogaert – Ghent University; Bahawal Haq; Johanna Rimböck, Bozena Matuskova, and Stefan Ertl – EV Group; Agnieszka Gocalinska, Emanuele Pelucchi, and Brian Corbett – Tyndall National Institute	***7. 4:45 PM – Post Wire Bonding Coating for Prevention of Corrosion of Wire Bonded Packages by Chlorine Containing Foreign Particles*** Varughese Mathew, Sheila Chopin, Guangming Li, and Sean Xu – NXP Semiconductors	***7. 4:45 PM - Key Steps from Laboratory Towards Mass Production: Optimization of Electroless Plating Process Through Numerical Simulation*** Simon Johannes Gräfner, Jeng-Hau Huang, Yu-An Chen, Po-Shao Shih, Ching-Han Huang, and C. Robert Kao – National Taiwan University

Program Sessions: Thursday, June 2, 8:00 a.m. - 11:40 a.m.

Session 13: Technologies for Heterogeneous Integration, Automotive and Power Electronics	Session 14: Novel Bonding and and Stacking Technologies	Session 15: Enhanced Methods & Processes for Heterogeneous Integration Assembly
Committee: Packaging Technologies	**Committee: Materials & Processing joint with Assembly & Manufacturing Technology**	**Committee: Assembly & Manufacturing Technology**
Silver Pearl 1	**Silver Pearl 2**	**Silver Pearl 3**
Session Co-Chairs: **Dean Malta – Micross Advanced Interconnect Technology** **Email: Dean.Malta@micross.com** **Peng Su – Juniper Networks** **Email: pensu@juniper.net**	**Session Co-Chairs:** **Bing Dang – IBM Corporation** **Email: dangbing@us.ibm.com** **Hongbin Yu – Arizona State University** **Email: yuhb@asu.edu**	**Session Co-Chairs:** **Christo Bojkov – Qorvo** **Email: cbojkov.ectc@gmail.com** **Jason Rouse – Corning Incorporated** **Email: rousejh@corning.com**
1. 8:00 AM - A Novel 3D Driver-Integrated Silicon Carbide Half-Bridge Power Module with Low Stray Inductance Chun-Kit Cheung and Ziyang Gao – Hong Kong Applied Science & Technology Research Institute	***1. 8:00 AM - Behavior of Bonding Strength on Wafer-to-Wafer Cu-Cu Hybrid Bonding*** Shunsuke Furuse, Nobutoshi Fujii, Kengo Kotoo, Naoki Ogawa, Taichi Yamada, Takaaki Hirano, Suguru Saito, Yoshiya Hagimoto, and Hayato Iwamoto – Sony Semiconductor Solutions Corporation	***1. 8:00 AM - Super Fine Jet Underfill Dispense Technique for Robust Micro Joint in Direct Bonded Heterogeneous Integration (DBHi) Silicon Bridge Packages*** Akihiro Horibe, Chinami Marushima, Takahito Watanabe, Aakrati Jain, Eric Turcotte, Isabel de Sousa, Takashi Hisada, and Kamal Sikka – IBM Corporation
2. 8:25 AM - Static/Transient Thermal Analysis and Design Optimization of a Lead Frame Based Dual Side Cooling SiC Power Module Gongyue Tang and Kazunori Yamamoto – Institute of Microelectronics (IME), A*STAR	***2. 8:25 AM - Development of Polyimide Base Photosensitive Permanent Bonding Adhesive for Middle to Low Temperature Hybrid Bonding Process*** Satoshi Yoneda, Kenya Adachi, Daisaku Matsukawa, and Takahiro Tanabe – HD Microsystems, Ltd.; Kaori Kobayashi, Toshiaki Shirasaka, Shizu Fukuzumi, and Tadashi Okuda – Showa Denko Materials Co., Ltd.	***2. 8:25 AM - Assembly Challenges and Demonstrations of Ultra-Large Antenna in Package for Automotive Radar Applications*** Sharon Pei Siang Lim, Ser Choong Chong, David Ho Soon Wee, and Tai Chong Chai – Institute of Microelectronics (IME), A*STAR
3. 8:50 AM - Impact of Reliability Tests on the Adhesion of the Epoxy Mold Compound David Guillon, Andris Avots, Katrin Schlegel, Milad Maleki, and Isabell Ehrler – Hitachi Energy	***3. 8:50 AM - Direct Bonding Using Low Temperature SiCN Dielectrics*** Serena Lacovo, Fuya Nagano, Venkat Sunil Kumar Channam, Anne Jourdain, Kris Vanstreels, Alain Phommahaxay, and Eric Beyne – Imec; Edward Walsby, Kath Crook, and Keith Buchanan – SPTS Technologies	***3. 8:50 AM - Investigation on Package Warpage and Reliability of the Large Size 2.5D Molded Interposer on Substrate (MIoS) Package*** Soohyun Nam, Jinhyun Kang, Ilbok Lee, Hae Jung Yu, Chajea Jo, and Dae-Woo Kim – Samsung Electronics Co., Ltd.
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Eventide Pavilion		
4. 10:00 AM - Advanced Thermal Integration for HPC Packages with Two-Phase Immersion Cooling Po-Yao Lin, Sheng-Liang Kuo, Kathy Yan, Wen-Ming Chen, and Marvin De-Dui Liao – Taiwan Semiconductor Manufacturing Company, Ltd.	***4. 10:00 AM - Heterogeneous Integration by the 3D Stacking of Thin Silicon Die*** Pavani Vamsi Krishna Nittala, Karthika Haridas, and Prosenjit Sen – Indian Institute of Science	***4. 10:00 AM - Characterizations and Challenges of Adhesion Promotion Solutions for HSIO Package Development*** Yi Yang, Marcel Wall, Rengarajan Shanmugam, Sarah Wozny, Xin Yan, Mohit Khurana, Rajeev Ranjan, Dilan Seneviratne, Kassandra Nikkhah, and Suddhasattwa Nad – Intel Corporation
5. 10:25 AM - Hybrid Stacked-Die Package Solution for Extremely Small-Form-Factor Package Heeseok Lee, Kyoung Min Lee, Daehan Youn, Kyojin Hwang, and Junghwa Kim – Samsung Electronics Co., Ltd.	***5. 10:25 AM - Prolongation of Surface Activation Effect Using Self-Assembled Monolayer for Low Temperature Bonding of Au*** Kai Takeuchi and Tadatomo Suga – Meisei University; Beomjoon Kim – University of Tokyo	***5. 10:25 AM - Heterogeneous Integration for Chiplets on FOWLP Development Line*** Chai Tai Chong, David Ho, Chong Ser Chong, Sharon Lim PS, and Surya Bhattacharya – Institute of Microelectronics (IME), A*STAR
6. 10:50 AM - Thermo-Mechanical Analysis of Thermal Compression Bonding Chip-Join Process Prabudhya Roy Chowdhury, Katsuyuki Sakuma, Sathya Raghavan, Marc Bergendahl, Kamal Sikka, Sayuri Kohara, Takashi Hisada, Hiroyuki Mori, Divya Taneja, and Isabel De Sousa – IBM Corporation	***6. 10:50 AM - Mini LED Array Transferred onto a Flexible Substrate Using Simultaneous Transfer and Bonding (SITRAB) Process and Anisotropic SITRAB Film (ASF)*** Jiho Joo, Gwang-Mun Choi, Chanmi Lee, In-Seok Kye, Ki-seok Jang, Yong-Sung Eom, and Kwang-Seong Choi – Electronics and Telecommunications Research Institute; Jeong Duck Kim and Seok Tae Hwang – Nexstar Technology Co., Ltd.	***6. 10:50 AM - Split-Fabric: A Novel Wafer-Scale Hardware Obfuscation Methodology Using Silicon Interconnect Fabric*** Yousef Safari and Boris Vaisband – McGill University; Yu-Tao Yang and Subramanian S. Iyer – University of California, Los Angeles; Toshifumi Nakatani – Maxentric Technologies LLC; Neal Levine – Defense Microelectronics Activity (DMEA)
7. 11:15 AM - Dimensional Parameters Controlling Capillary Underfill Flow for Void-Free Encapsulation of a Direct Bonded Heterogeneous Integration (DBHi) Si-Bridge Package Chinami Marushima, Toyohiro Aoki, Koki Nakamura, Risa Miyazawa, Akihiro Horibe, Isabel De Sousa, Takashi Hisada, and Kamal Sikka – IBM Corporation	***7. 11:15 AM - Characterization of Non-Conductive Paste Materials (NCP) for Thermocompression Bonding in a Direct Bonded Heterogeneously Integrated (DBHi) Si-Bridge Package*** Akihiro Horibe, Takahito Watanabe, Chinami Marushima, Hiroyuki Mori, Sayuri Kohara, Roy Yu, Marc Bergendahl, Teddie Magbitang, Rudy Wojtecki, Divya Taneja, and Maxime Godard – IBM Corporation	***7. 11:15 AM - A Self-Aligned Structure Based on V-Groove for Accurate Silicon Bridge Placement*** Yang Qiu, Yann Beilliard, and Isabel De Sousa – University of Sherbrooke; Dominique Drouin – IBM Corporation

Program Sessions: Thursday, June 2, 8:00 a.m. - 11:40 a.m.

Session 16: Hybrid & Direct Bonding Innovation, Optimization & Yield Improvement	Session 17: Novel Characterization Techniques and Test Methods	Session 18: Flexible, Wearable Sensors and Electronics
Committee: Interconnections	**Committee: Applied Reliability**	**Committee: Emerging Technologies**
Coral 1 & 2	**Coral 3 & 4**	**Coral 5**
Session Co-Chairs: **Xin Yan – Intel Corporation** **Email: xin.yan@intel.com** **Kangwook Lee – SK Hynix** **Email: steward.lee@sk.com**	**Session Co-Chairs:** **Sandy Klengel – Fraunhofer IZM** **Email: sandy.klengel@imws.fraunhofer.de** **Pei-Haw Tsao – Taiwan Semiconductor Manufacturing Company, Ltd.** **Email: phtsao@tsmc.com**	**Session Co-Chairs:** **Chukwudi Okoro – Corning Incorporated** **Email: okoroc@corning.com** **Isaac Robin Abothu – Siemens Healthineers** **Email: Isaac.abothu@siemens-healthineers.com**
1. 8:00 AM - The Wafer Bonding Yield Improvement Through Control of SiCN Film Composition and Cu Pad Shape Dail Rim, Byungho Lee, Jinwon Park, Changhyun Cho, Jiho Kang, and Ilseop Jin – SK Hynix	***1. 8:00 AM - Anisotropy of Curing Residual Stress of Underfill in the Encapsulation Under Three-Dimensionally Constrained Condition Based on In-Situ Characterization*** Tao Peng, Xiaohui Peng, Wenjie Wu, Liang Peng, Gang Li, Jingbao Yang, Yuanyuan Yang, Jing Chen, CaiPing Zhu, Pengli Zhu, and Rong Sun – Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences	***1. 8:00 AM - Robustness and Reliability of Novel Anisotropic Conductive Epoxy for Stretchable Wearable Electronics*** Andrew Stemmermann, Daniel Balder, and Madhu Stemmermann – SunRay Scientific, Inc.; Nancy Stoffel – General Electric; Riadh Al-Haidari, Behnam Garakani, Udara Somarathna, El Medhi Abbara, Mohammed Alhendi, and Mark Poliks – Binghamton University; Christopher Tabor – Air Force Research Laboratory
2. 8:25 AM - Low Temperature Wafer-to-Wafer Hybrid Bonding by Nanocrystalline Copper Wei-Lan Chiu, Ou-Hsiang Lee, Chia-Wen Chiang, and Hsiang-Hung Chang – Industrial Technology Research Institute	***2. 8:25 AM - QFN (Quad Flat No–Lead) Solder Joint Under Thermal Cycling: Identification of Two Failure Mechanisms*** Emna Ben Romdhane, Pierre Romanille, and Samuel Pin – IRT Saint-Exupéry; Alexandrine Guédon-Garcia and Hélène Frémont – IMS Laboratory; Patrick Nugyen – Elemca	***2. 8:25 AM - Wireless Nanomembrane Electronics and Soft Packaging Technologies for Noninvasive, Real-Time Monitoring of Muscle Activities*** Hojoong Kim and Woon-Hong Yeo – Georgia Institute of Technology; Hyojung J. Choo – Emory University
3. 8:50 AM - Cu-SiO2 Hybrid Bonding Yield Enhancement Through Cu Grain Enlargement M. Mariappan and T. Fukushima – Global INTegration Initiative; K. Mori and M. Koyanagi – T-Micro; M. Sawa and E. Sone – JCU Corporation	***3. 8:50 AM - Tracking In-Die Mechanical Stress Through Silicon Embedded Sensors for Advanced Packaging Applications*** Sharad Saxena, Christopher Hess, Michele Quarantelli, Alberto Piadena, Larg Weiland, Rakesh Vallishayee, Yuan Yu, Dennis Ciplickas, Tomasz Brozek, and Andrzej Strojwas – PDF Solutions	***3. 8:50 AM - Modeling of Spreading Behavior of UV-Curable Dielectric Ink from its Rheological Characteristics*** Sujie Kang, Jung Shin Lee, Jung Woo Cho, Sun Woo Park, Seungdon Lee, Hyunjin Lee, and Daniel Min Woo Rhee – Samsung Electronics Co., Ltd.
Refreshment Break: 9:15 a.m. - 10:00 a.m. Exhibit Hall - Eventide Pavilion		
4. 10:00 AM - A Holistic Development Platform for Hybrid Bonding Liu Jiang, Srikrishna Sitaraman, Sefa Dag, Mohammad Masoomi, Kwangwon Choi, Ying Wang, Prayudi Linato, Gilbert See, El Mehdi Bazizi, and Blessy Alexander – Applied Materials, Inc.	***4. 10:00 AM - Damage Evolution of Double-Sided Copper Conductor on Multi-Layer Flexible Substrate Under Bending*** Rui Chen, Justin Chow, and Suresh Sitaraman – Georgia Institute of Technology	***4. 10:00 AM - Fabrication of Flexible Li-ion Battery Electrodes Using "Battlets" Approach with Ionic Liquid Electrolyte for Powering Wearable Devices*** Guangqi Ouyang, Grace Whang, Emily MacInnis, Haoxiang Ren, Henry Sun, Randall Irwin, and Subramanian S. Iyer – University of California, Los Angeles
5. 10:25 AM - Low Temperature Fine-Pitch Cu-Cu Bonding Using Au Nanoparticles as Intermediate Jun-Peng Fang, Jian Cai, Qian Wang, and Xiu-Yu Shi – Tsinghua University; Kai Zheng and Yi-Kang Zhou – Semiconductor Technology Innovation Center (Beijing) Corporation	***5. 10:25 AM - Investigation of Stress Generated by Interconnection Processes with Micro-Raman Spectroscopy (mRS)*** E Liu, Sri Krishna Bhogaraju, Kerstin Lux, and Gordon Elger – Technische Hochschule Ingolstadt; Rokeya Mumtahana Mou – Fraunhofer IVI	***5. 10:25 AM - Smart Biofeedback Earbud Achieved by SIP with 3D Composite Polymer Package*** Kuei-Hao Tseng, Chih-Lung Lin, Kai-Hung Wang, and Harrison Chang – ASE Group
6. 10:50 AM - Wet Atomic Layer Etching of Copper Structures for Highly Scaled Copper Hybrid Bonding and Fully Aligned Vias Christopher Netzband and Sitaram Arkalgud – TEL Technology Center, America, LLC; Paul Abel and Jacques Faguet – Tokyo Electron America, Inc.	***6. 10:50 AM - Development and Application of the Moisture-Dependent Viscoelastic Model of Polyimide in Hygro-Thermo-Mechanical Analysis of Fan-Out Interconnect*** Chia-Ming Yang and Tz-Cheng Chiu – National Cheng Kung University; Wei-Jie Yin, Dao-Long Chen, Chin-Li Kao, and David Tarng – ASE Group	***6. 10:50 AM - Current Carrying Capacity of Inkjet Printed Nano-Silver Interconnects on Mesoporous PET Substrate*** El Mehdi Abbara, Gurvinder Singh Khinda, Mohammed Alhendi, Riadh Alhaidari, Behnam Garakani, Udara Somarathna, and Mark Poliks – Binghamton University
7. 11:15 AM - A Study on Bonding Pad Structure and Layout for Fine Pitch Hybrid Bonding SeonKyeong Seo, HyoEun Kim, YeongSeon Kim, Chaje Cho, and DaeWoo Kim – Samsung Electronics Co., Ltd.	***7. 11:15 AM - A Novel Quantitative Adhesion Measurement Method for Thin Polymer and Metal Layers for Microelectronic Applications*** Markus Woehrmann, Michael Schiffer, Piotr Mackowiak and Klaus-Dieter Lang – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University of Berlin	***7. 11:15 AM - Fabrication of Wearable Strain Sensor by Using a Novel Hybrid Cu Ink Composed of Bimodal Cu Particle Ink and Cu-Based Metal-Organic Decomposition Ink*** Cong Gan, Hai-Jun Huang, Bin Hou, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

Program Sessions: Thursday, June 2, 1:30 p.m. - 5:30 p.m.

Session 19: Advances in Fan-Out Panel Level Packaging

Committee:
Packaging Technologies

Silver Pearl 1

Session Co-Chairs:
Albert Lan – Applied Materials, Inc.
Email: Albert_Lan@amat.com
Jie Fu – Apple, Inc.
Email: fujie6@gmail.com

1. 1:30 PM - Panel Level Packaging – Where are the Technology Limits?
Tanja Braun, Ole Hölck, Mattis Obst, Steve Voges, Ruben Kahle, Lars Böttcher, Mathilde Billaud, Lutz Stobbe, Karl-Friedrich Becker, and Rolf Aschenbrenner – Fraunhofer IZM; Marcus Voitel – Technical University Berlin

2. 1:55 PM - Study of Reliable Via Structure for Fan-Out Panel Level Package (FOPLP)
Da-Hee Kim, Jae-Ean Lee, Gyujin Choi, Sunguk Lee, Giho Jeong, Hongwon Kim, Seokwon Lee, and Dong wook Kim – Samsung Electronics Co., Ltd.

3. 2:20 PM - A Hybrid Panel Level Package (Hybrid PLP) Technology Based on a 650-mm x 650-mm Platform
Eoin O´Toole, Luís Silva, Filipe Cardoso, José Silva, Aníbal Coelho, Márcio Souto, Nuno Delduque, José Silva, WonChul Do, and JinYoung Khim – Amkor Technology

Session 20: Enhancements in Fine-Pitch Interconnects, Redistribution Layers and Through-Vias

Committee:
Materials & Processing

Silver Pearl 2

Session Co-Chairs:
Ivan Shubin – RAM Photonics LLS
Email: ishubin@gmail.com
Jayaram Vidya – Intel Corporation
Email: vidya.jayaram@intel.com

1. 1:30 PM - A Study of Failure Mechanism in the Formation of Fine RDL Patterns and Vias for Heterogeneous Packages in Chip Last Fan-Out Panel Level Packaging
Yoon Young Jeon, Youngmin, Minju Kim, Sangyun Lee, Hyun-Dong Lee, Changbo Lee, and Joon Seok Oh – Samsung Electronics Co., Ltd.

2. 1:55 PM - Novel Plasma Process for Build-Up Film in the Fine Wiring Fabrication
Daisuke Hironiwa, Yasuhiro Morikawa, Atsuhito Ihori, and Ryuichiro Kamimura – ULVAC, Inc.

3. 2:20 PM - Fine Copper Lines with High Adhesion on High Rigidity Dielectrics
Masataka Nishida, Hirokazu Noma, Masaki Yamaguchi, and Kazuyuki Mitsukura – Showa Denko Materials Co., Ltd.

Session 21: Millimeter-Wave RF Components and Modules for 5G

Committee: RF, High-Speed Components & Systems

Silver Pearl 3

Session Co-Chairs:
Craig Gaw – NXP Semiconductor
Email: c.a.gaw@ieee.org
Jaemin Shin – Apple, Inc.
Email: sjm1218@gmail.com

1. 1:30 PM - Metaconductor Based Highly Energy Efficient Differential Striplines for 112 Gbps Data Bus with Sub 0.1 dB/mm Package Insertion Loss
Hae-In Kim, Saeyeong Jeon, and Yong-Kyu Yoon – University of Florida; Rockwell Hsu and Brice Achkir – Cisco Systems, Inc.

2. 1:55 PM - Multi-Terminal Ultra-Thin 3D Nanoporous Silicon Capacitor Technology for High-Speed Circuits Decoupling
Mohamed Mehdi Jatlaoui, Seiji Hidaka, and Ryo Kasai – Murata Integrated Passive Solutions, SAS; Sho Kubota, Masato Takesawa, Charles Muller, Florent Lallemand, Shunsuke Abe, Takashi Takeuchi, and Hitoshi Matsuno – Murata Manufacturing Co., Ltd.

3. 2:20 PM - Mechanical and Ka-Band Electrical Reliability Testing of Interconnects in 5G Wearable System-on-Package Designs Under Bending
Yi Zhou, Kexin Hu, Manos M. Tentzeris, and Suresh K. Sitaraman – Georgia Institute of Technology

Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall - Eventide Pavilion

4. 3:30 PM - Package Reliability Evaluation of 600mm FOPLP with 6-Sided Die Protection with 0.35mm Ball Pitch
Jacinta Aman Lim, Brett Dunlap, Sungeun Hong, Hyung-Jin Shin, and Byung Cheol Kim – nepes Corporation

5. 3:55 PM - Panel-Based Large-Scale RDL Interposer Fabricated Using 2-Micron Pitch Semi-Additive Process for Chiplet-Based Integration
Hiroshi Kudo, Takamasa Takano, Hiroshi Mawatari, Daisuke Kitayama, Takahiro Tai, Tsuyoshi Tsunoda, and Satoru Kuramochi – Dai Nippon Printing (DNP) Co., Ltd.

6. 4:20 PM - Harnessing the Power of 4nm Silicon with Gen 2 M-Series™ Fan-Out and Adaptive Patterning® Providing Ultra-High-Density 20µm Device Bond Pad Pitch
Robin Davis and Benedict San Jose – Deca Technologies

7. 4:45 PM - All Copper Is Not Created Equal – Examples of Grain Engineering In Plating
Yun Zhang, Jing Wang, Peipei Dong, Xingxing Zhang, Wei Zhao, and Josh Liang – Shinhao Materials LLC; Michael Herkommer, Klaus Leyendecker, and Volker Wohlfarth – Umicore Galvanotechnik GmbH

4. 3:30 PM - Fabrication and Characterization of Nanoporous Gold (NPG) Interconnects for Wafer Level Packaging
Lothar Dietrich, Hermann Oppermann, Christina Lopper, and Piotr Mackowiak – Fraunhofer IZM

5. 3:55 PM - Role of (111) Nanotwinned Cu on Dissolution Behavior and Interfacial Reaction in Micro-Scale Nanotwinned Cu/Sn/Ni Interconnects
Mingliang Huang, Shengbo Wang, and Jing Ren – Dalian University of Technology

6. 4:20 PM - Approaches for a Solely Electroless Metallization of Through-Glass Vias
Aleksandra M. Zawacka, Maren S. Prediger, Alexander Kassner, and Folke Dencker – Leibniz University Hannover; Marc C. Wurz – Ulm University

7. 4:45 PM - Atmospheric HF Vapor Based Silicon Etching with Pt Catalyst for High Fidelity Through Silicon Via (TSV) Fabrication
Sunghyun Hwang and Yong-Kyu Yoon – University of Florida; William N. Carr – Phononic MEMS, Inc.

4. 3:30 PM - X-band Passive Circuits Using 3-D Printed Hollow Substrate Integrated Waveguides
Yihang Chu, Yamini Kotriwar, Ethan Kepros, Brian Wright, and Premjeet Chahal – Michigan State University

5. 3:55 PM - A Novel Simulation Methodology Reflecting System Power Scenario Using a Markov-Chain-based Stochastic Random Power Model
Woo-Jin Na, Kun Joo, Rakjoo Sung, Kyudong Lee, Ji-Hye Yang, Kyungsun Kim, Young-Ho Lee, Seung-Hee Mun, SungJoo Park, and Jeong-Hyeon Cho – Samsung Electronics Co., Ltd.

6. 4:20 PM - Towards Mass Production of Air Filled Substrate Integrated Waveguides (AFSIW) for Ultra-Low Loss, Broadband Radar Applications
Heinrich Trischler and Erich Schlaffer – AT&S; Siddhartha Sinha and Ilja Ocket – Imec

7. 4:45 PM - Characterisation of RF Components and Connectors for Advanced 5G Applications
Kimmo Rasilainen, Marko E. Leinonen, Olli Kursu, Klaus Nevala, Shayan Hasan Naushahi, Juha-Matti Ojakoski, Markus Berg, and Aarno Pärssinen – University of Oulu

Program Sessions: Thursday, June 2, 1:30 p.m. - 5:30 p.m.

Session 22: AI, Quantum Computing and Novel 3D Packaging Solutions	Session 23: Advanced Processes for Manufacturing and Yield Enhancement	Session 24: Thermal Management and Warpage Analysis of Highly Integrated Packages
Committee: Emerging Technologies	**Committee: Assembly & Manufacturing Technology**	**Committee: Thermal/Mechanical Simulation & Characterization**
Coral 1 & 2	**Coral 3 & 4**	**Coral 5**
Session Co-Chairs: **Yang Liu – Nokia Bell Labs** **Email: yang3d@gmail.com** **Vaidyanathan Chelakara – Acacia Communications** **Email: cvaidyanathan@acacia-inc.com**	**Session Co-Chairs:** **Shichun Qu** **Email: shichun.qu@gmail.com** **Mark Gerber – ASE Group** **Email: mark.gerber@aseus.com**	**Session Co-Chairs:** **Karsten Meier – Technische Universität Dresden** **Email: karsten.meier@tu-dresden.de** **Suresh K. Sitaraman – Georgia Institute of Technology** **Email: suresh.sitaraman@me.gatech.edu**
1. 1:30 PM - RF Characterization on Nb-Based Superconducting Silicon Interconnect Fabric for Future Large-Scale Quantum Applications Yu-Tao Yang, Haoxiang Ren, Su Kong Chong, Gang Qiu, Shu-Yun Ku, Yang Cheng, Chaowei Hu, Tiema Qian, Kuan-Neng Chen, Ni Ni, and Kang L. Wang – University of California, Los Angeles	***1. 1:30 PM - Demonstration of Flexible Encapsulation in Assembly Industry*** Chao-Wei Liu, Ming-Hung Chen, Tun-Ching Pi, Jen-Chieh Kao, and Yung-I Yeh – ASE Group	***1. 1:30 PM - Thermal Challenges and Design Considerations in Heterogeneous Integrated Through-Silicon-Interposer Platform with Flipped III-V HEMT Chiplets*** Haoran Chen, Teck Guan Lim, and Gongyue Tang – Institute of Microelectronics (IME), A*STAR
2. 1:55 PM - Development of Cu-Cu Side-by-Side Interconnection Using Controlled Electroless Cu Plating Yu-An Chen, Po-Shao Shih, Fu-Ling Chang, Simon Johannes Gräfner, Jeng-Hau Huang, Ching-Han Huang, and C. Robert Kao – National Taiwan University; Yung-Sheng Lin, Yun-Ching Hung, Chin-Li Kao, and David Tarng – ASE Group	***2. Pretreatment and Structuring of Spatial Circuit Carriers Based on Alumina for High Temperatures and High Frequencies*** Philipp Braeuer, Thomas Stoll, Martin Muckelbauer, Alexander Hensel, and Joerg Franke – Institute FAPS, FAU	***2. 1:55 PM - Assessment of Thermal-Aware Floorplans in a 3D IC for Server Applications*** Ki Wook Jung, Sungeun Jo, Minwoo Cho, Seunggeol Ryu, Sunggu Kang, Jaechoon Kim, and Dan (Kyung Suk) Oh – Samsung Electronics Co., Ltd.
3. 2:20 PM - Design of Compact Microwave Multiplexer for RF Reflectometry Characterization of Silicon-Based Spin Qubits Vignesh Shanmugam Bhaskar and Mihai Dragos Rotaru – Institute of Microelectronics (IME), A*STAR	***3. 2:20 PM - 10µm Pitch Bumping of Singulated Die Using a Temporary Metal-Embedded Chip Assembly Process*** Souheil Nadri, B.-A. Clayton Tu, Florian Herrault, Courtney Wilt, Partia Naghibi, Marko Pavlov, Joel Wong, and Vu Phan – HRL Laboratories, LLC	***3. 2:20 PM - Effect of Storage on Reliability of Thin-Flexible Laminated and Unlaminated Batteries in Wearable Applications*** Pradeep Lall and Ved Soni – Auburn University
Refreshment Break: 2:45 p.m. - 3:30 p.m. Exhibit Hall - Eventide Pavilion		
4. 3:30 PM - Small Package Size Low Power CMOS Image Sensor Using Two Different Type Small Through Silicon Vias Technology for 3D Packaging Hoi-Jin Lee, Heeseok Lee, and Kyunghwan Lee – Samsung Electronics Co., Ltd.	***4. 3:30 PM - Realization of High A/R and Fine Pitch Cu Pillars Incorporating High Speed Electroplating with Novel Strip Process*** Se-Chul Park, Jong-Ho Park, Seonghoon Bae, Jun-young Park, Taehwa Jeong, Hyojin Yun, Kwangok Jeong, Seokbong Park, Ju-il Choi, Un-Byoung Kang, and Dongwoo Kang – Samsung Electronics Co., Ltd.	***4. 3:30 PM - Modeling and Design for System-Level Reliability and Warpage Mitigation of Large 2.5D Glass BGA Packages*** Vidya Jayaram, Omkar Gupte, and Vanessa Smet – Georgia Institute of Technology
5. 3:55 PM - Stability Analysis of Nanoscale Copper-Carbon Hybrid Interconnects Bhawana Kumari and Manodipan Sahoo – Indian Institute of Technology Dhanbad; Rohit Sharma – Indian Institute of Technology Ropar	***5. 3:55 PM - High Density Thin Film Flex Technology for Advanced Packaging Applications*** Kai Zoschke, Hermann Oppermann, Markus Wöhrmann, Christine Kallmayer, Christian Tschoban, Kevin Kröhnert, Christina Lopper, Danny Jaeger, Mario Lutz, and Olaf Wünsch – Fraunhofer IZM	***5. 3:55 PM - Effective Computational Models for Addressing Asymmetric Warping of Fan-Out Reconstituted Wafer Packaging*** Yu-Chin Lee, Chia-Yu Chen, and Kuo-Shen Chen – National Cheng-Kung University; Jen-Hsien Wong, Wei-Hong Lai, Tang-Yuan Chen, Dao-Long Chen, and David Tarng – ASE Group
6. 4:20 PM - Functional Testing of AI Cores Through Thinned 3D I/O Buffer Dies in 3D Die-Stacked Modules Mukta Farooq, Arvind Kumar, Saekyu Lee, Ravi Bonam, Juan Gomez, James Kelly, Kohji Hosokawa, Akiyo Nomura, Yasuteru Kohda, Timothy Dickson, and Katsuyuki Sakuma – IBM Corporation	***6. 4:20 PM - 300mm Full Thickness Si Based IC Singulation Using Plasma Dicing for Advanced Packaging Technologies*** Rajesh Surapaneni, Julia Chiu, Brad Hamlin, and Xavier Brun – Intel Corporation; Richard Barnett, Matthew Muggeridge, Hannah Bhaskar and N. Richards – KLA Corporation	***6. 4:20 PM - Warpage and RDL Stress Analysis in Large Fan-Out Package with Multi-chiplet Integration*** Jen-Hsien Wong, NanYi Wu, Wei-Hong Lai, Chung-Hao Chen, Yi-Hsien Wu, Tang-Yuan Chen, Teck Chong Lee, Chin-Li Kao, and C.P. Hung – ASE Group
7. 4:45 PM - Exploring the Impact of Parametric Variability on Eye Diagram of On-Chip Multi-Walled Carbon Nanotube Interconnects Using Fast Machine Learning Techniques Km Dimple, Surila Guglani, Rahul Kumar, Sourajeet Roy, and Brajesh Kumar Kaushik – Indian Institute of Technology Roorkee; Suyash Kushwaha and Rohit Sharma – Indian Institute of Technology Ropar	***7. 4:45 PM - Investigation of Low-k WLCSP Die Strength Impact Induced by Singulation Process*** C. C. Chen, Y. S. Wu, K. H. Chen, W. S. Tseng, P. H. Tsao, and S. T. Leu – Taiwan Semiconductor Manufacturing Company, Ltd.	***7. 4:45 PM - The Optimal Solution of Fan-Out Embedded Bridge (FO-EB) Package Evaluation during the Process and Reliability Test*** David Lai and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.

Program Sessions: Friday, June 3, 8:00 a.m. - 11:40 a.m.

Session 25: Advancements in 2.5D and 3D Packaging Technology

Committee:
Packaging Technologies

Silver Pearl 1

Session Co-Chairs:
John Knickerbocker – IBM Corporation
Email: knickerj@us.ibm.com
Subhash L. Shinde – Notre Dame University
Email: sshinde@nd.edu

1. 8:00 AM - A Study on Memory Stack Process by Hybrid Copper Bonding (HCB) Technology
Sanghoon Lee, Youngkun Jee, SangCheon Park, Soohwan Lee, Bohee Hwang, Gyeongjae Jo, Chungsun Lee, Jeomyoung Park, Unbyoung Kang, and Jongho Lee – Samsung Electronics Co., Ltd

2. 8:25 AM - High Performance and Energy Efficient Computing with Advanced SoICTM Scaling
S. W. Liang, Gene C. Y. Wu, K. C. Yee, C. T. Wang, Ji James Cui, and Douglas C. H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.

3. 8:50 AM - Investigation of Moisture-Induced Warpage of Chip-on-Wafer in 2.5D IC Package
Shuai Shao, Yi-Ting Chen, Shih-Yen Chen, Ken Lee, Shin Low, and Inderjit Singh – Xilinx, Inc.

4. 10:00 AM - 3D Packaging for Heterogeneous Integration
Rahul Agarwal, Patrick Cheng, Priyal Shah, Brett Wilkerson, Raja Swaminathan, John Wuu, and Chandrasekhar Mandalapu – Advanced Micro Devices, Inc.

5. 10:25 AM - Low Temperature Backside Damascene Processing on Temporary Carrier Wafer Targeting 7µm and 5µm Pitch Microbumps for N Equal and Greater Than 2 Die to Wafer TCB Stacking
Jaber Derakhshandeh, Eric Beyne, Gerald Beyer, Giovanni Capuz, Vladimir Cherman, Inge De Preter, Carine Gerets, Ehsan Shafahian, Koen Kennes, Geraldine Jamieson, and Tom Cochet – Imec

6. 10:50 AM - Demonstration of a Glass-Based 3D Package Architecture with Embedded Dies for High-Performance Computing
Siddharth Ravichandran, Vanessa Smet, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology

7. 11:15 AM - 3DIC Stacking Process Investigation by Soldering Bonding Technology
Jay Li, Wei Jhen Chen, Joe Lin, Mu Hsuan Chan, Tank Lo, Bruce Xu, Liang Yih Hung, Nicholas Kao, Don Son Jiang, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.

Session 26: Soldered and Sintered Interconnections

Committee:
Interconnections

Silver Pearl 2

Session Co-Chairs:
Bernd Ebersberger – Infineon Technologies
Email: bernd.ebersberger@infineon.com
Changqing Liu – Loughborough University
Email: c.liu@lboro.ac.uk

1. 8:00 AM - Novel Ag Salt Paste for Large Area Cu-Cu Bonding in Low Temperature Low Pressure and Air Condition
Chuantong Chen, Bowen Zhang, and Katsuaki Suganuma – Osaka University; Takuya Sekiguchi – Toppan Forms Co., Ltd.

2. 8:25 AM - Bonding Properties of Cu Paste in Low Temperature Pressureless Processes
Satoshi Konno, Takashi Hattori, Shinichi Yamauchi, and Kei Anai – Mitsui Mining & Smelting Co., Ltd.

3. 8:50 AM - Tight-Pitched 10 µm-Width Solder Joints for c-2-c and c-2-w 3D-Integration in NCF Environment
M. Mariappan, H. Hashimoto, J. Bea, and T. Fukushima – Global INTegration Initiative; S. Fukuzumi and T. Shibata – Showa Denko Materials; M. Koyanagi – T-Micro

4. 10:00 AM - Influence of Micro-Voids in Flip Chip Bump on Electromigration Reliability
Kei Murayama and Kiyoshi Oi – Shinko Electric Industries Co., Ltd.; Kor Lee – Intel Corporation; Toshiaki Ono – Nordson ES; Sze Lim – Indium Corporation; Yvonne Yeo – IBM Corporation; Keith Sweatman Martell – Nippon Superior Co., Ltd.; Haruo Shimamo – National Institute of Advanced Industrial Science and Technology; Masahiro Tsuriya – iNEMI

5. 10:25 AM - Study of Failure and Microstructural Evolution in SAC Solder Interconnects Induced by AC Electromigration Condition
Yi Ram Kim, Allison Osmanson, and Choong-Un Kim – University of Texas at Arlington; Patrick Thompson and Qiao Chen – Texas Instruments

6. 10:50 AM - A Study on Warpage and Reflow Profile for Extreme Extension of Mass Reflow Bonding
Ji-won Shin, Dong-uk Kwon, Young Ja Kim, Young Min Lee, and Dong Woo Kang – Samsung Electronics Co., Ltd.; Haoxiang Ren, Krutikesh Sahoo, Yu-Pei Huang, Yutao Yang, Ankit Kuchhangi, and Subramanian S. Iyer – University of California, Los Angeles

7. 11:15 AM - Low Temperature Formation of SAC-SnBi BGA Interconnections Using Solid Liquid Inter-Diffusion (SLID)
Divya Taneja, Richard Langlois, Nicolas Boyer, and Eric Dalpe – IBM Corporation; David Danovitch and Malak Kanso – University of Sherbrooke

Session 27: Interconnection Reliability

Committee:
Applied Reliability

Silver Pearl 3

Session Co-Chairs:
René Rongen – NXP Semiconductors
Email: rene.rongen@nxp.com
Seung-Hyun Chae – SK Hynix
Email: seunghyun1.chae@sk.com

1. 8:00 AM - Thermal Cycling Induced Interconnect Stability Degradation Mechanism in Low Melting Temperature Solder Joints
Kendra Young – Portland State University; Raiyo Aspandiar and Satyajit Walwadkar – Intel Corporation; Nilesh Badwe – Indian Institute of Technology Kanpur; Young-Woo Lee – MK Electron; Tae-Kyu Lee – Cisco Systems, Inc.

2. 8:25 AM - Interconnection Reliability of Mini LEDs for Display Applications
In-Seok Kye, Jiho Joo, Gwang-Mun Choi, Chanmi Lee, Ki-Seok Jang, Yong-Sung Eom, and Kwang-Seong Choi – Electronics and Telecommunications Research Institute; Yong-Jun Oh – Hanbat National University

3. 8:50 AM - Study of Long-Term Solder Joint and Board-Level Reliability Performance of Thin Nickel Plating ENEPIG Laminate LGA Package
Seok Phyo Tchun, Joo Yeop Kim, and Arun Raj – Analog Devices

Refreshment Break: 9:15 a.m. - 10:00 a.m. - Silver Pearl & Coral Foyers

4. 10:00 AM - Process-Reliability Relationships of SnBiAg and SnIn Solders for Component Attachment on Flexible Direct-Write Additive Circuits in Wearable Applications
Pradeep Lall and Jinesh Narangaparambil – Auburn University; Scott Miller – NextFlex National Manufacturing Institute

5. 10:25 AM - Fabrication and Reliability Analysis of Quasi-Single Crystalline Cu Joints by Using Highly <111>-Oriented Nanotwinned Cu
Jia-Juen Ong, Dinh-Phuc Tran, You-Yi Lin, Po-Ning Hsu, and Chih Chen – National Yang Ming Chiao Tung University

6. 10:50 AM - A Comparative Study of the Thermomechanical Reliability of Fully Filled and Conformal Through Glass Via (TGV)
Ke Pan, Yangyang Lai, and Seungbae Park – Binghamton University; Chukwudi Okoro, Dhananjay Joshi, and Scott Pollard – Corning Corporation

7. 11:15 AM - Broadband Characterization of Polymers Under Reliability Stresses and Impact of Capping Layer
Nicolas Pantano, Emmanuel Chery, Maaike Op de Beeck, John Slabbekoorn, and Eric Beyne – Imec

Program Sessions: Friday, June 3, 8:00 a.m. - 11:40 a.m.

Session 28: Packaging Assembly: Solder, Sintering, and Thermal Interface Materials	Session 29: Materials and Processes for Fan-Out and Advanced Packaging	Session 30: High-Speed Challenges in Power and Signal Integrity
Committee: Materials & Processing joint with High-Speed, Wireless & Components	**Committee: Materials & Processing**	**Committee: RF, High-Speed Components & Systems**
Coral 1 & 2	**Coral 3 & 4**	**Coral 5**
Session Co-Chairs: **Zia Karim – Yield Engineering Systems** **Email: zkarim@yieldengineering.com** **Mark Poliks – Binghamton University** **Email: mpoliks@binghamton.edu**	**Session Co-Chairs:** **Tanja Braun – Fraunhofer IZM** **Email: tanja.braun@izm.fraunhofer.de** **Praveen Pandojirao-S – Johnson & Johnson** **Email: praveen@its.jnj.com**	**Session Co-Chairs:** **Amit Agrawal – Microchip Technologies** **Email: amit.agrawal@microchip.com** **Chuei-Tang Wang – Taiwan Semiconductor Manufacturing Company, Ltd. • Email: ctwangm@tsmc.com**
1. 8:00 AM - High Thermal Graphite Thermal Interface Material (TIM) Solution Applied to Fan-Out Platform Pin-Jing Su, Dan Lin, Shane Lin, Xi-Zhang Xu, Rung Jeng Lin, Liang-Yih Hung, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.	***1. 8:00 AM - High Fluorescence Photosensitive Materials for AOI Inspection of Fan-Out Panel Level Package*** Kiseok Kim, Jinyoung Kim, Okseon Yoon, Seunghun Chae, Jihye Shim, and Sooryeon Kim – Samsung Electronics Co., Ltd.	***1. 8:00 AM - Novel Power Delivery Network Design and Pre-Silicon Validation Supporting Heterogeneous Dies on a Single Package*** Judy Amanor-Boadu, Rishik Bazaz and Priyanka Bakliw – Intel Corporation
2. 8:25 AM - Optimizing Reflowed Solder Thermal Interface Material (sTIMs) Processes for Emerging Heterogeneous Integrated Packages DaeWoon Lee, Bret Hable, David Heller, Robert Jarrett, Xike Zhao, and Thomas Nash – Heller Industries, Inc.; Ryan Mayberry and Andy Mackie – Indium Corporation	***2. 8:25 AM - Selective Epoxy Mold Compound Slurry for Advanced Packaging Technology*** Tri Widodo, Xavier Brun, and C. Noda – Intel Corporation; N. Tsunoda, Y. Ichige, S. Arata, S. Nomura, and S. Kondo – Showa Denko Materials Co., Ltd.	***2. 8:25 AM - Integration of Foundry MIM Capacitor and OSAT Fan-Out RDL for High Performance RF Filters*** Pao-Nan Lee, Yu-Chang Hsieh, Wei-Chu Hsu, and Chen-Chao Wang – ASE Group; Hung-Lun Lo, Chang Ho Li, Fan-Hsiu Huang, and James Lin – WIN Semiconductors Corp.
3. 8:50 AM - Large, High Conductivity Direct-Fill Copper Thermal Vias for High Power Devices Alfred Zinn, Nhi Ngo, Alex Capanzana, Hannah Zinn, and Randall Stoltenberg – Kuprion, Inc.	***3. 8:50 AM - Low Warpage Printable Liquid Mold Compound for Laser Direct Structuring*** Charlie (Chunlin) He, Ruud deWit, Jie Cao, Tim Champagne, Rose Guino, Tony Winster, Ramachandran Trichur, Mario Saliba, and Frank Song – Henkel Corporation; Florian Roick and Simon Heitmann – LPKF Laser & Electronics AG	***3. 8:50 AM - Optimization of 2.5D Organic Interposer Channel for Die and Chiplets*** Srikrishna Sitaraman, Steven Verhaverbeke, Samer Banna, Mukhles Sowwan, Liu Jiang, El Mehdi Bazizi, Blessy Alexander, and Buvna Ayyagari-Sangamalli – Applied Materials, Inc.
Refreshment Break: 9:15 a.m. - 10:00 a.m. - Silver Pearl & Coral Foyers		
4. 10:00 AM - Vacuum Fluxless Reflow Technology for Fine Pitch First Level Interconnect (FLI) Bumping Applications Yue Deng, Liang He, Hossein Madanipour, Jung Kyu Han, Gang Duan, and Rahul Manepalli – Intel Corporation; Xike Zhao, David Wright, Bret Halbe, Fred Tarazi, and Dror Trifon – Heller Industries, Inc.	***4. 10:00 AM - Large-Scale Production of Boron Nitride Nanosheets-Based Epoxy Nanocomposites with Ultrahigh Through-Plane Thermal Conductivity for Electronic Encapsulation*** Zhijian Sun, Michael Yu, Jiaxiong Li, Macleary Moran, Mohanalingam Kathaperumal, Kyoung-Sik Moon, Madhavan Swaminathan, and Chi-Ping Wong – Georgia Institute of Technology	***4. 10:00 AM - Reference Clock Assessment Techniques for PCIe Gen5 and Beyond*** Matt Doyle, Matteo Cocchini, Layne Berge, Dale Becker, Matteo Cocchini, and Jason Bjorgaard – IBM Corporation
5. 10:25 AM - Thermal Performance of Advanced Thermal Interface Materials for High Power Flip Chip Lidded Ball Grid Array (FCLBGA) YoungJoon Koh, SangHyuk Kim, EunSook Sohn, and JinYoung Khim – Amkor Technology	***5. 10:25 AM - Photonic Debond: Scalability and Advancements*** Luke Prenger, Xavier Martinez, and Andrea Chacko – Brewer Science, Inc.; Vikram Turkani, Lauren Reimnitz, Vahid Akhavan, and Kurt Schroder – NovaCentrix	***5. 10:25 AM - Co-Design and Signal-Power Integrity/EMI Co-Analysis of a Switchable High-Speed Inter-Chiplet Serial Link on an Active Interposer*** Min Miao, Xiaolong Duan, Liang Sun, Tao Li, Shiliang Zhu, Zhuanzhuan Zhang, Jin Li, Danya Zhang, Hao Wen, Xuena Liu, and Zhensong Li – Beijing Information Science & Technology University
6. 10:50 AM - Non-Oil Bleed Thermal Gap Fillers for Long-Term Reliability of Solid State Drive Vigneshwarram Kumaresan and Mutharasu Devarajan – Western Digital	***6. 10:50 AM - A Novel Method of Low Temperature, Pressureless Interconnection for Wafer Level Scale 3D Packaging*** Po-Shao Shih, Yu-An Chen, Simon Johannes Gräfner, Jeng-Hau Huang, Ching-Han Huang, and C. Robert Kao – National Taiwan University	***6. 10:50 AM - Fast Channel Analysis and Design Approach Using Deep Learning Algorithm for 112Gbs HSI Signal Routing Optimization*** Sodam Han, Sungwook Moon, Seungki Nam, Jiyoung Park, Sangin You, and Jungil Son – Samsung Electronics Co., Ltd.
7. 11:15 AM - Printed Silver Micro-Pillars Embedded in a Phase Change Material Matrix for Thermal Management Applications Roberto Aga and Laura Davidson – KBR/AFRL; Carrie Bartsch and Emily Heckman – Air Force Research Laboratories	***7. 11:15 AM - Cracking-Less Heat-Resistant Electroless Ni-P Plating Film for Wide Bandgap Power Modules*** Ming-chun Hsieh, Chuantong Chen, Aiji Suetake, Zheng Zhang, and Katsuaki Suganuma – Osaka University; Ryuji Saito, Norihiko Hasegawa, Kei Hashizume, and Kuniaki Otsuka – Okuno Chemical Industries Co., Ltd.	***7. 11:15 AM - Package Design and Measurements for Radar Emulator Using Accelerators and Photonics*** Mercy Daniel-Aguebor, Mutee Ur Rehman, Serhat Erdogan, Kyoung-sik Moon, Nikita Ambasana, Saibal Mukhopadhya, and Madhavan Swaminathan – Georgia Institute of Technology; Liang Yuan Dai, Keren Bergman, Daniel Jang, and Mingoo Seok – Columbia University

Program Sessions: Friday, June 3, 1:30 p.m. - 5:30 p.m.

Session 31: Fan-Out Packaging Technologies and Applications	Session 32: Advanced Interconnect and Wire Bond Technologies for Flexible Device Applications	Session 33: Advanced Reliability Modeling and Characterization
Committee: Packaging Technologies	**Committee: Interconnections joint with Applied Reliability**	**Committee: Thermal/Mechanical Simulation & Characterization**
Silver Pearl 1	**Silver Pearl 2**	**Silver Pearl 3**
Session Co-Chairs: **Sam Karikalan – Broadcom Inc.** **Email: sam.karikalan@broadcom.com** **Kuo-Chung Yee – Taiwan Semiconductor Manufacturing Corporation, Ltd. • Email: kcyee@tsmc.com**	**Session Co-Chairs:** **Ho-Young Son – SK Hynix** **Email: hoyoung.son@sk.com** **Matthew Yao – General Electric** **Email: matthew.yao@ge.com**	**Session Co-Chairs:** **Wei Wang – Qualcomm Technologies, Inc.** **Email: wwang@g.clemson.edu** **Tz-Cheng Chiu – National Cheng Kung University** **Email: tcchiu@mail.ncku.edu.tw**
1. 1:30 PM - Fan-Out Wafer Level Package for Memory Applications Ho-Young Son, Ki-Jun Sung, Bok-Kyu Choi, Jong-Hoon Kim, and Kangwook Lee – SK Hynix	***1. 1:30 PM - Infrared Curing of Flip Chip Electrically Conductive Adhesive (ECA) Interconnections*** Romaric Kabre and David Danovitch – University of Sherbrooke; Valerie Oberson and Magali Côté – IBM Corporation	***1. 1:30 PM - In-Situ Monitoring of Thermo-Mechanical Induced Stresses in Electronic Control Unit – from the Assembly to Use in the Field*** Przemyslaw Gromala, Daniel Riegel, Georg Konstantin, and Alexander Kabakchiev – Robert Bosch GmbH
2. 1:55 PM - Substrate Silicon Wafer Integrated Fan-Out Technology (S-SWIFT) Packaging with Fine Pitch Embedded Trace RDL SangHyun Jin, WonChul Do, JinSuk Seong, HyunGoo Cha, YunKyung Jeong, and JinYoung Khim – Amkor Technology	***2. 1:55 PM - Room-Temperature Cu Direct Bonding Technology Enabling 3D Integration with Micro-LEDs*** Yuki Susumago, Shunsuke Arayama, Tadaaki Hoshi, Hisashi Kino, Tetsu Tanaka, and Takafumi Fukushima – Tohoku University	***2. 1:55 PM - Reliability Challenges of High-Density Fan-Out Packaging for High-Performance Computing Applications*** Laurene Yip, Charles Lai, Rosa Lin, and Cooper Peng – MediaTek, Inc.
3. 2:20 PM - Advanced Fan-Out Packaging Technology for Hybrid Substrate Integration Lihong Cao, Teck Chong Lee, Rick Chen, Yung-Shun Chang, Hsingfu Lu, Nicholas Chao, Yen-Liang Huang, Chen-Chao Wang, and Chih-Yi Huang – ASE Group	***3. 2:20 PM - Ag to Ag Direct Bonding Via a Pressureless, Low-Temperature, and Atmospheric Stress Migration Bonding Method for 3D Integration Packaging*** Zheng Zhang, Aiji Suetake, Ming-Chun Hsieh, Chuantong Chen, Hiroshi Yoshida, and Katsuaki Suganuma – Osaka University	***3. 2:20 PM - A Comprehensive Study of Crack Initiation and Delamination Propagation at the Cu/Polyimide Interface in Fan-Out Wafer Level Package during Reflow Process*** Hong-Guang Wang, Guang-Chao Lyu, Yun-Kai Deng, Wei-Lin Hu, Bing-Xian Yang, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology
Refreshment Break: 2:45 p.m. - 3:30 p.m. - Silver Pearl & Coral Foyers		
4. 3:30 PM - Advanced Chip Last Process Integration for Fan-Out Wafer Level Packaging (WLP) Taewon Yoo, Seok Hyun Lee, Kyoung Lim Suk, Eung Kyu Kim, Won Kyoung Choi, Dae-Woo Kim, and Dong Wook Kim – Samsung Electronics Co., Ltd.	***4. 3:30 PM - Plating and Recrystallization of Galvanic Cu Films on Roll Annealed and Polycrystalline Cu Foils and the Effect of Intermediate Electroless Cu Layers*** Tobias Bernhard, R. Massey, Zhiou Li, Joerg-F. Schulze, Kilian Klaeden, Sebastian Zarwell, E. Steinhaeuser, and F. Bruening – Atotech Deutschland GmbH	***4. 3:30 PM - Observation of Fatigue and Creep Ratcheting Failure in Solder Joints Under Pulsed Direct Current Electromigration Testing*** Allison Osmanson, Yi Ram Kim, and Choong-Un Kim – University of Texas at Arlington; Patrick Thompson, Qiao Chen, and Sylvester Ankamah-Kusi – Texas Instruments
5. 3:55 PM - Development of Two-Tier FO-WLP AiPs for Automotive Radar Application Soon Wee Ho, Hsiang-Yao Hsiao, Boon Long Lau, Sharon Pei Siang Lim, Teck Guan Lim, and Tai Chong Chai – Institute of Microelectronics (IME), A*STAR	***5. 3:55 PM - Evaluation of an Anisotropic Conductive Epoxy for Interconnecting Highly Stretchable Conductors to Various Surfaces*** Riadh Al-Haidari, Behnam Garakani, Mohammed Alhendi, Udara Somarathna, and Mark Poliks – Binghamton University; Christopher Tabor and Michelle Yuen – Air Force Research Laboratory; Madhu Stemmermann – SunRay Scientific, Inc.; Nancy Stoffel – General Electric	***5. 3:55 PM - Evolution of SAC305 Mechanical Behavior Due to Damage Accumulation During Cycling*** Mohammad Ashraful Haq, Mohd Aminul Hoque, Golam Rakib Mazumder, Jeffrey C. Suhling, and Pradeep Lall – Auburn University
6. 4:20 PM - Chip-Last FOWLP Based Antenna-in-Package (FO-AiP) for 5G mmWave Application Klaus Ahn, Jade Park, Bruce Lee, Lewis Kang, Jay Kim, Kyeongrok Shin, Sung Hyuk Kim, Jea-Duck Lee, and Myoung Kee Kim – nepes Corporation; Ho-Seon Lee and Byeong-Gyu Park – RFcore, Ltd.	***6. 4:20 PM – Laser Soldered Wire Bonding on Liquid Printed and Sputtered Contact Structures on Thin-Flexes and Injection Molded Devices*** Matthias Fettke, Andrej Kolbasow, Timo Kubsch, and Thorsten Teutsch – PacTech Packaging Technologies GmbH; Tobias Seifert, Franz Selbmann, Frank Roscher, Kerstin Kreyssig, and Mario Baum – Fraunhofer Institute for Electronic Nano Systems ENAS; Soumya Deep Paul - Center for Microtechnologies, Technische Universität Chemnitz	***6. 4:20 PM - Board-Level Solder Joint Reliability of QFN Packages with Enclosure and Placement Effects in Various Form Factors*** Chun-Sean Lau, Ahmad Faridzul Hilmi, Ning Ye, and Yang Bo – Western Digital Corporation
7. 4:45 PM - A Heterogeneously Integrated and Flexible Inorganic Micro-Display on FlexTRATE(TM) Using Fan-Out Wafer-Level Packaging and Color Conversion Layers Henry Sun, Goutham Ezhilarasu, Guangqi Ouyang, Randall Irwin, and Subramanian S. Iyer – University of California, Los Angeles	***7. 4:45 PM - Cu/Co Metaconductor Based Highly Energy-Efficient Bonding Wires for Next Generation Millimeter Wave Electronic Interconnects*** Saeyeong Jeon, Hae-In Kim, Woosol Lee, and Yong-Kyu Yoon – University of Florida	***7. 4:45 PM - Shape Dependency of Fatigue Life in Solder Joints of Chip Resistors*** Jonghwan Ha, Chongyang Cai, Pengcheng Yin, Yangyang Lai, Ke Pan, Junbo Yang, and Seungbae Park – Binghamton University

Program Sessions: Friday, June 3, 1:30 p.m. - 5:30 p.m.

Session 34: Processing Enhancements in Fan-Out and Heterogeneous Integration

Committee: Materials & Processing joint with Applied Reliability

Coral 1 & 2

Session Co-Chairs:
Qianwen Chen – IBM Corporation
Email: chenq@us.ibm.com
Jae Kyu Cho – GlobalFoundries
Email: jaekyu.cho@globalfoundries.com

1. 1:30 PM - Optimization of Temporary Carrier Technology for HDFO Packaging
JinKun Yoo, DooWon Lee, KiYeul Yang, Ji Hyun Kim, WonChul Do, and Jin Young Khim – Amkor Technology

2. 1:55 PM - Optimization of PI & PBO Layers Lithography Process for High Density Fan-Out Wafer Level Packaging & Next Generation Heterogeneous Integration Applications Employing Digitally Driven Maskless Lithography
Thomas Uhrmann, Boris Povazay, Tobias Zenger, Bernd Thallner, Roman Holly, and Bozena Matuskova Lednicka – EV Group; Mario Reybrouck, Niels Van Herck, Bart Persijn, Dimitri Janssen, and Stefan Vanclooster – FUJIFILM Electronic Materials N.V.

3. 2:20 PM - Analysis of Pattern Distortion by Panel Deformation and Addressing it by Using Extremely Large Exposure Field Fine-Resolution Lithography
John Chang, James Webb, Corey Shay, and Timothy Chang – Onto Innovation

4. 3:30 PM - Solutions to Overcome Warpage and Voiding Challenges in Fan-Out Wafer-Level Packaging
Vidya Jayaram, Vipul Mehta, Yiqun Bai, and John C. Decker – Intel Corporation

5. 3:55 PM - Dry Etch Processing in Fan-Out Panel-Level Packaging – An Application for High-Density Vertical Interconnects and Beyond
Friedrich-Leonhard Schein, Christian Voigt, and Lutz Gerhold – Technische Universität Berlin; Ioannis Tsigaras, Mohamed Elghazzali, Hirofumi Sawamoto, Ewald Strolz, and Roland Rettenmeier – Evatec AG; Ruben Kahle and Lars Böttcher – Fraunhofer IZM

6. 4:20 PM - Fabrication, Characterization and Electromechanical Reliability of Stretchable Circuitry for Health Monitoring Systems
Behnam Garakani, Udara Somarathna, Riadh Alheydari, Firas Alshatnawi, Detlef-M. Smilgies, and Mark D. Poliks – Binghamton University

7. 4:45 PM - Buried Power Rails and Nano-Scale TSV: Technology Boosters for Backside Power Delivery Network and 3D Heterogeneous Integration
Anne Jourdain, Michele Stucchi, Geert Van der Plas, Gerald Beyer, and Eric Beyne – Imec

Session 35: Packaging with Additive Manufacturing for Harsh Conditions

Committee: Emerging Technologies

Coral 3 & 4

Session Co-Chairs:
Rohit Sharma – IIT Ropar
Email: rohit@iitrpr.ac.in
Benson Chan – Binghamton University
Email: chanb@binghamton.edu

1. 1:30 PM - High Temperature Die Interconnection Approaches
Firas Alshatnawi, Mohammed Alhendi, Rajesh Sivasubramony, Riadh Al-Haidari, El Mehdi Abbara, Udara Somarathna, Mark Poliks, and Peter Borgesen – Binghamton University; David Shaddock, Nancy Stoffel, and Cathleen Hoel – General Electric

2. 1:55 PM - 3D Cryogenic Interposer for Quantum Computing Application
Hongyu Li, Norhanani Jaafar, and King-Jien Chui – Institute of Microelectronics (IME), A*STAR; Aaron Chit Siong Lau, Rainer Cheow Siong Lee, Calvin Pei Yu Wong, and Kuan Eng Johnson Goh – Institute of Materials Research and Engineering (IMRE), A*STAR

3. 2:20 PM - Flexible Metamaterial Lens for Magnetic Field and Signal-to-Noise Ratio Improvements in 1.5 T and 3 T Magnetic Resonance Imaging
Woosol Lee, Marcelo Febo, and Yong-Kyu Yoon – University of Florida; Josh Lane – Texas Instrument

4. 3:30 PM - Self-Healing of Interconnect Cracks for Reliable and Defect-Free Smart Manufacturing of Flexible Packages
Akeeb Hassan, Asahi Tomitaka, Reshmi Banerjee, and P. Markondeya Raj – Florida International University

5. 3:55 PM - Additively Manufactured RF GRIN Lenses For Highly Directive, Low Power Transmitters
Jonathon Copley, Hatem Elbidweihy, and Connor S. Smith – United States Naval Academy; Christopher R. Milligan and Nam Nicholas Mai – Department of Defense

6. 4:20 PM - A Low Profile Two-Phase Immersion Cooling Stack-up based on Detachable Boiling Enhancement Layer on Lidded Electronic Packages
Jimmy Chuang, Y. L. Li, Jin Yang and David Shia – Intel Corporation

7. 4:45 PM - Ultraprecise Deposition of Micrometer-Size Conductive Features for Advanced Packaging
Aneta Wiatrowska, Piotr Kowalczewski, Karolina Fiaczyk, Lukasz Witczak, Jolanta Gadzalinska, Mateusz Lysien, Ludovic Schneider, and Filip Granek – XTPL SA

Session 36: Modeling and Characterization of Interfaces and Interconnects

Committee: Thermal/Mechanical Simulation & Characterization

Coral 5

Session Co-Chairs:
Tieyu Zheng – Microsoft Corporation
Email: tizheng@microsoft.com
Xuejun Fan – Lamar University
Email: xuejun.fan@lamar.edu

1. 1:30 PM - Sustained High Temperature Fracture Toughness Evolution of Chip-UF and Substrate-UF Interfaces in FCBGAs for Automotive Applications
Pradeep Lall, Padmanava Choudhury, and Aathi Pandurangan – Auburn University

2. 1:55 PM - Nonlinear Finite Element Analysis of an Automotive High-Power Module Under Impact Loading
Liangbiao Chen, Yong Liu, Alex Yao, Sam Lin, and CH Chew – ON Semiconductor

3. 2:20 PM - Magnetic-Based Interfacial Adhesion Measurement Technique with Environmental Conditions
Rui Chen and Suresh Sitaraman – Georgia Institute of Technology; Nicholas Ginga – University of Alabama in Huntsville

4. 3:30 PM - Fracture Simulation of Redistribution Layer in Fan-Out Wafer-Level Package Based on Fatigue Crack Growth Characteristics of Insulating Polymer
Koichi Nagase and Atsushi Fujii – Asahi Kasei Corporation; Kaiwen Zhong and Yoshiharu Kariya – Shibaura Institute of Technology

5. 3:55 PM - Development on Fatigue Life Model of Lead-Free Solder for First Failure Prediction
Faxing Che, Yeow Chon Ong, Hong Wan Ng, Ling Pan, Christopher Glancey, Koustav Sinha and Richard Fan – Micron Technology, Inc.

6. 4:20 PM - An Extensive Simulation Study of the Interfacial Delamination in Molded Underfill Flip-Chip Packages by Finite Element Method Based on Virtual Crack Closure Technique
Guang-Chao Lyu, Hong-Guang Wang, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

7. 4:45 PM - Mechanical Simulation and Modeling for Reliability of 6-in-1 Power Module
Rathin Mandal, Kazunori Yamamoto, and Gongyue Tang – Institute of Microelectronics (IME), A*STAR

Refreshment Break: 2:45 p.m. - 3:30 p.m. - Silver Pearl & Coral Foyers

Wednesday, June 1, 2022

Session 37: Interactive Presentations 1
Time: 9:00 AM – 11:00 AM

Committee: Interactive Presentations

Coral Foyer

Session Co-Chairs:
Mark Eblen
Kyocera Corporation
Email: mark.eblen@kyocera.com

Jeffrey Lee
iST-Integrated Service Technology, Inc.
Email: jeffrey_lee@istgroup.com

Kuo-Ning Chiang
National Tsinghua University
Email: knchiang@pme.nthu.edu.tw

1. The Effect of Thermal Stress on Reliability of Printed Vias on Flexible Substrates
Udara Somarathna, Mohammed Alhendi, and Mark Poliks – Binghamton University; Darshana Weerawarne – University of Colombo; Joseph Iannotti, Christopher J. Kapusta, and Nancy Stoffel – General Electric; Stephen G. Gonya – Lockheed Martin

2. Mechanical Property Evolution in SAC+Bi Lead Free Solders Subjected to Various Thermal Exposure Profiles
Mohammad Al Ahsan, S M Kamrul Hasan, Mohammad Ashraful Haq, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

3. Extreme Low-Temperature High Strain-Rate Constitutive Behavior Evolution of Doped and Undoped Lead Free Solders Under Sustained High Temperature Exposure
Pradeep Lall, Vishal Mehta, Vikas Yadav, Mrinmoy Saha, and Jeffrey C. Suhling – Auburn University; Dave Locker – US Army CCDC-AC

4. Effects of β-Sn Crystal Orientation on the Deformation Behavior of SAC305 Solder Joints
Debabrata Mondal, Mohammad Ashraful Haq, Jeffrey C. Suhling, and Pradeep Lall – Auburn University

5. Reconstructing More Sinterable Surfaces for Copper Nanoparticles to Form High-Strength Cu-Cu Joints in Air Atmosphere
Yudui Zhang, Tao Zhao, Pengli Zhu, Rong Sun, and Liang Xu – Shenzhen Institute of Advanced Electronic Materials; Chuncheng Wang and Yue Yao – Osaka University

6. Two/Multi-Photon Imaging for Characterization of Fine Line Features and Microvias in Advanced Packaging
Mohanalingam Kathaperumal, Pragna Bhaskar, Christopher Blancher, Pratik Nimbalkar, Fuhan Liu, and Madhavan Swaminathan – Georgia Institute of Technology; Bai Nie – Intel Corporation

7. Development of Advanced Liquid Cooling Solution on Data Centre Cooling
Xiaowu Zhang, Yong Han, Gongyue Tang, Haoran Chen, and Boon Long Lau – Institute of Microelectronics (IME), A*STAR

8. The Effects of Bi Doping and Aging on Viscoplasticity of Sn-Ag-Cu-Bi alloys
Vishnu Shukla, Nicholas Ayers, Andrea Moreno, Natalie Crutchfield, Devin Lyons, and Tengfei Jiang – University of Central Florida; Omar Ahmed, Peng Su, and Bernard Glasauer – Juniper Networks

9. Numerical Simulation of Cu/Polymer-Dielectric Hybrid Bonding Process Using Finite Element Analysis
Sasi Kumar Tippabhotla, Lin Ji, and Yong Han – Institute of Microlectronics (IME), A*STAR

10. Investigating Moisture Diffusion in Mold Compounds (MCs) for Fan-Out-Wafer-Level-Packaging (FOWLP)
Abdellah Salahouelhadj, Mario Gonzalez, Arnita Podpod, and Eric Beyne – Imec

11. Mechanical and Thermal Characterization Analysis of Chip-Last Fan-Out Chip on Substrate
Weijie Yin, Wei-Hong Lai, Ying-Xu Lu, KarenYU Chen, Hung-Hsien Huang, Tang-Yuan Chen, Chin-Li Kao, and CP Hung – ASE Group

12. Low Cost Copper Based Sintered Interconnect Material for Optoelectronics Packaging
Sri Krishna Bhogaraju, Maximilian Schmid, E Liu, Rodolfo Saccon, Gordon Elger, Klaus Müller, and Georg Pirzer – Institute of Innovative Mobility; Holger Klassen – Osram Opto Semiconductors GmbH

13. Study of Small Polyimide Open Size in Contact Resistance and Reliability for Flip Chip Cu Pillar Package
Kuei Hsiao Kuo, Shaun Xiao, Abram Hwang, Kui Chang, Jovi Chang, and Feng Lung Chien – Siliconware Precision Industries Co., Ltd.

14. Package Design Through Reliable Predictive Modeling and Its Validation
Pengcheng Yin and Seungbae Park – Binghamton University; Biju Jacob, Liang Yin, and Arun Gowda – General Electric

15. Thermo-Mechanical Reworkable Epoxy Underfill in Board-Level Package: Material Characteristics and Reliability Criteria
Lip Teng Saw and Mutharasu Devarajan – Western Digital

16. Block Thermal Model for High Power Lidded Packages
Daijiao Wang and Sam Karikalan – Broadcom, Inc.

17. A Parameter Study for the Design Optimization to Relieve Pattern Stress of PCB Under the Temperature Cycling Condition
Hyunggyun Noh, Kyungwoo Lee, Jinsu Bae, Yuchul Hwang, Hoosung Kim, and Sangwoo Pae – Samsung Electronics Co., Ltd.

18. Characterization and Reliability of a High Bandwidth, High Frequency Flexible Connector for Signal Delivery
Randall Irwin and Subramanian S. Iyer – University of California, Los Angeles

19. Investigation of Reflow Effect and Empirical Lifetime Modeling on the Board Level Solder Joint Reliability
Kwangwon Seo, Keunho Rhew, Choongpyo Jeon, Youngsung Choi, Jinsoo Bae, Hoosung Kim, and Sangwoo Pae – Samsung Electronics Co., Ltd.

20. Finite Element Influence Analysis of Power Module Design Options
Marius van Dijk and Olaf Wittler – Fraunhofer IZM; Ping-Chi Hung – Universal Scientific Industrial Co., Ltd.; Willy H. Lai, C. Y. Hsieh, and Thomas Wang – ASE Group; Martin Schneider-Ramelow – Technical University Berlin

21. Solder Joint Fatigue Studies Subjected to Board-Level Random Vibration for Automotive Applications
Valeriy Khaldarov and Alexander Shalumov – ASONIKA, LLC; Andy Zhang – Texas Instruments; Dongji Xie – Nvidia Corporation; Jeffrey Lee – iST-Integrated Service Technology; Xue Shi – Bosch Automotive Products; Romuald Roucou – NXP Semiconductors; Sushil Doranga – Lamar University

22. 2-D Fluid Simulation Approach for Miniwave Soldering
Reinhardt Seidel, Marcel Sippel, and Jörg Franke – FAPS, FAU Erlangen-Nürnberg

23. Component Level Reliability Evaluation of Low Cost 6-Sided Die Protection Versus Wafer Level Chip Scale Packaging with 350 µm Ball Pitch
Jacinta Aman Lim, Byung-Cheol Kim, Rizi Valencia-Gacho, and Brett Dunlap – nepes Corporation

24. Simulation of the Filler Stuck Mechanism in Molding Process and Verification
Tzu Chieh Chien, Shih Kun Lo, Yen Hua Kuo, Hui Chung Liu, Zong Yuan Li, Yi Nong Lin, Lu Ming Lai, and Kuang Hsiung Chen – ASE Group

25. Inlet/Outlet Induced Failures During Flip-Chip Bonding of Large Area Chip with Embedded Microchannels
Jianyu Du and Jiajie Kang – China University of Geosciences; Yuchi Yang, Han Xu, Deyin Zheng, Qi Wang, and Wei Wang – Institute of Microelectronics (IME), A*STAR; Huaiqiang Yu – Electronics Technology Group Corporation

Wednesday, June 1, 2022

Session 38: Interactive Presentations 2
Time: 2:00 PM – 4:00 PM

Committee: Interactive Presentations

Coral Foyer

Session Co-Chairs:
Pavel Roy Paladhi
IBM Corporation
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Amanpreet Kaur
Oakland University
Email: kaur4@oakland.edu

Saikat Mondal
Intel Corporation
Email: saikat.mondal@intel.com

1. Multi-Layers Chips on Wafer Stacking Technologies with Carbon Nano-Tubes as Through-Silicon Vias and Its Potential Applications for Power-Via technologies
Bo-Zhou Liao, Yi-Ting Tsai, Liang-Hsi Chen, Ting-Wei Chen, Kai-Cheng Chen, Yi-Cheng Chan, Hong-Yi Lin, Min-Hung Lee, and Ming-Han Liao, National Taiwan University

2. A De-Embedding and Embedding Procedure for High-Speed Channel Eye Diagram Oscilloscope Measurement
Zhaoqing Chen – IBM Corporation

3. Physics-Based Nested-ANN Approach for Fan-Out Wafer Level Package Reliability Prediction
Peilun Yao, Jun Yang, Yonglin Zhang, Xiaoshun Fan, Haibin Chen, Jinglei Yang, and Jingshen Wu – Hong Kong University of Science and Technology

Wednesday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. in Exhibit Hall - Eventide Pavilion

4. A Fully Additive Approach for the Fabrication of Split-Ring Resonator Metasurfaces
Roghayeh Imani, Sarthak Acharya, Shailesh Chouhan, and Jerker Delsing – Luleå University of Technology

5. 60 GHz 0-360˚ Passive Analog Delay Line in Liquid Crystal Technology Based on a Novel Conductor-Backed Fully-Enclosed Coplanar Waveguide
Jinfeng Li – Imperial College London

6. Development of Smart Sensor Array Mat for Retail Inventory Management
Ruiqi Lim, Musafargani Sikkandhar, and Ming-Yuan Cheng – Institute of Microelectronics (IME), A*STAR

7. Modeling and Mitigating Fiber Weave Effect Using Layer Equivalent Model and Monte Carlo Method
Chin-Hsun Wang and Ruey-Beei Wu – National Taiwan University; Ming-Tsun Lu, Jun-Rui Huang, and Ching-Sheng Chen – Unimicron Technology Corporation

8. Die Floorplan and PKG Design Impacts on Power Integrity Performances of Multiple Blocks in a Single Power Domain
Jun So Pak, James Jeong, Taehoon Kim, Byung-Su Kim, Minkyu Kim, Jisoo Hwang, Serhoon Lee, and Heeseok Lee – Samsung Electronics Co., Ltd.

9. System Level Power Supply Induced Jitter Suppression for Multi-lane High Speed Serial Links
Goeun Kim, Doohee Lim, Tamal Das, Eunjung Lee, and Sangin You – Samsung Electronics Co., Ltd.

10. Heterogeneously Integrated Quantum Chip Interposer Packaging
Ramesh Kudalippalliyalil, Sujith Chandran, Akhilesh Jaiswal, and Ajey P. Jacob – University of Southern California; Kang L. Wang – University of California, Los Angeles

11. System-Level Verification of a Packaged Silicon Photonics-Based Transceiver
Yao Sun, Po Dong, Minhua Chen, Kejia Zheng, Changyi Li, Li Zhang, Wei Si, Shanshan Zeng - II-VI Shihuan Ran and Linjie Zhou - Shanghai Jiaotong University

12. A Novel Frequency Mixing Based Beam-Steering Phased Array for K-Band Applications
Yu Ping Liu and Amanpreet Kaur – Oakland University

13. Automated Detection and Segmentation of HBMs in 3D X-ray Images Using Semi-Supervised Deep Learning
Ramanpreet Pahwa, Richard Chang, Wang Jie, Xu Xun, Lile Cai, and Sheng Foo Chuan – I2R; David Ho Soon Wee, Chong Ser Choong, and Vempati Srinivasa Rao – Institute of Microelectronics (IME), A*STAR

14. New Packaging Technology for Disruptive 1-and 2-Dimensional VCSEL Arrays and Their Electro-Optical Performance and Applications
Gottfried Rainer Dohle, Gerold Henning, Thomas Friedrich, Maximilian Wallrodt, - Micro Systems Engineering GmbH; Christoph Gréus, Christian Neumeyr, Jürgen Rosskopf, Robert Hohenleitner - VERTILAS GmbH

15. Electrospray Printing of Polyimide Films for Electronics Packaging Applications
Bryce Kingsley, Emma Pawliczak, Thomas Hurley, and Paul Chiarot – Binghamton University

16. Addressing 5G NR Filter Challenges with Hybrid Technologies
Lijun Chen and Feng Ling – Xpeedic

17. Hybrid Lithography Approach for Single Mode Polymeric Waveguides and Out of Plane Coupling Mirror
David Weyers, Akash Mistry, Krzysztof Nieweglowski, and Karlheinz Bock – TU Dresden

18. Performance of Flexible Microwave Antenna Under Environmental Stress
Emuobosan Enakerakpo, Ashraf I. Umar, Mohammed Alhendi, Dylan Richmond, and Mark D. Poliks – Binghamton University; Tom Rovere and Stephen Gonya – Lockheed Martin

19. TSV-less Power Delivery for Wafer-Scale Interposers
Haoxiang Ren, Saptadeep Pal, Guangqi Ouyang, Randall Irwin, Yu-Tao Yang, and Subramanian S. Iyer – University of California, Los Angeles

20. Modeling the Effect of Surface Roughness for Screen-Printed Silver Ink on Flexible Substrates
Mohamed Abdelatty, Ashraf Umar, Gurvinder Khinda, Mohammed Alhendi, and Mark Poliks – Binghamton University

21. Modeling the Effect Trace Profiles on the RF Performance of Additively Manufactured Microstrip Transmission Lines on Polyimide Substrates
Ashraf Umar, Mohamed Y. Abdelatty, Gurvinder S. Khinda, Mohammed Alhendi, and Mark D. Poliks – Binghamton University

22. A Broadband High-Efficiency Charge Pump for Ambient RF Energy Harvesting - Powering Underground and Wearable RFID Based Sensors
Yihang Chu and Premjeet Chahal – Michigan State University

23. Modeling of Adaptive Receiver Performance Using Generative Adversarial Networks
Priyank Kashyap, Dror Baron, Chau-Wai Wong, Tianfu Wu, Chris Cheng, and Paul Franzon – North Carolina State University; Yongjin Choi and Sumon Dey – Hewlett Packard Enterprise

Thursday, June 2, 2022

Session 39: Interactive Presentations 3
Time: 9:00 AM – 11:00 AM

Committee: Interactive Presentations

Coral Foyer

Session Co-Chairs:
Pat Thompson
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Pradeep Lall
Auburn University
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Michael Mayer
University of Waterloo
Email: mmayer@uwaterloo.ca

1. The Investigation of Dry Plasma Technology in Each Step for the Fabrication of High Performance Redistribution Layer
Daisuke Hironiwa, Haw Wen Chen, Yasuhiro Morikawa, Takashi Kurimoto, and Ryuichiro Kamimura – ULVAC, Inc.

2. Chip Last Fan-Out Chip on Substrate (FOCoS) Solution for Chiplets Integration
Teck-Chong Lee, Shu-Han Yang, Hsin-Yi Wu, and You-Jun Lin – ASE Group

3. Die to Wafer Hybrid Bonding for Chiplet and Heterogeneous Integration: Die Size Effects Evaluation-Small Die Applications
Guilian Gao, Laura Mirkarimi, Gill Fountain, Dominik Suwito, Jeremy Theil, Thomas Workman, Cyprian Uzoh, Bongsub Lee, KM Bang, and Gabe Guevara – Xperi Corporation

4. Yield Improvement in Chip to Wafer Hybrid Bonding
Ser Choong Chong, Cereno Daniel Ismael, Pei Siang Lim, Cheng Yi Shim, Wai Song Lai, and Woon Leng Loh – Institute of Microelectronics (IME), A*STAR

5. Study of Parameter Tuning for the Curing Condition on ABF Type for Large FCBGA Package
Rick Ye, Eric Chen, Wen-Yu Teng, Andrew Kang, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.

6. Next Gen Laser-Assisted Bonding (LAB) Technology
SeokHo Na, MinHo Gim, ChoongHoe Kim, DongHyeon Park, DongSu Ryu, DongJoo Park, and JinYoung Khim – Amkor Technology

7. Swelling Analysis of Negative-tone Photosensitive Dielectric Materials for Fine Pitch Redistribution Layers
Daiki Yukimori, Go Inoue, Nobuhiro Ishikawa, and Toshiyuki Ogata – TAIYO HOLDINGS Co., Ltd.

8. RF Characterization in Range of 18GHz in Fan-Out Package Structure Molded by Epoxy Molding Compound with EMI Shielding Property
Eun Ha, Haksan Jeong, Kyung Deuk Min, Kyung-Yeol Kim, Dong-Gil Kang, and Seung-Boo Jung – Sungkyunkwan University

9. Plasma Chamber Environment Control to Enhance Bonding Strength for Wafer-to-Wafer Bonding Processing
Wooyoung Kim, Yongin Lee, Wonyoung Choi, Kyeongbin Lim, Bumki Moon, and Minwoo Rhee – Samsung Electronics Co., Ltd.

10. Study of Large Exposure Field Lithography for Advanced Chiplet Packaging
Hiromi Suda, Douglas Shelton, Hiroki Takada, Yoshio Goto, Kosuke Urushihara, and Ken-Ichiro Shindoa – CANON

11. Epoxy Resin with Metal Complex Additives for Improved Reliability of Epoxy-Copper Joint
Jiaxiong Li, John Wilson, Dylan Cheung, Zhijian Sun, Kyoung-sik Moon, Madhavan Swaminathan, and Ching-Ping Wong – Georgia Institute of Technology

12. Wirebonding Based 3-D SiC IC Stacks for High Temperature Applications
Feng Li and Srividya Raveendran – University of Idaho

13. Electrical Design and Modeling of Silicon Carbide Power Modules for Inverter Application
Vignesh Shanmugam Bhaskar, Jong Ming Chinq, Kazunori Yamamoto, and Gongyue Tang – Institute of Microelectronics (IME), A*STAR

14. Reliability of Component Attachment Using ECA and LTS on Flexible Additively Printed Ink-Jet Circuits for Signal-Filtering in Wearable Applications

Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. in Exhibit Hall - Eventide Pavilion

Pradeep Lall, Kartik Goyal, and Jinesh Narangaparambil – Auburn University; Scott Miller – NextFlex National Manufacturing Institute

15. Micro-Spray with Silver Ink for Maskless Selective-Area EMI Shielding
Kisu Joo, Kyu Jae Lee, Jung Yoon Moon, Yoon-Hyun Kim, Jinhwan Chung, Se Young Jeong, and Seung Jae Lee – Ntrium, Inc.

16. Embedded-IC Package Using Si-Interposer for mmWave Applications
Hyun-Beom Lee and Jong-Min Yook – Korea Electronics Technology Institute; Young-Gon Kim and Wansik Kim – LIG Nex1 Corporation; Sosu Kim – Agency for Defense Development; Byung-Wook Min – Yonsei University

17. Carrier Systems for Collective Die-to-Wafer Bonding
Koen Kennes, Alain Phommahaxay, Samuel Suhard, Pieter Bex, Steven Brems, Xiao Liu, Sebastian Tussing, Gerald Beyer, and Eric Beyne – Imec; Alice Guerrero – Brewer Science, Inc.

18. Superb Sinterability of the Cu Paste Consisting of Bimodal Size Distribution Cu Nanoparticles for Low-Temperature and Pressureless Sintering of Large-Area Die Attachment and the Sintering Mechanism
Bin Hou, Hai-Jun Huang, Chun-Meng Wang, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

19. Reliability of Ag Bonding Wires and iCoated Variants from the Perspective of IMC Degradation and Correlation to Wire and Epoxy Molding Compound Material Properties Under Corrosive Environment
Randolph Flauta, April Joy Garete, Mark Luke Farrugia, and Sreetharan Sekaran – Nexperia; Haibin Chen – Hong Kong University of Science and Technology

20. Design and Simulation to Reduce the Crosstalk of Ultra-Fine Line Width/Space in the Redistribution Layer(RDL)
Ziyu Liu, Lin Chen, and Qingqing Sun – Fudan University; Long Bai and Ziyuan Zhu – Southwest University

21. Influence of Tribo-Mechanical Characteristics of Advanced EN Coating for Electronic Packaging Enclosures
Muralidharan Sundararajan and Mutharasu Devarajan – Western Digital

22. Analysis on Optimal Chip Floorplanning Considering Various Types of Decoupling Capacitors in Package PDN
Jisoo Hwang, James Jeong, Heejung Choi, Jun So Pak, Heeseok Lee, Minkyu Mike Kim, and Ilryong Kim – Samsung Electronics Co., Ltd.

23. Novel Polymer Design for Ultra-Low Stress Dielectrics
Matthias Koch, Jens Pradella, and Gregor Larbig – Merck KGaA

Thursday, June 2, 2022

Session 40: Interactive Presentations 4
Time: 2:00 PM – 4:00 PM

Committee: Interactive Presentations

Coral Foyer

Session Co-Chairs:
Mark Poliks
Binghamton University
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Rao Bonda
Amkor Technology, Inc.
Email: rao.bonda@amkor.com

Kristina Young
GlobalFoundries
Email: Kristina.Young@globalfoundries.com

1. Ultra-High Conductivity Interconnects for 77K CMOS Using Heterogeneous Integration
Golam Sabbir and Subramanian S. Iyer – University of California, Los Angeles

2. Functional Demonstration of < 0.4 pJ/bit, 9.8 µm Fine-Pitch Dielet-to-Dielet Links for Advanced Packaging Using Silicon Interconnect Fabric
Krutikesh Sahoo, Uneeb Rathore, SivaChandra Jangam, Tri Nguyen, Dejan Markovic, and Subramanian S. Iyer – University of California, Los Angeles

3. Integration of High Performance GaN LEDs for Communication Systems and Smart Society
Zeinab Shaban, Mehrdad Saei, Brian Corbett, and Zhi Li – Tyndall National Institute

4. Low Temperature Metal-to-Metal Direct Bonding in Atmosphere Using Highly (111) Oriented Nanotwinned Silver Interconnects
Ching-Yao Cheng, Po-Hsien Wu, Leh-Ping Chang, and Fan-Yi Ouyang – National Tsing Hua University

5. Scalable through Mold Interconnection Realization for Advanced Fan Out Wafer Level Packaging Applications
Aurélia Plihon, Edouard Déschaseaux, Rémi Franiatte, Jérome Dechamp, Simon Vaudaine, Jennifer Guillaume, Catherine Brunet-Manquat, Stéphane Moreau, and Perceval Coudrain – CEA-LETI

6. A Hybrid Bonding Interconnection with a Novel Low Temperature Bonding Polymer System
Yu-Min Lin, Po-Chih Chang, Wei-Lan Chiu, Tao-Chih Chang, and Hsiang-Hung Chang – Industrial Technology Research Institute; Baron Huang, Chia-Hsin Lee, Mei Dong, and Duo Tsai – Brewer Science, Inc.; Chang-Chun Lee – National Tsing Hua University; Kuan-Neng Chen – National Yang Ming Chiao Tung University

7. Signal Integrity Design and Analysis with Link Budget Results of HBM2E Module on Latest High Density Organic Laminate
Frank Libsch, Hiroyuki Mori, and Xiaoxiong Gu – IBM Corporation

8. Chiplets Integrated Solution with FO-EB Package in HPC and Networking Application
Po Yuan (James) Su, David Ho, Jacy Pu, and Yu Po Wang – Siliconware Precision Industries Co., Ltd.

9. Effect of Isothermal Aging on the Properties of In-48Sn and In-Sn-8Cu Alloys
Duy Le Han, Hiroaki Tatsumi, Fupeng Huo, and Hiroshi Nishikawa – Osaka University

10. Ag Die-Attach Paste Modified by WC Additive for High-Temperature Stability Enhancement
Yang Liu, Chuantong Chen, Takuya Naoe, Hiroshi Nishikawa, and Katsuaki Suganuma – Osaka University; Minoru Ueshima and Takeshi Sakamoto – Daicel Corporation

11. PSI Design Solutions for High-Speed Die-to-Die Interface in Chiplet Applications
Taeyun Kim, Sungwook Moon, Chanmin Jo, Seungki Nam, and Yongho Lee – Samsung Electronics Co., Ltd.

12. Thermal Compression Cu-Cu Bonding Using Electroless Cu and the Evolution of Voids Within Bonding Interface
Ching-Han Huang, Po-Shao Shih, Jeng-Hau Huang, S.J. Gräfner, Yu-An Chen, and C. Robert Kao – National Taiwan University

13. Novel Zero Side-Etch Process for <1µm Package Redistribution Layers
Pratik Nimbalkar, Pragna Bhaskar, Christopher Blancher, Mohanalingam Kathaperumal, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology

14. Printed Microwave Connector
Jotham Kasule, Shokat GanjeheizadehRohani, Mark Pothier, Yuri Piro, Alkim Akyurtlu, and Craig Armiento – University of Massachusetts Lowell

15. MaxQFP - A High Density QFP
Chu-Chung Stephen Lee, TuAnh Tran, Andrew Mawer, Glenn Daves, X. S. Pang, and J. Z. Yao – NXP Semiconductors

16. Creep and Microstructure Evolutions in SAC305 Lead Free Solder Subjected to Different Thermal Exposure Profiles
S. M. Kamrul Hasan, Mohammad Al Ahsan, Jeffrey C. Suhling, Pradeep Lall, Abdullah Fahim, and K. M. Rafidh Hassan – Auburn University

17. Modeling of Cu-Cu Thermal Compression Bonding
Kai-Cheng Shie, Dinh-Phuc Tran, Hung-Che Liu, and Chih Chen – National Yang Ming Chiao Tung University; A. M. Gusak – Cherkasy National University; K. N. Tu – City University of Hong Kong

18. Mechanical Properties and Microstructures of Cu/In-48Sn Alloy/Cu with Low Temperature TLP Bonding
DongGil Kang, KyungDeuk Min, Kyung-Yeol Kim, HakSan Jeong, Eun Ha, and Seung-Boo Jung – Sungkyunkwan University

19. Novel Pressure-Assist and Pressure-Less Silver Sintering Paste for SiC Power Device Attachment on Lead Frame Based Package
Leong Ching Wai, Kazunori Yamamoto, Gongyue Tang, and Jacob Jordan Soh – Institute of Microelectronics (IME), A*STAR

20. Modeling High-Frequency and DC Path of Embedded Discrete Capacitor Connected by Double-Side Terminals with Multi-Layered Organic Substrate and RDL Based Fan-Out Package
Heeseok Lee, Kyojin Hwang, Henry Kwon, Jisoo Hwang, Junso Pak, and Ju Yeon Choi – Samsung Electronics Co., Ltd.

21. Characterization of Low Loss Dielectric Materials for High-Speed and High-Frequency Applications
ZN Lee, John Lau, CT Ko, Tim Xia, Eagle Lin, Henry Yang, Bruce Lin, Tony Peng, Leo Chang, Jia Chen, and Yi-Hsiu Fang – Unimicron Technology Corporation

22. Evaluation on Bonding Reliability of SAC305/Sn-57.5Bi-0.4Ag BGA Solder Joints with Drop Impact Test
Geunsik Oh, Kyung Deuk Min, Eun Ha, Jun Ho Jang, and Seung-Boo Jung – Sungkyunkwan University

23. High Throughput Void-Free Soldering with Pneumatic Reflow Method in Lead-Free Solder Die Attach
Huan-Ping Su and Auger Horng – Ableprint Technology Co., Ltd.; Chun-Cheng Lee – Shenmao Technology Co., Ltd.

24. Influence of Prepreg Material Properties on Printed Circuit Board (PCB) Stack-up
Tomin Liu and Mutharasu Devarajan – Western Digital

Friday, June 3, 2022

Session 41: Student Interactive Presentations
Time: 8:30 AM – 10:30 AM

Committee: Interactive Presentations

Coral Foyer

Session Co-Chairs:

Ibrahim Guven
Virginia Commonwealth University
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Alan Huffman
SkyWater Technology
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Biao Cai
IBM Corporation
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1. Machine Learning Assisted Counterfeit IC Detection Through Non-Destructive Infrared (IR) Spectroscopy Material Characterization
Chengjie Xi, John True, Nathan Jessurun, Aslam Khan, Mark Tehranipoor, and Navid Asadizanjani – University of Florida

2. Pressureless and Low Temperature Sintering by Ag Paste for the High Temperature Die-Attachment in Power Device Packaging
Chuncheng Wang – Osaka University; Xu Zhang, Yudui Zhang, Tao Zhao, Pengli Zhu, Rong Sun, Hiroshi Nishikawa, and Liang Xu – Shenzhen Institute of Advanced Electronic Materials

3. Smartphone App-Enabled Flex sEMG Patch using FOWLP
Pragathi Venkatesh, Randall Irwin, Arsalan Alam, Michael Molter, Ayush Kapoor, Bilwaj Gaonkar, Luke Macyszyn, and Subramanian S. Iyer – University of California, Los Angeles; M. Selvan Joseph – California State University, Los Angeles

4. A Deep Learning Approach for Reflow Profile Prediction
Yangyang Lai, Jun Kataoka, Ke Pan, Jonghwan Ha, Junbo Yang, Karthik A. Deo, Jiefeng Xu, and Seungbae Park – Binghamton University

5. Effects of Temperature on the Adhesive Performance of High Tg Underfill in 2.5D Heterogeneous Integrated Packaging
Guolin Zhao, Haoliang Lin, Houya Wu, Bin Wang, Yuanyuan Yang, Gang Li, Pengli Zhu, and Rong Sun – Chinese Academy of Sciences; Ching-Ping Wong – Georgia Institute of Technology; Wenhui Zhu – Central South University

6. Demonstration and Comparison of Vertical Via-less Interconnects in Laminated Glass Panels from 40 -170GHz
Lakshmi Narasimha Vijay Kumar, Kyoung-Sik Moon, and Madhavan Swaminathan – Georgia Institute of Technology; Kimiyuki Kanno, Hirokazu Ito, Taku Ogawa, and Koichi Hasegawa – JSR Corporation

7. Monte Carlo Particle Simulation of Avalanche Breakdown in a Reverse Biased Diode with Full Band Structure
Ze Sun, Manish Kizhakkeveettil Mathew, and DongHyun Kim – Missouri University of S&T; Ryan From – Boeing

8. Characterization and Analysis of Moisture Absorption in Embedded System in Packaging
Rongwei Gao, Rui Ma, Jun Li, Qidong Wang, Liqiang Cao, and Meiying Su – Institute of Microelectronics of Chinese Academy of Science

9. Methods of Printing Copper for PCB Repair
Dylan Richmond, Emuobosan Enakerakpo, Mohammed Alhendi, and Mark Poliks – Binghamton University; Peter McClure and Jim Wilcox – Universal Instruments Corp.

10. Novel Sn–Cu Based Composite Solder Preforms Capable of Low Temperature Reflow for Die Attachment of High Temperature Power Electronics and the Transient Liquid Phase Bonding Process
Ru-Zeng Shi, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

11. Trust Validation of Chiplets Using a Physical Inspection Based Certificate Authority
Nidish Vashistha, Md Mahfuz Al Hasan, Fahim Rahman, Navid Asadizanjani, and Mark Tehranipoor – University of Florida

12. Security Challenges of MEMS Devices in HI Packaging
Aslam Khan, Keon Sahebkar, Chengjie Xi, Mark Tehranipoor, Ryan F. Need, and Navid Asadizanjani – University of Florida

13. Influence of Height Difference Between Chip and Substrate on RDL in Silicon-Based Fan-Out Package
Xiao Han, Wei Wang, and Yufeng Jin – Peking University

14. Symmetric-Cell EBG Theory and Its Applications to Vias Daisy Chain for Residual Stub Detection
Yu-Kuang Wang and Ruey-Beei Wu – National Taiwan University; Ming-Tsun Lu, Jun-Rui Huang, and Ching-Sheng Chen – Unimicron Technology Corporation

15. Millimeter-Wave Antenna Design and Performance Analysis for Automotive Applications
Mohammad Pervez, Amanpreet Kaur, and Md Mamun Ur Rashid – Oakland University

Friday Refreshment Break: 9:15 a.m. - 10:00 a.m. in Silver Pearl & Coral Foyers

Technology Corner Exhibits

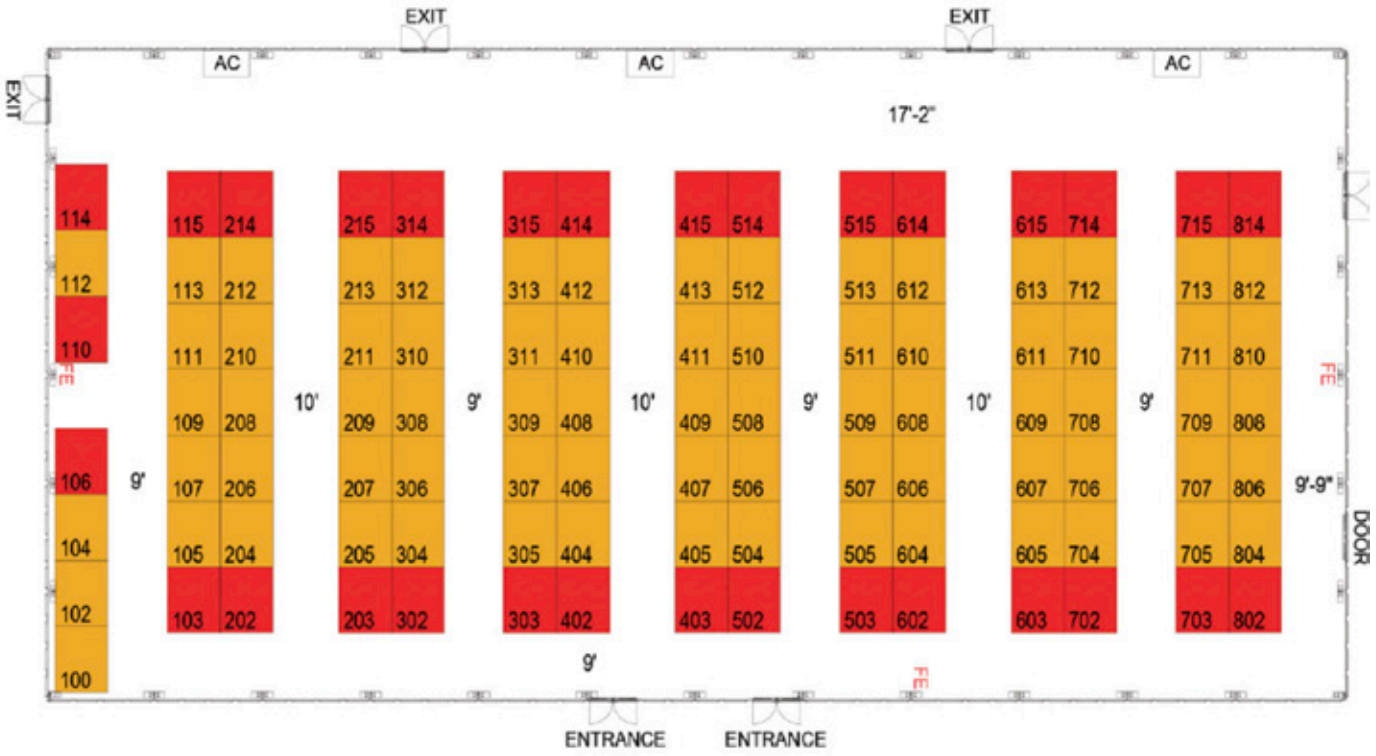
Wednesday, June 1

9:00 a.m. - 12:00 Noon / 1:30 p.m. - 6:30 p.m.

Thursday, June 2

9:00 a.m. - 12:00 Noon / 1:30 p.m. - 4:00 p.m.

Eventide Pavilion



Interactive Presentation Sessions

Wednesday, June 1

Session 37: 9:00 a.m. - 11:00 a.m. / Session 38: 2:00 p.m. - 4:00 p.m.

Thursday, June 2

Session 39: 9:00 a.m. - 11:00 a.m. / Session 40: 2:00 p.m. - 4:00 p.m.

Friday, June 3

Session 41: 8:30 a.m. - 10:30 a.m.

Coral Foyer

TECHNOLOGY CORNER EXHIBITORS

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The 3D Systems Packaging Research Center (PRC) at Georgia Tech is a graduated NSF Engineering Research Center focusing on advanced packaging and system integration leading to System on Package (SoP) technologies. The center conducts research and education in all aspects of packaging that includes design, materials, process, assembly, thermal management, and integration driven by applications, which include broad areas such as high-performance computing, artificial intelligence, automotive, broad-band wireless and space. The center team consists of 29 faculty from five schools, 11 research/administrative staff, 50+ graduate/undergraduate students and several visiting engineers. This is enabled through collaboration with over 40 industry/govt. organizations and 14 universities.

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Adeia is the newly launched brand for the intellectual property (IP) licensing business of Xperi Holding Corporation. Adeia invents, develops and licenses fundamental innovations that shape the way millions of people explore and experience entertainment and enhance billions of devices in an increasingly connected world. Leveraging the combination of highly experienced technologists, scientists and engineers and advanced research and development labs in San Jose, California and Raleigh, North Carolina, Adeia develops industry-leading 3D integration solutions such as hybrid bonding that meet the demand for greater functionality, higher performance and smaller size for next generation electronics

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AI Technology, Inc. (AIT) is an ISO9001:2008 certified United States manufacturer and one of the leading forces in the development of advanced material and adhesive solutions including: Gap-Filling Compressible Phase-Change Pads, Thermal Gels, Thermal Grease, Stress-free Adhesive Films, Adhesive Pastes, RF/EMI shielding solutions. We also offer Conductive and Dielectric materials, high temperature solutions and room temperature cure materials.

Our core products include: dicing die-attach adhesive films, conformal coatings, UV-block coatings, encapsulants, sealants, thermal gels, thermal greases, RF/EMI shielding solutions, gap-filling pads, compressible phase-change pads, stress-free and thermally conductive epoxy pastes and films in conductive or dielectric variations and dicing tapes,

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As the nation's first complete end-to-end silicon photonic manufacturing ecosystem, AIM Photonics provides small and medium enterprises with crucial technology on-ramps and access to strategic U.S. government, industry, and academic communities to accelerate the transition from concept to manufacturing-ready prototypes.

Our state-of-the-art 300 mm test, assembly and packaging facility in Rochester, NY is the nation's only accessible advanced wafer-level and die-level test and assembly facility offering both photonic and electronic packaging capabilities. Customers and members have access to an extensive toolset with capabilities for standard processes such as fiber attach, wire bonding, die attach, dicing and flip chip, as well as advanced packaging, co-packaging, and heterogeneous integration capabilities.

We also provide access to a full suite of advanced metrology tools and test capabilities, including waveguide loss, transmission, optical modulator and photodiode bit error rate testing, as well as DC/RF electronic testing.

Our silicon photonics Process Development Kits (PDKs) and experienced Multi-Project Wafer (MPW) team at Albany NanoTech are available to help you design, build and package your photonic integrated circuit prototypes from start to finish.

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Akrometrix is the leading global manufacturer of Thermal Warpage Measurement systems for R&D labs, as well as Room Temperature systems on the SMT line. All of our systems utilize Shadow Moiré as the base measurement technology. We have shipped over 350 systems to customers in over 20 countries worldwide. We also provide testing services for customers who do not have their own Akrometrix equipment at our headquarters in Atlanta, GA, and through our partnership with Nufesa Labs, based in Barcelona, Spain.

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Amkor Technology, Inc. is one of the world's largest providers of high-quality semiconductor packaging and test services. Founded in 1968, Amkor pioneered the outsourcing of IC packaging and test and is a strategic manufacturing partner for the world's leading semiconductor companies, foundries and electronics OEMs.

Amkor's broad package portfolio and technology leadership offer our customers semiconductor and test solutions to enable 5G, AI, Automotive, Communications, Computing, Consumer, Industrial, IoT and Networking products.

Services include package design and development, wafer probe and package test, wafer bumping and redistribution, package assembly and final test. Engineering services offer best-in-class thermal, electrical and mechanical modeling and characterization as well as design automation. Test engineering services range from test program development to full product characterization of packaged RF, mixed signal, logic and memory devices.

Amkor offers a flexible supply chain including

production facilities, product development centers and sales and support offices located in key electronics manufacturing regions in Asia, Europe and the US.

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AOI Electronics is the No.1 sales ranking OSAT in Japan, and its business focuses on the assembly and testing of electronic products. We have over 50 years of semiconductor packaging and testing experiences, and serve customers around the world. AOI Electronics provides a variety of packaging technologies, FOLP® (Fan-Out PLP), WLP, FC-QFN, Cu-Pillar, SiP, Sensor, MEMS etc. We offer advanced packaging technologies of 5G, RF, Power IC (Built-in passive, Embedded Multi-Chip, SiP) and test solutions for communications applications including mobile and infrastructure markets.

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Asahi Kasei is a leading chemical company developing and supplying high performance materials to the electronics industry for years.

Our PIMEL™ are photosensitive polyimide, PBO and new polymer base material for semiconductor buffer coatings, insulation layer for redistribution layers (RDL) in semiconductor packaging. PIMEL™ has been widely used in many IC fabs / OSATs with proven track records in most semiconductor companies. Based on our technology expertise and experiences in the field, our low temperature cure polyimides have rapidly increased its applications for Wafer Level Fan-Out (WLFO) and Panel Level Fan-out(PLFO), and other advanced packages for mobile, automotive, server and other emerging technologies.

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ASE, Inc. is the leading global provider of semiconductor manufacturing services in assembly and test. In a world increasingly reliant on semiconductor technology to achieve evolving lifestyle, efficiency and sustainability goals, innovation is at the heart of what ASE does. Alongside a broad portfolio of established assembly and test technologies, ASE is delivering innovative heterogeneous integration, advanced packaging, and chiplet solutions to meet growth momentum across a broad range of applications, including 5G, Automotive, AI, HPC, and more. To learn about our advances in SiP, RDL, Fanout, MEMS & Sensors, Flip Chip, and, 2.5D, 3D & TSV technologies, please ask the ASE experts at our ECTC booth or visit aseglobal.com or follow us on Linkedin: @asegroup_global.

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ASM AMICRA Microtechnologies GmbH, headquartered in Regensburg, Germany, is a worldwide leading supplier for ultra-high precision die attach systems. ASM AMICRA systems specialize in submicron placement accuracy to ±0.2µm@3s for the photonics and semiconductor market and also support die attach, flip chip, eutectic, epoxy and Mass Transfer Printing (MTP) processes. Markets served include silicon photonics, optoelectronics, active optical cable (AOC), VCSELs, laser diodes, 2.5D/3D ICs, wafer level packaging (WLP), large panel fan-out/ embedded wafer level packaging (EWLP), and automotive sensors/LiDAR.

ASM AMICRA is a subsidiary of ASM Pacific Technology Limited, a leading global supplier of hardware and software solutions for the manufacture of semiconductors and electronics, headquartered in Singapore.

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ASMPT, founded in 1975, is the only company in the world that offers high-quality equipment for all major steps in the electronics manufacturing process - from carrier for chip interconnection to chip assembly and packaging to SMT. No other supplier offers a comparable range and depth of process expertise.

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AT&S is one of the globally leading manufacturers of high-end printed circuit boards and IC substrates. At its locations in Europe and Asia, AT&S develops and produces high-tech solutions for its global partners, especially for applications in the areas of communication, computer and consumer electronics, mobility, industry and medical technology. As an international enterprise, AT&S has a global presence, with production facilities in Austria (Leoben and Fehring) and plants in India (Nanjangud), China (Shanghai, Chongqing) and Korea (Ansan, near Seoul).

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Atotech (NYSE: ATC) is a leading specialty chemicals technology company and a market leader in advanced electroplating solutions. Atotech delivers chemistry, equipment, software, and services for innovative

technology applications through an integrated systems-and-solutions approach. Atotech solutions are used in a wide variety of end-markets, including smartphones and other consumer electronics, communications infrastructure, and computing, as well as in numerous industrial and consumer applications such as automotive, heavy machinery, and household appliances.

Atotech, headquartered in Berlin, Germany, is a team of 4,000 experts in over 40 countries generating annual revenues of $1.2 billion (2020). Atotech has manufacturing operations across Europe, the Americas, and Asia. With its well-established innovative strength and industry-leading global TechCenter network, Atotech delivers pioneering solutions combined with unparalleled on-site support for over 9,000 customers worldwide. For more information about Atotech, please visit us at atotech.com.

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Besi is a leading supplier of assembly equipment for the global semiconductor and electronics industries offering high levels of accuracy, productivity and reliability at a low cost of ownership. Besi has developed leading edge assembly processes ranging from advanced Hybrid Bonding with sub-micron accuracy to equipment for leadframe, substrate and wafer level packaging applications. Besi's equipment offerings include conventional and advanced die attach, molding, trim & form, saw singulation and plating. Besi supports a wide range of end-user markets including electronics, mobile internet, computer, automotive, industrial, LED and solar energy. Besi customers are primarily leading semiconductor manufacturers, assembly subcontractors and electronics and industrial companies. The principal brand names for Besi's assembly equipment systems include Datacon, Esec, Fico and Meco.

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S3IP brings the capabilities and technical resources of Binghamton University, a leading research institution, at the disposal of electronics and energy systems manufacturers and similar manufacturing industries. Our 6 research centers address pressing real-world challenges in microelectronics manufacturing, flexible hybrid electronics, and heterogeneous integration of electronics, and thin film electronic devices for energy harvest and storage. Advanced battery research is directed by Dr. Stan Whittingham, 2019 Nobel Laureate for invention of the Li-ion battery. Our professional staff, backed by the deep expertise of faculty, assists companies in problem solving and use of our 7 laboratories addressing manufacturing methods and materials, thermal management, failure analysis, and reliability improvement.

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Cadence is a pivotal leader in electronic design, building upon more than 30 years of computational software expertise. We apply our underlying Intelligent System Design strategy to deliver software, hardware, and IP that turn design concepts into reality. Our customers are the world's most innovative companies, delivering extraordinary electronic products from chips to boards to systems for the most dynamic market applications, including consumer, hyperscale computing, 5G communications, automotive, mobile, aerospace, industrial, and healthcare. Six out of seven years in a row, Fortune magazine has named Cadence one of the 100 Best Companies to Work For.

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Canon U.S.A., Inc. (www.usa.canon.com) is a leader in Office Products, Imaging Systems, Medical Systems and Industrial Products. The Canon Industrial Products Division provides advanced wafer and panel process equipment for a wide range of applications, from FEOL semiconductor processes to More-Than-Moore applications including 3D-IC, Interposer, FOWLP and FOPLP Advanced Packaging processes.

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ZEISS is an internationally leading technology company operating in the fields of optics and optoelectronics.

ZEISS has the most comprehensive portfolio of light, X-ray, electron and ion beam microscope systems in the industry and is a leading solution provider to the global semiconductor community. Solutions span semiconductor manufacturing from wafer fab through packaging and assembly. ZEISS materials characterization and non-destructive failure analysis solutions deliver actionable information to both wafer fab and packaging/assembly processes to meet the semiconductor industry's challenges for next-generation devices.

ZEISS is active globally in almost 50 countries with around 30 production sites, 60 sales and service companies and 27 R&D facilities. Founded in 1846 in Jena, the company is headquartered in Oberkochen, Germany. The Carl Zeiss Foundation, one of the largest foundations in Germany committed to the promotion of science, is the sole owner of the holding company, Carl Zeiss AG.

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CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 1,900, a portfolio of 3,100 patents, 11,000 sq. meters

of cleanroom space and a clear IP policy, the institute is based in Grenoble, France, and has offices in Silicon Valley and Tokyo. CEA-Leti has launched 70 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

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Headquartered in Kalispell, Montana, ClassOne Technology has become a preferred provider of advanced wet-chemical wafer processing equipment for ≤200mm semiconductor wafers. The Solstice® series performs high-performance single-wafer electrochemical deposition (ECD) and wafer surface preparation processes. The Solstice platform can be configured with up to eight processing chambers to cover process development as well as low-, medium-, and high-volume production. The Trident™ series comprises an array of high-efficiency, highly dependable spin-rinse-dryers, and spray solvent tools for batch-processing. The company brings high-performance processing technology to compound semiconductors and key markets including photonics, power, 5G, microLED and MEMS. Hundreds of ClassOne tools are presently in use building leading-edge devices in major fabs and research facilities around the world.

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Corning offers advanced glass carriers in a wide range of CTEs in both wafer and panel formats. A CTE-matched carrier substrate helps customers minimize their problem of in-process warp. We offer quick sampling in small quantities in minimal turnaround time.

Corning has invented a new generation of high-performance ceramic substrates in entirely new form factors that can help solve customer problems and lead technology developers into the future. Corning Ribbon Ceramics are ceramics as you've never seen them before: thin, flexible, durable, and available in large area, continuous format.

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Powered by the 3DEXPERIENCE® platform, SIMULIA delivers realistic simulation applications that enable users to reveal the world we live in. SIMULIA applications accelerate the process of evaluating the performance, reliability and safety of materials and products before committing to physical prototypes.

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Deca was born of a passion to transform the way the world builds advanced electronic devices. In our first decade, our 10X thinking brought to life exciting breakthroughs with M-Series™ and Adaptive Patterning®. As a pure-play technology development, transfer and licensing company, Deca is the leading independent provider of advanced packaging technology in the semiconductor industry.

Our flagship M-Series is a fully encapsulated wafer & panel-level fan-out technology which provides an ideal structure for single & multi-die packaging, chiplet integration, 3D PoP and embedded die interposers. M-Series is delivering exceptional quality and reliability for leading Smartphone manufacturers around the globe with shipment volumes exceeding one billion units per year.

Deca's Adaptive Patterning technology compensates for natural variation in embedded die structures without costly processes or design limitations. After high-speed optical measurement, Adaptive Patterning generates a bespoke and optimized layout which is precisely aligned to each device. The power of Adaptive Patterning is realized through Adaptive Patterning Design Kits (APDKs) with provided integrated design templates, tech files, stack-ups, DRC decks, and AP Studio software.

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For 53 years, DISCO Hi-Tec America, Inc. has been a leader in the semiconductor industry in cutting (Kiru), grinding (Kezuru), and polishing (Migaku) technologies. DISCO's focus has expanded beyond mechanical dicing to include laser and plasma singulation. DISCO continues to be the leader in wafer thinning and polishing/stress relief with technologies such as SDBG enabling thinning of die to 20um or less. To support the increasing complexity in today's packages, DISCO has also released equipment capable of laser via drilling in non-silicon transparent materials, silicon carbide ingot slicing (KABRA), and laser lift off. In order to support research and development efforts, joint development initiatives, and next generation product prototyping, DISCO Hi-Tec America's KKM Services lab in Santa Clara offers capability to process materials with our latest advanced cutting, grinding, and polishing technologies.

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DuPont Electronics & Industrial is a global supplier of new technologies and performance materials serving the semiconductor, circuit board, display, digital and flexographic printing, healthcare, aerospace, industrial and transportation industries. From advanced technology centers worldwide, teams of talented research scientists and application experts work closely with customers, providing solutions, products and technical service to enable next-generation technologies.

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Ebinax provides advanced plating service. Our mission is to pursue new surface treatment possibilities to contribute to the future of manufacturing.

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Evatec provides PVD solutions that are tailored to the Advanced Packaging market combining best in class cost of ownership with unique technology innovations to meet up with today's and future requirements. Wafer platforms that process up to 300mm formats feature highest levels of throughput, support the use of long life targets and are equipped with a unique degassing technology that achieves best in class contact resistance and layer uniformity performance required in WLCSP, FOWLP and 2.5D/3D devices. FOPLP applications and next generation IC substrate technologies are supported by Evatec`s market leading CLUSTERLINE® 600 equipment platform. The panel focused PVD equipment platform is capable of processing substrate sizes up to 650 x 650 mm, delivering highest levels in outgassing performance, layer adhesion and stack uniformity. In EMI shielding of chips on a package level, Evatec offers production solutions with the step coverage, film adhesion and low process temperatures required to protect the chip effectively at high throughput.

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EV Group (EVG) is a leading supplier of high-volume production equipment and process solutions for the manufacture of semiconductors, MEMS, compound semiconductors, power devices and nanotechnology devices.

A recognized market and technology leader in wafer-level bonding and lithography for advanced packaging and nanotechnology, EVG's key products include wafer bonding, thin-wafer processing and lithography/nanoimprint lithography (NIL) equipment, photoresist coaters, as well as cleaning and inspection/metrology systems.

With state-of-the-art application labs and cleanrooms at its headquarters in Austria, as well as in North America and Asia, EVG is focused on delivering superior process expertise to its global R&D and production customer and partner base – from the initial development through to the final integration at the customer's site.

Founded in 1980, EVG services and supports an elaborate network of global customers and partners all over the world, with more than 1100 employees worldwide and fully-owned subsidiaries in the U.S., Japan, South Korea, China and Taiwan.

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F&K Delvotec offers ultrasonic wire bonding and laser bonding equipment for mass production and R&D. Our equipment is flexible and covers most of the interconnect processes. Our applications team also supports small volume production and prototyping.

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ficonTEC provides device micro-assembly and testing solutions for the photonics industry. These solutions are realized as cutting-edge, high-precision production systems utilizing advanced automation approaches, regardless of the device material and target application. Our modular system architecture is additionally scalable, so that exploratory, proof-of-process development as well as high-volume manufacturing requirements are addressable – and anything in between.

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From Prototype to Production, Finetech supplies sub-micron accuracy die bonders for die attach, advanced packaging, and micro assembly applications. Manual, motorized, and automated models provide high process flexibility within one platform utilizing a modular, flexible design. Bonding technologies include thermo-compression, ultrasonic, adhesive, eutectic, sintering, ACF/ACP, Indium, flip chip and precision vacuum die bonding. Application areas cover photonics assembly, optical packages, sensors, Si photonics, microLEDs, focal plane arrays, chip-on-glass, chip-on-flex, MEMs/MOEMs and more. Finetech also provides advanced rework systems for today's challenging applications. The deep process knowledge we have gained through 30 years of experience adds value to our equipment. Our engineers work with customers to create effective solutions for specific applications - they understand that "one size" does not necessarily fit all.

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The business unit "Materials and Components of Electronics" at the Fraunhofer IMWS investigate electronic components, systems and materials, for example integrated semiconductor circuits, sensors and electronic components and assemblies. These are comprehensively analyzed and tested in order to understand in detail the relationship between technological manufacturing processes, operating conditions, microstructure and material properties and the functional properties that depend on them.

We support our partners in:
• accelerating the development of innovative material solutions and technologies
• qualifying new manufacturing processes for industrial practice
• achieving an optimal yield in series production
• ensuring a long service life of products in use
• bringing improved methods of material diagnostics to the market

The benefits for our customers include an increased innovation rate, high cost efficiency and an improved competitive position and thus optimized marketability.

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Invisible – but indispensable – nowadays nothing works without highly integrated microelectronics and microsystem technology. Reliable and cost-effective assembly and interconnection technologies are the foundation of integrating these in products. Fraunhofer IZM, a worldwide leader in the development and reliability analysis of electronic packaging technologies, provides its customers with tailor-made system integration technologies on wafer, chip and board level. Our research also ensures that electronic systems are more reliable, so that we can accurately predict lifecycle.

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FUJIFILM Electronic Materials is a leading supplier of advanced materials to the electronics industry. We offer a full complement of advanced photoimageable and non-photoimageable polyimide and PBO materials designed to meet current and future advanced packaging challenges. We have a unique dry film photoimageable dielectric material available in film thickness range of <5um to 200um. Fujifilm has demonstrated an innovative magnetic material technology drawn from our proprietary photoresist and magnetic materials expertise.

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HD MicroSystems L.L.C. (HDM) is the leading manufacturer of liquid polyimide (PI) and polybenzoxazole (PBO) dielectric coatings. HDM is introducing new High-Reliability, Low Temp Cure PI's, including NMP-Free. HDM polymeric materials are the process-of-record (POR) in many front-end wafer applications for interlayer (ILD) and stress buffer coatings (SB), as well as back-end advanced packaging technologies such as Flip Chip, WL-CSP, redistribution dielectric layers (RDL) and bonding adhesives, both temporary and permanent for 3D/TSV, wafer thinning, Flexible Hybrid and Micro LED applications. HDM is developing materials for low loss, high frequency RF applications. In addition to conventional spin coating, HDM is enabling coating methods such as slot die, ink jet ultrasonic spray, gravure and 3D printing.

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Heidelberg Instruments - The power of direct writing
Heidelberg Instruments is a world leader in the development and production of high-precision photolithography systems, maskless aligners and nanofabrication tools. With over 35 years of experience and more than 1,200 systems worldwide at industrial customers and in academic facilities, we provide lithography solutions specifically tailored to meet the micro- and nanofabrication requirements of our customers - no matter how challenging.

The systems range from small and easy to use tabletop systems to highly complex photomask production equipment with exposure areas of several square meters, for the fabrication of binary layouts and complex 2.5 and 3D structures in micro-optics, photonics, microfluidics and nanobiotechnology, electronics and communication technology, and in materials science. Industry leaders in the fields of MEMS, BioMEMS, ASICS, TFT, displays, micro-optics, sensors, semiconductors and automotive are among our customers.

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Henkel is the premier materials supplier for the electronics assembly and semiconductor packaging industries. Our advanced formulations include a range of products that facilitate electrical interconnect, provide structural integrity, offer critical protection, and transfer heat for reliable performance. We're proud to create products that improve today's electronic technologies and enable tomorrow's advances.

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IBM Assembly and Test
IBM Bromont is a world leader in semiconductor packaging technology and services. We invite you to take advantage of our experience, system level mindset and skilled engineers to execute your most advanced packaging and test solutions. Tap into our deep competencies as the industry continues to shift to custom SoCs and SiPs. IBM is known for its multi-chip packaging and heterogeneous integration.

We offer full turnkey solutions from modelling and characterization through Burn-in and test. Our test capability spans digital, analog, mixed signal, RF as well as multi-site programming, test pattern conversion, and load board design. We provide high quality mechanical, thermal and electrical design (including high speed/ SERDES, signal integrity and power integrity), ensuring effective execution of new and updated platforms. Services include materials and process characterization, optimized substrate design, and failure analysis. Package platforms range from large organic substrates to 2.3D, Silicon Photonics technologies and Si-bridge for chiplet interconnection with our DBHI packaging solution.

IBM will help you deliver differentiated solutions and meet even the toughest application goals.

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Angstrom Scientific Inc. represents a number of leading manufacturers supporting materials imaging, testing, and analysis. These include Hitachi: tabletop SEMs, Imina: nano-probe system and Point: EBIC/EBAC, Deben: Tensile Stages, and NenoVision: in-Situ SEM AFM. and Alemnis in-situ SEM nano-indenters. Please visit our booth 211 at ECTC to discuss your analysis needs.

Booth 107
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Indium Corporation is a premier materials refiner, smelter, manufacturer, and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil® . Founded in 1934, the company has global technical support and factories located in China, Germany, India, Malaysia, Singapore, South Korea, the United Kingdom, and the U.S.

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TDM by Insidix offers state of the art deformation or warpage measurement systems while devices under evaluation are experiencing

thermal stress. The technology uses phase shifting Projection Moiré, advanced 3D sensors, and temperature chambers that can withstand temperatures between -65°C to 400°C.

The systems are ideal for research development, quality and reliability, process development, and failure analysis studies. Present in semiconductor, medical, automotive, aerospace, and electronics industries.

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Integra Technologies is a global leader in the sourcing, packaging, testing and characterization of highly specialized, mission-critical semiconductor components and related value-added services for high-reliability ("Hi-Rel") applications where dependability and failure-free performance are of paramount importance. Integra provides a span of in-house services and capabilities to support a broad variety of Hi-Rel components throughout the entire value-added life-cycle - from prototyping, through testing, and ultimately to volume production. More specifically, Integra specializes in semiconductor die prep, packaging, assembly, test, reliability qualification, DPA and FA service for high-reliability applications.

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iST-Lab Service Provider

Founded in 1994, iST began its business from IC circuit debugging and modification and gradually expanded its scope of operations, including Failure Analysis, Reliability Verification, Material Analysis, Automotive Electronic Verification Platforms, Space Electronic Platforms and Signal Integrity Testing Services. iST has offered full-scope verification and analysis services to the IC engineering industry, its customers cover the whole spectrum of the electronics industry from IC design to end products.

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Automatic Visual Inspection for advanced package manufacturing process like micro bump, die crack, mark, component, underfill, mark depth, package total height, substrate warpage and others

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INVENTEC PERFORMANCE CHEMICALS is a global provider of SOLDERING, CLEANING & COATING materials for Electronic, Semiconductor and Industrial applications.

For almost 60 years we have shown leadership in innovation by putting ENVIRONMENT & HEALTH IMPACT, SUSTAINABILITY and RELIABILITY at the core of our product development.

With ISO 9001 & 14001 production sites in France, Switzerland, USA, Mexico, Malaysia and China we can guarantee a smooth and cost-effective supply chain. On top of this, all our production facilities are equipped with a CLEANING APPLICATION CENTER, where customers are invited to test our proposed cleaning solutions.

INVENTEC supplies to many industries but the excellent performance of our products in applications which demand high reliability, leads us to focus especially on the AUTOMOTIVE, AEROSPACE, SEMICONDUCTOR, ENERGY and MEDICAL industry.

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JCET Group is the world's leading integrated-circuit manufacturing and technology services provider, offering a full range of turnkey services that include semiconductor package integration design and characterization, R&D, wafer probe, wafer bumping, package assembly, final test and drop shipment to vendors around the world. Our comprehensive portfolio covers a wide spectrum of semiconductor applications such as mobile, communication, compute, consumer, automotive and industry etc., through advanced wafer level packaging, 2.5D/3D, System-in-Packaging, and reliable flip chip and wire bonding technologies. JCET Group has two R&D centers in China and Korea, six manufacturing locations in China, Korea and Singapore, and sales centers around the world, providing close technology collaboration and efficient supply-chain manufacturing to customers in China and around the world.

Booth 611
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JIACO Instruments Microwave-Induced-Plasma decapsulation is the new standard for reliable Reliability Test & Failure Analysis. The fully automated decapsulation process is highly selective; critical failure sites in advanced packages (e.g. SiP, WLCSP, 2.5D, 3D) are retained without process induced damage to challenging materials e.g. Ag, Cu bond wire, GaAs, SiC, Cu RDL, BOAC, SAW/BAW filters etc.

The JIACO Instruments MIP system has been in the market since mid-2016 and is now in use by many renown global companies for reliable failure analysis and quality control.

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JSR's THB series of thick film photoresists, along with WPR series of dielectric coatings and LP series of lift-off photoresists, offer advanced packaging technology portfolios to enable manufacturing of WL-CSP, Flip Chip, TSV, LED and MEMS devices with fine-pitched and cost effective micro-bump, Cu-pillar, RDL, and lift-off processes

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KLA Corporation is a leading supplier of wafer processing, process control and yield management solutions for the semiconductor and related nanoelectronics industries. KLA's products and services are used by bare

wafer, IC, reticle and other manufacturers of materials and equipment around the world, from research and development to final volume manufacturing. Products and services include etch and deposition processes, inline unpatterned and patterned wafer defect inspection, review and classification; reticle defect inspection and metrology; packaging inspection and die sort; critical dimension (CD) metrology; pattern overlay metrology; film thickness, surface topography and composition measurements; measurement of in-chamber process conditions; wafer shape and stress metrology; computational lithography tools; and, overall yield and fab-wide data management and analytics.

Booth 115
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LB Semicon Inc. is a company that provides Bumping, Probe Test, Back-end and WLCSP Services for DDI, CIS, PMIC, etc of electronic devices such as TVs, monitors, mobile phones.

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Quality and Support you can count on. LINTEC's semiconductor manufacturing related products include a wide array of lines. Our Adwill product consists of high-functioning adhesive tapes such as Non UV and UV dicing tape, wafer surface protective tape for BG process, backside laminate tape and die attach specialty films. Additionally, LINTEC is the industry leader in providing Wafer Mounting Systems and UV Irradiation Systems.

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We put our expertise at the service of the automotive, electronic, industrial, semiconductor, medical, and military markets, offering a comprehensive portfolio of leading-edge PGM Powder and Flake materials to meet the most stringent quality requirements. Leveraging our core competencies in precious metals, particle formation, particle deformation, surface chemistry, and process technologies, we partner with customers to develop customized products that deliver timely solutions for the most demanding technical applications.

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Micro Materials Inc. (MMI) provides innovative technology for thin wafer, thin substrate/ panel handling, device processing surface protection and yield improvement solutions for fan-out wafer level packaging, compound semiconductor, advanced integrated circuit packaging, photonic packaging, glass substrate processing, MEMS manufacturing, CMOS image sensor back-end processing and flexible electronics fabrication etc.
MMI has a full set of application and service capability in house. Customers can evaluate the equipment, material and all processing aspects one-stop at MMI.KEY COMPETENCIES:
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Micro Systems Technologies (MST) is a leading manufacturer of high-performance electronic components, semiconductor packaging and microelectronics for medical technology, complemented by a wide range of product lifecycle management services.

The group develops and produces high-technology solutions for customers around the world, especially for applications in the fields of Life Sciences and Healthcare, Aerospace & Aviation, Internet-of-Things and Sensor technology, as well as Hi-Rel industrial electronics.

MST companies are DYCONEX AG in Bassersdorf (Switzerland), Micro Systems Engineering GmbH in Berg (Germany), Micro Systems Engineering, Inc. in Lake Oswego (USA), Litronik in Pirna (Germany) and Micro Connect Technologies in Nuremberg (Germany). For more information please visit our virtual showroom: www.showroom.mst.com

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MCL is the industry leading solutions provider for component level hermetic packaging. Services include package, cover and feedthrough design, development through production, including test. Hermetic cover seal with seam weld and seam AuSn with pristine headspace and wide margin compliance for MIL-STD-883 Test Method 1014 Seal; 1012 Lid Seal Void Rejection Criteria; 2009 External Visual; 1009 Salt Atmosphere; 2020 Particle impact noise detection (PIND) and JEDEC JESD9C. MCL is vertically integrated including all process, metrology and testing onsite.

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Micross is the most complete provider of advanced microelectronic services and component, die and wafer solutions. With the broadest authorized access to die & wafer suppliers, and the most comprehensive advanced packaging, assembly, modification and test capabilities, Micross is uniquely positioned to provide unparalleled high-reliability solutions from bare die, to fully packaged devices, to complete program lifecycle sustainment. For more than 40 years, Micross has been a trusted source for the aerospace, defense, space, medical and industrial markets.

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Mini-Systems, Inc. (MSI) is a world class leader in the manufacture of high-reliability passive components and hermetic packages. For over 54 years MSI has been delivering superior quality products for Military, Aerospace, Communications, Medical and Industrial applications. MSI manufactured products consist of precision: Thin/Thick film Chip

Resistors/Networks, QPL Resistors to MIL-PRF-55342, MOS Chip Capacitors, Chip Attenuators, Full Line of RoHS Compliant Products, QPL Jumpers to MIL-PRF-32159/ Mounting Pads, Glass-to-metal seal packages, and Custom Design Packages. Resistors values from 0.1 Ohm to 100GOhm and operating frequencies up to 40 GHz. Absolute tolerances starting at 0.005% and TCRs as low as ±2ppm/°C. Sizes start at 0101. The hermetic packages meet or exceed package evaluation requirements per MI-PRF-38534, Table C-VI. Hermeticity of the packages is less than 10-10 atm cc/sec per MIL-STD-883, method 1014, condition A4. MSI is ISO-9001 certified. Compliance includes RoHS, REACH, and DFAR. Standard deliveries start in just 2 WEEKS!

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us.mitsuichemicals.com/service/product/icros_tape.html
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"ICROS™ Tape" is brand of tape designed for the semiconductor and electronic components manufacturing process flow, such as backgrinding (BG), dicing, molding, debonding, sawing, reflow, metal lift off, protection for etching, CMOS image sensor handling, protection for back-metalizing, and etc. ICROS™ Tape has been the world's top protective tape used in semiconductor wafer BG for decades. Today, we now offer tapes used for many other processes (in semiconductor and electronic components manufacturing flow.). ICROS™ Tape is continuously evolving to keep up with the latest and future technologies in the semiconductor process, such as TSV wafer BG and dicing, fan-out WLP, PLP and many other processes. We optimize the entire production processes of our protective tapes from concept to raw material design to final inspection to meet the strict requirements of the semiconductor market. Everything takes place within a state-of-the-art clean room production facility with strict quality controls in place every step of the way. The result is ICROS™ Tape, for many applications, ultraclean tape with superior TTV (total thickness variation).

Booth 613
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About MRSI Systems

MRSI Systems (Mycronic Group) is the leading manufacturer of fully automated, high-speed, high-precision and flexible eutectic and epoxy die bonding systems. We offer solutions for research and development, low-to-medium volume production, and high-volume manufacturing of photonic devices such as lasers, detectors, modulators, AOCs, WDM/ EML TO-Cans, Optical transceivers, LiDAR, VR/AR, sensors, and optical imaging products. With 30+ years of industry experience and our worldwide local technical support team, we provide the most effective systems and assembly solutions for all packaging levels including chip-on-wafer (CoW), chip-on-carrier (CoC), PCB, and gold-box packaging. For more information visit

Mycronic is a Swedish high-tech company engaged in the development, manufacture and marketing of production equipment with high precision and flexibility requirements for the electronics industry. Mycronic's headquarters are located in Täby, north of Stockholm and the Group has subsidiaries in China, France, Germany, Japan, the Netherlands, Singapore, South Korea, United Kingdom and the United States. Mycronic is listed on Nasdaq Stockholm.

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Nagase ChemteX is a leading company for semiconductor encapsulant of epoxy resin, especially Liquid Molding Compound (LMC) and Sheet encapsulant for FOWLP, 2.5D, 3D, SiP, and several electric components. We also focus on conductive materials, negative photoresist, and optical adhesive for semiconductor, circuit assembly, photovoltaic, printer head, camera module, optical device, and photonics assembly product lines. Nagase ChemteX and Nagase Group companies create continual improvements guiding its customers into the future.

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NAMICS is a global technology leader of advanced materials for semiconductor devices and packages, passive components, and solar cells with over 75 years of experience and expertise. Headquartered in Niigata, Japan, NAMICS serves its worldwide customers with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea, Hong Kong, and China providing unmatched worldwide support.

Stop by our booth #405 to learn about NAMICS diverse product line of materials such as our packaging and board level underfills, liquid molding compounds, glob top encapsulants, pressure-less sintering technology for die attach, adhesives for sensor and camera modules and latest generation of stretchable printed materials for interconnects, heating, and bonding on flexible substrates.

We build more than products; we build relationships, and NAMICS sets the gold standard for customer service by offering customizing products, world class customer support to provide a solution for your personal application.

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nanosystec offers high-precision micro assembly stations. Joining methods include selective soldering with laser or hotbar, epoxy gluing and UV curing as well as laser welding. With up to 6 degrees of freedom and long-travel linear motor axes with encoders for position readout in the submicron range, the stations comply with complex geometries.

Selective laser soldering is used for applications where other methods fail. A laser heats an area without impacting the surrounding.

Hot bar heating processes multiple solder joints in one effort and serves as an alternative or addition to laser soldering. A strong current flows through the bar and the heat is transferred to the solder joints.

In the laser welding stations, fiber lasers or Lamp-pumped Nd:YAG lasers with multiple outputs serve for low shift spot and seam welding.

Automated machine vision utilizes the images from the process optics and external cameras for motion control purposes, such as seam

tracking and the recognition of difficult shapes. Device-specific machine vision algorithms reduce the processing time to a minimum.

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nepes is a leading-edge provider of Wafer Level Packaging, providing full turnkey assembly solutions that includes Test and Die Processing Services (DPS). Since 2001, nepes has been providing OSAT services in partnership with Fabless and IDM customers worldwide. Nepes is also the first 600mm x 600mm Fan-Out PLP OSAT in the world in high volume production since September 2021.

With IATF16949, ISO 14001, OHSAS 18001 and AEO certified facilities in South Korea, China and Philippines, nepes provides an extensive range of packaging options such as, WLCSP, FOWLP/PLP, SiP, PoP as well as 2.5D/ 3D modules without conventional substrates. nepes strengthened its Fan-Out packaging portfolio by licensing M-Series™ and developing the Fan-Out based 3D-IC and CiB(Chip-in-Board) platform technology.

The trend of package technology is gradually evolving toward smaller form factors while satisfying better thermal management, electrical performance, reliability and higher integration while being cost effective. nepes is well positioned to support leading semiconductor companies, foundries and electronics IDMs with their advanced packaging requirements.

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Nikon Metrology offers the broadest range of metrology solutions for applications ranging from miniature electronics to the largest aircrafts. Nikon Metrology's innovative measuring and precision instruments contribute to a high performance design-through-manufacturing process that allows manufacturers to deliver premium quality products in a shorter time.

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nScrypt designs and manufactures high-precision industrial Microdispensing and Direct Digital Manufacturing equipment with unmatched accuracy and flexibility. nScrypt has award-winning technologies and is thrived to provide complete solutions for various applications in electronics & packaging, 3D printing, life science and textile industries via cutting edge multi-materials, multi-processes and Factory in a Tool approach. nScrypt's headquarters is based in Orlando, Florida.

Advanced technology has the ability to connect two people miles apart, to mobilize people and enable them to do business in their offices, homes and cars, to protect our homes and our country, to diagnose and treat sickness, to entertain and teach. Simply put, advanced technology provides opportunities that were nonexistent a hundred, fifty, or even just five years ago. At nScrypt, we appreciate our position at the forefront of high-tech innovation, while at the same time we recognize God's hand in the development of technology. We respect life at all levels and seek to promote technology for the betterment of humankind.

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Onto Innovation is a leader in process control with leading-edge technologies that include: Unpatterned wafer quality; 3D metrology spanning chip features from nanometer scale transistors to large die interconnects; macro defect inspection of wafers and packages; elemental layer composition; overlay metrology; factory analytics; and lithography for advanced semiconductor packaging.

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Pac Tech - Packaging Technologies GmbH (group member of NAGASE & CO. Ltd.) is headquartered in Germany with wholly owned subsidiaries: PacTech USA Inc. in Silicon Valley, USA, and PacTech ASIA Sdn. Bhd. in Penang, Malaysia. PacTech is comprised of three business units: EQUIPMENT MANUFACTURING: Manual & Automatic ENIG & ENEPIG plating tools, Laser solder jetting equipment, Wafer-level solder ball transfer systems, Laser assisted flip-chip bonders. SUBCONTRACT SERVICES: Flip Chip and Wafer Level Package Bumping Services including ENIG or ENEPIG for UBM (solder bumping) or OPM (wirebond). Other services include Electroplating, Laser Solder Jetting, Solder Rework & Solder Reballing, Wafer Level Solder Balling, Re-passivation, RDL, Backmetal, Wafer Thinning, Wafer Dicing, Tape & Reel, AOI, X-Ray, SEM, FIB. CHEMISTRY: Pre-Treatment and process chemistry for electroless plating.

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Partnering to Go Beyond - Panasonic Electronic Materials is a premier global supplier of leading-edge electronic materials including semiconductor encapsulation materials, IC substrates, high-speed circuit board laminates and advanced display films.

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At QP Technologies (formerly Quik-Pak), we offer a range of services to meet your packaging and assembly requirements. These include wafer preparation (backgrinding, dicing, die sort and inspection); IC assembly for a variety of package types and materials, as well as die attach, wire bonding, flip chip, encapsulation and marking; advanced assembly for new and complex packaging structures; laser micromachining; and design and engineering. In addition, we support design, fabrication, and assembly of PCB's for MCM and SiP applications. Our PCB supply chain is solid and supports FR-4 to ABF, fine line/spacing. We have added wire bond equipment to support heavy Al wire and challenging RF requirements. We are ITAR Registered and service the Mil-Aero market as well as commercial. Pls visit us at Booth #508 to discuss your needs and how we can apply our expertise and resources to support your project.

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QualiTau
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QualiTau offers a variety of reliability test equipment for characterization and development of new materials used in the manufacturing of Integrated Circuits, as well as process monitoring and process qualification. The MIRA, Infinity, ACE, and Multi-Probe reliability test systems perform tests for Hot Carrier Injection (HC), Dielectric Breakdown (TDDB), and electromigration(EM) of interconnects, TSV, Solder Bump (8 amperes max) at test temperatures of up to 450°C. QualiTau's Test Lab service is ideal for both fabless companies and foundries seeking: Reliable, independent evaluation and analysis. "Virtual" capacity during times of under-capacity. Cost-effective means of performing tests on an irregular or infrequent basis. A productive and beneficial way to "test drive" the equipment before committing to a purchase.

Booth 104
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Realizing the need for a service and a relationship based representative company, Bill Winn founded Sales & Service Incorporated in 1989. Located in the heart of Orange County, SSI has emerged as a proven and dedicated manufacturer's representative for over 20 years. Our mission is to provide an exceptional level of service that is mutually beneficial to our customers and principals. We at SSI understand the importance of communication and strive to provide a smooth channel of correspondence that ensures a productive and supportive link to facilitate the flow of business. At SSI, all our efforts are focused towards building strong, long-term relationships between ourselves, the customer, and the principal. SSI's product line includes industry leading consumable products and equipment for the packaging, testing, and reliability areas of the Semiconductor, Aerospace, and Hybrid industries. SSI takes great care in selecting our partners and are proud to offer products from these companies.

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SavanSys is the industry's leading electronics packaging cost modeling company, in business since 1995. Our cost modeling methods are widely recognized as the most accurate on the market. SavanSys cost models include the following technologies: PCB fabrication and assembly, wire bonding, flip chip substrate and assembly, fan-in WLP, fan-out WLP, panel-level fan-out, interposer-based packaging, and more.

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Pioneering – responsibly – together
These attributes characterize SCHOTT as a manufacturer of high-tech materials based on specialty glass. Founder Otto Schott is considered its inventor and became the pioneer of an entire industry.Always opening up new markets and applications with a pioneering spirit and passion – this is what has driven the #glasslovers at SCHOTT for more than 130 years. Represented in 34 countries, the company is a highly skilled partner for high-tech industries: Healthcare, Home Appliances & Living, Consumer Electronics, Semiconductors & Datacom, Optics, Industry & Energy, Automotive, Astronomy & Aerospace. In the fiscal year 2021, its 17,300 employees generated sales of 2.5 billion euros. SCHOTT AG is owned by the Carl Zeiss Foundation, one of the oldest foundations in Germany. It uses the Group's dividends to promote science. As a foundation company, SCHOTT has anchored responsibility for employees, society and the environment deeply in its DNA. The goal is to become a climate-neutral company by 2030.

Booth 411
SEKISUI Chemical Co., Ltd.
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sekisui.co.jp/electronics/en/catalog
Contact: Takaichi Hiratsuka
takaichi.hiratsuka@sekisui.com
Sekisui is a Japanese chemical manufacturing company with a history of 75 years. For the semiconductor market, we manufacture and sell interlayer insulating films used for high-spec semiconductors, TIM with unique and high heat dissipation using carbon fiber, and semiconductor process materials with temporary fixing and easy peeling.

Booth 410
Semiconductor Equipment Corp.
5154 Goldman Ave.
Moorpark, CA 93021
+1 805-529-2293
semicorp.com
Contact: Lester Salvatierra
sales@semicorp.com
Semiconductor Equipment Corporation is recognized as the leading manufacturer and distributor of standard and customized die handling equipment and semiconductor dicing tape. Since 1975, SEC has installed thousands of production units worldwide for work in packaging and assembly operations including edge emitting lasers, flip chip, surface mount and hi-reliability devices such as ball grid arrays, quad flat packs and multichip modules.

Highly trained and experienced technical and support staff provide on-going training, service and support at the corporate facility and installation and on-site training at the customer's facility.

Semiconductor Equipment Corporation is headquartered in a specially developed modern plant located in Moorpark, California, U.S.A. north of Los Angeles. Its staff includes a team of professionals with acknowledged records of outstanding performance in the semiconductor/electronic components industry. Many of SEC's engineers, including its officers, possess industry experience dating back to the early days of assembly, handling and test.

Booth 208
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senju.com
Contact: Derek Daily
ddaily@senju.com
Senju Metal Industry Co (SMIC) of Japan is a world class provider of solder materials and related equipment. Senju Comtek Corp, our Americas affiliate, manufactures solder paste here in the US. Please ask us about Senju's latest technologies in solder spheres, attach fluxes and other semiconductor or electronics assembly related products.

Booth 103
SETNA
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set-na.com
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jfriot@set-na.com

SETNA is the exclusive North American distributor of SET device bonding equipment. SET is globally renowned for the unsurpassed accuracy and the flexibility of its flip-chip bonders.

Ranging from manual loading to fully automated version, the SET bonders adapt to all main bonding techniques: fluxless reflow, thermo-compression, adhesive joining compression, thermosonic…

SET offers a comprehensive product portfolio of flip-chip bonders for fast growing markets and serving clients through a global network of representatives and in-depth customer training.

Additionally, SETNA is also the North American distributor for Ontos Equipment Systems (OES) Atmospheric Plasma equipment. OES' Atmospheric Plasma Systems are used for surface preparation. It provides a simple, effective, clean surface modification method which does not require the throughput- robbing vacuum chamber associated with traditional plasma systems.

Booth 209
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shenmao.com
Contact: Sisi Wang
sales@shenmao.us

Founded in 1973, SHENMAO Technology Inc. offers total solutions of solder materials to customers by meeting and exceeding their quality and reliability requirements with products and service satisfaction accumulated over four decades of research and development experience.

SHENMAO works closely with customers to develop new application nanotechnology products for the electronics and other industries. From production to shipment, strictly controlling each step, SHENMAO uses only ultra-pure virgin raw materials to produce high-quality products. Through continuous improvement, cost reduction, swift sales and service, SHENMAO works hard to help customers remain competitive, creating a win-win situation. SHENMAO Technology Inc., as the third largest Solder Materials provider, produces and markets SMT Solder Paste, Semiconductor Packaging Solder Spheres, Wafer Bumping Solder Paste, Dipping Flux, Wave Solder Bar, Solder Wire, Flux and Solder Preforms distributed from 10 worldwide locations, as the strategic manufacturing partner of leading OSATs, the 2017 top 12 of 13 largest EMS Companies and OEMs. SHENMAO Technology Inc. strives to offer the best quality without compromising cost and time-to-market while providing maximum value to all customers, always through superior customer service and technical support. Customer satisfaction and sustainable high quality are always SHENMAO's priority.

Booth 706
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Shibuya supplies innovative back-end semiconductor manufacturing tools such as sub-micron accuracy flip chip bonders, micro solder ball placers and high-speed turret handlers. Shibuya is now offering newly-developed "Fluxless LATCB" solution to the advanced HPC (High Performance Computing) packaging industry. LATCB stands for Laser Assisted Thermo-Compression Bonding and Shibuya combines this cutting edge technology with its own fluxless bonding technology. Fluxless LATCB's 3600mm^2 large die bonding capability with its super high-speed laser heating and simple and flexible fluxless bonding technology can bring industry leading ultra-high solder interconnection density with highest productivity and no corrosive residues.

Booth 510
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furukin@shikoku.co.jp

SHIKOKU CHEMICALS Co. has developed new crosslinking agents featuring an isocyanuric acid skeleton for PPE resins and special BMI resins using our organic synthesis technology.

These crosslinking agents can improve various properties of PPE resins and special BMI resins, such as Dk/Df, adhesiveness, heat resistance, and flame retardance, which have been issues for PPE resins and special BMI resins.

Booth 604
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Founded in 1984 as a subsidiary of the General Electric Company, Shin-Etsu MicroSi is a driving force in both the semiconductor and microelectronics industries worldwide. By infusing science and chemistry with innovation and collaboration, we create leading-edge solutions that turn possibilities into realities– while providing the proven quality and time-tested dependability on which our customers rely.

From computers to cell phones, 5G, automobiles, coatings, and more, our products are used by companies throughout the world to make the integrated circuits and semiconductor devices that power everyday living.

Our dedication to research is incomparable. Our devotion to improvement and discovery, unwavering. Our commitment to quality and dependability is unparalleled. And our customer satisfaction, second to none.

Booth 712
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shinko.com
Contact: Justin Goodman
justin.goodman@shinko.com

SHINKO Electric Industries Co., LTD., is a leading manufacturer of products used in the assembly of IC's such as Organic Substrates, Etched and Stamped Leadframes, TO Packages and Integrated Heat Spreaders. We manufacture a full line of Organic Substrate structures including coreless options offering enhanced electrical performance and package miniaturization. SHINKO also provides subcontract IC assembly services with an emphasis on packaging solutions such as PoP, SiP as well as advanced technologies such as Molded Core Embedded Package (MCeP®) and Module assembly and test. Our headquarters and primary production plants are in the greater Nagano, Japan area. In addition to our production facilities we also provide the ultimate in service and solutions for customers with Sales and Engineering support Worldwide. See us to learn more about our latest product offerings for fine pitch interconnection, miniaturization and high density mounting for 3D assembly.

Booth 806
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Contact: Sylvia Lewis
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Sigray, Inc. is a San Francisco Bay Area company founded with the aim to accelerate progress in packaging & integration by providing fast, flexible, and high-resolution x-ray technologies to labs & fabs. Our breakthrough Apex XCT provides fast sub-micron 3D x-ray capabilities on wafers, PCBs, and dies, while our flagship AttoMap MicroXRF provides sub-ppm elemental detection and non-destructive layer thickness measurements to the sub-angstrom regime. These systems represent a major step-change from existing laboratory x-ray systems and their breakthrough performance are uniquely enabled by Sigray's patented innovations in x-ray source, optics, and detector technologies. Since its founding in 2013, Sigray's products have already been adopted by prominent scientific leaders in Asia, America, and Europe. The company holds over 40 patents on x-ray component and system technologies.

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Silitronics provides IC Assembly, Package Design and Substrate Fabrication service to support Silicon Photonics, LiDAR, AR/VR, SiP, Chiplets and Heterogeneous Integration. Silitronics is located in San Jose, CA, the heart of the Silicon Valley, with Assembly, R&D, and Cleanroom 1K and 10K facilities over 10,000 sq.ft. with Fully Automated Flip Chip, Wire Bond, Optical Assembly and Active Alignment with +/-0.5um.

Booth 303
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SkyWater (NASDAQ: SKYT) is a U.S.-owned semiconductor manufacturer and a DOD-accredited Trusted supplier. SkyWater's Technology as a Service model streamlines the path to production for customers with development services, volume production and heterogeneous integration solutions in its world-class U.S. facilities. This pioneering model enables innovators to co-create the next wave of technology with diverse categories including mixed-signal CMOS, read-out ICs, rad-hard, power discretes, MEMS, superconducting ICs, photonics, carbon nanotubes and interposers. SkyWater serves growing markets including aerospace & defense, automotive, biomedical, cloud & computing, consumer, industrial and IoT.

Booth 206
Smart High Tech
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sht-tek.com
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WE KEEP IT COOL
With our flexible and soft graphene-based interface materials for all sorts of thermal management applications. And this is only the beginning. Our products have the potential of changing every industry- depending on heat dissipation- for the better. Using less energy, saving time, money and our environment.

Booth 113
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sono-tek.com
Contact: Bennett Bruntil
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Sono-Tek's ultrasonic coating technology is currently being used at the package level for EMI shielding coatings. Tested and approved using market-available EMI materials, our unique non-clogging spray coating systems, with a low temperature heat cure, offer a more cost effective and faster alternative to costly sputtering equipment. Our FlexiCoat EMI system was designed to run continuously in production at a higher throughput than sputtering, at roughly 1/10th the cost.

Sono-Tek's ultrasonic coating technology also is well known for thin, repeatable, and low waste coatings. Other applications include: Photoresist deposition, polyimide, flux dispensing for flip chip applications, and nano suspensions (CNT, graphene, nano-wires, etc).

Booth 502
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suss.com
Contact: Daniel Barry
dbarry@suss.com
SUSS MicroTec is a leading supplier of equipment and process solutions for microstructuring in the semiconductor industry and related markets.
Our portfolio covers a comprehensive range of products and solutions for backend lithography, wafer bonding and photomask processing, complemented by micro-optical components. In close cooperation with research institutes and industry partners SUSS MicroTec contributes to the advancement of next-generation technologies such as 3D Integration and Imprint Lithography as well as key processes for Wafer-Level Packaging, MEMS and LED manufacturing. With its global infrastructure for applications and service, SUSS MicroTec supports more than 8,000 installed systems worldwide.

Booth 515
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taiyo-hd.co.jp/en
Contact: Yuya Suzuki
yuyas@taiyo-america.com
High performance and high reliability materials showcased by TAIYO INK are beneficial for advanced IC packaging, as well as conventional packaging applications. Consequently, Taiyo Ink has more than 90% market share of solder resist products for the IC packaging industry. One of the latest materials from TAIYO is a photo-imageable dry film with 10 μm resolution, PVI-3 HR100S, which has low curing temperature of 180°C, and can be applied as high-density RDL dielectrics for advanced packaging substrates & PLP/WLP. Taiyo also develops a variety of new dielectric materials with additional performance, such as magnetic, optical, or electrical performances. We look forward to talking with you at our booth.

Booth 804
TATSUTA Electric Wire & Cable Co. Ltd.
6-5-1 Kunimidai Kizugawa City
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+81 774-66-5551
tatsuta.com
Contact: Mike Sakaguchi
m-sakaguchi@tatsuta.com
TATSUTA Electric Wire & Cable Co., Ltd is a leading manufacturer of innovative advanced paste for high performance electronics. By using our electrically and thermally conductive paste , higher density interconnect (HDI), longer product life and outstanding reliability are achievable. With our knowledge of metal-resin formulation technology, our materials support development cycles/process time shorten and lower process temperature as well, which enables lower carbon emission and eco-friendly process. For more information, please visit our booth #804 and you will see

our latest developments related with carbon neutrality, low temperature curing, thermal management and EMI shielding.

Booth 205
TDK Corporation
475 Half Day Rd., Ste. 300
Lincolnshire, IL 60069
+1 972-409-4519
product.tdk.com/en/products/fa/index.html
Contact: Sara Lambeth
sara.lambeth@tdk.com
TDK is a leader in factory automation systems. Our products include TDK precision AFM 15 Thermosonic and AFM 15 Thermal Compression flip chip die bonders. TDK flip chip die bonders use a micro scrub process to lower heat required for die attach process. TDK micro scrub process eliminates flux and supports 5~10 mm line width and 3mm spacing.

Additionally, TDK load ports feature high-performance that meet your needs for particle-free operation, high throughput and high durability of continual motion. In addition to the TAS300 load port, we also offer the TAS300 J1 and the TAS450.

Booth 312
TechSearch International, Inc.
4801 Spicewood Springs Rd, Ste. 150 / Austin, Texas 78759
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techsearchinc.com
Contact: Jan Vardaman
jan@techsearchinc.com
TechSearch International, Inc. has a 34-year history of market and technology trend analysis focused on semiconductor packaging, materials, and assembly. The company is able to provide market and technical analysis identifying key inflection points in the semiconductor packaging area. TechSearch International is known worldwide for its timely, relevant, and accurate analysis. Research topics include WLP, FO-WLP, Flip Chip, CSPs, BGAs, 3DICs, IC package substrates and materials, System-in-Package (SiP) and Heterogeneous Integration, ADAS and automotive electronics. TechSearch International professionals have an extensive network of more than 21,000 contacts in North America, Asia, and Europe. Follow us on twitter @Jan_TechSearch.

Booth 100
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+1 480-794-1926
teikoku-taping.com/en
Contact: Robert Garrett
robert.garrett@teikoku-taping.com
Teikoku Taping System, a wholly owned subsidiary of Nippon Kayaku, specializes in the design, development and manufacture of semiconductor equipment used for taping, de-taping and handling of wafers and panel/substrates. TTS is the leader in Dry Film Resist lamination, as well as the handling of thin wafers for back grind tape lamination, UV irradiation, removal and mounting to dicing tape on film frame. Customer support for demos, process development, field service are all based in our offices in Phoenix, AZ.

Booth 814
TECNISCO, Ltd.
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tecnisco.co.jp/en
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TECNISCO is in the microfabrication business for metal products used in heat sinks and glass products used in MEMS packages. TECNISCO is also a manufacturer of silver diamond composite, a material with high thermal conductivity(>900W/mK).

Booth 109
TOKYO OHKA KOGYO AMERICA, INC.
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+1 940-293-3089
tokamerica.com
Contact: Satoshi Teranishi
satoshi.teranishi@tokamerica.com
TOK's state-of-the-art micro processing technology produces groundbreaking and innovative products. We have pioneered the development of polymer-containing functional photoresists based on photolithography technologies that are essential for the formation of semiconductor circuits.

Along with advancement in the micro-fabrication of an electronic circuit, our sophisticated technologies provide solutions to enhance the functionality of semiconductors, such as miniaturization, high-integration, multi-functionality, and high-speed. We offer various new materials necessary for many device manufacturers, including advanced immersion photoresists enabling the formation of several tens nanometer scale features.

Booth 406/408
Toray International America Inc
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San Mateo, CA 94402
+1 650-524-2735
electronics.toray/en
Contact: Koichi Maruyama
koichi.maruyama.p6@mail.toray
Toray Industries, Inc. has devoted itself to developing new fields and materials as a basic materials manufacturer. We have supplied both film-type and coating-type materials in the semiconductor market over decades.

Film type: "FALDA" is a photo-definable adhesive film for build-up substrates and packages with cavity structures.

Coating type: "Photoneece" is a photo-definable polyimide coating for the front-end buffer and back-end re-distribution layers for WLP and TSV.

Toray's unique polyimide and film processing technologies provide excellent reliability and performance, already proven in the market. We also offer newly developed materials specifically designed to be implemented for the low dielectric loss 5G/mmWave applications (B-stage and liquid products available).

Toray Engineering Co., Ltd. provides state-of-the-art Flip Chip Bonding Equipment for semiconductor packaging with alignment accuracy from +/-0.5um.

Wafer Inspection Equipment with high speed, and substrate manufacturing equipment such as high-precision coating systems are lined-up.

Booth 509
TOWA USA Corporation
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towajapan.co.jp/en
Contact: Terence Koh
tkoh@towa-usa.com
TOWA is a leading company in the semiconductor molding equipment market. We offer equipment using our high quality / flow free compression molding method and our proven transfer molding method. We also manufacture ultra-precision molds that have been highly acclaimed by customers. Together with our molding equipment, our singulation system was developed from both aspects of the dicer and product handler to provide the optimal method of singulation for each product type. The result is high quality cutting whilst improving customers' productivity with high throughput.

Booth 305
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royceinstruments.com
Contact: Matt Wilson
mwilson@royceinstruments.com
V-TEK, Inc. through its Royce Instruments brand is your preeminent supplier for Bond Testing and Die Sorting equipment. Our high-precision equipment covers the spectrum of bond test and die sorting requirements. We are dedicated to developing and supplying dynamic solutions for our customers. The Royce 600 Series Bond Test Instruments bring unparalleled networking capability and scalability to the market. With three bond testers, Royce offers an instrument solution to meet the evolving needs of institutions worldwide. Royce Die Sorters (DE35-ST and AP+) offer semi- and fully automatic die sorting solutions for die as small as 200um square or 50um thick. Our automated sorter, the AP+, has the capability to handle diverse input and output mediums (carrier tape, waffle pack, Gel-Pak, JEDEC tray, film frame and more) while maintaining input to output traceability at the die level. Automated top, bottom, and/or facet inspection options are available on the AP+ to allow visual defects to be detected during the die sort process.

Booth 203
XYZTEC, Inc
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xyztec.com
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Tom.Haley@xyztec.com
XYZTEC, Inc. manufactures bond testers. Bond Testers are typically used to validate a process. Although bond testing is a relatively mature inspection technique, most manufacturers have made very few changes to their product over the years. XYZTEC has revolutionized this technology by eliminating cartridge changeovers, automating non-destructive and destructive bond test and by significantly increasing measurement accuracy. They have made significant advancements in camera technology and ergonomics that truly enhance the bond test process.

Booth 612
Yamaha Robotics Holding Co., Ltd
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+81-3-5937-6401
yamaha-robotics.com/en
Contact: Doug Day
d_day@shinkawausa.com
The Company was established in July 2019 as a holding company, with Yamaha Motor Co., Ltd. as the parent company and three operating subsidiaries, SHINKAWA LTD, APIC YAMADA CORP., and PFA Corp.

We aim to provide a total solution that exceeds our customers' expectations as the "Turn-Key Provider" in the field of semiconductor back-end processing by integrating the technologies of the above three companies.

For leading edge packaging technology, Shinkawa provides innovative solutions with high-accuracy and ultra-high throughput flip chip bonders for TCB and C2/C4 processes, also wire and die bonders for advanced packaging. Apic Yamada is the No.1 supplier of wafer level molding systems.

Booth 702
YES (Yield Engineering Systems, Inc.)
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+1 510-954-6889
yieldengineering.com
Contact: Joseph Simas
sales@yieldengineering.com
Yield Engineering Systems, Inc. (YES) is a preferred provider of material modification and surface enhancement solutions at the nanoscale. The company's renowned vacuum curing technology has been selected by the world's largest IDMs, foundries and OSATs for its ability to improve process speed, reliability, and cost-effectiveness. YES thermal processing equipment addresses process temperature requirements from 100°C to 1200°C using convective, radiative, infrared and UV sources, for wafer and panel substrates. YES's coating systems enable life science applications in genetic testing and the identification of infectious agents like SARS-CoV-2, as well as providing key process technology for optics, AR/VR and nanoimprint lithography. And the YES-SPEC product line offers industry-leading wet process performance, including electroless and electrolytic plating.

Booth 304
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Contact: Jeff Perkins
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Yole Développement provides market research, technology analysis, strategy consulting, targeted media, and financial advisory services.

With a strong focus on emerging applications using silicon and/or micro manufacturing since 1998, Yole Développement has expanded to include more than 80 collaborators worldwide covering Photonics – Lighting – Imaging – Sensing & Actuating – Display – RF Devices & Technologies – Compound Semiconductors & Emerging Materials – Power Electronics – Batteries & Energy Management – Semiconductor Packaging and Substrates – Semiconductor Manufacturing – Memory – Computing and Software.

The market research, technology and strategy consulting company Yole Développement, along with its partners System Plus Consulting and PISEO – all part of the Yole Group of Companies-, support industrial companies, investors and R&D organizations worldwide to follow technology trends to grow their business and help them understand the 6 specific markets.

Booth 414
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zymet.com
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Zymet manufactures Adhesives & Encapsulants and has been serving the electronics industry for over 30 years. Products include reworkable underfills and edgebond adhesives for high reliability and harsh environment applications. Other products include ultra-low stress adhesives, electrically conductive adhesives, thermally conductive adhesives, and non-conductive pastes.

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FIRST CALL FOR PAPERS

IEEE 73rd Electronic Components and Technology Conference • www.ectc.net
To be held May 30 - June 2, 2023 at The JW Marriott Orlando Grande Lakes, Orlando, Florida, USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Electronics Packaging Society (EPS) of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to the topics listed below for each technical program committee. Authors are encouraged to review the sessions of the previous ECTC programs to determine which committees to select for their abstracts.

Applied Reliability

Reliability of 2D, 2.5D, Si-bridge, 3D, chiplets, WLCSP, FOWLP, FOPLP & heterogeneous integration, interconnect reliability in micro-bump, micro-pillar, Cu-pillar, TSV, RDL, stacked-die, hybrid-bond, flip chip & wire bonded packages, novel reliability test methods, life models, FA techniques & materials characterization, component and board level reliability in computing, HPC, mobile, networking, automotive, power electronics, harsh/hi-temp environments, IoT, sensors, AI, autonomous vehicles, medical, wearable electronics, LEDs, displays and memory.

Assembly and Manufacturing Technology

Assembly and manufacturing challenges for new markets; Die bonding methods and processes; Wafer level process/materials technologies; Die and package singulation manufacturing; New & next generation substrates; Smart factory/manufacturing; Assembly related test/yield hardware development; Integrating advanced thermal solutions in manufacturing: Design/performance, integrating solutions, thermal materials, low stress/high thermal; Process advancements/yield enhancements; Cost of inspection, sampling, metrology, new processes for fine RDL, small via fabrication, transfer/compression/injection mold; Heterogeneous integration and process: chiplets, 3D stacking, bridge technology, large body, warpage management; Shielding/protection technologies and manufacturing and market requirements.

Emerging Technologies

Emerging, novel and unique packaging and material technologies for: soft and intelligent packaging, flexible/stretchable hybrid electronics, implantable biosensors and bioelectronics, extreme harsh environment, green/bio-resorbable packaging, nanomanufacturing, paper sensors/electronics pop-up/origami, MEMS and NEMS, Close-To-Motor high-voltage power electronics, packaging for wide band gap devices, anti-tamper, cryptography, additive manufacturing, packaging for quantum computing and electro-optical integration, recyclable and sustainable electronics packaging, packaging for quantum computing and electro-optical integration, recyclable and sustainable electronics packaging, AI, ML and computer vision for packaging, point-of-care diagnostic packaging, packaging for quantum computing/sensing/communication, and space hardened packaging technologies.

RF, High-Speed Components & Systems

5G/6G, IoT, cloud computing, autonomous vehicles, AI/machine learning; Antennas, sensors, power transfer, EM shielding, wired/wireless communications, RF to THz; Electrical and multi-physics modeling, simulation and characterization of interconnects, components, modules, and heterogeneous integration; Signal/power integrity, chip/package/board co-design.

Interconnections

Interconnection Technology and Processing: Fan-out, panel-level, chiplets, SiP, flip-chip, 2.5D/3D, Si/glass/organic interposers, TSV, micro-bump, Cu pillar, wirebonds, high I/O thermo-compression/hybrid bonding, fine-pitch/multi-layer RDL, printable interconnects, flexible substrates, photonic interconnects, quantum interconnects; Interconnection Material;Characterization and Reliability: Conductive/non-conductive adhesives, low temperature solder, underfill, molding compounds, thermal interface materials, thermal/mechanical/electrical tests and reliability; Interconnection physical co-design and architectures for emerging applications: HPC, mobile, 5G, IoT, power and rugged electronics, medical and health, automotive, aerospace, flexible hybrid electronics, micro-LED display.

Materials & Processing

Wafer/panel level packaging materials and process advancements; Advanced materials and processes for FOWLP, FOPLP, 2.5D/3D, SiP, TSV, chiplets, and advanced packaging architectures; Harsh environment resistant materials; Packaging substrates; Flexible, stretchable, & wearable electronics; Temporary wafer bond/debond materials/processes; Permanent adhesives; TCB and hybrid bonding; Adhesives, dielectrics and underfills; Emerging electronic materials & processes; Conductive adhesives; Novel solder metallurgies; Molding compounds; Thermal interface materials; Advanced wire bonding.

Packaging Technologies (formerly Advanced Packaging):

Architectures, methods, and applications for 2.5 & 3D, TSV & interposer; Advanced flip-chip, SiP, CSP, PoP, MEMS, sensors & IoT; Automotive & power electronics; Bio, medical, flexible & wearable packaging; embedded & advanced substrates; Fan-out, wafer & panel level processes; heterogeneous integration.

Photonics

PhotonicComponents Packaging for computing, communications, data processing, mobility, healthcare, green energy photonics, agriculture, horticulture, food, environmental, climate and atmosphere monitoring, space, automobile, underwater, industrial, defense, process integration, co-packaging (Photonics – Electronics - Laser Integration), free space optics, microscopy and advanced spectroscopy, 3D printing of micro-optical components for packaging, assembly and manufacturing; Packaging for the quantum photonics world; Packaging of new photonics materials; Optical characterization of packaging components; Equipment and tools for photonics packaging.

Thermal/Mechanical Simulation & Characterization

Thermal/mechanical simulation and characterization at component, board, and system levels for all packaging technologies; Reliability related modeling including fracture mechanics, fatigue, electromigration, warpage, delamination, moisture, drop, shock and vibration, and modeling for harsh environments (thermal, chemical, etc.); Material constitutive relations; chip-package interaction for heterogeneous integration, wafer fabrication and package assembly process related modeling; novel modeling techniques including multi-scale physics, co-design approaches; quantum computing; Measurement methodologies, characterization and correlations, model order reduction, sensitivity analysis, optimization, statistical analysis; pplication of artificial intelligence on modeling, characterization, and digital twin.

Interactive Presentations

Abstracts may be submitted related to any of the nine major program committee topics listed above. Interactive presentations of technical papers are highly encouraged at ECTC. They allow for significant interaction between the presenter and attendees, which is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to submit an abstract of no more than 750 words and add one figure/table that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net.

If you have any questions, contact:
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Abstracts must be received by October 10, 2022. All abstracts must be submitted electronically at www.ectc.net. You must include the affiliation, mailing address, business telephone number, and email address of all co-authors with your submission. The authors will be notified about the abstract selection outcome by December 16, 2022.

Professional Development Courses

Proposals are solicited from individuals interested in teaching educational, four-hour long Professional Development Courses (PDCs) on topics described above. From the proposals received, 16 PDCs will be selected for offering at the 73rd ECTC on Tuesday, May 30, 2023.

Each selected course will be given a minimum honorarium of $1,500. In addition, instructors of the selected courses will be offered the speaker discount rate for the conference. Attendees of the PDCs will be offered Continuing Education Units (CEUs). These CEUs are recognized by employers as a formal measure of participation and attendance in "noncredit" self-study courses, tutorials, symposia, and workshops.

Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the ECTC website at www.ectc.net by October 23, 2022. Authors will be notified of course acceptance with instructions by December 16, 2022. If you have any questions, contact:

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Meeting Space Capacity Chart: Marina Tower

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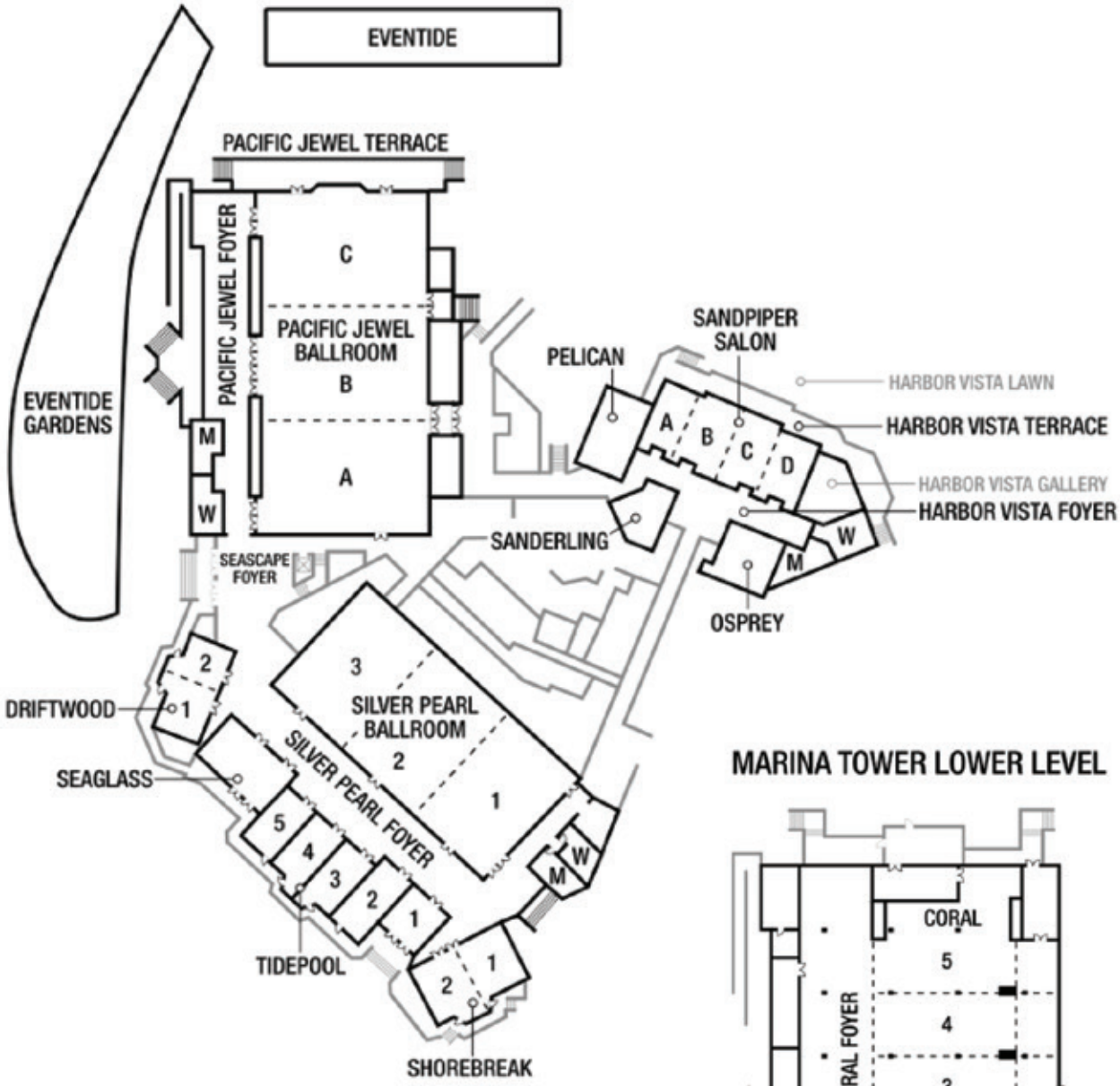

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JW Marriott Orlando, Grande Lakes, Orlando, FL
May 30 – June 2, 2023

Make your Florida escape an extraordinary one at JW Marriott Orlando, Grande Lakes. The luxury resort at Grande Lakes is located on a lush, 500-acre property and is ideal for exploring the Orlando area -- or for relaxing poolside in the Florida sunshine. Choose from modern rooms offering luxury bedding, marble bathrooms, 65-inch HDTVs and sweeping views of this Florida resort. Unwind at the outdoor pool complex, including a lazy river, or try our challenging 18-hole golf course designed by PGA great Greg Norman. Select from enticing in-house dining options, from luxury Italian fare at Primo to a farm-to-table menu and craft beer at Whisper Creek Farm. Take advantage of our hotel's excellent location to explore gorgeous Central Florida. Reserve your stay at JW Marriott Orlando, Grande Lakes for an exceptional resort experience that you and the family will remember.

With more than 500 acres to explore, there's always something to do at Grande Lakes Orlando. Whatever your idea of a fun-filled or relaxing getaway is our resort has it all. Championship golf, luxury spa services, outdoor activities like kayaking and mountain biking, and unique experiences like falconry and eco tours are just a few of the things you can do at Grande Lakes.

CONFERENCE AT A GLANCE

REGISTRATION

Monday, May 30, 2022
3:00 p.m. - 5:00 p.m.

Tuesday, May 31, 2022
6:45 a.m. - 8:15 a.m.
(AM PD Courses & Special Session Only)

Tuesday, May 31, 2022
8:15 a.m. - 5:00 p.m.
(All conference attendees)

Wednesday, June 1, 2022
6:45 a.m. - 4:00 p.m.

Thursday, June 2, 2022
7:30 a.m. - 4:00 p.m.

Friday, June 3, 2022
7:30 a.m. - 12:00 p.m.

ECTC Registration Desk located in the Seascape Foyer.

TECHNOLOGY CORNER EXHIBITS

Wednesday
9:00 a.m. - 12:00 p.m.
1:30 p.m. - 6:30 p.m.
Reception - 5:30 p.m. - 6:30 p.m.

Thursday
9:00 a.m. - 12:00 p.m.
1:30 p.m. - 4:00 p.m.
Eventide

TUESDAY – FRIDAY

Speaker Preparation Room
Tuesday - Friday
7:00 a.m. – 5:00 p.m.
Tidepool 1

TUESDAY ONLY

PDC Instructors and Proctors Briefing & Breakfast
7:00 a.m. – 7:45 a.m.
Pacific Jewel B

Professional Development Courses (PDCs)
8:00 a.m. – Noon
1:30 p.m. - 5:30 p.m.
See page 8 for locations

IEEE EPS Heterogeneous Integration Roadmap (HIR) Workshop
8:00 a.m. – 4:30 p.m.
Pacific Jewel C

Special Sessions:
ECTC Special Session 1
8:00 a.m. – 10:00 a.m.
Pacific Jewel A

Special Session 2 (HIR)
10:15 a.m. – 12:00 Noon
Pacific Jewel C

Special Session 3
1:30 p.m. – 3:00 p.m.
Pacific Jewel A

Special Session 4
3:30 p.m. – 5:00 p.m.
Pacific Jewel A

Refreshment Breaks
10:00 a.m. – 10:20 a.m.
3:00 p.m. – 3:20 p.m.
Silver Pearl Foyer, Coral Foyer, Pacific Jewel A

Lunch for PDCs
12:00 Noon
Pacific Jewel B

Technology Corner SetUp
1:00 p.m. – 5:00 p.m.
Eventide

ECTC Student Reception
5:00 p.m. – 6:00 p.m.
Pacific Jewel Foyer

General Chair's Speakers Reception
6:00 p.m. – 7:00 p.m.
Pacific Jewel B
By invitation only

Young Professionals Panel and Reception
7:00 p.m. – 7:45 p.m.
Silver Pearl 3

EPS President's Panel
7:45 p.m. – 9:15 p.m.
Silver Pearl 1 & 2

WEDNESDAY – FRIDAY

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Pacific Jewel A

Sessions
8:00 a.m. – 11:40 a.m. or
1:30 p.m. – 5:30 p.m.
see pages 10 -21 for specifics

Sessions 1, 7, 13, 19, 25, 31
Silver Pearl 1

Sessions 2, 8, 14, 20, 26, 32
Silver Pearl 2

Sessions 3, 9, 15, 21, 27, 33
Silver Pearl 3

Sessions 4, 10, 16, 22, 28, 34
Coral 1 & 2

Sessions 5, 11, 17, 23, 29, 35
Coral 3 & 4

Sessions 6, 12, 18, 24, 30, 36
Coral 5

Interactive Presentations
9:00 a.m. - 11:00 a.m. or
2:00 p.m. - 4:00 p.m.
(8:30 a.m. - 10:30 a.m. on Friday)
see pages 22 - 25 for specifics

Sessions 37 - 41
Coral Foyer

Lunch
12 Noon – 1:15 p.m.
Pacific Jewel Ballroom

Refreshment Breaks
9:15 a.m. – 10:00 a.m.
2:45 p.m. – 3:30 p.m.
Wednesday & Thursday
Eventide
Friday
Silver Pearl Foyer & Coral Foyer

WEDNESDAY ONLY

Diversity and Career Growth Panel & Reception
6:30 p.m. – 7:30 p.m.
Silver Pearl 3

ECTC Plenary Session
7:30 p.m. – 9:00 p.m.
Silver Pearl 1 & 2

THURSDAY ONLY

72nd ECTC Gala Reception
6:30 p.m. – 7:30 p.m.
Eventide Gardens
(Backup Location: Pacific Jewel ABC)

IEEE EPS Seminar
8:00 p.m. – 9:30 p.m.
Silver Pearl 1 & 2

MARK YOUR CALENDARS NOW!

ECTC

The 2023 IEEE 73rd Electronic Components and Technology Conference

May 30 - June 2, 2023

JW Marriott Orlando, Grande Lakes
Orlando, Florida, USA

For more information, visit:

www.ectc.net

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