INTRODUCTION FROM THE IEEE 73RD ECTC PROGRAM CHAIR FLORIAN HERRAULT

The 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC) at the JW Marriott Orlando, Grande Lakes, Orlando, Florida • May 30 - June 2, 2023

On behalf of the Program and Executive Committee, it is my pleasure to invite you to IEEE’s 73rd Electronic Components and Technology Conference (ECTC), which will be held at JW Marriott Orlando, Grande Lakes, Orlando, Florida from May 30 to June 2, 2023. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor and electronics manufacturing companies, design houses, foundry and OSAT service providers, substrate makers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1500 people attended ECTC 2022 in what was our first in-person event in three years.

At the 73rd ECTC, around 350+ technical papers are scheduled to be presented in 36 oral sessions and 5 interactive presentation sessions, including one interactive presentation session exclusively featuring papers by student authors. The oral sessions will feature selected papers on key topics such as wafer-level and fan-out packaging, 2.5D, 3D and heterogeneous integration, interposers, chiplets, advanced substrates, assembly, materials and thermal modeling, reliability, packaging for harsh conditions, packaging for quantum and AI applications, interconnections, packaging for high speed and high bandwidth, photonics, flexible and printed electronics. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over twenty countries are expected to present their work at the 73rd ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry, such as additive manufacturing, heterogeneous integration, flexible and wearable electronics.

ECTC will also feature seven special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, five special sessions, 90 minutes each, are scheduled.

On Tuesday morning, May 30th at 8:30 a.m. Tanja Braun, Fraunhofer IZM, and Przemyslaw Gromala, Robert Bosch GmbH, will chair the session on Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment, followed by Thomas Gregorich, Infineon, and Chaoqi Zhang, Qualcomm chairing a special session at 10:30 a.m. on Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications. On Tuesday afternoon at 1:30 p.m. Stéphane Bernabé, CEA-Leti, and Hiren Thacker, Cisco, will host a special session on the topic of Photonic Integrated Circuit Packaging, followed by a special session on the CHIPS Act, organized by Nancy Stoffel, GE Research, Jan Vardaman, TechSearch International, and William Chen, ASE. As in previous years, HIR will host a parallel track throughout the day.

On Tuesday afternoon, the Young Professionals reception will be organized by Yan Liu, Medtronic. On Tuesday evening, Takashi Hisada, IBM, and Yasumitsu Orii, Rapidus, will co-chair the IEEE EPS Seminar on High-Density Substrates.

New this year, the following days (Wednesday-Friday) will kick off with a single-room special session from 8:00 a.m. to 9:15 a.m., which will then be followed by our traditional technical sessions with six parallel tracks.

On Wednesday May 31st at 8 a.m., join us early to receive our Welcome message from our General Chair Ibrahim Guven, followed by a captivating presentation and Q&A session by our Keynote speaker Prof. Michael Manfra from Purdue University; the title of the Keynote is “Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging”. At the end of the day, at 6:30 p.m., a special session, co-hosted by ECTC and ITherm, will discuss workforce development for semiconductors and packaging. The panel will be chaired by Kim Yess, Brewer Science, Nancy Stoffel, GE Research, and Christina Amon, University of Toronto. This reception/panel event should not be missed.

On Thursday June 1st at 8 a.m., we will have the pleasure of starting the day with our ECTC Plenary Session, featuring an extensive panel of experts focused on next-generation millimeter-wave packaging. The 75-min session will be chaired by Kevin Gu, Metawave Corporation, and Ivan Ndjip, Fraunhofer IZM / Brandenburg Technical University.

Kitty Pearsall, Boss Precision, Inc., IEEE EPS President, and David McCann, Lyte, will chair the EPS President’s ECTC panel session on Friday morning at 8 a.m. The session will focus on how photonics can enable the bandwidth densities with lower energy per bit in emerging SIP.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and the ECTC Exhibition. Co-located with the IEEE ITherm Conference, the 73rd ECTC will offer 16 CEU-approved PDCs, organized by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 30th and are taught by distinguished experts in their respective fields. The ECTC Exhibition will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging, and services fields. More than one hundred exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. I invite you to make your plans now to join us for the 73rd ECTC and to be a part of all the exciting technical and professional opportunities. I also want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 73rd ECTC a success. I look forward to meeting you at the JW Marriott Orlando, Grande Lakes, Orlando, Florida, May 30 – June 2, 2023.

Florian Herrault
73rd ECTC Program Chair
Email: floherrault@gmail.com

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Advance Registration

Online registration is available at www.ectc.net. For more information on registration rates, terms, and conditions, see page 32.

Register early … save US$100 or more! All registrations received after May 5, 2023, will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk in the Mediterranean Foyer.

On-Site Registration Schedule

Registration will be held in the Mediterranean Foyer on the Lobby Level.

Monday, May 29, 2023   3:00 p.m. – 6:00 p.m.
Tuesday, May 30, 2023   6:45 a.m. – 7:45 p.m.*
*6:45 a.m. – 8:00 a.m.: Morning PDCs & morning ECTC Special Sessions only
Wednesday, May 31, 2023  6:45 a.m. – 4:00 p.m.
Thursday, June 1, 2023  7:30 a.m. – 4:00 p.m.
Friday, June 2, 2023  7:30 a.m. – 12:00 Noon

The above schedule for Tuesday will be rigorously enforced to prevent students from being late for their courses.

General Information

Conference organizers reserve the right to cancel or change the program without prior notice. The JW Marriott Orlando Grande Lakes, as well as the ECTC, are both smoke free environments.

ITherm 2023

ITherm is co-located with ECTC! All ITherm sessions and exhibits will take place in the same location, the JW Marriott Orlando Grande Lakes, as ECTC.

Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual’s belongings is the individual’s responsibility.

ECTC Sponsors

With more than 70 years of history and experience behind us, ECTC is recognized as the premier semiconductor packaging conference and offers an unparalleled opportunity to build relationships with more than 1,500 individuals and organizations committed to driving innovation in semiconductor packaging.

We have a limited number of sponsorship opportunities in a variety of packages to help get your message out to attendees. These include Platinum, Gold, Silver, Program, and several other sponsorship options that can be customized to your company’s interest. If you would like to enhance your presence at ECTC and increase your impact with a sponsorship, please take a look at our sponsorship brochure on the website www.ectc.net under “Sponsors.”

To sign-up for sponsorship or to get more details, please contact Wolfgang Sauter at wsauter2@gmail.com or +1-802-922-3083.

Hotel Accommodations

Rooms for ECTC attendees have been reserved at the JW Marriott Orlando Grande Lakes. The special conference rate for a single/double occupancy room is:

US $233.00 per night

This price includes single or double occupancy in one room.

Please note these rooms are on a first come, first served basis. If the conference rate is no longer available, attendees will be offered the next best price available.

Please make sure to book a room as soon as possible as the conference room rate is sure to sell out! Rooms can be booked through our website at www.ectc.net/location. If you need to cancel a reservation, please do so by 6 p.m. Eastern time, AT LEAST 5 days prior to arrival for a full refund. Check-in time: 4 p.m. & check-out time: 11 a.m.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2023 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2023 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. ECTC’s only authorized site for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that you personally have used in the past to book travel. Please be advised, there are scam artists out there and if it’s too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: lrenzi@renziandco.com.

Transportation Services

There is no complimentary transportation to and from the hotel and airport. All attendees must make their own transportation arrangements to the hotel upon arriving at the airport.

Note about Hotel Rooms

Attendees should note that only reputable sites should be used to book a hotel room for the 2023 ECTC. Be advised that you may receive emails about booking a hotel room for ECTC 2023 from 3rd party companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. ECTC’s only authorized site for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that you personally have used in the past to book travel. Please be advised, there are scam artists out there and if it’s too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: lrenzi@renziandco.com.
2023 ECTC Special Session on Advanced Packaging for Harsh Environments

**Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment – Current Status and Opportunities**

*Tuesday, May 30, 2023, 8:30 a.m. – 10:00 a.m.*

**Chairs:** Tanja Braun, Fraunhofer IZM, and Przemyslaw Gromala, Robert Bosch GmbH

Electronic components and systems are among the main contributors to the most innovative ideas and products of today’s world. In the automotive industry, electronic components and systems are accountable for more than 80% of all innovation.

When we think about highly automated and autonomous systems, advanced packaging is a must. Nowadays, most advanced electronic components such as CPUs or GPUs are being introduced into harsh environments such as automotive, avionics or space applications almost at the same time as in consumer products. Therefore, in our special session, we would like to discuss with the top experts from industry and academia what the current status and opportunities are for advanced packaging for harsh environments.

Azeem Sarwar, General Motors
Giuseppe Barone, Robert Bosch GmbH
Vikas Gupta, ASE US, Inc.
Dae-Woo Kim, Samsung
Shin-Puu Jeng, TSMC
Ram Trichur, Henkel
Kauchi Zhang, TU Delft
Vanessa Smet, Georgia Tech

2023 ECTC Special Session on Hybrid Bonding

**Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications**

*Tuesday, May 30, 2023, 10:30 a.m. – 12:00 p.m.*

**Chairs:** Thomas Gregorich, Infinera, and Chaoqi Zhang, Qualcomm

This Special Session will explore the applications, requirements, and challenges of Copper Hybrid Bonds (CHB) for Chip-to-Wafer (C2W) applications. Wafer-to-wafer CHB has been in HVM for many years and continues to expand.

While C2W is in production, challenges remain. This panel will discuss challenges and solutions for the expanded use of C2W Copper Hybrid Bonds.

The session will include a moderator and speakers, each with a 10-minute presentation followed by a joint 20-minute Q&A session:

- Jan Vardaman, TechSearch International
- Eric Beyne, IMEC
- Ming Zhang, Synopsys
- Raja Swaminathan, AMD
- Thomas Uhrmann, EVG
- Chris Scanlan, Besi

2023 ECTC Special Session on Photonics Packaging

**Photonic Integrated Circuit Packaging: Challenges, Pathfinding, and Technology Adoption**

*Tuesday, May 30, 2023, 1:30 p.m. – 3:00 p.m.*

**Chairs:** Stéphane Bernabé, CEA-Leti, and Hiren Thacker, Cisco

Photonic integrated circuit (PIC) technologies are proliferating into many application spaces; from hyperscale data center, high-performance computing to sensing including LiDAR. Packaging remains the greatest challenge to high-throughput manufacturing at high yield. The main challenges are: Optical coupling, TSV integration for chiplet or photonic interposer approaches, laser integration, thermal management, manufacturability, and reliability. While there are currently only limited standardization activities (OIF, COBO, IEC SC86C/WG4) addressing these challenges, the need for innovative solutions is growing to merge semiconductor 3D packaging technologies and photonics. This session will feature leading practitioners who are actively driving PIC packaging innovation and technology adoption toward high-volume reality.

Peter De Dobbeleer, Cisco
Thierry Moulier, CEA-Leti
Hesham Taha, Teramount
Alexander Janta-Polczynski, IBM
Peter O’Brien, Tyndall Institute
Colin Dankwardt, Ficontec Service GmbH

2023 ECTC Special Session on CHIPS Act

**Advanced Packaging Manufacturing in North America: Building the Ecosystem**

*Tuesday, May 30, 2023, 3:30 p.m. – 5:00 p.m.*

**Chairs:** Nancy Stoffel, GE Research, Jan Vardaman, TechSearch International, and William Chen, ASE

North America has companies that excel in design for electronics systems, device, and advanced packaging. However less than 2% of the packaging occurs in the US. This session will discuss the ambitious goals being set through the CHIPS ACT to bring Advanced Packaging to North America. We will review the targets and developing plans of the US government, funded through the CHIPS Act. The panelists will overview major initiatives launched in R&D and Manufacturing. We will also discuss the challenges to meeting the goals.

Ajit Dubey, Google
Frank Gayle, NIST, Office of Advanced Manufacturing
Subramanian Iyer, University of California Los Angeles
Carl McCants, DARPA
Dick Otte, Promex Industries, Inc.
Hem P. Takiar, Micron Technology Inc.
These sessions are open to all conference attendees.
2023 ECTC Plenary Session on
mm-Wave Phased Array Packaging

Millimeter-Wave Phased Array Front-End Integration and Packaging for Next-Generation Communication and Radar Systems

Thursday, June 1, 2023, 8:00 a.m. – 9:15 a.m.
Chairs: Kevin Gu, Metawave Corporation, and Ivan Ndip, Fraunhofer IZM / Brandenburg University of Technology

Phased arrays are critical components in next generation communication and radar sensing systems. Current state-of-the-art and rapidly emerging research and development on millimeter-wave front-end implementations have created tremendous opportunities for innovation in packaging technologies. In this plenary panel session, we invite six leading domain experts to present their pioneering works in this area. The panel discussion will be focused on major challenges and the latest advancements in packaging and integration technologies for designing and implementing phased array front-end modules, including different substrates, interconnects, antennas, hetero-integration of silicon and III-V chips, co-design with RFICs, thermal management, system demos/prototypes, and so on.

Jonathan Hacker, Teledyne Scientific
Augusto Gutierrez-Aitken, Northrop Grumman Space Systems
Hasan Sharifi, HRL Laboratories, LLC
Madhavan Swaminathan, Pennsylvania State University
Shahriar Shahramian, Nokia Bell Labs
Alberto Valdes-Garcia, IBM Research

2023 IEEE EPS President Panel on Photonics

How Can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP

Friday, June 2, 2023, 8:00 a.m. – 9:15 a.m.
Chairs: Kitty Pearsall, Boss Precision, Inc., and David McCann, Lyte

This panel will discuss the tools, technologies, and approaches that will enable the industry to enhance the bandwidth density of interconnections in SIP enabled by photonics. To be adopted, such capabilities must be provided with energy per bit that meets the roadmaps and standards targets for the interconnection protocols within the package and on the chip.

Amr S. Helmy, University of Toronto
Ritesh Jain, Lightmatter
Ajey Jacob, University of Southern California
Stefano Oggioni, ATS

Luncheons

This year ECTC will be offering a daily luncheon (Tuesday – Friday) for all attendees registered for the full conference. Lunch tickets, found in your registration badge holder, must be presented for entrance into the lunch room. Lost lunch tickets will cost $75 to replace. Please come and enjoy time with other attendees and colleagues in the industry! Lunch times will vary, see below for specific details for each day.

Tuesday: 12:00 Noon – 1:15 p.m.
Wednesday: 12:45 p.m. – 2:00 p.m.
Thursday: 12:45 p.m. – 2:00 p.m. – Sponsored by: The IEEE Electronics Packaging Society
Friday: 12:45 p.m. – 2:00 p.m. – Don’t miss out on this lunch! We will be raffling off a number of prizes including a hotel stay, free conference registrations, and many other industry gadgets!

General Chair’s Speakers Reception

Tuesday, May 30, 2023 • 6:00 p.m. – 7:00 p.m.
(by invitation only)

ECTC Student Reception

Tuesday, May 30, 2023 • 5:00 p.m. – 6:00 p.m.
Hosted by Texas Instruments, Inc.

Students, have you ever wondered what career opportunities exist at Texas Instruments and in the industry and how you could use your technical skills and innovative talent? If so, you are invited to attend the ECTC Student Reception, where you will have the opportunity to talk to industry professionals about what helped them to be successful in their first job search and reach their current positions. You will have the chance to enjoy good food and network with industry leaders and achievers. Don’t miss the opportunity to interact with people that you might not have the chance to meet otherwise! You will also be able to submit your resumes to our sponsoring partners.

Exhibitor Reception

Wednesday, May 31, 2023 • 5:30 p.m. – 6:30 p.m.
Open to all conference attendees.

73rd ECTC Gala Reception

Thursday, June 1, 2023 • 6:30 p.m.
All badged attendees and their guests are invited to attend a reception hosted by Gala Reception sponsors.
1. HIGH RELIABILITY OF LEAD-FREE SOLDER JOINTS – MATERIALS CONSIDERATIONS

Course Leader: Ning-Cheng Lee – ShinePure Hi-Tech

Course Description:
This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions, and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in detail. The selection of novel alloys with reduced fragility will be presented. Crucial parameters for high reliability solder alloy for automotive industry will be presented. Electromigration, and tin whisker growth will also be discussed. The emphasis of this course is placed on the understanding of how the numerous factors contribute to the failure modes, and how the selection of proper solder alloys and surface finishes for achieving high reliability are key.

Course Outline:
1. Mainstream Lead-free Soldering Practices
2. Surface Finishes Issues
3. Mechanical Properties
4. Intermetallic Compounds
5. Failure modes
6. Reliability – Thermal cycle
7. Reliability - Fragility
8. Reliability – Rigidity and Ductility
9. Reliability – Composite Solder Enable Hierarchy Assembly & Shock Resistance
10. Reliability – Tin Whiskers

Who Should Attend:
Directors, managers, design engineers, process engineers, and reliability engineers who care about achieving high reliability lead-free solder joints and would like to know how to achieve it should take this course.

2. WAFFER-LEVEL CHIP-SCALE PACKAGING (WCSP) FUNDAMENTALS

Course Leader: Patrick Thompson – Texas Instruments, Inc.

Course Description:
This course will provide an overview of the Wafer-Level-Chip Scale Packaging (WLCSP) technology. The market drivers, end applications, benefits, and challenges facing industry-wide adoption will be discussed. Typical WLCSP configurations (bump-on-pad, bump-on-polymer, fan-in, and fan-out) will be discussed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Extensions to higher pin count packages and other arenas such as RF sensors and MEMS will be reviewed. Future trends covered will include enhanced lead-free solder balls, large die size, wafer level underfill, thin and ultra-thin WLCSP, RDL (redistribution layer), stacked WLCSP, MCM in “reconstituted wafers,” embedded components, and applications to large format (panel) processing. Since the technology marks the convergence of fabrication, assembly, and test, discussion will address questions on the industrial supply chain such as: Does it fit best with front-end or back-end processing? Are the current standards for design rules, outline, reliability, and equipment applicable? What are the challenges for memory? And what about other complex devices such as ASICs and microprocessors?

Course Outline:
1. WLCSP Definition
2. Trends, Categories, Examples, Challenges, Supply Chain
3. Historical Overview, Package Highlights, Assembly Flow
4. Processing and Reliability, Flex, Temperature Cycling, Drop, Electromigration
5. Fan-Out Technologies
6. Embedded Technologies
7. Conclusions

Who Should Attend:
The course will be useful to the following groups of engineers: newcomers to the field who would like to obtain a general overview of WLCSP; R&D practitioners who would like to learn new methods for solving CSP problems; and those considering WLCSP as a potential alternative for their packaging solutions.

3. FUNDAMENTALS OF RF DESIGN AND FABRICATION PROCESSES OF FAN-OUT WAFER/LEVEL AND ADVANCED RF PACKAGES

Course Leaders: Ivan Ndip – Fraunhofer IZM/Budapest Technical University and Markus Wöhrmann – Fraunhofer IZM

Course Description:
Due to their myriad of advantages in system-integration, fan-out wafer/panel-level packages (FO WLPs/PLPs) and other advanced RF packages (e.g., glass interposers and chip-embedding packages) will play a key role in the development of emerging electronic systems. The fabrication processes and RF performance of these packages will contribute significantly to the cost and performance of the entire system. The objective of this course is to provide and illustrate the fundamentals of the fabrication processes and RF design of these advanced packages for emerging RF/wireless applications.

An overview of distinct types of wafer-level packages, fan-out technologies, glass interposers and chip-embedding packages will first be given. This will be followed by a presentation of new fan-out-packaging and interposer-based concepts for emerging and future applications (e.g, 5G mmWave, mmWave radar sensors, 6G) as well as a thorough discussion of the materials and fabrication processes of FO-WLPs/PLPs, multilayered RDLs, glass interposers and chip embedding packages. The basics of efficient RF design and measurement of the fundamental building blocks of these advanced packages will be given for frequencies up to the millimeter-wave range. Finally, examples of these advanced packages designed and fabricated at Fraunhofer IZM will be discussed.

Course Outline:
1. Overview: Different Types of Wafer-level Packages, Fan-out Technologies, and Advanced RF Packages
2. Requirements of 5G Packaging and New Fan-out Packaging Concepts for 5G mmWave Applications
3. Materials and Fabrication Processes: FO-WLPs/PLPs, Multi-layered RDLs, Glass Interposers and Chip Embedding Packages
5. Examples of Advanced Packages Designed and Fabricated at Fraunhofer IZM

Who Should Attend:
Engineers, scientists, researchers, designers, managers, and graduate students interested in the fundamentals of electronic packaging as well as those involved in the process of electrical design, layout, processing, fabrication and/or system-integration of electronic packages for emerging applications (e.g., 5G, 6G, mmwave radar sensors) should attend.
4. ELIMINATING FAILURE MECHANISMS IN ADVANCED PACKAGES

Course Leader: Darvin Edwards – Edwards Enterprises

Course Description:
Reliability failure mechanisms that plague semiconductor packages will be explored with an emphasis on new package technologies such as heterogeneous package integration as well as an overview of reliability issues in high volume packages. Topics studied include reliability of TSV-chip interactions, Direct Cu Bond (DCB) and micro bump mechanical reliability, high density interconnect (HDI) reliability, electromigration performance, stress induced interlevel dielectric (ILD) damage under bumps and Cu pillars, saw induced ILD damage, solder joint reliability, system level drop reliability, the impact of aging on reliability performance and many more. Primary failure analysis techniques will be described. For each failure mode, the resultant failure mechanisms and failure analysis techniques required to verify the mechanisms will be summarized. This solutions-focused course concentrates on key process parameters, design techniques and material selections that can eliminate failures and improve reliability, ensuring participants can design-in reliability and design-out failures for quicker time to market. Characterization and implementation of test structures and design guidelines that enable reliable first pass products will be described and encouraged. A methodology for early detection of chip/package interaction (CPI) reliability risks will be described.

Course Outline:
1. Introduction to Package Reliability
2. Failure Modes vs. Failure Mechanisms
3. Failure Analysis Techniques
4. FC-BGA Package Failure Mechanisms
5. WLCSP Package Failure Mechanisms
7. TSV Failure Mechanisms
8. High Density Interconnection Reliability
9. Direct Bond Interconnect Reliability and Testing
10. Materials, Modeling, Design Rules, and Reliability
11. Summary

Who Should Attend:
This class is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial. Beginning engineers and those skilled in the art will benefit from the holistic failure mechanism descriptions and the provided proven solutions.

5. RELIABILITY ENGINEERING TESTING METHODOLOGY AND STATISTICAL KNOWLEDGE FOR QUALIFICATIONS OF CONSUMER AND AUTOMOTIVE ELECTRONIC COMPONENTS

Course Leader: Fen Chen – Cruise LLC (a GM company)

Course Description:
The consumer electronics industry and today’s fast-growing automotive industry continue to demand ever-higher product hardware reliability. This tutorial will provide an overview of reliability testing methodology and statistical knowledge for qualifications of consumer and automotive electronic components. The reliability testing management includes various Rel testing methods and their application to product development at different phases will be first introduced. Some important statistic/probabilistic concepts including uncertainty, confidence level, and how to minimize/deal with them will be discussed. An effective approach to mitigate low sample size and short test duration will be introduced. Then the tutorial will focus on the physics of failure-based acceleration life models for some common reliability testing failures. A deep dive discussion on the temperature cycling model considering df acceleration, dwell time acceleration, ramp rate acceleration, and Tmin acceleration will be explored. Next, a typical methodology to develop a PoF-based Rel validation testing plan reference to the product field mission profile will be introduced. The mission profiles of conventional vehicles and consumer smartphones will be compared. How to develop a customized mission profile for an autonomous vehicle specifically per its deployment location will be described. Finally, some examples of hardware failure modes with their risk assessments and lifetime modeling will be presented.

Course Outline:
1. Reliability Engineering Product Qualification Methodology (Strategic Planning)
2. Reliability Engineering General Introduction
3. Knowledge-based and Standard-based Rel Qualification Approach
4. DfR, Rel R&R, Various Rel Testing Methods, and Their Applications During Product Development
5. Reliability Engineering Basic Knowledge of Probabilities and Statistics
6. Rel Test Uncertainty and How to Minimize & Deal with Common Rel Engineering Statistical Concepts, Methods, and Uses
7. Reliability Engineering Acceleration Lifetime Modeling Overview (Physics of Failure)
8. Various Life Acceleration Models for Consumer Products and Automotive Components Rel Failures
9. Reliability Test Plan Development Based on Mission Profile Overview (Standards, Knowledge, and Experience)
10. Customized Mission Profile Development
11. GMW3172 Based Rel Validation Plan for Automotive Electronic Components
12. A Company Specific Reliability Validation Plan for Smartphones
13. Failure Modes and Lifetime Prediction Case Studies
14. Thermal-mechanical Interaction Impacts on the Chip Thermal Performance Case Study

Who Should Attend:
Engineers and tech managers already involved in the consumer product and automotive product fields, and those who need a fundamental understanding or a broad overview of the product reliability qualification.

6. RELIABILITY PHYSICS AND FAILURE MECHANISMS IN ELECTRONICS PACKAGING

Course Leader: Xuejun Fan – Lamar University

Course Description:
This course presents an overview of the physics of failures in electronics packaging. The course discusses key fundamental concepts of reliability physics associated with various stress conditions, including thermal degradation, thermo-mechanical stress, dynamic and vibrational loading, moisture, and humidity, as well as electrical current stress. Failure mechanisms studied include chip-package interactions, micro bump reliability, electromigration performance, inter-layer dielectric (ILD) damage under bumps and Cu pillars, solder joint reliability, drop and vibrational damage, interfacial delamination, and the impact of moisture and environmental humidity. Acceleration factor models for different failure mechanisms are introduced. Stress analysis methods using finite element analysis (FEA) with specific applications to packaging are described.

Course Outline:
1. Introduction to Advanced Package Reliability Physics
2. Thermal and Thermo-mechanical Driven Failure Mechanisms
3. Dynamic and Vibrational-driven Damages
4. Moisture and Humidity-induced Failures
5. Electromigration

Who Should Attend:
This course is for all who work with IC packaging, package reliability, package development, package design, and package processing where a working knowledge of package failure mechanisms is beneficial.
7. RELIABLE INTEGRATED THERMAL PACKAGING FOR POWER ELECTRONICS

Course Leader: Patrick McCluskey – University of Maryland

Course Description:
Power electronics are becoming ubiquitous in engineered systems as they replace traditional ways to control the generation, distribution, and use of energy. They are used in products as diverse as home appliances, cell phone towers, aircraft, wind turbines, radar systems, smart grids, and data centers. This widespread incorporation, and the fact that power electronics have become key components of heterogeneous integration, have made it essential that the reliability of power electronics be characterized and enhanced. Furthermore, increased power levels combined with increased packaging density have led to higher heat densities in power electronic systems making thermal management more critical to performance and reliability of power electronics. This course will emphasize approaches to integrated thermal packaging that addresses performance limits and reliability concerns associated with increased power levels and power density. Following a quick review of active heat transfer techniques, along with prognostic health management, this short course will present the latest developments in the materials (e.g., organic, flexible), packaging, assembly, and thermal management of power electronic modules, MEMS, and systems and in the techniques for their reliability assessment.

Course Outline:
1. Motivation for Heterogeneously Integrated Thermal Packaging for Reliable Power Electronic Systems
2. Simulation and Assessment of Active Thermal Management Techniques
3. Application of Thermal Management Techniques to Commercial Power Systems
4. Durability Assessment (Failure Modeling, Simulation, Testing, and Health Monitoring)
5. Reliability and Thermal Packaging of Active Devices and Interconnects
6. Reliability and Thermal Packaging of Switching Modules, including Organic Encapsulants
7. Reliability in Rigid Assembly Packaging
9. Reliability of Additive Manufactured and Embedded Power Electronics

Who Should Attend:
This PDC is aimed at both new and veteran practicing engineers and technical managers who seek to incorporate thermal management into heterogeneously integrated power electronics packaging for use in a wide variety of power and energy generation and distribution applications.

8. INTRODUCTION TO PWB THERMAL ANALYSES

Course Leader: Patrick Loney - Northrop Grumman

Course Description:
Printed Wire Boards (PWBs) are present in almost every piece of electronics. This includes the SIM card in your phone, the backbone in your laptop, and the high-power card assembly in power supplies. Usage and complexity are increasing. Increasing part and power densities on PWBs necessitates increased attention to PWB thermal performance. No two PWBs are identical but the approaches needed to develop thermal models all follow good, sound, thermal engineering basics. In this course, attendees will learn how to categorize cooling techniques for PWBs, predict temperature gradients, and compare part temperature predictions with acceptable limits.

Course Outline:
1. Purpose of the PWB Thermal Analysis
2. Cooling Configurations Covered in this Course
3. Basic Inputs
4. Defining the Component Model
5. Harvesting Data from the Datasheet
6. Modeling the Part on the Board
7. Applying Boundary Conditions
8. The PWB Stacking
9. Determining Run Cases and Configurations
10. Augmenting Heat Transport Capability

Who Should Attend: The class targets the front-line thermal engineer. Since the course material focuses on the process of PWB thermal modeling, all experience levels of engineers and managers will benefit from attending.

9. ADDITIVE FLEXIBLE HYBRID ELECTRONICS – MANUFACTURING AND RELIABILITY

Course Leader: Pradeep Lall – Auburn University

Course Description:
This course will cover manufacturing, design, assembly, and accelerated testing of additively printed flexible hybrid electronics for applications in some emerging areas. Manufacturing processes for additive fabrication of flexible hybrid electronics will be discussed. Flexible hybrid electronics enable opportunities to develop stretchable, bendable, foldable form-factors in electronics applications, previously not possible with rigid electronics technologies. The manufacture of thin electronic architectures requires the integration of thin chips, flexible encapsulation, compliant interconnects, and nano-particle inks for metallization traces. Several additive-printed electronics processes for fabricating and assembling flexible hybrid electronics have become tractable. Pick-and-place of thin-silicon, and compliant interposers through interconnection processes such as reflow require an understanding of the deformation and warpage processes. Modeling operational stresses in flexible electronics requires the material behavior under large deformation and constant exposure to human body temperature, saliva, sweat, ambient temperature, humidity, dust, wear, and abrasion. The failure mechanisms, failure modes, and acceleration factors in flexible electronics under operational loads of stretch, bend, fold, and loads resulting from human body proximity significantly differ from rigid electronics. Several product areas for applying flexible electronics are tractable in the near term, including Internet-of-Things (IoT), medical wearable electronics, textile woven electronics, robotics, communications, asset monitoring, and automotive electronics.

Course Outline:
1. Additive Technologies in Flexible Electronics
2. Aerosol-jet Printing
3. Ink-jet Printing
4. Screen Printing and Gravure Printing
5. Laser-direct Sintering
6. In-mold Labeling
7. Ultra-thin Chips
8. Die-attach Materials for Flexible Semiconductor Packaging
9. Flexible Encapsulation Materials
10. Dielectric Materials for Large-area Flexible Electronics
11. Flexible Substrates
12. Stretchable Inks for Printed Traces
13. Flexible Power Sources

Who Should Attend: The targeted audience includes scientists, engineers and managers considering the use of additively printed flexible electronics or considering moving from rigid electronics to flexible electronics, as well as reliability, product or applications’ engineers who need a deeper understanding of additively printed flexible electronics: the advantages; limitations; and failure mechanisms.

10. FAN-OUT PACKAGING AND CHIPLET HETEROGENEOUS INTEGRATION

Course Leader: John Lau - Unimicron

Course Description:
Fan-out wafer/panel-level packaging has been getting lots of traction since TSMC used their integrated fan-out to package the application processor chipset for the iPhone 7. In this
lecture, the following topics will be presented and discussed. Emphasis is placed on the fundamentals and latest developments of these areas in the past few years. Their future trends will also be explored. Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with varied sizes and functions, and from different fabrication design houses, foundries, wafer sizes, and feature sizes into a system or subsystem on a common package substrate. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented.

Course Outline:
1. Formation of FOWLP. (a) Chip-first (Face-Down), (b) Chip-first (Face-up), and (c) Chip-last Fabrication of Redistribution Layers (RDLs) Formations of FOPLP. (a) Chip-first (Face-down), (b) Chip-first (Face-up), and (c) Chip-last
2. Reliability of FOWLP and FOPLP. (a) Thermal-Cycling and (b) Drop Course - Many Examples of FOWLP and FOPLP
3. Chiplet Design and Heterogeneous Integration (HI) Packaging vs. System-on-chip (SoC) Advantages and Disadvantages of Chiplet Design and HI Packaging - Many Examples of Chiplet Design and HI Packaging
4. Chiplets Lateral Interconnects (Bridges) - Many Examples
5. Chiplet Design and HI Packaging on Organic Substrates (SiP) - Many Examples
6. Chiplet Design and HI Packaging on Silicon Substrates (TSV-Interposers) - Many Examples
7. Chiplet Design and HI Packaging on Fan-Out RDL Substrate - Many Examples
8. Assembly Technologies for Chiplet Design and HI Packaging

Who Should Attend: If you are involved with any aspect of the electronics industry, you should attend this course. The lectures are based on the publications by many distinguished authors and the books (by the lecturer) such as Fan-Out Wafer-Level Packaging (Springer, 2018) and Chiplet Design and Heterogeneous Integration Packaging (Springer, 2023).

11. PHOTONIC TECHNOLOGIES FOR COMMUNICATION, SENSING, AND DISPLAYS
Course Leader: Torsten Wipiejewski – Huawei Technologies

Course Description:
This course will provide an overview on the various photonic technologies that enable optical communication, optical sensing, and modern display applications. These applications are key for the information and communication technology of today and pave the way to the future. High speed optical communication from board level in data centers to long haul transmission requires photonic components with high speed and high reliability. We will discuss the main components such as laser diodes of several types, high speed optical modulators and photodetectors as well as integration schemes such as photonic integrated circuits (PICs) and packaging aspects. Photonic technologies are also widely used as sensors for various applications including health monitoring. One key advantage is the potential for non-invasive measurements that facilitates the usage by end-users without specific medical knowledge. Packaging should provide high accuracy solution at low cost. Displays are the main media nowadays for bringing information to people. They range in size from smart watches to smart phones, laptops and tablets all the way to large screen TVs and video walls. We review current technologies and new developments such as quantum dots and micro-LEDs as well as some features of 3D displays. Micro-LEDs for large size displays require novel assembly technologies to mount chips of only several micrometers in size with extremely high yield at very low cost. The mass transfer of thousands of chips simultaneously is an option to achieve this challenging target.

Course Outline:
1. Fundamental Properties of Photonic Components
2. Light Sources (LEDs, Laser Diodes, Others)
3. Transmitter and Receiver Components in Optical Communication (Lasers, Modulators, Photodetectors, Passive Optical Components, Photonic Integrated Circuits (PICs), Silicon Photonics, Optical Modules), Monolithic and Hybrid Integration, Packaging
4. Optical Sensing Elements and Applications (Spectrometers, Light Sources, Photacoustic Sensors, Frequency Combs)
5. Display Technologies Liquid Crystal Displays (LCD), Organic Light Emitting Diode (OLED) Displays, Quantum Dot Emissive Displays, Micro-LED Arrays and Large Size Displays using Chiplet Mass Transfer and Bonding, 3D Displays
6. Summary and Outlook

Who Should Attend: The course addresses engineers, scientists and students who would like to get a general overview of various photonics technologies used in today’s products and future developments. The aim is to describe which photonic technologies can be used in various applications and what current limitations are and which new technologies are being developed for further improvements or aiming at technology break-throughs.

12. FLIP CHIP TECHNOLOGIES
Course Leaders: Shengmin Wen – HaiSemi and Eric Perfecto – IBM Research

Course Description:
This course will cover the fundamentals of all aspects of flip chip assembly technologies, including various types of wafer bumping technologies, solder joint formation, substrate selection, underfill type and selection, and reliability evaluation. The course is divided into two sections. The first section focuses on the key steps of flip chip assembly technologies and their associated equipment and materials. Plenty of examples are presented to show the versatile flip chip integrations, including single die, monolithic multi-die, multi-level multi-die, as well as multi-form interconnection such as wire bond / flip chip mixed integration. Major flip chip assembly packages are discussed, such as the BGA packages, CSP packages, wafer-level fan-in and fan-out packages, chip-on-chip packages, chip-on-wafer packages, and 2.5D/3D flip chip packages that uses Si or organic interposers, together with actual industrial leading application cases. In-depth discussions include chip package interaction (CPI), package warpage control, yield detractors for flip-chip assembly, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, and Si die floor plan optimization and its consequence on packaging, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their project’s success. The second section dives into the depth of the fundamental aspect of flip chip technology. It will detail the various interconnect technologies used in today’s flip chip assembly, i.e., lead-free solder bumping, highly customized Cu-Pillar bumping, intermetallic and Cu-to-Cu joining. It will discuss the various under-bump metallurgy (UBM) fabrication methods (electroplating, electrolec, plated and sputtering) and solder depositions methods (electroplating, ball drop, IMS, and solder screening). The course will cover the various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, and electromigration.
1. Introduction to Flip Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Substrate Technologies, Underfill, Package Warpage Control, and Yield
5. Flip Chip Reliability Assessment, Failure Modes, Examples, and Modeling
6. Flip Chip Si Package Co-Design and Chip-Package Interaction
8. Bumping Ground Rules
9. Flip Chip Under-bump Metal and Intermetallic
10. Flip Chip Solder Deposition Processes
11. Cu Pillar Technology
12. Flip Chip Solder Selection and Characterization
13. Flip Chip Electromigration
14. Non-Solder Interconnects
15. Review and Package Selection Exercise

Who Should Attend:
The goal of this course is to provide the students with a list of options to apply to their flip chip assembly applications so that a reliable, innovative, better time to market, and more cost-effective solution can be achieved. Students are encouraged to bring topics and technical issues from their past, present, and future job function for group discussions. A group exercise at the end of the class is planned to serve as a capstone project, making sure that the students can walk away with an in-depth understanding of the technology, and are ready to apply and meet their real-world packaging needs.

13. PACKAGING AND HETEROGENEOUS INTEGRATION FOR AUTOMOTIVE ELECTRONICS AND ADVANCED CHARACTERIZATION OF EMCS
Course Leader: Przemyslaw Gromala – Robert Bosch GmbH
Course Description:
Demand for more advanced packaging technologies is growing rapidly in the automotive, avionics and energy industries. Today, electronic components developed for the consumer market are simultaneously used in harsh environments. Advanced packaging and heterogeneous integration are major contributors to the most innovative ideas, new products, and services. These electronic components are composed of many different materials. Stress due to a mismatch in coefficient of thermal expansion (CTE) between adjacent materials is one of the main causes of reliability problems (e.g. warpage, delamination, fatigue, aging). In addition, these materials are subject to aging during long-term use. Numerical simulations are used to accelerate the development process. This course will discuss the details of how a simulation driven design allows for the efficient development of innovative electronic components and systems. You will be able to learn what is needed to select optimal materials, how to perform material characterization and modeling. I will demonstrate how to quantitatively predict the stress state in design element using multi-domain simulations. Finally, I will present the application of AI/ML techniques to create a digital twin of an electronic control module.

Course Outline:
1. Introduction
2. Selection of the Material
3. Curing Shrinkage
4. Coefficient of Thermal Expansion
5. Linear Viscoelastic Properties
6. Modeling of Linear Viscoelastic Behavior
7. Nonlinear Viscoelasticity
8. Fracture Test and Implementation
9. Thermal Aging
10. Digital Twin
11. Summary

Who Should Attend: Engineers and technical managers who are already involved in the material characterization and modelling, numerical modelling, process engineers and PhD students who need fundamental understanding or broad overview.

14. ANALYSIS OF FRACTURE AND DELAMINATION IN MICROELECTRONIC PACKAGES
Course Leader: Andrew Tay - National University of Singapore
Course Description:
The main objective of this course is to provide a fundamental understanding as well as techniques of applying the fracture mechanics methodology to predicting fracture and delamination in microelectronic packages. The mechanism of delamination failure due to thermal stress and moisture will be described and analyzed. Simulation of transient heat transfer and moisture diffusion processes occurring during package qualification will be described. An introduction to the fundamentals of interfacial fracture mechanics will be given together with descriptions of some numerical methods of calculating fracture mechanics parameters. Experiments which verify the methodology for predicting delamination in packages will then be described followed by some interesting case studies.

IMPORTANT NOTICE
Anyone taking PDC courses, please register on-line in advance to prevent door registration delays.

Course Outline:
1. Development of Hygrothermal Stresses in Microelectronics Packages
2. Finite Element Analysis and Stress Singularities in Microelectronic Packages
3. Inadequacy of Maximum Stress Failure Criterion
4. Fundamentals of Fracture Mechanics Methodology
5. Computation of Fracture Mechanics Parameters
6. Measurement of Fracture Toughness
7. Experimental Verification of the Methodology
8. Case Studies on Delamination of Pad-encapsulant Interfaces, Die-attach Layers, and On-chip Interconnect Structures (BEOL)
9. Cohesive Zone Modeling of Delamination and Case Study

Who Should Attend: This course is designed for packaging design engineers who perform reliability analysis of microelectronics and photonics packages.

15. POLYMERS IN WAFER LEVEL PACKAGING
Course Leader: Jeffrey Gotro – InnoCentrix, LLC
Course Description:
The course has been completely updated to include a detailed discussion of the polymers and polymer-related processing for Fan-Out Wafer Level (FOWLP) packaging as well as Fan-Out Panel Level packaging (FOPLP). The course will provide an overview of the important structure-property-process-performance relationships for polymers used in wafer level packaging. The main learning objectives will be:

1) Gain insights on how polymers are used in Fan Out Packaging, specifically mold compounds and polymer redistribution layers (RDL).
2) Understand the key polymer and processes challenges in Fan-Out Wafer-Level Packaging.
3) Learn about polymers and processes used in Fan Out Panel Level Packaging including new materials for mold compounds and a detailed description of the polymers used for RDL in FOPLP.

Course Outline:
1. Overview of Polymers used in Fan-Out Wafer-Level Packaging (FOWLP)
2. Wafer-level Process Flows (Chip-first Versus Chip-last (RDL first))
3. Epoxy Mold Compounds for Fan-Out Packages
4. Photosensitive Polyimides and Polybenzoxazoles for RDL
5. Polymer Reliability Challenges in Fan-out Wafer-level Packaging
14

**AREA ATTRACTIONS**

Make your Florida escape an extraordinary one at JW Marriott Orlando, Grande Lakes. Located on a lush, 500-acre property, our resort is the ideal base for those wishing to explore the Orlando area - or for sunny family vacations. Stretch out in modern rooms offering luxury bedding, marble bathrooms, 65-inch HDTVs and sweeping views of the resort. Unwind at our outdoor pool complex, which includes a lazy river, or try our challenging 18-hole golf course, designed by PGA legend Greg Norman. Select from several enticing in-house dining options, from luxury Italian fare at Primo to a farm-to-table menu and craft beer at Whisper Creek Farm. Take advantage of our resort’s excellent location to explore gorgeous central Florida. JW Marriott Orlando, Grande Lakes provides an exceptional experience that you and your family will never forget.

**16. THERMAL MANAGEMENT OF ELECTRONICS**

*Course Leader: Jaime Sanchez – Intel Corporation*

**Course Description:**
This course provides the fundamentals of heat transfer applied to the design of thermal systems used to cool electronic components with an emphasis in semiconductor packages. We start with the basic theory of heat transfer and demonstrate simple concepts used today to calculate the cooling requirements for an electronic package and the impact of various parameters on the electronic package. This course covers in-depth heat transfer theory and analysis to give the student a comprehensive understanding of the key modes of heat transfer and their applications. Practical topics such as thermal interface materials, heat sink design and advanced cooling techniques are reviewed.

**Course Outline:**
1. Fundamentals of Heat Transfer and Its Application to Electronics Cooling
2. Techniques to Determine Cooling Requirements for a Package and Its Impact
3. Simplification of Heat Transfer Equations to Analyze Cooling Solutions
4. Governing Principles of Cooling Solutions
5. Application of Numerical Methods to Calculate the Performance of Cooling Solutions
6. Introduction to Thermal Interface Materials and Their Applications
7. Techniques to Size Cooling Requirements and Trade-offs
8. Parameters that Impact the Performance of Cooling Solutions
9. Introduction to Experimental Characterization of Cooling Solutions and Instrumentation

**Who Should Attend:** This class is intended for senior undergraduate and graduate students, as well as engineers working in the field of thermal management.

**IMPORTANT NOTICE**

Morning PD Courses 1 through 8 or afternoon PD Courses 9 through 16 run concurrently.

Make sure you indicate which course you plan to attend in the morning and/or in the afternoon. As sessions run concurrently, attendance is only allowed at one session in the morning and one session in the afternoon.

See page 32 for registration information.

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**Wafer Versus Panel Processing; Polymer Challenges and Solutions**

**Pre-applied Underfills and Wafer-level Underfills, Chemistry and Process**

**Who Should Attend:**
Packaging engineers involved in the development, production, and reliability testing of semiconductor packages would benefit from the course. R&D professionals interested in gaining a basic understanding of the structure/property/process/performance relationships in polymers and polymer-based materials used in electronic packaging will also find this course valuable.

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Program Sessions: Wednesday, May 31, 9:30 a.m. -12:35 p.m.

Session 1: Heterogeneous Chiplet Integration

Committee: Packaging Technologies

Session Co-Chairs:
Andrew Kim
Apple, Inc.
Email: hkim34@apple.com

Mike Gallagher
Dupont Electronics and Imaging
Email: michael.gallagher@dupont.com

1. 9:30 AM – Ultra High Density Low Temperature SoICTM With Sub-0.5 µm Bond Pitch

2. 9:50 AM – Process Integration of Photonic Interposer for Chiplet-Based 3D Systems
Damién Saint-Patrice, Stéphane Malhouitre, Myriam Assous, Thierry Pellerin, Remi Velard, Leopold Virot, Edouard Deschaseaux, Maria-Luisa Calvo-Munoz, Karim Hassan, Stéphane Bernabe, Yvain Thonnart, Jean Charbonnier – CEA-Leti

3. 10:10 AM – Aggressive Pitch Scaling (Sub-0.5 µm) of W2W Hybrid Bonding Through Novel Materials and Process Innovations

4. 11:15 AM – Design Space Explore (DSE) for Over-136 Gb/s Bandwidth With LPDDR5X SDRAM Packages on SOC Package in 200 mm²
Heeseok Lee, Jun So Pak, James Jung, Jisoo Hwang – Samsung Electronics Co., Ltd.

5. 11:35 AM – 3D Stacking of Heterogeneous Chiplets on Modified FOWLP Platform With Thru-Silicon Redistribution Layer
Tae Chong Chai, Boon Long Lau, Lim Pei Siang Sharon, David Ho Soon Wee – Institute of Microelectronics A*STAR; Rob Van Kampen, Paul Castillou, lance barron, Mickael Renault, jay ko, Jonathan Hammond – Qorvo, Inc.

Session 2: High-Performance Packaging Materials

Committee: Materials & Processing

Session Co-Chairs:
Yoichi Taira
Keio University
Email: taira@appi.keio.ac.jp

Yi Li
Intel Corporation
Email: yi.li@intel.com

1. 9:30 AM – High Modulus Photosensitive Permanent Film Utilizing Novel Polymerization System for Advanced MEMS Structure Fabrication
Ken-nichi Yamagata, Shiroy Yuge, Ryosuke Nakamura, Hirofumi Imai – Tokyo Ohka Kogyo Co., Ltd.

2. 9:50 AM – Lithographic Performance and Insulation Reliability of a Novel i-Line Photosensitive Dielectric Material
Go Inoue, Daki Yuki Morimi, Kaho Shibasaki, Ayano Okuda, Nobuhiro Ishikawa, Toshiyuki Ogata – TAIYO HOLDINGS Co., Ltd.

3. 10:10 AM – Effect of Surface Roughness of Polymer Dielectric Materials on Resolution of Fine Line Features
Pragya Bhaskar, Mohanalagum Kathaperumal, Mark Lossgo, Madhavan Swaminathan – Georgia Institute of Technology

4. 11:15 AM – A Novel High Reliability and Low DiK/Df Dielectric Material for 5G mmWave and HPC
Koari Hamada, Hiroshi Ozaki, Toshiyuki Sato, Shin Teraki, Fumitaka Komatsu, Masaki Yoshida, Hirotsugu Ikarashi – NAMICS Corporation

Okuno Takahisa, Shinji Tetsuya, Usui Yuki, Fukuda Takuya, Yana Masaki, Nagayoshi Masamune – Nissan Chemical Industries

Session 3: Advancements in Copper/Silicon-Oxide Hybrid Bonding

Committee: Interconnections

Session Co-Chairs:
Katsuyuki Sakuma
IBM Corporation
Email: ksakuma@us.ibm.com

Matthew Yao
GE Aviation
Email: matthew.yao@ge.com

1. 9:30 AM – A Study on the Surface Activation of Cu and Oxide for Hybrid Bonding Joint Interface
Boo Hee Hwang, Soo Won Lee, Youngkun Lee, Sangcheon Park, Gyeongjae Jo, Kwangbae Kim, Sungjin Han, Ilhwan Kim, Junmyong Park, Hyunchul Jung, Dongwoo Kang, Un-Byoung Kong – Samsung Electronics Co., Ltd.-Test and System Package

2. 9:50 AM – Fine Pitch Die-to-Wafer Hybrid Bonding
Thomas Workman, Jeremy Theil, Gill Fountain, Dominik Suwito, Cyprian Uzoh, Guilian Gao, K. M. Bang, Bongsuk Lee, Laura Mirkarimi – Adeia

3. 10:10 AM – Direct Die to Wafer Cu Hybrid Bonding for Volume Production
Chun Ho Fan, Hoi Ping Ng, Siu Cheung So, Ping Li, Siu Wing Lau, Thomas Uhwmann, Juergen Burggraff, Mariana Pires – ASMIPT Hong Kong, Ltd.

4. 11:15 AM – Demonstration of a Wafer Level Face-To-Back (F2B) Fine Pitch Cu-Cu Hybrid Bonding With High Density TSV For 3D Integration Applications
Jerzy Javier Suarez Bernu, Stephane Nicolas, Nicolas Bresson, Myriam Assous, Stephan Borel – CEA-Leti

5. 11:35 AM – Cu-Cu Wiring: The Novel Structure of Cu-Cu Hybrid Bonding
Yoshishis Kagawa, Takumi Kamibayashi, Nobutoshi Fuji, Shunsuke Furuse, Taichi Yamada, Tomoyuki Hirano, Hayato Iwamoto – Sony Semiconductor Solutions Corporation

Refreshment Break: 10:30 a.m.-11:15 a.m.
<table>
<thead>
<tr>
<th>Session 4: Assembly and Manufacturing Process Enhancement</th>
<th>Session 5: Flexible Packaging and Chip-Package Interaction</th>
<th>Session 6: Co-packaged Optical Assembly</th>
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<tr>
<td><strong>Committee:</strong> Assembly and Manufacturing Technology</td>
<td><strong>Committee:</strong> Thermal/Mechanical Simulation &amp; Characterization</td>
<td><strong>Committee:</strong> Photonics</td>
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<tr>
<td>Session Co-Chairs: Rameen Hadizadeh</td>
<td>Session Co-Chairs: Xuejun Fan Lamar University</td>
<td>Session Co-Chairs: Ajey Jacob University of Southern California</td>
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<td>Cirrus Email: <a href="mailto:rameen.hadizadeh@gmail.com">rameen.hadizadeh@gmail.com</a></td>
<td>Email: <a href="mailto:xuejun.fan@lamar.edu">xuejun.fan@lamar.edu</a></td>
<td>Email: <a href="mailto:ajey@isi.edu">ajey@isi.edu</a></td>
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<td>Christo Bojkov Qorvo, Inc. Email: <a href="mailto:cbojkov.ectc@gmail.com">cbojkov.ectc@gmail.com</a></td>
<td>Yong Liu ON Semiconductor Email: <a href="mailto:Yong.Liu@onsemi.com">Yong.Liu@onsemi.com</a></td>
<td>Takaaki Ishigure Keio University Email: <a href="mailto:isigure@appl.keio.ac.jp">isigure@appl.keio.ac.jp</a></td>
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1. 9:30 AM – Heterogeneous Integration of Diamond Heat Spreaders for Power Electronics Application
   Henry Antony Martin – Chip Integration Technology Center/Delft University of Technology; Marisa Reitnus, Xiao Tung – Mitrens BV; Dave Reij, Sander Dornsteiner, Martin Kagen, Sebastian Libor, Ediger Smits, Marco Koolk – Chip Integration Technology Center; Rene Poelma, Willeim Van Dien, GuoQi Zhang – Delft University of Technology

2. 9:50 AM – Optimum Re Control and Productivity Boost in Wafer-Level-Packaging Enabled by High-Throughput UBM/RDL Technology
   Carl Drechsel, Patrik Carazzetti, Juergen Weichart, Ewald Strobl – Evatec AG; Carl Wang – Evatec AG, Taiwan; Kay Vlieghweger – Fraunhofer IZM

3. 10:10 AM – Assembly Challenges and Approaches for 2.5D Chiplet Based System
   Sharon Pei Siang Lim, Mihai Dragos Rotaru, Wen Wei Sei, Hsiao Hsiang Yao – Institute of Microelectronics A*STAR

4. 11:15 AM – A Methodology to Optimize Dicing Parameters to Maximize Dicing Quality Through Machine Learning
   Aakrati Jain, Satyha Raghavan, Prabudhya Roy Chowdhury, Katsuuyaki Sakuma – IBM Research; Roman Doll, Kees Beshuvel, Faysal Boughorbel, Jeroen Van Borkulo, Mark Mueller – ASM Laser Separation International B.V.

5. 11:35 AM – Maskless Lithography for High-Density Package Redistribution Layers
   Prhalad Murah, Pratik Nimbalkar, Mohanalingam Kailapurooral, Mark D. Losego, Rao Tummala, Madhavan Swaminathan – Georgia Institute of Technology

6. 11:55 AM – Exploring an Additive Approach to Embed Chips in Metallic Matrix Inside a Printed Circuit Board
   Roberto Aga, Fahima Ouchen – KBR, Inc./U.S. Air Force Research Laboratory; Rachel Aga – Wright State University; Carrie Batsch, Emily Heckman – AFRL

7. 12:15 PM – Micro Transfer Printing 100 μm Thick Components Directly from Dicing Tape
   Kevin Oswalt, David Gomez, Tanya Moore, Prasanna Ramaswamy, Alin Fecioru – X-Celeprint Ltd.

Refreshment Break: 10:30 a.m.–11:15 a.m.

4. 11:15 AM – A Methodology to Optimize Dicing Parameters to Maximize Dicing Quality Through Machine Learning
   Aakrati Jain, Satyha Raghavan, Prabudhya Roy Chowdhury, Katsuuyaki Sakuma – IBM Research; Roman Doll, Kees Beshuvel, Faysal Boughorbel, Jeroen Van Borkulo, Mark Mueller – ASM Laser Separation International B.V.

5. 11:35 AM – Maskless Lithography for High-Density Package Redistribution Layers
   Prhalad Murah, Pratik Nimbalkar, Mohanalingam Kailapurooral, Mark D. Losego, Rao Tummala, Madhavan Swaminathan – Georgia Institute of Technology

6. 11:55 AM – Exploring an Additive Approach to Embed Chips in Metallic Matrix Inside a Printed Circuit Board
   Roberto Aga, Fahima Ouchen – KBR, Inc./U.S. Air Force Research Laboratory; Rachel Aga – Wright State University; Carrie Batsch, Emily Heckman – AFRL

7. 12:15 PM – Micro Transfer Printing 100 μm Thick Components Directly from Dicing Tape
   Kevin Oswalt, David Gomez, Tanya Moore, Prasanna Ramaswamy, Alin Fecioru – X-Celeprint Ltd.

   Sasi Kumar Tippabhotla, Ji Lin – Institute of Microelectronics A*STAR

9. 1:15 PM – A Methodology to Optimize Dicing Parameters to Maximize Dicing Quality Through Machine Learning
   Aakrati Jain, Satyha Raghavan, Prabudhya Roy Chowdhury, Katsuuyaki Sakuma – IBM Research; Roman Doll, Kees Beshuvel, Faysal Boughorbel, Jeroen Van Borkulo, Mark Mueller – ASM Laser Separation International B.V.

10. 1:45 PM – Exploring an Additive Approach to Embed Chips in Metallic Matrix Inside a Printed Circuit Board
    Roberto Aga, Fahima Ouchen – KBR, Inc./U.S. Air Force Research Laboratory; Rachel Aga – Wright State University; Carrie Batsch, Emily Heckman – AFRL

11. 2:15 PM – Micro Transfer Printing 100 μm Thick Components Directly from Dicing Tape
    Kevin Oswalt, David Gomez, Tanya Moore, Prasanna Ramaswamy, Alin Fecioru – X-Celeprint Ltd.
<table>
<thead>
<tr>
<th>Session 7: Large Formfactor Dense System Integration by Fan-Out</th>
<th>Session 8: Novel Reliability Test Methods</th>
<th>Session 9: Innovations in Copper Chip-to-Wafer Bonding</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Committee:</strong> Packaging Technologies</td>
<td><strong>Committee:</strong> Applied Reliability</td>
<td><strong>Committee:</strong> Interconnections</td>
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<tr>
<td><strong>Session Co-Chairs:</strong></td>
<td><strong>Session Co-Chairs:</strong></td>
<td><strong>Session Co-Chairs:</strong></td>
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<tr>
<td>Steffen Kroehnert</td>
<td>S. B. Park</td>
<td>Wei-Chung Lo</td>
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<tr>
<td>ESPAT Consulting, Germany</td>
<td>Binghamton University</td>
<td>Industrial Technology Research Institute</td>
</tr>
<tr>
<td>Email: <a href="mailto:steffen.kroehnert@espat-consulting.com">steffen.kroehnert@espat-consulting.com</a></td>
<td>Email: <a href="mailto:sbpark@binghamton.edu">sbpark@binghamton.edu</a></td>
<td>Email: <a href="mailto:lo@itri.org.tw">lo@itri.org.tw</a></td>
</tr>
<tr>
<td>Bora Baloglu</td>
<td>Sandy Klengel</td>
<td>Ou Li</td>
</tr>
<tr>
<td>Intel Corporation</td>
<td>Fraunhofer IMWS</td>
<td>Advanced Semiconductor Engineering, Inc.</td>
</tr>
<tr>
<td>Email: <a href="mailto:bora.baloglu@intel.com">bora.baloglu@intel.com</a></td>
<td>Email: <a href="mailto:sandylkengel@imws.fraunhofer.de">sandylkengel@imws.fraunhofer.de</a></td>
<td>Email: <a href="mailto:ou.li@aseus.com">ou.li@aseus.com</a></td>
</tr>
</tbody>
</table>

1. 2:00 PM – 3D Freeform Antenna-in-Package Approach for FOWLP
Tanja Braun, Tina Thomas, Karl-Friedrich Becker, Thi Huyen Le, Christian Tschoban, Rolf Aschenbrenner – Fraunhofer IZM; Martin Schneider-Ramelow – Technical University Berlin

1. 2:00 PM – A New Vibration Test Method for Automotive and Consumer Electronic Devices: Calibration and Fatigue Test

1. 2:00 PM – Solderless Interconnection Studies for Advanced Memory Chip-to-Wafer Stacking
Wei Zhou, Bharat Bhushan, Yingta Chiu, Ava Yang, Huimin Guo, Bret Street, Kunal Parekh, Akshay Singh – Micron Technology, Inc.

2. 2:20 PM – High-Speed Performance Validation Testing of Die-to-Die Interconnects in High-Density Fan-Out Package
Cindy Muir, Carlton Hannah, Bernd Waitdas, Abdallah Bacha, Hui Zhang – Intel Corporation

2. 2:20 PM – Magnetic Force-Based Measurement Technique to Investigation the Effect of Lead-Free Solder Intermetallic Compounds (IMC) on Interconnect Reliability
Rui Chen, Suresh Sitaraman – Georgia Institute of Technology; Nicholas Gingo – University of Alabama in Huntsville

2. 2:20 PM – Development of Copper Thermal Coefficient for Low Temperature Hybrid Bonding

3. 2:40 PM – Extremely Large Area Integrated Circuit (ELAIC): An Advanced Packaging Solution for Chiplets
Rabinda Das, Jason Plant, Alex Wynn, Matthew Ricci, Ryan Johnson, Matthew Stamplis, Brian Tyrrell, Kenneth Schultz, Paul Juodawlkis – MIT Lincoln Laboratory

3. 2:40 PM – Residual Stress Measurement of Build-Up Layer in Silicon Wafers
Junbo Yang, Chongyang Cai, Yangyang Lai, Jong Hwan Ha, Seungbae Park – Binghamton University; Hyuan Wang, Suresh Ramalingam, Gamal Refai-Ahmed – Advanced Micro Devices, Inc.

3. 2:40 PM – Impact of Plasma Activation on Copper Surface Layer for Low Temperature Hybrid Bonding
Christopher Netzband, Kandabarla Tapily, Dylan Burns, Ibeok Song, Cory Wajda – TEL Technology Center, America, LLC

4. 3:45 PM – Advanced Fan-Out Panel Level Package (FO-PLP) Development for High-End Mobile Application
Hyungwon Kim, Jaehoon Choi, Seok Won Lee, Eun Seok Cho, Hwasub Oh, Junho Lee, Seungiu Ha, Wonkyung Choi, Dong Wook Kim – Samsung Electronics Co., Ltd.

4. 3:45 PM – Chip Level Evaluation of Wafer-to-Wafer Direct Bonding Strength With Bending Test
Juno Kim, Kyungmni Baek, Min-soo Hn, Kyeongbin Lim, Minwoo Daniel Rhee – Samsung Electronics Co., Ltd.-Mechatronics Research

4. 3:45 PM – Investigation of Cu-Cu Direct Bonding Process Utilized by High Porosity and Nanocrystal Structure
Takuma Nakagawa, Daki Furuyama, Sho Nakagawa, Yutaro Morii, Kotoro Iwata, Kyotaka Nakaya, Takuma Katae – Mitsubishi Materials Corporation

5. 4:05 PM – Incorporating Chiplets Using Chips First Ultra-High-Density Fan-Out With Maskless Laser Direct Imaging and Adaptive Patternning for High Performance Computing
Benedict San Jose, Cliff Sandstrom, Erick Talain, Jan Kellar, Tim Olson – Deca Technologies, Inc.; Mary Maye Melgo, Rzi Gacho, Byung Cheol Kim – Nepes Hayyim Corporation

5. 4:05 PM – In-Situ Observation of Microscale Crack-Tip Strain Field Evolution in Underfill With Different Toughening Agents and Temperatures Via SEM-DIC Coupled Method
Xuecheng Yu, Gang Li, Younan Fan, Rong sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology

5. 4:05 PM – A High Throughput Two-Stage Die-to-Wafer Thermal Compression Bonding Scheme for Heterogeneous Integration
Krutikesh Sahoo, Haoxiang Ren, Subramanian S. Iyer – University of California, Los Angeles

6. 4:25 PM – Reliability Challenges of Large Organic Substrate With High-Density Fan-Out Package
Rosa Lin, Laurene Yip, Charles Lai, Cooper Peng – MediaTek, Inc.

6. 4:25 PM – Experimental Identification of the Failure Modes and Failure Mechanisms of Fiber Arrays Under Cyclic Tensile Loading
Asane Dione, Jean-Francois Morissette, Julien Sylvestre, Patrick Jacques – University of Sherbrooke; Richard Langlois, Papa Momar Souare – IBM Canada, Ltd.

6. 4:25 PM – Optimization of Cu Interconnects - SICN Interfacial Adhesion by Surface Treatments

6. 4:25 PM – Selective Cobalt Atomic Layer Deposition for Chip-to-Wafer 3D Heterogeneous Integration
Madsen Manley, Ming-Mou Li, Muhammad S. Bakir – Georgia Institute of Technology; Zachary Deveraux, Niy Myat Khine Lin, Charles Winter – Wayne State University; Andrew Kummel – University of California, San Diego

7. 4:45 PM – Flip Chip Process Enablement in DRAM Stacked Die Package
Chen-Yu Huang, Tsung-Han Chiang, Jongbabe Lee, Kohan Lir, Chong-Leong Gan – Micron Memory Taiwan, Co., Ltd.; Travis Jensen – Micron Technology, Inc.

7. 4:45 PM – A Predictive Metallurgical Means to Identify the Relative Risk of Failure for Plated Micro Vias
Roger Massey, Tobias Bernhard, Kilan Klaeeden, Sebastian Zarwell, Edith Steinhaeuser, Sascha Dieter, Stefan Kempa, Frank Bruening – MKS Atochek

7. 4:45 PM – Selective Cobalt Atomic Layer Deposition for Chip-to-Wafer 3D Heterogeneous Integration
Madsen Manley, Ming-Mou Li, Muhammad S. Bakir – Georgia Institute of Technology; Zachary Deveraux, Niy Myat Khine Lin, Charles Winter – Wayne State University; Andrew Kummel – University of California, San Diego
### Program Sessions: Wednesday, May 31, 2:00 p.m. - 5:05 p.m.

<table>
<thead>
<tr>
<th>Session 10: Packaging Interconnects</th>
<th>Session 11: Additive Manufacturing and Packaging for Flexible Electronics</th>
<th>Session 12: mm Wave Antenna-in-Package and Arrays</th>
</tr>
</thead>
<tbody>
<tr>
<td>Committee: Thermal/Mechanical Simulation &amp; Characterization</td>
<td>Committee: Emerging Technologies</td>
<td>Committee: RF, High-Speed Components &amp; Systems</td>
</tr>
<tr>
<td>Session Co-Chairs: Suresh K. Sitaraman Georgia Institute of Technology Email: <a href="mailto:suresh.sitaraman@me.gatech.edu">suresh.sitaraman@me.gatech.edu</a></td>
<td>Session Co-Chairs: Tengfei Jiang University of Central Florida Email: <a href="mailto:Tengfei.jiang@ucf.edu">Tengfei.jiang@ucf.edu</a></td>
<td>Session Co-Chairs: Jaemin Shin Qualcomm Technologies, Inc. Email: <a href="mailto:jaemin@qebl.qualcomm.com">jaemin@qebl.qualcomm.com</a></td>
</tr>
<tr>
<td>Jiamin Ni IBM Corporation Email: <a href="mailto:jiamin9810@gmail.com">jiamin9810@gmail.com</a></td>
<td>Dishit Parekh Intel Corporation Email: <a href="mailto:dishit.parekh@intel.com">dishit.parekh@intel.com</a></td>
<td>Dongji Xie, Minghong Jian – Nvidia</td>
</tr>
<tr>
<td>1. 2:00 PM – Finite Element Analysis of Shock and Vibration of a Printed Circuit Board With Multiple Ball-Grid-Array Packages Using Beam Elements to Model the solder Joints to Achieve Design-for-Reliability Tiey Zheng – Microsoft Corporation; Babu Aminijikarai – ANSYS, Inc.</td>
<td>1. 2:00 PM – Electromechanical and Thermal Characterization of Printed Liquid Metal ink on Stretchable Substrate for Soft Robotics Multi-Sensing Applications El Mehdi Abbara, Mohammed Alhendi, Riadh Al-haidari, Nathaniel Gee, Mark Poliks – Binghamton University; Emily Boggs, Tan Yewteck, Deepak Trivedi – GE Research; Christopher Tabor – AFRL</td>
<td>1. 2:00 PM – A Scalable Heterogeneous AiP Module for a 256-Element 5G Phased Array Duxian Liu, Xiaoxiong Gu, Christian Baks, Arun Padaimani, Atom Watarabe, Alberto Valdes-Garcia – IBM Corporation; Koichiro Masuko, Yuijro Tojo, Gokul Chandran, Yuta Hasegawa, Xu Lei, Ning Guan – Fujikura, Ltd.</td>
</tr>
<tr>
<td>3. 2:40 PM – High-Temperature Creep Properties of Solder Interconnects (SnBiAgCu) and Its Thermal Fatigue Properties Under Different Potting Compounds: Leiming Du, Guoqi Zhang – Delft University of Technology; Xijuan Zhao, Willem Van Driel – Signify; Rene Poelma – Nexpria</td>
<td>3. 2:40 PM – Additively Manufactured Flexible Material Characterization and On-Demand Smart Packaging Topologies for 5G/mmWave Wearable Apparatuses: Kexin Hu, Yi Zhou, Suresh Sitaraman, Manos Tentzeris – Georgia Institute of Technology</td>
<td>3. 2:40 PM – A Low-Cost Antenna-in-Package (AiP) for D-Band Application Hung-Chun Kuo, Po-I Wu, Sheng-Chi Hsieh, Ming-Fong Jhong, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.</td>
</tr>
<tr>
<td>5. 4:05 PM – Sustainable-Ink Process Recipes for the Fabrication of Additively Printed Circuits and Component Attachment Pradeep Lal, Jineesh Narangaparambil, Ved Soni, Shriram Kulkarni, Kartik Goyal – Auburn University; Scott Miller – NextFlex</td>
<td>5. 4:05 PM – Advances in Conductive Features in Digitally Manufactured Electronics Bryce Gray, Jason Benoit, Mark Kloza, Kenneth Church – Sciperio</td>
<td>5. 4:05 PM – 5G mmWave Patch Antenna Array on Extremely Low Loss Alumina Ribbon Ceramic Substrates for Antenna-in-Package (AiP): Choelbok Kim, Hoon Kim, Rajesh Viddi, Eun Ju Moon, David Peters – Corning, Inc.</td>
</tr>
<tr>
<td>7. 4:45 PM – Physics-Driven Regression Algorithm on Solder Joint Fatigue Life Prediction for Mobile SIP Packages Fuxing Che, Yecow Chon Ong, Hong Wan Nge, Ling Pan, Christopher Glancey, Gokul Kumar – Micron Semiconductor Asia Operations Pte. Ltd; Koustate Sinha – Micron Technology, Inc.</td>
<td>7. 4:45 PM – Evaluation of Screen Printing Process in Fabrication of Small Profile Conductive Ink-Based Contact Force Sensor Maria Ramonara Nina Bautista Damalerio, Ruiji Lim, Ven Wei James Yap, Ming-Yuan Cheng – Institute of Microelectronics A*STAR; Ran Young Lim – Kalos Medical, Inc.</td>
<td>7. 4:45 PM – Design and Fabrication of A Sub-THz Co-Reflectively Curved Patch-Reflector Antenna Array for Gain Enhancement and Near Field Focusing Ching-Jen Lee, Pin-Cheng Tseng, Wei-Chian Wang, Yun-Hao Liou, Yu-Ting Cheng, Chen-Nan Kuo – National Yang Ming Chiao Tung University</td>
</tr>
</tbody>
</table>

**Refreshment Break: 3:00 p.m. - 3:45 p.m.**
### Program Sessions: Thursday, June 1, 9:30 a.m. -12:35 p.m.

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<th>Session 13: Wafer/Panel-Level and Advanced Substrate Technologies</th>
<th>Session 14: Advances in Heterogeneous Integration Bonding Technology</th>
<th>Session 15: Innovative Interposer and Through-Via Technologies</th>
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</thead>
<tbody>
<tr>
<td><strong>Committee:</strong> Packaging Technologies</td>
<td><strong>Committee:</strong> Materials &amp; Processing</td>
<td><strong>Committee:</strong> Interconnections</td>
</tr>
<tr>
<td>Session Co-Chairs: Markus Leitgeb</td>
<td>Session Co-Chairs: Jae Kyu Cho</td>
<td>Session Co-Chairs: C. Key Chung</td>
</tr>
<tr>
<td>AT&amp;S AG Email: <a href="mailto:m.leitgeb@ats.net">m.leitgeb@ats.net</a></td>
<td>GlobalFoundries, Inc. Email: <a href="mailto:jaekyu.cho@globalfoundries.com">jaekyu.cho@globalfoundries.com</a></td>
<td>TongFu Microelectronics Co., Ltd Email: <a href="mailto:chungckey@hotmail.com">chungckey@hotmail.com</a></td>
</tr>
<tr>
<td>Dean Malta Micross Advanced Interconnect Technology Email: <a href="mailto:Dean.Malta@micross.com">Dean.Malta@micross.com</a></td>
<td>Qianwen Chen IBM Research Email: <a href="mailto:cheng@us.ibm.com">cheng@us.ibm.com</a></td>
<td>Chuan Seng Tan Nanyang Technological University Email: <a href="mailto:tancs@alum.mit.edu">tancs@alum.mit.edu</a></td>
</tr>
<tr>
<td><strong>1. 9:30 AM – Supercarrier Redistribution Layer to Realize Ultra High Performance 2.5D Wafer Scale Packaging by CoWoS</strong> S.Y. Hou, Chen-Hsun Lee, Tsung-Ding Wang, Hao Cheng Hou – Taiwan Semiconductor Manufacturing Company, Ltd.</td>
<td><strong>1. 9:30 AM – Characterization of 300 mm Low Temperature SiCN PVD Films for Hybrid Bonding Application</strong> Xavier Brun, Md M. Haan – Intel Corporation; Patrick Carazetti, Carl Drehsel, Ewald Strobl – Evatec AG</td>
<td><strong>1. 9:30 AM – Assembly-Based Through-X-Via (TXV) Integration Technology by Advanced Fan-Out Wafer-Level Packaging</strong> Atsushi Shinoda, Chang Liu, Tadaaki Hoshi, Jiayi Shen, Yuki Susumago, Hisashi Kino, Tetsu Tanaka, Takafumi Fukushima – Tohoku University</td>
</tr>
</tbody>
</table>

**Refreshment Break: 10:30 a.m.-11:15 a.m.**
### Program Sessions: Thursday, June 1, 9:30 a.m. -12:35 p.m.

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<tr>
<th>Session 16: Sintering and Soldering for High-Power, High-Reliability, and RF Devices</th>
<th>Session 17: Advanced Reliability Modelling and Characterization</th>
<th>Session 18: Advanced Photonic Packaging and Interconnect</th>
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<tbody>
<tr>
<td><strong>Committees:</strong> Assembly and Manufacturing Technology and Materials &amp; Processing</td>
<td><strong>Committees:</strong> Thermal/Mechanical Simulation &amp; Characterization and Applied Reliability</td>
<td><strong>Committee:</strong> Photonics</td>
</tr>
<tr>
<td><strong>Session Co-Chairs:</strong> Mark Poliks Binghamton University  Email: <a href="mailto:mpoliks@binghamton.edu">mpoliks@binghamton.edu</a> Omkant Gupta Advanced Micro Devices, Inc.  Email: <a href="mailto:Omkant.Gupta@amd.com">Omkant.Gupta@amd.com</a></td>
<td><strong>Session Co-Chairs:</strong> Wei Wang Qualcomm Technologies, Inc.  Email: <a href="mailto:wwang@g.clemson.edu">wwang@g.clemson.edu</a> Ts-Cheng Chiu National Cheng-Kung University  Email: <a href="mailto:tcchiu@mail.ncku.edu.tw">tcchiu@mail.ncku.edu.tw</a></td>
<td><strong>Session Co-Chairs:</strong> Richard Pitwon Resolute Photonics, Ltd.  Email: <a href="mailto:richard.pitwon@resolutephotonics.com">richard.pitwon@resolutephotonics.com</a> Soon Jang ficonTEC USA  Email: <a href="mailto:soon.jang@ficontec.com">soon.jang@ficontec.com</a></td>
</tr>
<tr>
<td>4. 11:15 AM – Substrate Copper Trace Crack Characterization and Simulation Wei Yu, Faxing Che, Yeow Chong Ong, Hong Wan Ng – Micron Semiconductor Asia Operations Pte. Ltd; Vance Liu, Milly Lin, Jay Lin – Micron Memory Taiwan Co., Ltd; Brad Rumsey – Micron Technology, Inc.</td>
<td>5. 11:35 AM – Design-for-Manufacturing and Design-for-Reliability Strategies for Large 80mm+ 2.5D Devices Peng Su, Omar Ahmed, Leif Hutchinson, Bernard Ghisauer, Gautam Ganguly – Juniper Networks</td>
<td>5. 11:35 AM – Scalable Fiber-Array-to-Chip Interconnections With Sub-Micron Alignment Accuracy Shengtao Yu, Muhammad S. Bakir, Thomas Gaylord – Advanced Industrial Science and Technology Committee: Photonics</td>
</tr>
<tr>
<td>5. 11:35 AM – An In-Containing Lower-Temperature Lead-Free Solder Paste for Wafer-Level Package Application that Outperforms SAC305 Hongwen Zhang, Tyler Richmond, Huaguang Wang – Indium Corporation</td>
<td>6. 11:55 AM – A Continuum Damage Mechanics Approach for the Reliability of Lead-Free Solders Subjected to Cyclic Loading Golam Rakib Mazumder, Mohammad Ashraful Haq, Jeffrey Suhling, Pradeep Lall – Auburn University; Yaoying Chen, Torsten Hauck, Abdullah Fahim – NXP Semiconductors, Inc.</td>
<td>6. 11:55 AM – Realization, Multi-Field Coupled Simulation and Characterization of a Thermo-Mechanically Robust LiDAR Front End on a Copper Coated Glass Substrate Marius Kettlinger Nord, Arindam Ghorai, Gordon Edger – Technical University of Applied Science Ingolstadt; Peter Meuser, Magi Taxiakostis, Bernhard Wunderle – Chemnitz University of Technology; Gunnar Boettger, Michael Johannes Hauser – Fraunhofer IZM; Hassan Erdag – Continental AG; Ralph Schütz – Brandenburg University of Technology</td>
</tr>
<tr>
<td>Session 19: Advances in 3D Integration and Hybrid Bonding</td>
<td>Session 20: Automotive/Board-Level Reliability</td>
<td>Session 21: Fine-Pitch and Intermetallic Considerations in Advanced Solder Interconnections</td>
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<td><strong>Committee:</strong> Interconnections</td>
</tr>
<tr>
<td>Session Co-Chairs: Peng Su, Juniper Networks Email: <a href="mailto:pensu@juniper.net">pensu@juniper.net</a> Jaesik Lee Meta Platforms, Inc. Email: <a href="mailto:jaesiklee@fb.com">jaesiklee@fb.com</a></td>
<td>Session Co-Chairs: Paul Tiner Texas Instruments, Inc. Email: <a href="mailto:p-tiner@ti.com">p-tiner@ti.com</a> Varughese Mathew NXP Semiconductor, Inc. Email: <a href="mailto:varughese.mathew@nxp.com">varughese.mathew@nxp.com</a></td>
<td>Session Co-Chairs: Nathan Lower Consultant Email: <a href="mailto:nplower@hotmail.com">nplower@hotmail.com</a> Jian Cai Tsinghua University Email: <a href="mailto:jamescai@tsinghua.edu.cn">jamescai@tsinghua.edu.cn</a></td>
</tr>
<tr>
<td>1. 2:00 PM – Thermal Improvement of HBM With Joint Thermal Resistance Reduction for Scaling 12 Stacks and Beyond Taehwan Kim, Youngdeuk Kim, Heejung Hwang, Hwanjoo Park, Jaechoon Kim, Dan (Kyang Suk) Oh – Samsung Electronics Co., Ltd.</td>
<td>1. 2:00 PM – Impact of Temperature Cycling Conditions on Board Level Vibration for Automotive Applications Varun Thukral, Irene Bacquet, Michiel Soestbergen, Jeroen Zaal, Romuald Roucou, Rene Rongen – NXP Semiconductor, Inc. Willem Driel, G.Q. Zhang – Delft University of Technology</td>
<td>1. 2:00 PM – Copper Pillar Voids in a Flip Chip Package During High Temperature Application Mao Wang, Amar Mavinkurve, Romuald Roucou, Amirul Arifin, CS Foong, Trent Uehling, Nishant Lakhera – NXP Semiconductor, Inc.</td>
</tr>
</tbody>
</table>

**Refreshment Break: 3:00 p.m. - 3:45 p.m.**
Program Sessions: Thursday, June 1, 2:00 p.m. - 5:05 p.m.

Session 22: Large Substrate Process Integration Challenges
Committee: Assembly and Manufacturing Technology
Session Co-Chairs: Valerie Oberson IBM Canada, Ltd.
Email: voberson@ca.ibm.com
Jobert Van Eisdien Atotech USA, Inc.
Email: Jobert.Van-Eisdien@atotech.com

1. 2:00 PM – Extremely Large 3.5D Heterogeneous Integration for the Next-Generation Packaging Technology
Ilbok Lee, Soohyun Nam, Sung-Geun Kim, Sangho Shin, Young-hung Kim, Sun-Kyung Seo, Hae Jung Yu, Dae-Woo Kim – Samsung Electronics Co., Ltd.

2. 2:20 PM – Study of Fabrication and Reliability for the Extremely Large 2.5D Advanced Package
Kosuke Muri, Hitoshi Onozoki, Dongchul Kang, Kazue Hirano, Mitsukura Kazuyuki – Resonac Corporation

3. 2:40 PM – Controlling Underfill on Die in Multi-Chip Heterogeneous Integration With Die Height Delta
Zyiin Lin, Wei Li, Edwin Cetegen, Yang Guo, Naiyuan Lu, Harinyi Okalor, Yipal Mehta, Xavier Brun, Shun Zhong, Hisin-yu Li, Christopher Rumer – Intel Corporation

Refreshment Break: 3:00 p.m. - 3:45 p.m.

Session 23: Next Generation Quantum, AI, and Secure System Design
Committee: Emerging Technologies
Session Co-Chairs: Rohit Sharma Indian Institute of Technology Ropar
Email: rohit@iitrpr.ac.in
Santosh Kudtarkar Analog Devices, Inc.
Email: santosh.kudtarkar@analog.com

1. 2:00 PM – Thermal-Aware SoC Macro Placement and Multi-Chip Module (MCM) Package Design With Mixed-Vary Bayesian Optimization
Michael Molter, Eliese Rosenbaun – University of Illinois; Rahul Kumar, Osama Wagar, Bhatti, Madhavan Swaminathan – Indian Institute of Technology; Sonja Koller – Intel Corporation

2. 2:20 PM – 3D Defect Detection and Metrology of HBM Using Semi-Supervised Deep Learning

3. 2:40 PM – A Si-Interposer With Buried Cu Metal Stripes and Bonded to Si-Substrate Backside for Security IC Chips
Takuya Wadatsumi, Rikuu Hasegawa, Kazuki Monta, Takaji Miki, Makoto Nagata – Kobe University; Takaaki Oikdono – SUGU Co., Ltd.

4. 3:45 PM – Physical Authentication of Electronic Devices Using Synthetically Generated 3D Material Signatures
Tejas Ravindra Kulkarni, Nikhilesh Chawla, Ganesh Subbarayan – Purdue University

5. 4:05 PM – Modeling and Analysis of CMOS-based Folded Memristive Crossbar Array for 3D Neuromorphic Integrated Circuits
Sherin A. Thomas, Sahibia Kaur Vohra, Syahush Kushwaha, ROHIT SHARMA, Devarshi Mrinal Das – Indian Institute of Technology Ropar

6. 4:25 PM – Cryogenic Integration for Quantum Computer Using Diamond Color Center Spin Qubits
Toshiki Iwai, Kenichi Kagawauchi, Tetsuya Miyatake, Tetsuro Ishiguro, Shoichi Miyahara, Shintaro Sato – Fujitsu, Ltd.; Salahuddin Nur, Ryoichi Ishihara – Delft University of Technology

7. 4:45 PM – Signal Integrity Interconnects for 112 Gbps SerDes Interface With Channel Analysis
Hae-In Kim, Alexander Wilcher, Saeyeong Jeon, Yong-Kyu Yoon – University of Florida; Brice Achkir, Rockwell Hsu – Cisco Systems, Inc.

Session 24: High-Speed Signal and Power Integrity
Committee: RF, High-Speed Components & Systems
Session Co-Chairs: Rockwell Hsu Cisco Systems, Inc.
Email: rohsu@cisco.com
Chuei-Tang Wang Taiwan Semiconductor Manufacturing Company, Ltd.
Email: ctwang10492@hotmail.com

1. 2:00 PM – Comprehensive PDN/PSII Analysis of Silicon Capacitor Use for 8.533 GT/s LPDDR4X Application

2. 2:20 PM – Design Considerations for Power Delivery Network and Metal Insulator Metal Capacitor Integration in Bridge-Chips for 2.5-D Heterogeneous Integration
Ankit Kaul, Madison Manley, Muhammad S. Bakir – Georgia Institute of Technology

3. 2:40 PM – Statistical Analysis of Off-Chip Power-Integrity for Multicore Systems
Sodam Han, Sungwook Moon, Jungil Soo, Seungki Nam – Samsung Electronics Co., Ltd.-Foundry Business

4. 3:45 PM – HBM3 Modules on Latest 2.3D High Density Organic Laminate: Signal Integrity Design and Analysis With Interconnect Budget Results
Frank Lisich – IBM Research; Hiroyuki Mori – IBM Research, Tokyo

5. 4:05 PM – Signal and Power Integrity Design and Analysis for Bunch-of-Wires (BoW) Interface for Chiplet Integration on Advanced Packaging
Ram Krishna, Eliese Rosenbaum – University of Illinois; Atom Watanabe, John Goitz, Ravi Borani, Frank Lisich, Arvind Kumar – IBM Corporation

6. 4:25 PM – Metaconductor-Based High Signal Integrity Interconnects for 112 Gbps SerDes Interface With Channel Analysis
Hae-In Kim, Alexander Wilcher, Saeyeong Jeon, Yong-Kyu Yoon – University of Florida; Brice Achkir, Rockwell Hsu – Cisco Systems, Inc.

7. 4:45 PM – Signal Integrity Co-Design of a High-Speed (20 Gbps) Analog Passive CMOS Bidirectional Switch
Srikanth Manian, S. Shanmuganarayanan, Rajan Murugan, Sylvester Ankamah-Kusi – Texas Instruments, Inc.
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<th>Session 26: Materials Reliability</th>
<th>Session 27: Next Generation Wafer-to-Wafer Copper Bonding</th>
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<td><strong>Committee:</strong> Applied Reliability</td>
<td><strong>Committee:</strong> Interconnections</td>
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<td><strong>Session Co-Chairs:</strong> Eric Tremble Marvell</td>
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<td>Email: <a href="mailto:etremble@marvell.com">etremble@marvell.com</a></td>
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<td>Subhash L. Shinde, Notre Dame University</td>
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<td>Email: <a href="mailto:sshinde@nd.edu">sshinde@nd.edu</a></td>
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<td><strong>Session Co-Chairs:</strong> Tae-Kyu Lee Cisco Systems, Inc.</td>
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<td>Email: <a href="mailto:taeklee@cisco.com">taeklee@cisco.com</a></td>
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<td>Darvin R. Edwards, Edwards Enterprise Consulting, LLC</td>
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<td><strong>Session Co-Chairs:</strong> Li Li Infinera</td>
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<td>Email: <a href="mailto:packaging@yahoo.com">packaging@yahoo.com</a></td>
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<td>Dingyou Zhang, Broadcom, Inc.</td>
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<tr>
<td>Email: <a href="mailto:dingyouzhang.brcm@gmail.com">dingyouzhang.brcm@gmail.com</a></td>
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<tr>
<td><strong>1. 9:30 AM – CoWoS Architecture Breakthrough for Next Generation HPC Demand</strong></td>
<td><strong>1. 9:30 AM – Control of Solder Microstructure Stimulated by Interface Condition of the UBM/Solder and Enhancement of Electromigration Reliability</strong></td>
<td><strong>1. 9:30 AM – 0.5 µm Pitch Next Generation Hybrid Bonding With High Alignment Accuracy for 3D Integration</strong></td>
</tr>
<tr>
<td><strong>2. 9:50 AM – Reliability Performance of S-Connect Module (Bridge Technology) for Heterogeneous Integration Packaging</strong></td>
<td><strong>2. 9:50 AM – Al2O3-Coated Bond Wire With Adhesion Promoter and Electrical Insulation</strong></td>
<td><strong>2. 9:50 AM – Low Temperature and Fine Pitch Nanocrystalline Cu/SiCN Wafer-To-Wafer Hybrid Bonding</strong></td>
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<tr>
<td><strong>3. 10:10 AM – Advanced Packaging Design Platform for Chiplets and Heterogeneous Integration</strong></td>
<td><strong>3. 10:10 AM – Evolution of Propensity for High Strain-Rate Damage Accrual in Doped and Undoped SnAgCu Lead-Free Solders in Temperature Range of -65 °C to +200 °C After 1-Year Sustained High Temperatures Exposure</strong></td>
<td><strong>3. 10:10 AM – 0.5 µm Pitch Wafer-to-Wafer Hybrid Bonding With SiCN Bonding Interface for Advanced Memory</strong></td>
</tr>
<tr>
<td>Po Yuan (James) Su, David Ho, Jocy Pu, Yu Po Wang – Siliconware Precision Industries Co., Ltd.</td>
<td>Ji-Youn Kwak – University of Utah; Emmanuel Chery, John Sabbeekoon, Julien Bertheau, Joke De Messermaeker, Eric Beyne – imec</td>
<td>Hisan-Wei Tsai, Yong-Sheng Lin, Chun-Wei Chiang, Yun-Ching Hung, Chiu-Li Kao, Ping-Hung Hsieh, I-Ting Lin, Chih-Yuan Hsu – Advanced Semiconductor Engineering, Inc.</td>
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<tr>
<td><strong>6. 11:55 AM – Silicon Interposer Based 2.5 D Integration of TeraPHY Chiplet for Co-Packaged Optics</strong></td>
<td><strong>6. 11:55 AM – The Failure Mechanisms of Bonding Between Copper Substrate and Encapsulation Epoxy Under High-Temperature Aging</strong></td>
<td><strong>6. 11:55 AM – Not All Nanograined Copper is Created Equal - In Pursuit of a Robust Low Temperature Copper to Copper Bonding Process</strong></td>
</tr>
<tr>
<td>Haiwei Lu, Chong Zhang, Chen sun, Steve Groothuis, Mark Wade, Chen Li, Chandru Ramamurthy, Norman Chan, Jie Ding, Byungchae Kim, Michael Rust, Forrest Sedgwick – Ayar Labs, Inc.</td>
<td>Shuajie Zhao, Chuantong Chen, Katsuaki Suganuma – Osaka University; Minoru Ueshima, Motoharu Haga – Daicel Corporation</td>
<td>Yun Zhang, Peipei Dong, Jing Wang, Xingong Zhang – Shinan Materials LLC; Klaus Leyendecker, Tsvetina Dobrovolska, Michael Herkommer, Volker Wohlfarth, Josh Liang – Umicore Galvanotechnik GmbH</td>
</tr>
</tbody>
</table>

**Program Sessions: Friday, June 2, 9:30 a.m. -12:35 p.m.**

**Refreshment Break: 10:30 a.m.-11:15 a.m.**
Program Sessions: Friday, June 2, 9:30 a.m. -12:35 p.m.

Session 28: Process Enhancements in 3D, FOWLP, and TSV Technologies
Committee: Materials & Processing
Session Co-Chairs: Vidya Jayaram, Intel Corporation; Email: vidya.jayaram@intel.com
Dwayne Shirley, Marvell; Email: dwayne.shirley@marvell.com

1. 9:30 AM – Magneto-Assisted Graphene Reinforcement: A New Method to Enhance Nanostructure and Properties of Electrodeposited Copper
Nitin Nandurakkad, Vanessa Smet – Georgia Institute of Technology

2. 9:50 AM – Exploring Capabilities of Maskless Lithography for Dual Image Exposure in FO WLP

3. 10:10 AM – Alignment Through Thick Si Layer for High Resolution Patternning on Bumped Wafers With Tight Overlay Margin Using Immersion Lithography
Arvind Sundaram, Chin Kiang Tew, Guo Wei Tan, Hongyu Li, Nandini Venkataraman, Yuan-Hsiang Fu, Chandra Rao BheSetti, Navab Singh – Institute of Microelectronics A*STAR

4. 11:15 AM – Recent Progress in the Development of High-Density TSV for 3-Layers CMOS Image Sensors
Stephan Borel, Myriam Assous, Stephane Moreau, Patrick McCluskey – University of Maryland; Email: mcclusky@umd.edu

5. 11:35 AM – The Advantages of Low Temperature (<400 °C) Carbon Nano-Tubes (CNTs) as Through Silicon Vias (TSVs) in Multi-Layers Stacking and Backside Power-Up Via Applications
Nilabh Basu, H.-Y. Lin, T.-W. Chen, Y.-C. Chan, Y.-T. Tsai, H.-C. Guo, T.-H. Wu, P.-C. Lin, Y.-C. Lin, Ming-Han Liao – National Taiwan University

6. 11:55 AM – A Precise Wafer Thinning Integration Flow for Nano-TSV Formation
Ya-Ching Tseng, Nandini Venkataraman, King Jen Chui – Institute of Microelectronics A*STAR

7. 12:15 PM – Next Generation Infrared (IR) Laser Debonding / Silicon Handle Technology for Precision Chiplet Technology Applications
Qianwen Chen, Michael Belyansky, Yasir Sulehria, Akhiro Horibe, Eric Perfecto, Katsuyuki Sakuma – IBM Corporation; Email: mcclusky@umd.edu

Session 29: AI-based Prediction for Heterogeneous Integration and Advanced Packaging
Committee: Thermal/Mechanical Simulation & Characterization
Session Co-Chairs: Patrick McCluskey – University of Maryland; Email: mcclusky@umd.edu
Rui Chen, Georgia Institute of Technology; Email: chenru@gatech.edu

1. 9:30 AM – Feasibility Investigation of Machine Learning for Electronic Reliability Analysis Using FEA
Robert David Johannes Hoehne, Yichen Qi, Oliver Albrecht, Karsten Meier, Karlheinz Bock – TU Dresden

2. 9:50 AM – NAND Package Warpage Prediction and Design With Tolerance Through Machine Learning
Yuhang Yang, Chaolun Zheng, Min Lin – Western Digital Technologies, Inc.; Tim Huang, Hedian Zhang, Ning Ye, Bo Yang – Western Digital Corporation

3. 10:10 AM – Reduced-Order Models of Digital Twin Applications for Design Platform of Flexible Hybrid Electronics
Chang-Chung Lee – National Tsing Hua University; Jui-Chang Chuang, Chen-Tsai Yang, Chung-Li Lin – Industrial Technology Research Institute

4. 11:15 AM – Methodology of Artificial Intelligence Aided Hybrid Modeling on Solder Joint Reliability Study of BGA Package
Sang Ju, Taek-Soo Kim – Korea Advanced Institute of Science and Technology; Sung Woo Ma, Jin Hee Lee, Woong-Sun Lee – SK Hynix, Inc.

5. 11:35 AM – Effect of Li-ion Battery Form Factor on the SoH Degradation Under Randomized Charge-Discharge Cycles and C-Rates
Pradeep Lall, Ved Soni – Auburn University

Jihoon Hong, Junjie Wang, Min Su Kim, Jaewon Lee – Korea University of Science and Technology; Sung Hoon Jang, Taek-Soo Kim – Korea Advanced Institute of Science and Technology

7. 12:15 PM – Thermal Characterization of 3-D Stacked Heterogeneous Integration (HI) Package for High-Power Computing Applications
Akakri Jain, Sathyachughavan, Prabudhya Roy Chowdhury, Mukta Ghate Farooq, Arvind Kumar, Katsuyuki Sakuma – IBM Research; Risa Miyazawa – IBM Research, Tokyo

Session 30: Trends in Encapsulants and Low Dk/Df Dielectrics
Committee: Materials & Processing
Session Co-Chairs: Tanja Braun – Fraunhofer IZM; Email: tanja.braun@izm.fraunhofer.de
Kimberly Yess – Brewer Science, Inc.; Email: kyess@brewer.com

1. 9:30 AM – Liquid Compression Mold Underfill Optimization With Low Warpage and Narrow Gap Flow
Tsyuoshi Kamimura, Shinichi Sato, Yugo Shigeno – NAMICS Corporation; Brian Schmaltz – NAMICS Technologies, Inc.

2. 9:50 AM – Effect of High-Temperature Exposure on the Thermo-Mechanical Behavior of Epoxy Molding Compound and Warpage of Molded Wafers
Junmo Kim, Myoung Song, Chang-Yeon Gu, Min Sang Ju, Taek-Soo Kim – Korea Advanced Institute of Science and Technology; Sung Woo Ma, Jin Hee Lee, Woong-Sun Lee – SK Hynix, Inc.

3. 10:10 AM – Low Temperature Fine Pitch All-Copper Interconnects Combining Photopatterning Underfill Films
Xunji Ji, Herk Van Zeijl, Weiping Jiao, Shan He, Leiming Du, Guoqi Zhang – Delft University of Technology

4. 11:15 AM – Novel Low Dk/Df Photoimageable Dielectric for Redistribution Layer
Guillermo Fernandez Zapico, Fumihiko Kawauchi, Shinya Kawaiishi, Manabu Hirasawa, Kitaru Sato, Tetsuya Imai, Hidekazu Kondo, Tatsuya Makino – Resonac Corporation

5. 11:35 AM – Novel Photo-Definable Low Dk & Df Polyimide for Advanced Package of High Frequency Application
Hitoshi Araki, Akira Shimada, Hisashi Ogawa, Masuya Ijaki, Masao Tomikawa – Toray Industries, Inc.

6. 11:55 AM – Novel Low Dk/Df Film for High Frequency Substrate and RDL
Mette Koh, Kazuyoshi Yoneda, Kazutaka Nakada, Yoshitomo Aoyama, Kazumi Hashimoto, Kota Oki – Taiyo Ink Mfg. Co., Ltd.
<table>
<thead>
<tr>
<th>Program Sessions: Friday, June 2, 2:00 p.m. - 5:05 p.m.</th>
</tr>
</thead>
</table>

### Session Co-Chairs:
- Young-Gon Kim
- Renesas Electronics America
- Email: young.kim.jp@renesas.com
- Deepak Goyal
- Intel Corporation
- Email: deepak.goyal@intel.com

### Session Co-Chairs:
- Pradeep Lall
- Auburn University
- Email: lall@auburn.edu
- Tieyu Zheng
- Microsoft Corporation
- Email: tzzheng@microsoft.com

### Session Co-Chairs:
- Takafumi Fukushima
- Tohoku University
- Email: fukushima@bics.mech.tohoku.ac.jp
- Bernd Ebersberger
- Infineon Technologies AG
- Email: bernd.ebersberger@infineon.com

### Session 1:
1. **2:00 PM – Enabling Backside Processing for Perforated Microfluidic Devices**
   - Jakob Viker, Yang Han, Evert Visker, Chi Ding Thi Thuy, Mateusz Gocyla, Jan Adkaert, Aurelie Humbert, Serge Vanhaelee, Peng – imec

2. **2:20 PM – Wafer Level Chip Scale Package Technology Applied to MEMS Pressure Sensor**
   - Luca Maggi, Marco Del Sarto, Tiziano Chiariello, Enri Duqi, Lorenzo Baldo, Adriano Abbisogni – STMicroelectronics

3. **3:40 PM – A Novel FOWLP Method to Integrate Delicate MEMS Components**
   - Markus Woehrmann, Tanja Braun, Michael Schiffer, Martin Schneider-Ramelow – Fraunhofer IZM; Marc Dreissigacker – Technical University Berlin

4. **4:05 PM – On the Path to AI Hardware**
   - Griselda Bonilla – IBM Research; Brian Quinlan, Tom Wassick, Russell Kastberg, Shidong Li, Monali Basutkar

   - Cheng-Chao Wang, Chih-Yi Huang, Chih-Pin Hung, Ching-Hung Lai, Hsing-Hsien Huang, Hung-Chun Kuo, Ming-Fong Jhong, Fu-Chen Chu – Advanced Semiconductor Engineering, Inc.

### Session 2:
1. **2:00 PM – Mechanical Simulation and Characterization on Flexural Fracture of Stacked Die Memory Package**
   - Yangming Liu, Ning Ye, Bo Yang, Qi Zhang, Wei Wang, Xu Wang – Western Digital Corporation

2. **2:20 PM – Simulation of Device Structure Impacts on Bonding Wave and Strain in Wafer to Wafer Cu-Cu Hybrid Bonding**
   - Takaaki Hirano, Taichi Yamada, Shoji Kobayashi, Yoshiya Hagimoto, Hayato Iwamoto – Sony Semiconductor Solutions Corporation

   - Ran Tao, Aaron M. Forster – National Institute of Standards and Technology; Sukrut Prashant Phansalkar, Saskia Gesche Huber, Andreas Stegmaier, Marius van Dijk, Nina Nguyen, Ole Hoelck, Olaf Wittler, Martin Schneider-Ramelow – Fraunhofer IZM

4. **4:05 PM – Development of a Plasma Etching Process of Copper for the Microfabrication of High-Density Interconnects in Advanced Packaging**
   - Juliano Borges, Maxime Daron, Yann Belliard, Serge Ecoffey, Dominique Drouin – University of Sherbrooke; Isabel De Sousa – IBM Canada, Ltd.

5. **4:25 PM – On the Path to AI Hardware Via Chiplet Integration Enabled by High Density Organic Substrates**
   - Griselda Bonilla – IBM Research; Brian Quinlan, Tom Wassick, Russell Kastberg, Shidong Li, Monali Basutkar – IBM Systems

### Session 3:
1. **2:00 PM – Enhancement of Thermal Performance and Characterization of the solder interconnection for Terabit/s Transceivers Based on High-Speed TSVs**
   - Bogdan Srub, Kai Zoschke, Tolga Tekin – Fraunhofer IZM; Ukyo Suzuki, Quentin Wilmart – CEA-Leti

2. **2:20 PM – Creative Design and Structure Applied to Chiplets Packaging**
   - Chen-Chao Wang, Chih-Yi Huang, Chih-Pin Hung, Ching-Hung Lai, Hsing-Hsien Huang, Hung-Chun Kuo, Ming-Fong Jhong, Fu-Chen Chu – Advanced Semiconductor Engineering, Inc.

3. **3:40 PM – Increase of Interconnect Density on Organic Substrates**
   - Yangming Liu, Ning Ye, Bo Yang, Qi Zhang, Wei Wang, Xu Wang – Western Digital Corporation

4. **4:05 PM – Development of High Reliability 5-µm-pitch Cu-Cu Connections Using Over-400 mm²-Large Chip on Wafer Bonding Process**
   - Takahiro Kamei, Hirotaka Yoshioka, Tatsunasa Hiratsuka, Akhisa Sakamoto, Kan Shimizu, Hayato Iwamoto – Sony Semiconductor Solutions Corporation

5. **4:25 PM – On the Path to AI Hardware**
   - Griselda Bonilla – IBM Research; Brian Quinlan, Tom Wassick, Russell Kastberg, Shidong Li, Monali Basutkar – IBM Systems

### Session 4:
1. **2:00 PM – Improving Warpage of Large Wafers in Fan-Out Packaging Technology**
   - Saska Gesche Huber, Andreas Stegmaier, Marius van Dijk, Nina Nguyen, Ole Hoelck, Olaf Wittler, Martin Schneider-Ramelow – Fraunhofer IZM


3. **3:40 PM – Ultra-Fine Pitch RDL (UFPRDL) Using Polymer Dual Damascene Processing**
   - Nelson Pinho, Emmanuel Chery, Nicolas Pantano, John Stappaker, Andy Miller, Eric Beune – imec

4. **4:05 PM – A Comprehensive Study of Solder Joint Reliability Dependent on Temperature Cycling Profiles and Material Selections With Emphasis on an Improved Solder Fatigue Lifetime Model**

5. **4:25 PM – On the Path to AI Hardware Via Chiplet Integration Enabled by High Density Organic Substrates**
   - Griselda Bonilla – IBM Research; Brian Quinlan, Tom Wassick, Russell Kastberg, Shidong Li, Monali Basutkar – IBM Systems

### Session 5:
1. **2:00 PM – Simulation-Assisted Board Level Solder Joint Reliability Optimization for Large 80 mm²-2.5D Devices**
   - Omar Ahmed, Lefi Hutchinson, Peng Su, Bernard Glaser – Juniper Networks; Vishnu Shukla, Chengfei Jiang – University of Central Florida

2. **2:20 PM – Development of a Plasma Etching Process of Copper for the Microfabrication of High-Density Interconnects in Advanced Packaging**
   - Juliano Borges, Maxime Daron, Yann Belliard, Serge Ecoffey, Dominique Drouin – University of Sherbrooke; Isabel De Sousa – IBM Canada, Ltd.


### Refreshment Break: 3:00 p.m. - 3:45 p.m.

### Session Co-Chairs:
- Pradeep Lall
- Auburn University
- Email: lall@auburn.edu
- Tieyu Zheng
- Microsoft Corporation
- Email: tzzheng@microsoft.com

### Session Co-Chairs:
- Takafumi Fukushima
- Tohoku University
- Email: fukushima@bics.mech.tohoku.ac.jp
- Bernd Ebersberger
- Infineon Technologies AG
- Email: bernd.ebersberger@infineon.com

### Session Co-Chairs:
- Young-Gon Kim
- Renesas Electronics America
- Email: young.kim.jp@renesas.com
- Deepak Goyal
- Intel Corporation
- Email: deepak.goyal@intel.com

### Committees:
- Packaging Technologies and Applied Reliability
- Thermal/Mechanical Simulation & Characterization
- Interconnections

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## Program Sessions: Friday, June 2, 2:00 p.m. - 5:05 p.m.

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<th>Session 35: Packaging and Materials for Flexible Medical Technologies</th>
<th>Session 36: RF, Heterogeneous, and Chiplet Modules</th>
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<tr>
<td><strong>Committee:</strong> Assembly and Manufacturing Technology</td>
<td><strong>Committee:</strong> Emerging Technologies</td>
<td><strong>Committee:</strong> RF, High-Speed Components &amp; Systems</td>
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</table>

| Session Co-Chairs: | Session Co-Chairs: | Session Co-Chairs: |
| Jason Rouse | Zia Karim | Email: dhe@qti.qualcomm.com |
| Taio America, Inc. | Yield Engineering Systems | Qualcomm Technologies, Inc. |
| Email: jhrouse@taio-america.com | Email: zkarin@yieldengineering.com | Email: dhe@qti.qualcomm.com |

### 1. 2:00 PM – Laser-Assisted Bonding With Compression (LABC) Based Tiling Bonding Process, Enabling Technology for Chiplet Integration
Kwang-Seong Choi, Jiho Joo, Gwang-Mun Choi, Channri Lee, Ho-Gyeong Yun, Seok Hwan Moon, Ki-Seok Jang, Jin-Hyuk Moon, Yoon-Hwan Moon, Yong-Sung Eom – Electronics Telecommunications Research Institute

### 1. 2:00 PM – Fully Portable Wireless Soft Stethoscope and Machine Learning for Continuous Real-Time Auscultation and Automated Disease Detection
Sung Hoon Lee, Yun-Saung Kim, Woon-Hong Yeo – Georgia Institute of Technology

### 1. 2:00 PM – Heterogeneous Radio Chiplet Module for 5G Millimeter Wave Application
Ayageta Ljungbro, Emil Nylander, Martin Hansson – Ericsson AB; Marcel Wieland, Selaka Bulumulta – GlobalFoundries, Inc.

### 2. 2:30 PM – Contamination-Free Cu/ SiCN Hybrid Bonding Process Development for Sub-µm Pitch Devices With Enhanced Bonding Characteristics

### 2. 2:20 PM – Patch-Type Flex SiP Platform for Healthcare Application
Ming-Hung Chen, Wei-Hao Chang, Hui-Ping Jian, Chao-Wei Liu, Shang-Lin Wu, Yi-Chun Chou, Sung-Hung Chiang, Jung-Kai Chang, Tun-Ching Pi, Wei-Chun Lee, Jen-Chieh Kao, Yung-Ih Yeh – ASE Corporate R&D Center

### 2. 2:20 PM – Design and Analysis of 3D Heterogeneous Chiplet Stack for RF Front-End Module Miniaturization
Mihai Rotaru, Chai Tai Chong, Chui King Jen – Institute of Microelectronics A*STAR; Shashank Tiwari – GlobalFoundries, Inc.; Paul Castillou – Qorvo, Inc.

### 3. 2:40 PM – Integration and Process Challenges of Self-Assembly Applied to Die-to-Wafer Hybrid Bonding
Emilie Bourjot, Alice Bond, Noura Nadi, Thierry Enot, Loïc Sanchez, Pierre Mortmert, Benoît Martin, Alain Campe, Frank Fourrel – CEA-Leti; Feras Eid, Johanna Swan – Intel Corporation

### 3. 2:40 PM – Development of PMUT Array Packaging from Characterisation Prototypes to Customer Samples
Mark Andrew Shaw, Domenico Castr, Fabio Quaglia, Alex Gritti – STMicroelectronics; Gerald Mug, Mitsui Haelino – DISCO Hitac Europe; Venatet Srinivesa Ruo, Dutta Rahul, Devdutt Ho Soon Wiese – Institute of Microelectronics A*STAR; Heiyoaki Sandori, Masatoki Wakahara – DISCO Corporation; Alessandro Savio – Roma Tre University

### 3. 2:40 PM – Embedded mm-Wave Chiplet Based Module Using Fused-Silica Stitch-Chip Technology: RF Characterization and Thermal Evaluation
Ting Zheng, Madison Manley, Muhammad S. Bakir – Georgia Institute of Technology

### Refreshment Break: 3:00 p.m. - 3:45 p.m.

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<tr>
<th>5. 4:05 PM – A Study of SiCN Wafer-to-Wafer Bonding and Impact of Wafer Warpage</th>
<th>5. 4:05 PM – Electrospray Printing of Polymeric and Metallic Coatings for Electronics Packaging</th>
<th>5. 4:05 PM – Amplified and Filtered x2 Multiplier Chip</th>
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<tr>
<td>Serenai Iacovu, Oguzhan Orkut Okudur, Koen D’Havie, Johan Meerschaut, Liesbeth Witters, Thierry Conard, Alain Phommahaxay, Mark Andrew Shaw, Domenico Castr, Fabio Quaglia, Alex Gritti – STMicroelectronics; Gerald Mug, Mitsui Haelino – DISCO Hitac Europe; Venatet Srinivesa Ruo, Dutta Rahul, Devdutt Ho Soon Wiese – Institute of Microelectronics A*STAR; Heiyoaki Sandori, Masatoki Wakahara – DISCO Corporation; Alessandro Savio – Roma Tre University</td>
<td>Emma Pawliczak, Bryce Kingsley, Paul Chiarot – Bingham University</td>
<td>Elizabeth Kunkee, Dah-Welh Duan, Ricardo Medina, Nancy Lin, R. Yogi, Chunbo Zhang, Robert Mendoza, Kevin Leong, Alex Zamora, Scott Sing, David Miller – Northrop Grumman Corp.</td>
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<tr>
<th>7. 4:45 PM – Impact of Thermal Annealing and Other Process Parameters on Hybrid Bonding Performance for 3D Advanced Assembly Technology</th>
<th>7. 4:45 PM – Performance Evaluation of RF Novel Microstrip Lines Printed on Flexible Substrates</th>
<th>7. 4:45 PM – 3D MIM Ultra-Small Silicon Capacitor Design for High Capacitance Density With Extremely Low ESR and ESL</th>
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</table>
Interactive Presentations: Wednesday, May 31, 10:00 a.m. - 12:00 Noon and Wednesday, May 31, 2:30 p.m. - 4:30 p.m.

**Wednesday May 31, 2023, 10:00 a.m. – 12:00 Noon**

Session 3: Interactive Presentations 1

**Committee: Interactive Presentations**

**Session Co-Chairs:** Mark Politis – Binghamton University

Email: mpolitis@binghamton.edu

Pradeep Lall – Auburn University

Email: lall@auburn.edu

**Kristina Young – GlobalFoundries, Inc.**

Email: kristina.youngfisher@gmail.com

**Jae Kyu Cho – GlobalFoundries, Inc.**

Email: jaekyu.cho@globalfoundries.com

1. Signal Integrity of 2-µm-Pitch RDL Interposer for High-Performance Signal Processing in Chiplet-Based System

Takamasa Takano, Hiroshi Kudo, Masaya Tanaka, Satoru Kuramochi – Dai Nippon Printing Co., Ltd.; Tomoya Sasawaga – DNP America, LLC

2. Investigation of Cu-to-Cu and Oxide-to-Oxide Bonding

Sangmin Lee, Gwangok Oh, Junyoung Choi, Yoonho Kim, Sangwoo Park, Sarah Kim – Seoul National University of Science and Technology

3. Doping-Selective Etching of Silicon for Wafer Thinning in the Fabrication of Backside-Illuminated Stacked CMOS Image Sensors


4. Study of Solder Resist Crack Resistance for Flip Chip Ball Grid Array Substrate


5. Reliability Analysis on Ag and Cu Nanoparticles Sintered Discrete Power Device With Various Frontside and Backside Interconnect

Dong Hu, Yu Li, Stan Velkeleng, Jiaji Fan, Guozhi Zhang – Shenzhen University of Technology; Ali Roshanghias – Silicon Austria Labs Corporation; Yukinori Oda – C. Uyemura & Co., Ltd.

6. Wafer Level Batch Fabrication of an MRI Compatible Neural Probe With Electrical, Optical, and Microfluidic Functions

Ziq Jia, Shuyi Shi, YongKyo Yoon – University of Florida

7. High Reliability Design of Ag Sinter Joining on a Softened Crackless Ni-P/Pd Metallization AMB Substrate During Aging and Harsh Thermal Cycling

Chuantong Chen, Yang Liu, Hupeng Huo, Kazutoshi Suganuma – Osaka University; Minoru Fukuda, Masahiro Kanbayashi, Toshimasa Shimoda, Isao Shiomi, Shinya Sakamoto, Kishou Takahata, Tomohiro Chiba, Atsushi Kamashita, Masashi Okada, Masanori Aramata, Takashi Shinoda, Ken-Ichiro Mori – Canon, Inc.; Douglas Shelton – Canon Manufacturing Company, Ltd.

8. Process Parameters on Vacuum Fluxless Solder Reflow Performance in Backend Applications With Bump Pitch of 15 µm and Below

Le Jingt, Vladimir Kuznetsova, Taylor Nguyen, Jed Hsu, Tapani Laaksonen, Alvin Lin, Xinuan Tan, Kay Song, Alex Chow, Chris Lane, Zia Karim – Yield Engineering Systems

9. Reliability Performance Study of Molding Compounds on High Voltage Molded Loaded Package

April Joyce Garete, Zhemin Li, Yee Wai Fung, Pe Po Wang – GlobalFoundries

10. Characterization and Modeling of 2 and 1.5-µm Line-and-Space High-Density Signal Wiring on Organic Interposer

Atom Watanabe, Hiroyuki Mori, Xiaowei Gu, Frank Luach, Gristelda Borilia – IBM Corporation

11. 6-Sided Die Protection for Chiplet Package With Multi-Layer RDL

ByungCheol Kim, Mary Pyelego, Rui Gachio, Jacinta Amor Lin, Hye Yeoul You, Kwan Sun Oh – Cypress Corporation; Clifford Sandstrom, Benedikt San Jose – Desa Technologies, Inc.

28. SIC Power Module Packaging and Interconnection Using Flexible Hybrid Electronics Materials and Processes

Rashid AH-Haidar, Mohanned Ahend, Dylan Richardson, El Mehdi Ablbara, Abdullah Obesat, Mark Politis, Mark Schadt – Binghamton University; Arun Gawda, Jeffrey Erbbaum, Han Xiong, Colin Hinchlack – GE Research


Joon Woo Kim, Xinghe Li, Xiaoxi Jia, Kyoung-Sik Moon, Madhavan Swaminathan – Georgia Institute of Technology

30. Demonstration of TSV- less Efficient and Cost-Effective Power Delivery for Large Interposers and Wafer-Scale Systems

Haoxian Ren, Subramanian S. Iyer – University of California, Los Angeles

31. Metal Additively Microfabricated SIPs With Embedded Microfluidic Cooling Toward Heterogeneous Integration With SoCs

Bhushan Lohani, Sheik Dobir Hossain, Robert C. Roberts – University of Texas, El Paso

**Wednesday May 31, 2023, 2:30 p.m. – 4:30 p.m.**

Session 3B: Interactive Presentations 2

**Committee: Interactive Presentations**

**Session Co-Chairs:** Rao Bonda – Amkor Technology, Inc.

Email: rao.bonda@amkor.com

Mohammad Enamul Kabir – Intel Corporation

Email: enamul101b@yahoo.com

Saklat Mandal – Intel Corporation

Email: saklat.mandal@intel.com

Donna M. Noctor – Nokia Corporation

Email: donna.noctor@nokia.com

1. Advanced Overlay Metrology for CIS Bonding Applications

Florett Dettoni, Emilie DELOFRE – STMicroelectronics; Yoav Grazer, Shlomo Eisenbach, Moti Persia, Arka Simkin, Dhir Bhai, Ainer Safrani, Marco Polli, Francesco De Paola – KLA Corporation

2. Implementation of New Robustness Assessment Methodology for Crack Stop Constructions by Using Dedicated Binning in Automated Optical Inspection

Maria Hedenstedt, Michael Gorlin – Infinetix Technologies AG

3. Comparable Study for Redistribution Layers in FO POP RDL First and Last (Fan-Out Package on Package)

Kuei Hsiao Ku, Derrick Tai, Sam Peng, Feng Lung Chien – SPLL

4. Hybrid Bonding Utilizing Molding Compound and Dielectric Systems

Yuki Inoue, Kazuyuki Mitsukura – Resonac Corporation

5. A Short Time and N2-sinterable Cu Sinter Paste With Highly Dispersed Submicron Cu Particles

Takashi Eymai, Shinya Iwaya, Ukyo Suzuki, Masaki Takeda – Kao Corporation


Jing-Hua Huang, Po-Siao Shih, Chang-Hsien Sheng, Yung-Luann Renganathan, Simon Johannes Graefner, Yu-Chin Lin, C. Robert Kao – National Taiwan University; Chin-Li Kao, Young-Sheng Lin, Yu-Ching Hung, Chun-Wei Chiang – Advanced Semiconductor Engineering Institute

7. 50 nm Overlay Accuracy for Wafer-to-Wafer Bonding by High-Precision Alignment Technologies

Hajime Mitsuishi, Hiroshi Mori, Hidehito Maeda, Miko Ushijima, Atsushi Kamatani, Masashi Okada, Masanori Aramata, Takashi Shiono, Shinya Sakamoto, Kiyoh Tsuchida, Tomohiro Chiba, Minoru Fukuda, Masahiro Kanbayashi, Tetsuya Shinoda, Isao Sugaya – Nikon Corporation
28

8. Multi-Stack Hybrid Cu Bonding Technology Development Using Ultra-Thin Chips
Mi-Ki Kim, Hyunsoo Lee, Jeong Jun, Seunguk Bask, Ewhan Kim, Youngjin Jee, Hyun-Chul Jung, Un-Byoung Kang, Daesoo Kim – Samsung Electronics Co., Ltd.-Test and System Package

9. An Investigation on Particle Embedding Capability of Wafer Level Spin-on Polymer Underfill Enabling Low Temperature Bonding of Hybrid Bonding System
Hiroto Nakao, Naoaki Nakajima – JJI Garnet; Jaber Derakhshandeh, John Sableboom, Eric Beyne – imec


Yi Chen, Xiaoxia Zhou, Changli Luan – Loughborough University

12. Selective Self-Assembled Monolayer on Copper Surface Protection During Plasma Activation of Hybrid-Bonded Wafers
Jack Rogers – TEL Technology Center, America, LLC.

13. Development of a Heterogeneous Integration of GaN Power Device on Si-LSI
Shin Miseki, Yukiya Yokota, Ayane Fuse, Satoko Shinkai, Satoshi Matsumoto – Kyushu Institute of Technology

14. Seed Layer Etching, Thermal Relow and Bonding of Cu-Sn Micro Bumps With 5 µm Diameters
Yunfan Shi, Zhen Wang, Zheyao Wang – Tsinghua University

15. Integrated pH and Strain Sensors Development for Nanoscale Tissue Placement Application
Rui Su, Yu Chen, James Wei Yee Yap, Musafargani Sikkandhar, Jingping Qiao – Institute of Microelectronics A*STAR


17. Chip-to-Chip Hybrid Bonding with Larger-Oriented Cu Grains for µ-Joints Beyond 100 K
Meyongseok Planapap – GNTI, Tohoku University, Masahiro Sawa, Eiko Sone – JCU, Takamichi Miyazaki, Tadaharu Fukuma – Tohoku University, Mitsunari Kosayari – T-Micro

18. Application of Nickel Micro-Plating Bonding (NMPB) Technology to Crystalline Silicon Solar Cell Interconnection
Xingang Yu, Zhi Fu, Issamu Morisako, Kohei Koshita, Tomonori Iizuka, Kohei Tatsumi – Tohoku University

19. Embedded Microchannel Cooling System Based on Flexible Manifold for High-Performance Computing ICs
Je Wang, Yanni Kong, Binbin Liu, Ruiwen Liu, Yunyi Ye, Xiangbin Du, Liang Hua, Yun Shi, Shichang Yang, Dichen Liu, Ziyu Liu, Jingping Qiao – Institute of Microelectronics Chinese Academy of Sciences

20. CMOS-Compatible Fine Pitch Aluminum to Aluminum Bonding
Hemanth Kumar Chemalameili, Binu Varghese, Sharma Jabir, Hong Ou, B. S. S. Chandrasekhar, Navid Singh, Srivani Rao Vennapu, King Jin Chiu – Institute of Microelectronics A*STAR

Matthias Fettke, Anne fisch, Georg Friedrich, Masih Nassar, Thorsten Teutsch – Pac Tech GmbH

22. Board Level FEA Reliability and Stress Modeling for Chip-to-Wafer Bonded Chiplet Package
Ratit Harmandar, Qai Tsai-Chong – Institute of Microelectronics A*STAR

23. High Density VR Solution Using Immersion Cooling
Jesus G. Ruelas Flores, Arturo Sanchez Hernandez, Ernesto A Padilla Ramirez, Oscar A Del Rio Gonzalez, Carlos E Mora Flores, Andres Ramirez Masc – Intel Corporation

24. Demonstration of Eight Metal Layer Redistribution on Glass Substrate With Fine Features and Microvias
Christopher Blancker, Mohanalingam Kathaperumal, Fuhai Liu, Madhavan Swaminathan – Georgia Institute of Technology

Thomas Luehrmann, Peter Urban, Boris Povazay, Michael Josef Gruber, Julian Bravin, Daniel Burgstaller, Markus Wimpflinger, Bernd Thaller – EV Group, Inc.

26. Robust Edge Coupling Probe Applied in Wafer-Level Optical Testing
Sheng-Ho Huang, Chen-Yu Lin, Yi-Kang Fu – Industrial Technology Research Institute; Mei-Ju Lu, Shy-Yuan Mu, Chi-Sheng Lin, Jian-Chen Chen – ASE Corporate R&D Center

27. An Intensive Study of Effects of Orientations of Single Crystal Cu Bumps on Cu Direct Bonding for 3D Integration by Molecular Dynamics Simulation
Deng Wu, Min-Bo Zhou, Shui Liu, Chang Bo Ke, Xin-Ping Zhang – South China University of Technology

28. Reconstituted-SiO2, Tier With Integrated Copper Heat Spreader
Ashita Victor, Madison Marley, Shane Oh, Muhammad S Bakir – Georgia Institute of Technology

29. Reflow Oven Zone Temperature Advisor Using the AI-Driven Smart Recipe Generator
Yanggang Li, Junbo Yang, Ji-Hwan Ha, Pengying Yin, Kartik A. Desai, Seungbee Park – Binghamton University

Kartik Arun Deo, Seungbae Park, Liiho Yang, Ji-Hwan Ha, Pengying Yin, Seungbee Park – Binghamton University

31. A Novel Polymer-Based Ultra-High-Density Bonding Interconnection
Yu-Min Lin, Tsung-Yu Ou, Yang-Hung Lee, Ching-Kuan Lee, Wei-Lun Chiu, Tao-Chih Chang, Hsang-Hung Chang – Industrial Technology Research Institute; Michael Gallagher, Po-Yao Chuang, Po-Hao Tsai, Po-Chun Huang – DuPont Electronics and Industrial Technologies Chang-Chun Lee – National Taiwan Hua University

32. Comparison of Sintering Methodologies for 3D Printed High-Density Interconnects (2.3 µm I/S) on Organic Substrates for High-Performance Computing Applications
Shrivani Pandiya, Sergio Escofet, Yann Beillard, Dominique Drouin – University of Sherbrooke; Christophe Sansregret – Centre de Collaboration Micro-Plasmation (C2MP); Isabel De Sousa – IBM Canada, Ltd.

33. Formation and 3D Stacking Process of CMOS Chips With Backside Buried Metallic Power Distribution Networks
Naoya Watanabe, Yuuki Araga, Haruo Shimamoto, Katsuya Kitoh – National Institute of Advanced Industrial Science and Technology; Makoto Nagata – Kobe University

34. Cu Pillar With Nanoporous Copper Cap: A Step Towards Chip-to-Substrate Hybrid Bonding
Ramón A. Sosa, Vanessa Smet, Antonia Antonucci – Georgia Institute of Technology

Thursday June 1, 2023, 10:00 a.m. – 12:00 Noon

Session 39: Interactive Presentations 3

Committee: Interactive Presentations
Session Co-Chairs: Patrick Thompson – Texas Instruments, Inc.
Email: patrick.thompson@ti.com
Amarnar Kaur – Oakland University
Email: kaur4@oakland.edu
Frank Libsch – IBM Corporation
Email: libsch@us.ibm.com
Yoichi Taira – Keio University
Email: taira@appi.keio.ac.jp

1. Voltage Controlled Nanoscale Magnetic Devices For Non Volatile Memory and Scalable Quantum Computing
Jayarama Sasivaram, Md. Majid Rajh – Virginia Commonwealth University

2. Polymer Optical Waveguide Type 3-D MUX Device for Mode Division Multiplexing Links
Ryoto Ichinose, Tatsuni Kowata, Takashi Ishigaki – Kao University

3. Extracting Anisotropic Permeability of PCB Substrate From VNA Measurement on a Rectangular Stripline Resonator Loaded With A Wire Array
Zhaoxing Chen, Hung Nguyen, Matteo Cocchi – IBM Corporation

4. Silicon Photonic Co-Packaging: Adhesive Dispense Challenge and Control

5. Design of Single Miniaturized Dielectric Resonant Antenna for Millimeter Wave 5G Application
Chi-Chu Li, Sam Lin, Tery Shih, Yu-Po Wang, Tom Tang, Mike Tsai, Rani Chiu, Kevin Chang, Yu-Chang Dong – Sincorwave Precision Industries Co., Ltd.

6. Inverse Prediction of Capacitor Multiphysics Dynamic Parameters Using Gerative Model
Kart Leong Lim, Rahul Dutta, Mihai Rotaru – Institute of Microelectronics A*STAR

7. New Interconnection Technologies Based on Ni-Nano-Particle and Ni-Micro-Particle Bonding Method
Kohei Tatsuti, Kohei Koshita, Yasunori Takeda, Moya Miyagawa, Xinguan Yu, Shun Furuya, Tomonori Iizuka – Waseda University

8. High-Performance Amplifier Package Design for Heterogeneous Integration on Si-Interposer
Teck Guan Lin, Lim Zhao, Haoran Chen, Eva Leong Ching, Wei Sui, Kumar Tippabhotla, Lin Ji, Gongue Ting – Institute of Microelectronics A*STAR; Wei Je, Chee Heng Goh, Jun Wei Agnes Loh – DSO National Laboratories

Jeouan Yu, Qian Wang, Yao Zhang, Changming Song, Junpeng Fang, Zeyong Wang, Jian Cai – Tsinghua University; Tiefu Liu, Tiangang University/Beijing Academy of Quantum Information Sciences; Hualiu Wu – Beijing Academy of Quantum Information Sciences

10. Additive Manufacturing of Millimeter Wave Passive Circuits on Ultra-Thin Alumina Substrates
Ethan Kaspor, Yiang Chu, Bhragav Aivini, Brian Wright, Premjeet Chahal – Michigan State University

11. Frequency Selective Surface (FSS) Based Antenna Array Design for Satellites Capable of All Four Polarizations
Lih-Ting Hwang, Ming-Yuan Huang, Hsing-Chih Lin – National Sun Yat-Sen University

12. Novel Low-Loss IC Substrate Material for 5G IC Packaging
Tomio Muguruma, Andy Behr, Tom Shi – Panasonic Industrial Devices Sales Company of America; Umehara Hiroaki, Sachi Yuasa, Kishiro Kaji – Panasonic Industry Co., Ltd.

13. Deep Learning Based Refinement for Package Substrate Routing
Peng-Tai Huang, Tsuabasu Koyama, Tsung-Yi Ho – National Tsing Hua University; Keng-Tuan Chang, Chih-Yi Huang, Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.

14. Laser Integration on Photonic Integrated Circuit With High Alignment Accuracy for Data Transmission

15. Copper Nanowire Interconnection for Additive Manufacturing Dies in PCB
Cao Cesar De Oliveira, Julian Morland, Guillaume Lefevre – Mitsubishi Electric R&D Centre Europe; Vincent Bley, Jean-Pascal Gruber, Julian Bravin, Daniel Burgstaller, Eric Turcotte, Steve Whitehead, Elaine Cyr – IBM Corporation

16. High Density Photonic Reservoir Computing Using Optical Fiber and Polymer Waveguide
Hideshito Numata, Toshiki Yamane, Daiji Nakano – IBM Research, TokyoIBM Corp., Japan; Jean Heroux – IBM Systems/IBM Corp., Canada
interactive presentations: Thursday, June 1, 10:00 a.m. - 12:00 noon and 2:30 p.m. - 4:30 p.m.

17. machine learning based PCB/package stack-up optimisation for signal integrity
Wenchang Huang, Jiahuan Huang, Chutolu Huang, - Missouri University of Science and Technology; Mingyou Kim, Bumhee Bae, Sulin Kim, - Samsung Electronics Co., Ltd.

18. self-aligned optical connector assembly on polymer waveguide integrated package substrate for co-packaged optics
Akhiro Noriki, Takers Armani - National Institute of Advanced Industrial Science and Technology

19. solder paste stamping process investigation for heterogeneous integration of III-V lasers on a 300 mm Si Photonics Platform
Sarah Baranowski, Jevrey Mann, Lewis Carpenter, Amit Dilkhot, Colin McDonough, David Harame - SUNY Research Foundation

20. 2.5D silicon Photonics Interposer Flip Chip Attach Pushkarjit Tumne, Joseph Wang, Dwayne Shirley, Roberto Coccioleti - Marvell Semiconductor, Inc.

21. A study of the design and parameter effects on system level characteristics of advanced Fan-Out Wafer Level Package (FOWLp): results from in-situ analysis
Kyeong-Lim Suk, Jhiwong Kim, Suxiang Lin, Jiechao Lin, Myung Sung Kim, Won Young Choe, Dongwook Kim, Young Son, Cheolhoon Shin - Samsung Electronics Co., Ltd.

22. Development of Electronic-Photonic 3D System in Package: Architecture, Integration, and Scaling
Jagj Kihore Bhandari, Verikas Ramana Pandighram, Divya Sri Rajaswari, Robin Kumar Yudapati - LightSpeed Photonics Pvt Ltd

23. additive manufacturing of strain gauges for high temperature applications
Nicolas Delayse, Tanguy Lacondemine, Remy Kalmar, Manuel Fender - CEA Tech Grand Est, Sofiaene Achaich, Frederic Sandetche - UTT LAAMS

24. Highly Compact and High Gain 2 x 2 Patch Array Antenna With Slotted Meanderline Loading
Hanna Jing, Payman Pahlavan, Yong-Kyu Yoon - University of Florida

25. Highly energy efficient and electromagnetic interference immune coaxial through-substrate-vias (cx-TSVs) for Millimeter Wave Applications
Saegeun Jeon, Hae-In Kim, Yong-Kyu Yoon - University of Florida

26. Design of a compact Size-Bridge Connected Multibond MIMMO Antenna for automotive AG and DSRC Communications System
Mohammad Pervez, Amanpreet Kaur - Oakland University

27. A fully additive fabrication approach for creating small microvia with diameter < 10 μm suitable for 3D system-in-package integration
Raghiyeh Irani, Shalesh Chouhan, Jerker Deling - Luks University of Technology; Sarthak Acharya, Jasti Potluri, John Hagberg, Sami Myllylä, Olli Nousiainen, Hei Jartunen - University of Oulu

28. The performance and reliability of flexible screen-printed multilayer conductive leads for wearable vital sign monitoring devices
Karkkange Udornmanga, Behnam Garekani, Mohammed Ahrandi, Mark Poliks - Binghamton University; Danzhang Weierwase - University of Colorado; Matthew Minzer, Andrew Burns, Gurnvinder Khinda, Azar Abrash - GE Global Research

29. Demonstration of Compact, Leadframe-Based SiC Nibhanupudi, Meizhi Wang, Jaydeep Kulkarni – University of Sirish Oruganti, Nishant Gupta, Sai Subrahmanya Teja - Marvell Semiconductor, Inc.

30. First demonstration of die-embedded alumina Alhendi, Mark Poliks – Binghamton University; Darshana Wijewardena, Ravi Padmanabha Sastry - Florida University; Sarthak Acharya, Jussi Putaala, Juha Wilde – University of Freiburg

31. Simulation of Solder Crack Phenomenon in Molding Process
Tao Chien Chen, Shin Kun La, Zong Yuan Li, Yen Hua Kuo, Ming Shaw Shy, Hui Ching Liu, Lu Ming Lai, Kuang Hsien Chen - Advanced Semiconductor Engineering, Inc.

32. Automated Solder Joint Failure Mode Analysis Based on Dry and Pity Image Processing
Yin Lu, Chun-Sean Liu, Zhi Zhang Kao, Choukin Zheng, Bo Yang – Western Digital Corporation

33. Embedded Micro-pin Fin Heat Sink of Two-Phase Liquid Cooling for High Heat Flux 3D ICs
Hucheng Feng, Gengqiu Tang, Xiaozeng Zhang, Boon Long Lai, Ming-Ching Kang, Keng Yuan Jason Au, King Jern Chai – Institute of Microelectronics ASTAR, Jing Lou, Hongming Li, Dui Vinh Le – Institute of High Performance Computing ASTAR

34. Wearage Estimation of Panel-level Package from Panel to Strip by Using Multi-scaling Sub-modeling Technique
Chang Chuan Lee, Chi-Wei Wang, Che-Pei Jiang, Chih-Jang Chuang – National Tsing Hua University

35. A thermally friendly bonding scheme for 3D system integration

36. Effects of Boundary and Precipitates on Board Level Reliability in Sn-Ag-Gu (SAC) Solder Joints Under Ebsd Analysis
Daolin Yoon, Byoungsoo Lee, Jieyue Li, Sungho Hyun, Gyutee Lee, Kangwook Lee – SK Hynix Inc.

37. Optimization of 2.2D underfill process by novel methodology and direct observation of capillary underfill process
Chia-Peng Sun, Yu-Eting Liang – CoreTech System (Molded3D); Duy-Chung Hu, Eric-Hao Chen – SiKos Co., Ltd; Jeffrey Chang; Da Liu – IST-Integrated Service Technology, Inc; Shih-Yu Lo; Molded3D North America, Inc

38. Reliability in Selective Thinning Technology of Solder Resist for New IC Substrate Architecture

39. simulation, verification, and prediction of the corrosion behavior of Cu-Ag composite solder paste for power semiconductor die-attach applications
Xihye Wang, Zhongdong Yang, Pan Liu – Fudan University; Guoji Zhang – Dalian University of Technology; Jing Zhang – Huzhou Materials Technology Shanghai Ltd.

40. Thermal characterization and management of GAn-on-SiC high Power Amplifier MMC
Yang Han, Gengqiu Tang, Boon Long Lai – Institute of Microelectronics ASTAR

41. A thin-film reconfigurable Sic thermal Test Chip for Reliability Monitoring in harsh Environments
Ronina Sattari, Henk van Zall, Guo Zhang – Dalian University of Technology

42. Life-Prediction of SAC305/Bi-Based Hybrid Solder Joints Considering Bi-Diffused Layers With Gradual Bi Concentrations
Yangrue Jang, Boqian Han – University of Maryland; Hakt-Sung Kim – Hanyang University

Wen Chen, Xuan Yang, Jie Yang – Fudan University; Pasin S. Ibrahim – Hong Kong Polytechnic University; Jing Jang – Sky Chip Interconnection Technology Co. Ltd; Xuejun Fan – Lamar University; Guoziang Zhong – Dalian University of Technology

14. Out of plane stress control via design of Experiment and Machine Learning
Ziq Jia, Shuyi Shi, Yang-Kyu Yoon – University of Florida

15. Mold Flow Simulation on Wire Sweep for Two-Stack NAND BGA Package
Hanguo Yu, Yangming Liu, Shenghua Huang, Bo Yang, Ning Ye – Western Digital Corporation

Quang-Duc Pham, Norbert Holle – Robert Bosch GmbH; Juergen Wilde – University of Freiburg

17. Optimization of the Cu Microstructure to Improve Cu-to-Cu Direct Bonding for 3D Integration
Ralf Schmidt, Christian Schate – Atotech (MKS Instruments)

18. Addressing Sub-Micron Thermal Warpage: Industrial Application
Safis Benkoula – STMicroelectronics; Rodolfo Cruz, Pierre Verron – NXP

Yangbin Zhang, Fangyi Wei, Rui Guo, Xiaofeng Li, Dan Liu, Yongfeng He – Alibaba Group; Hailong Gang – Intel Corporation

20. Effect of Ceramic filler in epoxy Mold Compound on Thermomechanical Property of FOwLP
Taspoon Nibh, Hakan Jeon, Seung-boo Jung – Sungkyunkwan University

21. ARTSim: A Robust Thermal Simulator for Heterogeneous Integration Platforms
Yousef Sabri, Adam Corbier, Dima Al Saeed, Boris Vaidyan – McGill University

22. Atomic simulation study of plasma surface activation in wafer-to-wafer Oxide Fusion Bonding
Hojin Kim, Yu-Hao Tsai, Satozako Hoshino, Baeok Son, Kaooru Masekawa, Peter Biolsi, Staran Araguid – TEL Technology Center, America, LLC

23. Inorganic Copolymer Layers in Advanced Photosensitive Polymer Based RDL Processes: processing and Reliability
Nelson Pinho, Emmanuel Cherry, John Shabbeloom, MKdra Kristinabt, Andy Milier, Eric Beeney – imec; Riekw Bhatia, Ganesh Sundaram – Veeco

24. A combined Simulation and Experimental Study on Cracking and Delamination Behavior at the Cu/Polyimide Interface of RDLs in Chiplet Package Subjected to Thermos-Mechanical Loads
Bin Chen, Gang-Chao Lyu, Hong-Gang Wang, Long Zheng, Yun-Kai Deng, Xin-Ping Zhang – South China University of Technology

25. Evolution of the creep response of SAC/Bi lead free solders subjected to various thermal exposures
Mohammad Al Ahsan, S. M. Kamran Haasan, Jeffrey Sulhing, Pradeep Lal – Auburn University

26. Modeling Grain size effects on deformation behavior of SAC solder joints
Deborah Mundal, Jeffrey Sulhing, Pradeep Lal – Auburn University

27. reliaность исследования Photo Imageable Dielectric for advanced Package
Okseon Yoon, Jinyoung Kim, Kiseok Kim, Seongyoung Yoo, Jiye Shin, Soochang Lee, Myoun Lee, Suexyoon Kim – Samsung Electronics Co., Ltd

28. a novel indium metal thermal interface Material and package Design Configuration to Enhance High-power Advanced Si Package thermal Performance
Kuo-Chin Chang, Pjmy Li, Kuan-Min Wang, Chien-Chang Wang, Bang-Lu Wu – Taiwan Semiconductor Manufacturing Company, Ltd

29. High temperature storage of Cu-Cu joints fabricated by Highly (111)-oriented Nanotwinned Cu Shih-Chi Yang, Chih Chen – National Yang Ming Chiao Tung University
30. Ionic Sensor Package Design for the Survivability in Drop-Impact During Deployment
Pengcheng Yin, Jong Hwan Ha, Junbo Yang, Yangzong Lai, Seungjae Park – Binghamton University, Biju Jacob, Anur Gowda – GE Research

31. Time-Dependent Bulk Behavior of Partially Cured Epoxy Molding Compound
Salmit Prashant Prasharkar, Bongae Han – University of Maryland, College Park

32. High-Performance, Multilayer Copper-Graphene Micro-Fluid Wicks for Vapor Chambers
James Moss, Vanessa Smet, Antonia Antoniou – Georgia Institute of Technology

33. Module, Antenna, and Package Design Considerations for mm-Scale IoT Devices
Anur Paidimarri, Dusitan Li, Christian Baas, Bodhisatwa Sadhu, Alberto Valdes-Garza – IBM Research

34. 3W/cm² Heat Transfer Coefficient Vapor Chamber for HPC Server Cooling Applications
Takashi Futakushi, Kazunori Komahana – Fujitsu, Inc., Hiroyuki Ryoson, Kosuke Suzuki, Tomoki Nakamura, Takayuki Ohita – Tokyo Institute of Technology

Friday June 2, 2023, 10:00 a.m. – 12:00 Noon
Session 41: Student Interactive Presentations

Committee: Interactive Presentations
Session Co-Chairs:
Alan Huffman – SkyWater Technology
Email: alan.huffman@ieee.org
Biao Cai – IBM Corporation
Email: biaocai@us.ibm.com
Pavel Roy Paladhi – IBM Corporation
Email: rpaladhi01@gmail.com
Jin Yang – Samsung Electronics
Email: jin1.yang@ieee.org

1. An Ultra-Fine Wiring Method for Polymer-Based Embedded Silicon Fan-Out Packaging (P-esIFO)
Lang Chen, Bo Wen, Xiao Han, Jinwen Zhang, Wei Wang, Chevli Lin – Peking University-Institute of Microelectronics

Shuye Zhang, Xin Jing, Peng He – Harbin Institute of Technology; Kyungs-Wook Park – Korea Advanced Institute of Science and Technology

3. Warpage Modeling and Optimization for Polymer-Based Embedded Silicon Fan-Out Packaging (P-esIFO) During Thermal Process Loadings
Jianyu Du, Lang Chen, Han Xu, Jinwen Zhang, Wei Wang – Peking University

4. Alternative Copper-to-Copper Direct Bonding Process Using Current-Induced Bonding Method
Byungkoon Kwak, JiHyun Lee, Sangho Yoon, Byongsung Yoo – Hanyang University

5. Secure and Scalable Key Management for Waferscale Heterogeneous Integration
Yousef Safin – McGill University, University of California, Los Angeles; Pooya Aghamohy, Subramanian S. Iyer, Nader Sehatbakhsh – University of California, Los Angeles

6. A Method to Improve 3D Interconnections Resource Utilization and Reliability in Hybrid Bonding Process Considering the Effects on Signal Integrity
Ang Li, Jiarui Jiang, Qin Wang, Zheng Dong, Shua Ji, Jialian Cheng, Yuhang Zhao – Shanghai Jiao Tong University

7. Wafer-Level Integration of Atomic Vapor Cell Chip With Thermal and RF Modules
Zhi Wang, Jiantang Shang – Southeast University

8. Optimization of Embedded Manifold Cooling Characteristic Parameters for GaN HEMT
Dichen Lu, Yusen Ye, Mei Wu, Ruwen Liu, Xiangbin Du, Lihang Yu, Ye Wang, Jingping Qiao, Ziyu Liu, YunLi Shi, Binbin Jiao, Yanmei Kong – Chinese Academy of Science-Institute of Microelectronics

9. Low-Stress TSVs for High-Density 3D Integration
Jingping Qiao, Binbin Jiao, Shijia Ji, Ruwen Liu, Shichang Yun, Yanmei Kong, Yusen Ye, Xiangbin Du, Lihang Yu, Dichen Liu, Ziyu Liu – Chinese Academy of Science-Institute of Microelectronics; Jie Wang – Institute of Microelectronics, Chinese Academy of Science, Beijing, China

10. Low Dk/Df Thermosetting Silicon Hybrid Material for Fabrication of Microwave Communication Printed Circuit Board
Seung-Mo Kang, Byeonggi Soo Bae – Korea Advanced Institute of Science and Technology

11. Optimization of Si Phonic MEMS Nanowaves for Ultra-Low Thermal Conductivity
Sunghyun Hwang, James D. Overmeyer, S. M. Esmaili-Hoque Yusaf, Philip X.-L. Feng, Yong-Kyu Yoon – University of Florida; William C. Nann – Pharmacology, Inc.

12. Rapid Formation of High-Strength Sintered Silver Joints With High Reliability
Xu Zhang, Pengli Zhu, Tao Zhao, Lang Xu, Rong Sun – Chinese Academy of Science-Shenzhen Institute of Advanced Technology

13. Reference Thermal Chips for 2D and 3D Co-Packaging Process Development

14. Wideband Circular Polarized FOWLP Antenna in Package for Satellite Communications
Kaibo Zhang, Mei Sun – Institute of Microelectronics-APSTAR; Yongguo Guo – National University of Singapore

15. A High Precision Analysis Method Based on Thermal Test Chip for Thermal Characteristics of Thermal Interface Materials
Yulin Shi, Binbin Jiao, Qing Yao, Yanmei Kong, Ruwen Liu, Shichang Yun, Yusen Ye, Lihang Yu, Xiangbin Du, Ye Wang, Jingping Qiao, Dichen Liu – Chinese Academy of Science-Institute of Microelectronics

Lihang Yu, Binbin Jiao, Yusen Ye, Xiangbin Du, Yanmei Kong, Ruwen Liu, Shichang Yun, Yunli Shi, Shijia Ji, Wei Wang, Dichen Liu, Ziyu Liu, Jingping Qiao – Institute of Microelectronics Chinese Academy of Sciences

17. Generative Adversarial Network Based Adaptive Transmitter Modeling
Piyush Kashyap, Prashanth Prabhu Radhakrishnan, Dtor Baron, Chau-Wai Wong, Tianfu Wu, Paul Franzen – North Carolina State University

18. FISHI: Fault Injection Detection in Secure Heterogeneous Integration Via Power Noise Variation
Tao Zhang, Md Latifur Rahman, Had Mandani Kamila, Kamila Zamiri Aza, Mark Tehranpoor, Farinaz Farahmand – University of Florida

19. Wafer-Level Vacuum Packaging for Micro-Spherical Atomic Vapor Cell
Wenli Li, Jiantang Shang, Ziyu Wang, Jin Zhang – Southeast University

20. Design and Fabrication of Manifold Microfluidic Cooling Package Structure Based on Embedded Silicon Fan-Out (esIFO)
Yuchi Yang, Peijue Lyu, Jianyu Du, Lang Chen – Peking University; Zhou Yang – University of Geosciences Beijing

21. RFID Based Vehicular Positioning System for Safe Driving Under Adverse Weather Conditions
Bhargav Aireeri, Yihua Chu, Ethan Kopres, Premjeet Chahal – Michigan State University

22. Fingerprint Extrication With Near-Field Terahertz Time-Domain Spectroscopy (THz-TDS) for IC Hardware Assurance
Chengxi Ji, John True, Navid Asadzadeh – University of Florida

23. Additively Manufactured Near Chip Scale Interposers for DC and RF Applications
Emily Lamport, Andrew M. Luce, Yui Pho, Alkim Akyurtlu – UMass Lowell; Susan Trull – Raytheon Technologies

Zhi Du, Dylan Richmond, Mark Schadt, Mohammed Alkendi, Mark Polko – Binghamton University; Rafael Tudela – Tapecon, Inc.

25. Comparative Mechanical Behavior of Sn-Bi based Low Temperature Solder Alloys Under Different Pad Surface Finish and Pretest Aging Conditions
Sukshita Achar P. L., Colin Greene, Sean Li, Radu Radulescu, Hannah Fowler, John Bendall, Coral Handwerker, Ganesh Subramanyan – Purdue University; Nikesh Badve – Indian Institute of Technology Roorkee; Raaya Asandyaar – Intel Corporation

Konan Kauwe, Maxime Dorne, Gwenaëlle Hamon – University of Sherbrooke

Christopher Lewis, Jacob Marchia, Drew Sellers, Michael Hamilton – Auburn University

28. A Comparison of Dual-Band Wearable Metasurfaces
Adria Kajenski, Guinevere Strack, Alkim Akyurtlu – University of Massachusetts, Lowell; Shahnar Khahnavihi – Notre, Inc.

29. TrueAdapt™ – AI Based Maskless Patterning to Compensate for Die-Shift in Fan-Out Wafer Level Packaging
Golam Salber, Subramanian S. Iyer, Lenny Wu, Henry Sun – University of California, Los Angeles

30. Optimization of Copper Filled Through Package Via Geometry to Minimize Thermal Induced Stresses at Glass – TPV Interface in Borosilicate Glass Interposer
Kritha Bhavani Srinivas, Veeraputhran Pilligundu, Rabin Bhandari, Derajj Agonafer – University of Texas, Arlington; Akhil R.K. Kalapals – Intel Corporation

31. Fabrication of Flexible and Stretchable Highly Conductive Ag-PDMS Tri-Layer Interconnect and Its Integration Into Li-Ion Pouch Cells
Mayukh Nandy, Syang Liu, Hongbin Yu – Arizona State University

32. High-Density Array of 50 µm-Pitch Compressible Microinterconnects in a Replaceable Integrated Chiplet Assembly
Michael Nieves Calderon, Shengtao Yu, Muhannad S. Bakir – Auburn University; Anthony Kuo, Joon Woo Kim, Kyoung-Sik Moon, Christopher Lewis, Jacob Marchia, Drew Sellers, Michael Hamilton – Auburn University; Ruiwen Liu, Shichang Yun, Yulin Shi, Jie Wang, Dichen Lu, Ziyu Liu, Jingping Qiao – Institute of Microelectronics Chinese Academy of Sciences

33. Die Embedded Glass Interposer With Minimum Warpage for 5G/6G Applications
Xingchen Li, Xiaofan Jia, Joon Woo Kim, Kyung-Sik Moon, Mathavan Sivamani – Georgia Institute of Technology; Matthew Jordan – Sandia National Laboratories

Interactive Presentations: Thursday, June 1, 2:30 p.m. - 4:30 p.m and Friday, June 2, 10:00 a.m. - 12:00 p.m.
The 2023 ECTC Exhibition is pleased to showcase dozens of companies and organizations representing the full spectrum of materials, services, equipment, and products for the electronic packaging industry. Complementing the strength of the ECTC technical program, the Exhibition provides an unparalleled opportunity for engineers and decision makers to discuss and collaborate with representatives from leading electronic packaging companies. With scheduled refreshment breaks and social events that will take place in the Exhibition space, exhibitors and attendees will enjoy continual interactions with conference attendees. We also want to introduce the new ECTC Lounge, where attendees and exhibitors can take a few minutes to relax or converse with colleagues. Exhibit hours will be from 9:00 AM to Noon and 1:30 to 6:30 PM on Wednesday, May 31, 2023, and 9:00 AM to Noon and 1:30 to 4:00 PM on Thursday, June 1, 2023. Exhibit booth remaining availability is extremely limited for 2023. The 2023 Exhibit Application can be found at www.ectc.net and by clicking the ‘Exhibits’ link. For additional information or questions, please contact Alan Huffman, ECTC Exhibits Chair at +1-336-380-5124 or email alan.huffman@ieee.org and exhibits@ectc.net.

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or …

2) Log onto www.ectc.net and click on the Location tab near the top of the page to find a special online hotel registration link.

**Note about Hotel Rooms**

Attendees should note that only reputable sites should be used to book a hotel room for the 2023 ECTC. Be advised that you may receive emails from hotel booking companies. These emails and sites are not to be trusted. The only formal communication ECTC will convey about hotel rooms will come in the form of ECTC e-blasts or ECTC emails from our Executive Committee. ECTC’s only authorized site for reserving a room is through our website (www.ectc.net). You may, however, use other trusted sites that you personally have used in the past to book travel. Please be advised, there are scam artists out there and if it’s too good to be true it likely is. Should you have any questions about booking a hotel room please contact ECTC staff at: lrenzi@renziandco.com.
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<td></td>
<td></td>
</tr>
<tr>
<td>Attendee (full ECTC conference)</td>
<td>US $825</td>
<td>US $950</td>
</tr>
<tr>
<td>Attendee (Joint ECTC + Itherm conferences)</td>
<td>$1075</td>
<td>$1250</td>
</tr>
<tr>
<td>Attendee One-Day Registration</td>
<td>$625</td>
<td>$625</td>
</tr>
<tr>
<td>Speaker or Chair (full ECTC conference)</td>
<td>$700</td>
<td>$850</td>
</tr>
<tr>
<td>Speaker or Chair One-Day Registration</td>
<td>$550</td>
<td>$550</td>
</tr>
<tr>
<td>Non-IEEE Member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attendee (full ECTC conference)</td>
<td>$1025</td>
<td>$1150</td>
</tr>
<tr>
<td>Attendee (Joint ECTC + Itherm conferences)</td>
<td>$1250</td>
<td>$1500</td>
</tr>
<tr>
<td>Attendee One-Day Registration</td>
<td>$625</td>
<td>$625</td>
</tr>
<tr>
<td>Speaker or Chair (full ECTC conference)</td>
<td>$700</td>
<td>$850</td>
</tr>
<tr>
<td>Speaker or Chair One-Day Registration</td>
<td>$550</td>
<td>$550</td>
</tr>
<tr>
<td>Student</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attendee or Speaker (full conference)</td>
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<td>$340</td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>Conference Registration</th>
<th>Advance Registration (until May 5)</th>
<th>Door Registration (May 6 and beyond)</th>
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<tbody>
<tr>
<td>IEEE Member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full PDC (both a.m. and p.m.)</td>
<td>$625</td>
<td>$625</td>
</tr>
<tr>
<td>Single PDC (a.m. or p.m.)</td>
<td>$440</td>
<td>$440</td>
</tr>
<tr>
<td>Non-IEEE Member</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full PDC (both a.m. and p.m.)</td>
<td>$675</td>
<td>$675</td>
</tr>
<tr>
<td>Single PDC (a.m. or p.m.)</td>
<td>$490</td>
<td>$490</td>
</tr>
<tr>
<td>Student</td>
<td></td>
<td></td>
</tr>
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<td>$150</td>
<td>$150</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Registration Option</th>
<th>Advance Registration (until May 5)</th>
<th>Door Registration (May 6 and beyond)</th>
</tr>
</thead>
<tbody>
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<td>$75</td>
<td>$75</td>
</tr>
<tr>
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<td>$50</td>
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</tbody>
</table>

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<thead>
<tr>
<th>Sponsor</th>
<th>Website</th>
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</thead>
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<td>micross.com</td>
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</tbody>
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<thead>
<tr>
<th>Sponsor</th>
<th>Website</th>
</tr>
</thead>
<tbody>
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</thead>
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</tr>
<tr>
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<td>intel.com</td>
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</tr>
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</tbody>
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<tr>
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<th>MEDIA</th>
</tr>
</thead>
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- Semiconductor Review: semiconductorreview.com
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May 30, 2023
Morning Professional Development Courses
8:00 a.m. - 12:00 p.m.
1. High Reliability of Lead-Free Solder Joints – Materials Considerations
2. Wafer-Level Chip-Scale Packaging (W CSP) Fundamentals
3. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Level and Advanced RF Packages
4. Eliminating Failure Mechanisms in Advanced Packages
5. Reliability Engineering Testing Methodology and Statistical Knowledge for Qualifications of Consumer and Automotive Electronic Components
6. Reliability Physics and Failure Mechanisms in Electronics Packaging
7. Reliable Integrated Thermal Packaging for Power Electronics
8. Introduction to PWB Thermal Analysis

ECTC Special Session on Advanced Packaging for Harsh Environment
8:30 a.m. - 10:00 a.m.
“Advanced Packaging and Heterogeneous Integration Roadmap for Harsh Environment – Current Status and Opportunities”

ECTC Special Session on Hybrid Bonding
10:30 a.m. - 12:00 p.m.
“Copper Hybrid Bond Interconnections for Chip-to-Wafer Applications”

Afternoon Professional Development Courses
1:30 p.m. - 5:30 p.m.
9. Additive Flexible Hybrid Electronics – Manufacturing and Reliability
10. Fan-Out Packaging and Chiplet Heterogeneous Integration
11. Photonic Technologies for Communication, Sensing, and Displays
12. Flip Chip Technologies
13. Packaging and Heterogeneous Integration for Automotive Electronics and Advanced Characterization of EMCs
14. Analysis of Fracture and Delamination in Microelectronic Packages
15. Polymers in Wafer Level Packaging
16. Thermal Management of Electronics

ECTC Special Session on Photonics Packaging
1:30 p.m. - 3:00 p.m.
“Photonic Integrated Circuit Packaging: Challenges, Pathfinding, and Technology Adoption”

ECTC Special Session on CHIPS Act
3:30 p.m. - 5:00 p.m.
“Advanced Packaging Manufacturing in North America: Building the Ecosystem”
Young Professionals Networking Panel
7:00 p.m. - 7:45 p.m.

ECTC EPS Seminar on High-Density Substrates
7:45 p.m. - 9:15 p.m.
“The Future of High-Density Substrates – Towards Submicron Technology”
May 31, 2023
ECTC Keynote
8:00 a.m. - 9:15 a.m.
“Unlocking the Potential of Quantum Computers: Challenges and Opportunities in Electronic Devices, Interconnects, and Packaging”

Technical Sessions
9:30 a.m. - 12:35 p.m.
1. Heterogeneous Chiplet Integration
2. High-Performance Packaging Materials
3. Advancements in Copper/Silicon-Oxide Hybrid Bonding
4. Assembly and Manufacturing Process Enhancement
5. Flexible Packaging and Chip-Package-Interconnection
6. Co-packaged Optical Assembly

Interactive Presentation Session 37
10:00 a.m. - 12:00 p.m.
Wednesday Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.
7. Large Formfactor Dense System Integration by FanOut
8. Novel Reliability Test Methods
9. Innovations in Copper Chip-to-Wafer Bonding
10. Packaging Interconnects
11. Additive Manufacturing and Packaging for Flexible Electronics
12. mm Wave Antenna-in-Package and Arrays

Interactive Presentation Session 38
2:30 p.m. - 4:30 p.m.

ECTC/IHERM Diversity and Career Growth Panel and Reception
6:30 p.m. - 7:30 p.m.
“Diversifying our Technical Workforce to meet National Needs including the CHIPS Act Initiative”

June 1, 2023
ECTC Plenary Session on mm-Wave Phased Array Packaging
8:00 a.m. - 9:15 a.m.
“Millimeter-Wave Phased Array Front-End Integration and Packaging for Next-Generation Communication and Radar Systems”

Technical Sessions
9:30 a.m. - 12:35 p.m.
13. Wafer/Panel-Level and Advanced Substrate Technologies
14. Advances in Heterogeneous Integration Bonding Technology
15. Innovative Interposer and Through-Via Technologies
16. Sintering and Soldering for High-Power, High-Reliability, and RF Devices
17. Advanced Reliability Modelling and Characterization
18. Advanced Photonic Packaging and Interconnect

Interactive Presentation Session 39
10:00 a.m. - 12:00 p.m.
EPS Awards Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.
19. Advances in 3D Integration and Hybrid Bonding
20. Automotive/Board-Level Reliability
21. Fine-Pitch and Intermetallic Considerations in Advanced Solder Interconnections
22. Large Substrate Process Integration Challenges
23. Next Generation Quantum, AI, and Secure System Design
24. High-Speed Signal and Power Integrity

Interactive Presentation Session 40
2:30 p.m. - 4:30 p.m.

June 2, 2023
ECTC EPS President Panel Session on Photonics
8:00 a.m. - 9:15 a.m.
“How can Photonics Enable the Bandwidth Densities with Lower Energy per Bit in Emerging SIP?”

Technical Sessions
9:30 a.m. - 12:35 p.m.
25. Next Generation High-Performance Computing Architectures
26. Materials Reliability
27. Next Generation Wafer-to-Wafer Copper Bonding
28. Process Enhancements in 3D, FOWLP, and TSV Technologies
29. AI-based Prediction for Heterogeneous Integration and Advanced Packaging
30. Trends in Encapsulants and Low Dk/Df Dielectrics

Student Interactive Presentations Session 41
10:00 a.m. - 12:00 p.m.
Raffle Prize Luncheon
12:45 p.m. - 2:00 p.m.

Technical Sessions
2:00 p.m. - 5:05 p.m.
31. MEMS Sensor, Bio, and Advanced Interconnect Reliability
32. Thermo-Mechanical Modelling and Characterization
33. Advances in RDL, Via, and TSV Technologies for Chiplet Integration
34. Bonding Assembly - Novel Packaging, Process, and Characterization
35. Packaging and Materials for Flexible Medical Technologies
36. RF, Heterogeneous, and Chiplet Modules

Session Summary by Interest Area
Packaging Technologies
S1, S7, S13, S19, S25, S31

Applied Reliability
S8, S17, S20, S26, S31

Assembly & Manufacturing Technology
S4, S16, S22, S34

Emerging Technologies
S11, S23, S35

RF, High-Speed Components & Systems
S12, S24, S36

Interconnections
S3, S9, S15, S21, S27, S33

Materials & Processing
S2, S14, S16, S28, S30

Thermal/Mechanical Simulation & Characterization
S5, S10, S17, S29, S32

Photonics
S6, S18

Interactive Presentations
S37, S38, S39, S40, S41
Mark your calendar for ECTC 2023!
JW Marriott Orlando, Grande Lakes
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May 30 – June 2, 2023