ECTC 2022 Special Sessions Information

2022 ECTC Special Session

MicroLED Display Technology: High Volume Manufacturing (HVM) Progress and Challenges

Tuesday, May 31, 2022, 8:30 a.m. – 10:00 a.m.

Chairs: Chukwudi Okoro – Corning Inc, USA and Benson Chan – Binghamton University, USA

Liquid crystal display (LCD) and organic light-emitting diode (OLED) displays are the leading technologies in today's display industry. With continuous interest in performance improvements in areas including higher dynamic range, wider color gamut, lower power consumption, and borderless designs, however, emerging microLED display technology offers several potential advantages. Combinations of these potential advantages apply to applications such as AR/VR, tiled displays, smartwatches, and automotive displays. While progress in these technology areas has been demonstrated at the R&D level, technical challenges exist to transition the emerging microLED technology into industry pilot or manufacturing scales. Some of these challenges include, microLED fabrication, transfer assembly, light management, backplane architecture, device design and integration, and much more.

This panel session aims at addressing the progress and the remaining challenges associated with the commercialization of cost-effective microLED enabled display technology. This will be tackled with the help of a panel of microLED technology experts having diverse areas of expertise.

Dr. John Kymissis	Principal Engineer, Lumiode
Dr. Eugene Chow	Principal Scientist, Palo Alto Research Center (PARC)
Dr. Falcon Liu	Marketing Director, Playnitride
Dr. Chris Bower	CTO, XDisplay
Dr. Sean Garner	Principal Scientist, Corning Inc
Dr. Eric Virey	Senior Market and Technology Analyst, Yole Development

2022 ECTC Special IEEE EPS HIR Session

Selected Topics of IEEE EPS Heterointegration Roadmap

Tuesday, May 31, 2022, 10:30 a.m. – 12:00 a.m.

Chairs: Amr Helmy (Professor at U of Toronto)

This panel session will focus on the hardware design and packaging approaches that can enable scaling Machine Learning and AI systems in SiP by utilizing heterogenous integration as a tool to expand the capabilities of SiP. Aspects including system design and architecture, CMOS chip design, hybrid integration methodologies, interconnect approaches will all be discussed in this panel

Speakers will be confirmed soon

2022 ECTC Special Session
Meeting Next Generation Packaging Challenges: Chiplets to Co-Packaged Optics.
Tuesday, May 31, 2022, 1:30 p.m. – 3:00 p.m.
Chairs: E. Jan Vardaman, TechSearch International, Inc.

The next generation of advanced packaging will see greater adoption of heterogeneous integration in the form of chiplets as we move into the 3nm semiconductor node. The design, assembly, and test of packages will become more complex, new substrates may be required, and with 3D formats, the move to hybrid bonding is anticipated. Energy requirements in datacenters and performance needs are driving the adoption of co-packaged optics. This panel will discuss changes in the infrastructure required to meet these needs, including the role that the foundry and the OSAT will play. New material requirements will be addressed, the importance of co-design will be highlighted, the need for new thermal solutions will be discussed, and changes in the test approach will be investigated.

Speakers
Ashkan Seyedi, NVIDIA (presence, as long as travel is allowed by company)
Jie Xue, CISCO (presence, as long as travel is allowed by company)
Kevin O'Buckley, General Manager, ASICs, MARVELL
Raja Swaminathan, AMD

2022 ECTC Special Session
How will IC substrate technology evolve to enable next generation Heterogeneous Integration schemes for high performance applications?
Tuesday, May 31, 2022, 3:30 p.m. – 5:00 p.m.
Chairs: Kuldip Johal – Atotech Group and Bora Baloglu – Amkor

The Electronics industry continues to push the limits of silicon and advanced packaging especially for applications in AI and MI that use high performance computing with HBW memory. These types of applications are the key drivers for higher I/O counts and decreasing bump pitch. This increase in I/O density continues to accelerate as silicon process note geometry continues the shrink, enabling more use of silicon interposers, to prevent this gap increasing the IC substrate manufactures also need to follow suit in terms of enabling higher I/O density while maintaining the cost advantage. The objective of this special panels session, is to have range of industry experts from OEM, OSAT, IC substrate manufacturing and material process/ equipment, to discuss how IC susbtrate technology can evolve to enable shrinkage of features (Line/ space, via/Pad) enabling increase I/O density for next generation high performance applications.

Special panel experts (all panelists confirmed)

OEM : Intel Rahul Manepalli Intel Fellow & Director of Substrate TD Module Engineering. Confirmed on site
OSAT : Amkor JinYoung Khim, (Sr. VP Head of R&D) Confirmed on site

IC Substrate : Markus Leitgeb R&D Manager AT&S (Markus will step down from chairing the session.) Confirmed on site
Materials: Habib Hichri Senior Fellow, Global Applications and Business Development at Ajinomoto Fine-Techno USA Corporation. Confirmed on site
Process + Tools: Frank Bruening Global Product Director Mentalization. Atotech Confirmed on site

2022 Young Professionals Networking Panel
Tuesday, May 31, 5:30 p.m. - 7:00 p.m.
Chair: Yan Liu (Medtronic) and Adeel Bajwa (Kulicke and Soffa)

This event is designed just for you – young professionals (including current graduate students). In this active event, we will pair you with senior EPS members and professionals through a series of active and engaging activities. You will have opportunities to learn more about packaging-related topics, ask career questions, and meet some professional colleagues.

2022 ECTC Panel Session
State-of-the-Art Heterogeneous Integrated Packaging Program
Tuesday, May 31, 2022, 7:30 p.m. – 9:00 p.m.
Chairs: Kitty Pearsall, EPS President – Boss Precision, Inc. and Christopher Riso, Booz Allen Hamilton

The EPS President's Panel at this year's ECTC explores the Department of Defense (DoD) State of The Art (SOTA) Heterogeneous Integrated Packaging (SHIP) program. The primary goal of the SHIP program is the development of a sustainable business and operational model for addressing government needs in the Microelectronics (ME) packaging industry. SHIP will leverage the expertise of commercial industry to develop and demonstrate a novel model to ensure sustained DoD access to secure heterogeneous integration, advanced packaging, and test of SOTA advanced packaging and create a catalog of solution components which consist of both die and package components, IP, protocols, tool sets, and design/manufacturability and test methodologies. The session will describe present and future technology implementations for both SHIP Digital and SHIP RF. There will be three panelists:

Brian Olson, SHIP RF Lead – Office of the Undersecretary of Defense for Research and Engineering
John Sotir, SHIP Program Director – Intel Corporation
Ted Jones, Sr. Product Line Director High Performance Solutions Services – Qorvo Inc.

2022 ECTC Plenary Session

Digital Transformation - The Cornerstone of Future Semiconductor and Advanced Packaging Growth

Wednesday, June 1, 2022, 7:30 p.m. – 9:00 p.m.

Chairs: Rozalia Beica AT&S and Ed Sperling (Semiconductor Engineering)

Panel discussions with industry experts and executives across the supply chain, with global participation, to address the impact of digital transformation on our industry, industry dynamics and future trends. Main topics that will be addressed:

- Digital transformation impact on economies and industries
- How are companies preparing for digital transformation in the semiconductor and packaging industry
- Industry trends & applications driving semiconductor adoption and growth of advanced packaging
- The economics of packaging vs. SoCs
- Industry dynamics: business model evolution, investments, supply challenges and disruption

Panelists:

Carolyn Evans - Chief Economist, Intel (US)

Doug Yu - VP Pathfinding and System Integration – TSMC (TW)

Jean Christophe Eloy - CEO Yole Developpement (FR)

Mike Rosa – CMO, SVP Strategy, Onto Innovation (US)

Seoung Wook Yoon - VP Corporate R&D, Samsung (KR)

2022 ECTC/ITherm Diversity and Career Growth Panel and Reception

Solving Diversification Challenges and Workforce Retention Issues

Wednesday, June 1, 2022, 6:30 p.m. – 7:30 p.m.

Chair: Kim Yess (Brewer Science/ECTC) and Christina Amon (Univ. of Toronto/iTherm), Moderator; Francoise von Trapp (3D InCites)

The microelectronics industry is in the midst of a workforce crisis that began long before we heard the word: COVID 19. Companies are desperately seeking new young talent while simultaneously trying to retain the workforce they've worked so hard to build. By 2022, it's well understood that a diverse and inclusive workforce improves innovation, productivity, and the bottom line, yet companies in the microelectronics industry struggle to recruit both women and under-represented minorities to fill thousands of open positions.

In this discussion, we will address these challenges head on with some practical advice from the trenches. Each of our panelists bring real-life experience associated with attracting and retaining a diverse and inclusive workforce, and they are ready to share tips. So come prepared with your questions and leave with actionable items.

Panelists:

Emma Cheer, Head of DEI at GlobalFoundries
Bina Hallman, VP IBM System Client Advocacy and Head of D&I System business
Antoinette Hamilton, Head of DEI at Lam Research
KT Moore, VP Corporate Marketing at Cadence,
Debbie Gustafson, CEO Energetiq Technology
Scott Balaguer, President, Americas for Edwards Vacuum

ECTC Luncheon Keynote
Title to be confirmed soon
Wednesday, June 1, 2022
Keynote Speaker: Chris Koopmans – Chief Operations Officer, Marvell

2022 IEEE EPS Seminar
Interconnect Technologies for Chiplets
Thursday, June 2, 2022, 8:00 p.m. – 9:30 p.m.
Chairs: Yasumitsu Orii - Nagase, Japan and Shigenori Aoki - Fujitsu

The EPS Seminar will discuss the several interconnect technologies for Chiplets such as Silicon Bridge, Advanced Interposer, Fan-out wafer-level packaging, and optical interconnection. Each panelist will prepare a short set of slides to present within 10-15 minutes, followed by panel discussion.

Panelists
Ravi Mahajan, Intel , "HI Interconnects for today and tomorrow"
Akihiro Horibe, IBM Research Tokyo, "Direct Bonded Heterogeneous Integration DBHi Si Bridge"
Yu-Hua Chen, Unimicron, "The Challenges of Advanced Substrate for Heterogeneous Integration"
Shin-Puu Jeng, TSMC, "Heterogeneous I ntegration A pproaches in F oundry"
Yu-Po Wang, SPIL, "Trend and Solution for Memory Integrated Advanced Packages"
Hideyuki Nasu, Furukawa Electric " High-Density Optical Transceivers and Pluggable Electrical Interfaces for Co-Packaged Optics"